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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	54MHz
Connectivity	I ² C, IrDA, SCI, SD/SDIO, SPI, SSI, USB OTG
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	43
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f52315cdfm-30

1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications, and Table 1.2 gives a comparison of the functions of the products in different packages.

Table 1.1 is for products with the greatest number of functions, so the number of peripheral modules and channels will differ in accordance with the package type. For details, see Table 1.2, Comparison of Functions for Different Packages.

Table 1.1 Outline of Specifications (1/4)

Classification	Module/Function	Description
CPU	CPU	- Maximum operating frequency: 54 MHz 32-bit RX CPU (RX v2) - Minimum instruction execution time: One instruction per clock cycle - Address space: 4-Gbyte linear - Register set - General purpose: Sixteen 32-bit registers - Control: Ten 32-bit registers - Accumulator: Two 72-bit registers - Basic instructions: 75 (variable-length instruction format) - Floating-point instructions: 11 - DSP instructions: 23 - Addressing modes: 10 - Data arrangement - Instructions: Little endian - Data: Selectable as little endian or big endian - On-chip 32-bit multiplier: 32-bit × 32-bit → 64-bit - On-chip divider: 32-bit ÷ 32-bit → 32 bits - Barrel shifter: 32 bits - Memory protection unit (MPU)
	FPU	- Single precision (32-bit) floating point - Data types and floating-point exceptions in conformance with the IEEE754 standard
Memory	ROM	- Capacity: 128/256/384/512 Kbytes - Up to 32 MHz: No-wait memory access 32 to 54 MHz: Wait state required. No wait state if the instruction is served by a ROM accelerator hit. - Programming/erasing method: - Serial programming (asynchronous serial communication/USB communication), self-programming
	RAM	- Capacity: 32/64 Kbytes 54 MHz, no-wait memory access
	E2 DataFlash	- Capacity: 8 Kbytes - Number of erase/write cycles: 1,000,000 (typ)
MCU operating mode		Single-chip mode, on-chip ROM enabled expansion mode, and on-chip ROM disabled expansion mode (software switching)
Clock	Clock generation circuit	- Main clock oscillator, sub-clock oscillator, low-speed on-chip oscillator, high-speed on-chip oscillator, PLL frequency synthesizer, USB-dedicated PLL frequency synthesizer, and IWDG-dedicated on-chip oscillator - Oscillation stop detection: Available - Clock frequency accuracy measurement circuit (CAC) - Independent settings for the system clock (ICLK), peripheral module clock (PCLK), external bus clock (BCLK), and FlashIF clock (FCLK) - The CPU and system sections such as other bus masters run in synchronization with the system clock (ICLK): 54 MHz (at max.) - MTU2a runs in synchronization with the PCLKA: 54 MHz (at max.) - The ADCLK for the S12AD runs in synchronization with the PCLKD: 54 MHz (at max.) - Peripheral modules other than MTU2a and S12ADE run in synchronization with the PCLKB: 32 MHz (at max.) - Devices connected to external buses run in synchronization with the BCLK: 32 MHz (at max.) - The flash peripheral circuit runs in synchronization with the FCLK: 32 MHz (at max.)
Resets		RES# pin reset, power-on reset, voltage monitoring reset, watchdog timer reset, independent watchdog timer reset, and software reset
Voltage detection	Voltage detection circuit (LVDAb)	- When the voltage on VCC falls below the voltage detection level, an internal reset or internal interrupt is generated. - Voltage detection circuit 0 is capable of selecting the detection voltage from 4 levels - Voltage detection circuit 1 is capable of selecting the detection voltage from 14 levels - Voltage detection circuit 2 is capable of selecting the detection voltage from 4 levels

Table 1.1 Outline of Specifications (3/4)

Classification	Module/Function	Description
Timers	Independent watchdog timer (IWDtA)	14 bits × 1 channel - Count clock: Dedicated low-speed on-chip oscillator for the IWDtA Frequency divided by 1, 16, 32, 64, 128, or 256
	Realtime clock (RTCe)	- Clock source: Sub-clock - Time/calendar - Interrupts: Alarm interrupt, periodic interrupt, and carry interrupt - Time-capture facility for three values
	Low power timer (LPT)	16 bits × 1 channel - Clock source: Sub-clock, Dedicated low-speed on-chip oscillator for the IWDtA Frequency divided by 2, 4, 8, 16, or 32
	8-bit timer (TMR)	(8 bits × 2 channels) × 2 units - Seven internal clocks (PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, and PCLK/8192) and an external clock can be selected - Pulse output and PWM output with any duty cycle are available - Two channels can be cascaded and used as a 16-bit timer
Communication functions	Serial communications interfaces (SCIg, SCIlh)	7 channels (channel 0, 1, 5, 6, 8, 9: SCIg, channel 12: SCIlh) - SCIg - Serial communications modes: Asynchronous, clock synchronous, and smart-card interface - Multi-processor function - On-chip baud rate generator allows selection of the desired bit rate - Choice of LSB-first or MSB-first transfer - Average transfer rate clock can be input from TMR timers for SCI5, SCI6, and SCI12 - Start-bit detection: Level or edge detection is selectable. - Simple I²C - Simple SPI 9-bit transfer mode - Bit rate modulation - Event linking by the ELC (only on channel 5) - SCIlh (The following functions are added to SCIg) - Supports the serial communications protocol, which contains the start frame and information frame - Supports the LIN format
	IrDA interface (IRDA)	1 channel (SCI5 used) - Supports encoding/decoding of waveforms conforming to IrDA standard 1.0
	I ² C bus interface (RIICa)	1 channel - Communications formats: I²C bus format/SMBus format - Master mode or slave mode selectable - Supports fast mode
	Serial peripheral interface (RSPIa)	1 channel - Transfer facility - Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPI clock) enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) - Capable of handling serial transfer as a master or slave - Data formats - Choice of LSB-first or MSB-first transfer - The number of bits in each transfer can be changed to 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. 128-bit buffers for transmission and reception - Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) - Double buffers for both transmission and reception
	USB 2.0 host/function module (USBd)	- USB Device Controller (UDC) and transceiver for USB 2.0 are incorporated. - Host/function module: 1 port - Compliant with USB version 2.0 - Transfer speed: Full-speed (12 Mbps), low-speed (1.5 Mbps) - OTG (ON-The-Go) is supported. - Isochronous transfer is supported. - BC1.2 (Battery Charging Specification Revision 1.2) is supported. - Internal power supply for USB (allows operation without external power input to the VCC_USB pin when VCC = 4.0 to 5.5V)
	CAN module (RSCAN)	1 channel - Compliance with the ISO11898-1 specification (standard frame and extended frame) 16 Message boxes

Table 1.4 List of Products: G Version ($T_a = -40$ to $+105^\circ\text{C}$) (2/2)

Group	Part No.	Order Part No.	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency	Security Function	SDHI	CAN	Operating Temperature
RX231	R5F52315AGFL	R5F52315AGFL#30	PLQP0048KB-B	128 Kbytes	32 Kbytes	8 Kbytes	54 MHz	Not available	Not available	Available	-40 to +105°C
	R5F52315CGFL	R5F52315CGFL#30						Not available	Not available	Not available	
RX230	R5F52306AGFP	R5F52306AGFP#30	PLQP0100KB-B	256 Kbytes	32 Kbytes	8 Kbytes	54 MHz	Not available	Not available	Not available	-40 to +105°C
	R5F52306AGND	R5F52306AGND#U0	PWQN0064KC-A					Not available	Not available	Not available	
	R5F52306AGFM	R5F52306AGFM#30	PLQP0064KB-C					Not available	Not available	Not available	
	R5F52306AGNE	R5F52306AGNE#U0	PWQN0048KB-A					Not available	Not available	Not available	
	R5F52306AGFL	R5F52306AGFL#30	PLQP0048KB-B					Not available	Not available	Not available	
	R5F52305AGFP	R5F52305AGFP#30	PLQP0100KB-B	128 Kbytes				Not available	Not available	Not available	
	R5F52305AGND	R5F52305AGND#U0	PWQN0064KC-A					Not available	Not available	Not available	
	R5F52305AGFM	R5F52305AGFM#30	PLQP0064KB-C					Not available	Not available	Not available	
	R5F52305AGNE	R5F52305AGNE#U0	PWQN0048KB-A					Not available	Not available	Not available	
	R5F52305AGFL	R5F52305AGFL#30	PLQP0048KB-B					Not available	Not available	Not available	

Table 1.5 Pin Functions (4/4)

Classifications	Pin Name	I/O	Description
SD host interface	SDHI_D3 to SD_D0	I/O	SD data bus pins
	SDHI_CD	Input	SD card detection pin
	SDHI_WP	Input	SD write-protect signal
USB 2.0 host/ function module	VCC_USB	Input	Power supply pin for USB. Connect this pin to VCC or connect this pin to VSS via a 0.33 μ F smoothing capacitor for stabilizing the internal power supply.
	VSS_USB	Input	Ground pin for USB. Connect this pin to VSS.
	USB0_DP	I/O	D+ I/O pin of the USB on-chip transceiver.
	USB0_DM	I/O	D- I/O pin of the USB on-chip transceiver.
	USB0_VBUS	Input	USB cable connection monitor pin.
	USB0_EXICEN	Output	Low-power control signal for the OTG chip.
	USB0_VBUSEN	Output	VBUS (5 V) supply enable signal for the OTG chip.
	USB0_OVRCURA, USB0_OVRCURB	Input	External overcurrent detection pins.
	USB0_ID	Input	Mini-AB connector ID input pin during operation in OTG mode.
12-bit A/D converter	AN000 to AN007, AN016 to AN031	Input	Input pins for the analog signals to be processed by the A/D converter.
	ADTRG0#	Input	Input pin for the external trigger signal that start the A/D conversion.
12-bit D/A converter	DA0, DA1	Output	Analog output pins of the D/A converter.
Comparator B	CMPB0 to CMPB3	Input	Input pin for the analog signal to be processed by comparator B.
	CVREFB0 to CVREFB3	Input	Analog reference voltage supply pin for comparator B.
	CMPOB0 to CMPOB3	Output	Output pin for comparator B.
CTSU	TS0 to TS9, TS12, TS13, TS15 to TS20, TS22, TS23, TS27, TS30, TS33, TS35	Output	Electrostatic capacitance measurement pins (touch pins).
	TSCAP	Output	LPF connection pin.
Analog power supply	AVCC0	Input	Analog voltage supply pin for the 12-bit A/D converter and D/A converter. Connect this pin to VCC when not using the 12-bit A/D converter and D/A converter.
	AVSS0	Input	Analog ground pin for the 12-bit A/D converter and D/A converter. Connect this pin to VSS when not using the 12-bit A/D converter and D/A converter.
	VREFH0	Input	Analog reference voltage supply pin for the 12-bit A/D converter.
	VREFL0	Input	Analog reference ground pin for the 12-bit A/D converter.
	VREFH	Input	Analog reference voltage supply pin for the 12-bit D/A converter.
	VREFL	Input	Analog reference ground pin for the 12-bit D/A converter.
I/O ports	P03, P05, P07	I/O	3-bit input/output pins.
	P12 to P17	I/O	6-bit input/output pins.
	P20 to P27	I/O	8-bit input/output pins.
	P30 to P37	I/O	8-bit input/output pins (P35 input pin).
	P40 to P47	I/O	8-bit input/output pins.
	P50 to P55	I/O	6-bit input/output pins.
	PA0 to PA7	I/O	8-bit input/output pins.
	PB0 to PB7	I/O	8-bit input/output pins.
	PC0 to PC7	I/O	8-bit input/output pins.
	PD0 to PD7	I/O	8-bit input/output pins.
	PE0 to PE7	I/O	8-bit input/output pins.
	PH0 to PH3	I/O	4-bit input/output pins.
	PJ3	I/O	1-bit input/output pin.

Table 1.6 List of Pins and Pin Functions (100-Pin TFLGA) (2/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCI, RSPI, RIIIC, RSCAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
E8		PA4	A4	MTIOC5U/MTCLKA/TMRI0/TIOCA1	TXD5/SMOSI5/SSDA5/SSLA0/SSITXD0/IRTXD5			IRQ5 / CVREFB1
E9		PA5	A5	TIOCB1	RSPCKA			
E10		PA3	A3	MTIOC0D/MTCLKD/TIOC0D/TCLKB	RXD5/SMISO5/SSCL5/SSIRXD0/IRRXD5			IRQ6 /CMPB1
F1	EXTAL	P36						
F2	VCC							
F3	UPSEL	P35						NMI
F4		P32		MTIOC0C/TMO3/TIOCC0/RTCOUT/RTCIC2	TXD6/SMOSI6/SSDA6/USB0_VBUSEN			IRQ2
F5		P12		TMCI1	SCL			IRQ2
F6		PB3	A11	MTIOC0A/MTIOC4A/TMO0/POE3#/TIOC0D/TCLKD	SCK6	SDHI_W P		
F7		PB2	A10	TIOCC3/TCLKC	CTS6#/RTS6#/SS6#			
F8		PB0	A8	MTIC5W/TIOCA3	RXD6/SMISO6/SSCL6/RSPCKA	SDHI_C MD		
F9		PA7	A7	TIOCB2	MISOA			
F10	VSS							
G1		P33		MTIOC0D/TMRI3/POE3#/TIOC0D	RXD6/SMISO6/SSCL6		TS1	IRQ3
G2		P31		MTIOC4D/TMCI2/RTCIC1	CTS1#/RTS1#/SS1#/SSISCK0			IRQ1
G3		P30		MTIOC4B/TMRI3/POE8#/RTCIC0	RXD1/SMISO1/SSCL1/AUDIO_MCLK			IRQ0/CMPOB3
G4		P27	CS3#	MTIOC2B/TMCI3	SCK1/ SSIWS0		TS2	CVREFB3
G5	BCLK	P53					TS17	
G6		P52	RD#				TS18	
G7		PB5	A13	MTIOC2A/MTIOC1B/TMRI1/POE1#/TIOCB4	SCK9/USB0_VBUS	SDHI_CD		
G8		PB4	A12	TIOCA4	CTS9#/RTS9#/SS9#			
G9		PB1	A9	MTIOC0C/MTIOC4C/TMCI0/TIOCB3	TXD6/SMOSI6/SSDA6	SDHI_CL K		IRQ4/CMPOB1
G10	VCC							
H1		P26	CS2#	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1/SSIRXD0		TS3	CMPB3
H2		P25	CS1#	MTIOC4C/MTCLKB/TIOCA4			TS4	ADTRG0#
H3		P16		MTIOC3C/MTIOC3D/TMO2/TIOCB1/TCLKC/RTCOUT	TXD1/SMOSI1/SSDA1/MOSIA/SCL/USB0_VBUS/USB0_VBUSEN/USB0_OVRCURB			IRQ6/ADTRG0#
H4		P15		MTIOC0B/MTCLKB/TMCI2/TIOCB2/TCLKB	RXD1/SMISO1/SSCL1/CRXD0		TS12	IRQ5/CMPB2
H5		P55	WAIT#	MTIOC4D/TMO3	CRXD0		TS15	
H6		P54	ALE	MTIOC4B/TMCI1	CTXD0		TS16	
H7	UB	PC7	A23/CS0#	MTIOC3A/MTCLKB/TMO2	TXD8/SMOSI8/SSDA8/MISOA			CACREF
H8		PC6	A22/CS1#	MTIOC3C/MTCLKA/TMCI2	RXD8/SMISO8/SSCL8/MOSIA		TS22	
H9		PB6	A14	MTIOC3D/TIOCA5	RXD9/SMISO9/SSCL9	SDHI_D1		
H10		PB7	A15	MTIOC3B/TIOCB5	TXD9/SMOSI9/SSDA9	SDHI_D2		
J1		P24	CS0#	MTIOC4A/MTCLKA/TMRI1/TIOCB4	USB0_VBUSEN		TS5	
J2		P21		MTIOC1B/TMCI0/TIOCA3	RXD0/SMISO0/SSCL0/USB0_EXICEN/SSIWS0		TS8	
J3		P17		MTIOC3A/MTIOC3B/TMO1/POE8#/TIOCB0/TCLKD	SCK1/MISOA/SDA/SSITXD0			IRQ7/CMPOB2
J4		P13		MTIOC0B/TMO3/TIOCA5	SDA			IRQ3
J5	VSS_USB*1	PH0*1						CACREF*1

Table 1.8 List of Pins and Pin Functions (64-Pin WFLGA) (2/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCI, RSPI, IIC, RSCAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
F4		PC5	MTIOC3B/MTCLKD/TMRI2	SCK8/RSPCKA/USB0_ID			TS23
F5		P15	MTIOC0B/MTCLKB/TMC12/TIOCB2/TCLKB	RXD1/SMISO1/SSCL1/CRXD0		TS12	IRQ5/CMPB2
F6		PB1	MTIOC0C/MTIOC4C/TMC10/TIOCB3	TXD6/SMOSI6/SSDA6	SDHI_CLK		IRQ4/CMPOB1
F7		PB5	MTIOC2A/MTIOC1B/TMRI1/POE1#/TIOCB4	SCK9/USB0_VBUS	SDHI_CD		
F8		PB3	MTIOC0A/MTIOC4A/TMO0/POE3#/TIOC3D/TCLKD	SCK6	SDHI_WP		
G1	EXTAL	P36					
G2		P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1/USB0_VBUSEN/SSIRXD0		TS3	CMPB3
G3	VCC_USB*1	PH3*1	TMC10*1				
G4	VSS_USB*1	PH0*1					CACREF*1
G5	UB	PC7	MTIOC3A/MTCLKB/TMO2	TXD8/SMOSI8/SSDA8/MISOA			CACREF
G6		PC6	MTIOC3C/MTCLKA/TMC12	RXD8/SMISO8/SSCL8/MOSIA/USB0_EXICEN		TS22	
G7		PC3	MTIOC4D/TCLKB	TXD5/SMOSI5/SSDA5/IRTXD5	SDHI_D0	TS27	
G8		PB6/PC0	MTIOC3D/TIOCA5	RXD9/SMISO9/SSCL9	SDHI_D1		
H1	XTAL	P37					
H2		P17	MTIOC3A/MTIOC3B/TMO1/POE8#/TIOCB0/TCLKD	SCK1/MISOA/SDA/SSITXD0			IRQ7/CMPOB2
H3		PH2*1	TMRI0*1	USB0_DM*1			IRQ1*1
H4		PH1*1	TMO0*1	USB0_DP*1			IRQ0*1
H5		P55	MTIOC4D/TMO3	CRXD0		TS15	
H6		P54	MTIOC4B/TMC11	CTXD0		TS16	
H7		PC2	MTIOC4B/TCLKA	RXD5/SMISO5/SSCL5/SSLA3/IRRXD5	SDHI_D3	TS30	
H8		PB7/PC1	MTIOC3B/TIOCB5	TXD9/SMOSI9/SSDA9	SDHI_D2		

Note 1. RX230: PH0/CACREF, PH1/IRQ0/TMO0, PH2/IRQ1/TMRI0, PH3/TMC10
 RX231: VSS_USB, USB0_DP, USB0_DM, VCC_USB

(9) Floating-point status word (FPSW)

The floating-point status word (FPSW) indicates the results of floating-point operations.

When an exception handling enable bit (Ej) enables the exception handling (Ej = 1), the exception cause can be identified by checking the corresponding Cj flag in the exception handling routine. If the exception handling is masked (Ej = 0), the occurrence of exception can be checked by reading the Fj flag at the end of a series of processing. Once the Fj flag has been set to 1, this value is retained until it is cleared to 0 by software (j = X, U, Z, O, or V).

2.3 Accumulator

The accumulator (ACC0 or ACC1) is a 72-bit register used for DSP instructions. The accumulator is handled as a 96-bit register for reading and writing. At this time, when bits 95 to 72 of the accumulator are read, the value where the value of bit 71 is sign extended is read. Writing to bits 95 to 72 of the accumulator is ignored. ACC0 is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, FMUL, MUL, and RMPA, in which case the prior value in ACC0 is modified by execution of the instruction.

Use the MVTACGU, MVTACHI, and MVTACLO instructions for writing to the accumulator. The MVTACGU, MVTACHI, and MVTACLO instructions write data to bits 95 to 64, the higher-order 32 bits (bits 63 to 32), and the lower-order 32 bits (bits 31 to 0), respectively.

Use the MVFACGU, MVFACHI, MVFACMI, and MVFACLO instructions for reading data from the accumulator. The MVFACGU, MVFACHI, MVFACMI, and MVFACLO instructions read data from the guard bits (bits 95 to 64), higher-order 32 bits (bits 63 to 32), the middle 32 bits (bits 47 to 16), and the lower-order 32 bits (bits 31 to 0), respectively.

4.1 I/O Register Addresses (Address Order)

Table 4.1 List of I/O Registers (Address Order) (1/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK $\geq$ PCLK	ICLK < PCLK
0008 0000h	SYSTEM	Mode Monitor Register	MDMONR	16	16	3 ICLK	
0008 0006h	SYSTEM	System Control Register 0	SYSCR0	16	16	3 ICLK	
0008 0008h	SYSTEM	System Control Register 1	SYSCR1	16	16	3 ICLK	
0008 000Ch	SYSTEM	Standby Control Register	SBYCR	16	16	3 ICLK	
0008 0010h	SYSTEM	Module Stop Control Register A	MSTPCRA	32	32	3 ICLK	
0008 0014h	SYSTEM	Module Stop Control Register B	MSTPCRB	32	32	3 ICLK	
0008 0018h	SYSTEM	Module Stop Control Register C	MSTPCRC	32	32	3 ICLK	
0008 001Ch	SYSTEM	Module Stop Control Register D	MSTPCRD	32	32	3 ICLK	
0008 0020h	SYSTEM	System Clock Control Register	SCKCR	32	32	3 ICLK	
0008 0026h	SYSTEM	System Clock Control Register 3	SCKCR3	16	16	3 ICLK	
0008 0028h	SYSTEM	PLL Control Register	PLLCR	16	16	3 ICLK	
0008 002Ah	SYSTEM	PLL Control Register 2	PLLCR2	8	8	3 ICLK	
0008 002Ch	SYSTEM	USB-dedicated PLL Control Register	UPLLCR	16	16	3 ICLK	
0008 002Eh	SYSTEM	USB-dedicated PLL Control Register 2	UPLLCR2	8	8	3 ICLK	
0008 0030h	SYSTEM	External Bus Clock Control Register	BCKCR	8	8	3 ICLK	
0008 0031h	SYSTEM	Memory Wait Cycle Setting Register	MEMWAIT	8	8	3 ICLK	
0008 0032h	SYSTEM	Main Clock Oscillator Control Register	MOSCCR	8	8	3 ICLK	
0008 0033h	SYSTEM	Sub-Clock Oscillator Control Register	SOSCCR	8	8	3 ICLK	
0008 0034h	SYSTEM	Low-Speed On-Chip Oscillator Control Register	LOCOCR	8	8	3 ICLK	
0008 0035h	SYSTEM	IWDT-Dedicated On-Chip Oscillator Control Register	ILOCOCR	8	8	3 ICLK	
0008 0036h	SYSTEM	High-Speed On-Chip Oscillator Control Register	HOCOCR	8	8	3 ICLK	
0008 0037h	SYSTEM	High-Speed On-Chip Oscillator Control Register 2	HOCOCR2	8	8	3 ICLK	
0008 003Ch	SYSTEM	Oscillation Stabilization Flag Register	OSCOVFSR	8	8	3 ICLK	
0008 003Eh	SYSTEM	CLKOUT Output Control Register	CKOCR	16	16	3 ICLK	
0008 0040h	SYSTEM	Oscillation Stop Detection Control Register	OSTDCR	8	8	3 ICLK	
0008 0041h	SYSTEM	Oscillation Stop Detection Status Register	OSTDSR	8	8	3 ICLK	
0008 0060h	SYSTEM	Low-Speed On-Chip Oscillator Trimming Register	LOCOTRR	8	8	3 ICLK	
0008 0064h	SYSTEM	IWDT-Dedicated On-Chip Oscillator Trimming Register	ILOCOTRR	8	8	3 ICLK	
0008 0068h	SYSTEM	High-Speed On-Chip Oscillator Trimming Register 0	HOCOTRR0	8	8	3 ICLK	
0008 006Bh	SYSTEM	High-Speed On-Chip Oscillator Trimming Register 3	HOCOTRR3	8	8	3 ICLK	
0008 00A0h	SYSTEM	Operating Power Control Register	OPCCR	8	8	3 ICLK	
0008 00A1h	SYSTEM	Sleep Mode Return Clock Source Switching Register	RSTCKCR	8	8	3 ICLK	
0008 00A2h	SYSTEM	Main Clock Oscillator Wait Control Register	MOSCWTCR	8	8	3 ICLK	
0008 00AAh	SYSTEM	Sub Operating Power Control Register	SOPCCR	8	8	3 ICLK	
0008 00B0h	LPT	Low-Power Timer Control Register 1	LPTCR1	8	8	3 ICLK	
0008 00B1h	LPT	Low-Power Timer Control Register 2	LPTCR2	8	8	3 ICLK	
0008 00B2h	LPT	Low-Power Timer Control Register 3	LPTCR3	8	8	3 ICLK	
0008 00B4h	LPT	Low-Power Timer Cycle Setting Register	LPTPRD	16	16	3 ICLK	
0008 00B8h	LPT	Low-Power Timer Compare Register 0	LPCMR0	16	16	3 ICLK	
0008 00BCh	LPT	Low-Power Timer Standby Return Enable Register	LPWUCR	16	16	3 ICLK	
0008 00C0h	SYSTEM	Reset Status Register 2	RSTSR2	8	8	3 ICLK	
0008 00C2h	SYSTEM	Software Reset Register	SWRR	16	16	3 ICLK	
0008 00E0h	SYSTEM	Voltage Monitoring 1 Circuit Control Register 1	LVD1CR1	8	8	3 ICLK	
0008 00E1h	SYSTEM	Voltage Monitoring 1 Circuit Status Register	LVD1SR	8	8	3 ICLK	
0008 00E2h	SYSTEM	Voltage Monitoring 2 Circuit Control Register 1	LVD2CR1	8	8	3 ICLK	
0008 00E3h	SYSTEM	Voltage Monitoring 2 Circuit Status Register	LVD2SR	8	8	3 ICLK	
0008 03FEh	SYSTEM	Protect Register	PRCR	16	16	3 ICLK	
0008 1300h	BSC	Bus Error Status Clear Register	BERCLR	8	8	2 ICLK	
0008 1304h	BSC	Bus Error Monitoring Enable Register	BEREN	8	8	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (14/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK $\geq$ PCLK	ICLK < PCLK
0008 B003h	CAC	CAC Interrupt Request Enable Register	CAICR	8	8	2 or 3 PCLKB	2 ICLK
0008 B004h	CAC	CAC Status Register	CASTR	8	8	2 or 3 PCLKB	2 ICLK
0008 B006h	CAC	CAC Upper-Limit Value Setting Register	CAULVR	16	16	2 or 3 PCLKB	2 ICLK
0008 B008h	CAC	CAC Lower-Limit Value Setting Register	CALLVR	16	16	2 or 3 PCLKB	2 ICLK
0008 B00Ah	CAC	CAC Counter Buffer Register	CACNTBR	16	16	2 or 3 PCLKB	2 ICLK
0008 B080h	DOC	DOC Control Register	DOCR	8	8	2 or 3 PCLKB	2 ICLK
0008 B082h	DOC	DOC Data Input Register	DODIR	16	16	2 or 3 PCLKB	2 ICLK
0008 B084h	DOC	DOC Data Setting Register	DODSR	16	16	2 or 3 PCLKB	2 ICLK
0008 B100h	ELC	Event Link Control Register	ELCR	8	8	2 or 3 PCLKB	2 ICLK
0008 B102h	ELC	Event Link Setting Register 1	ELSR1	8	8	2 or 3 PCLKB	2 ICLK
0008 B103h	ELC	Event Link Setting Register 2	ELSR2	8	8	2 or 3 PCLKB	2 ICLK
0008 B104h	ELC	Event Link Setting Register 3	ELSR3	8	8	2 or 3 PCLKB	2 ICLK
0008 B105h	ELC	Event Link Setting Register 4	ELSR4	8	8	2 or 3 PCLKB	2 ICLK
0008 B108h	ELC	Event Link Setting Register 7	ELSR7	8	8	2 or 3 PCLKB	2 ICLK
0008 B109h	ELC	Event Link Setting Register 8	ELSR8	8	8	2 or 3 PCLKB	2 ICLK
0008 B10Bh	ELC	Event Link Setting Register 10	ELSR10	8	8	2 or 3 PCLKB	2 ICLK
0008 B10Dh	ELC	Event Link Setting Register 12	ELSR12	8	8	2 or 3 PCLKB	2 ICLK
0008 B10Fh	ELC	Event Link Setting Register 14	ELSR14	8	8	2 or 3 PCLKB	2 ICLK
0008 B110h	ELC	Event Link Setting Register 15	ELSR15	8	8	2 or 3 PCLKB	2 ICLK
0008 B111h	ELC	Event Link Setting Register 16	ELSR16	8	8	2 or 3 PCLKB	2 ICLK
0008 B113h	ELC	Event Link Setting Register 18	ELSR18	8	8	2 or 3 PCLKB	2 ICLK
0008 B114h	ELC	Event Link Setting Register 19	ELSR19	8	8	2 or 3 PCLKB	2 ICLK
0008 B115h	ELC	Event Link Setting Register 20	ELSR20	8	8	2 or 3 PCLKB	2 ICLK
0008 B116h	ELC	Event Link Setting Register 21	ELSR21	8	8	2 or 3 PCLKB	2 ICLK
0008 B117h	ELC	Event Link Setting Register 22	ELSR22	8	8	2 or 3 PCLKB	2 ICLK
0008 B118h	ELC	Event Link Setting Register 23	ELSR23	8	8	2 or 3 PCLKB	2 ICLK
0008 B119h	ELC	Event Link Setting Register 24	ELSR24	8	8	2 or 3 PCLKB	2 ICLK
0008 B11Ah	ELC	Event Link Setting Register 25	ELSR25	8	8	2 or 3 PCLKB	2 ICLK
0008 B11Bh	ELC	Event Link Setting Register 26	ELSR26	8	8	2 or 3 PCLKB	2 ICLK
0008 B11Ch	ELC	Event Link Setting Register 27	ELSR27	8	8	2 or 3 PCLKB	2 ICLK
0008 B11Dh	ELC	Event Link Setting Register 28	ELSR28	8	8	2 or 3 PCLKB	2 ICLK
0008 B11Eh	ELC	Event Link Setting Register 29	ELSR29	8	8	2 or 3 PCLKB	2 ICLK
0008 B11Fh	ELC	Event Link Option Setting Register A	ELOPA	8	8	2 or 3 PCLKB	2 ICLK
0008 B120h	ELC	Event Link Option Setting Register B	ELOPB	8	8	2 or 3 PCLKB	2 ICLK
0008 B121h	ELC	Event Link Option Setting Register C	ELOPC	8	8	2 or 3 PCLKB	2 ICLK
0008 B122h	ELC	Event Link Option Setting Register D	ELOPD	8	8	2 or 3 PCLKB	2 ICLK
0008 B123h	ELC	Port Group Setting Register 1	PGR1	8	8	2 or 3 PCLKB	2 ICLK
0008 B124h	ELC	Port Group Setting Register 2	PGR2	8	8	2 or 3 PCLKB	2 ICLK
0008 B125h	ELC	Port Group Control Register 1	PGC1	8	8	2 or 3 PCLKB	2 ICLK
0008 B126h	ELC	Port Group Control Register 2	PGC2	8	8	2 or 3 PCLKB	2 ICLK
0008 B127h	ELC	Port Buffer Register 1	PDBF1	8	8	2 or 3 PCLKB	2 ICLK
0008 B128h	ELC	Port Buffer Register 2	PDBF2	8	8	2 or 3 PCLKB	2 ICLK
0008 B129h	ELC	Event Link Port Setting Register 0	PEL0	8	8	2 or 3 PCLKB	2 ICLK
0008 B12Ah	ELC	Event Link Port Setting Register 1	PEL1	8	8	2 or 3 PCLKB	2 ICLK
0008 B12Bh	ELC	Event Link Port Setting Register 2	PEL2	8	8	2 or 3 PCLKB	2 ICLK
0008 B12Ch	ELC	Event Link Port Setting Register 3	PEL3	8	8	2 or 3 PCLKB	2 ICLK
0008 B12Dh	ELC	Event Link Software Event Generation Register	ELSEGR	8	8	2 or 3 PCLKB	2 ICLK
0008 B300h	SCI12	Serial Mode Register	SMR	8	8	2 or 3 PCLKB	2 ICLK
0008 B301h	SCI12	Bit Rate Register	BRR	8	8	2 or 3 PCLKB	2 ICLK
0008 B302h	SCI12	Serial Control Register	SCR	8	8	2 or 3 PCLKB	2 ICLK
0008 B303h	SCI12	Transmit Data Register	TDR	8	8	2 or 3 PCLKB	2 ICLK
0008 B304h	SCI12	Serial Status Register	SSR	8	8	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (23/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
000A 00B0h	USB0	BC Control Register 0	USBBCCTRL0	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ²
000A 00CCh	USB0	USB Module Control Register	USBMC	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ²
000A 00D0h	USB0	Device Address 0 Configuration Register	DEVADD0	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ²
000A 00D2h	USB0	Device Address 1 Configuration Register	DEVADD1	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ²
000A 00D4h	USB0	Device Address 2 Configuration Register	DEVADD2	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ²
000A 00D6h	USB0	Device Address 3 Configuration Register	DEVADD3	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ²
000A 00D8h	USB0	Device Address 4 Configuration Register	DEVADD4	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ²
000A 00DAh	USB0	Device Address 5 Configuration Register	DEVADD5	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ²
000A 0900h	CTSU	CTSU Control Register 0	CTSUCR0	8	8	2 or 3 PCLKB	2 ICLK
000A 0901h	CTSU	CTSU Control Register 1	CTSUCR1	8	8	2 or 3 PCLKB	2 ICLK
000A 0902h	CTSU	CTSU Synchronous Noise Reduction Setting Register	CTSUSDPRS	8	8	2 or 3 PCLKB	2 ICLK
000A 0903h	CTSU	CTSU Sensor Stabilization Wait Control Register	CTSUSST	8	8	2 or 3 PCLKB	2 ICLK
000A 0904h	CTSU	CTSU Measurement Channel Register 0	CTSUMCH0	8	8	2 or 3 PCLKB	2 ICLK
000A 0905h	CTSU	CTSU Measurement Channel Register 1	CTSUMCH1	8	8	2 or 3 PCLKB	2 ICLK
000A 0906h	CTSU	CTSU Channel Enable Control Register 0	CTSUCHAC0	8	8	2 or 3 PCLKB	2 ICLK
000A 0907h	CTSU	CTSU Channel Enable Control Register 1	CTSUCHAC1	8	8	2 or 3 PCLKB	2 ICLK
000A 0908h	CTSU	CTSU Channel Enable Control Register 2	CTSUCHAC2	8	8	2 or 3 PCLKB	2 ICLK
000A 0909h	CTSU	CTSU Channel Enable Control Register 3	CTSUCHAC3	8	8	2 or 3 PCLKB	2 ICLK
000A 090Ah	CTSU	CTSU Channel Enable Control Register 4	CTSUCHAC4	8	8	2 or 3 PCLKB	2 ICLK
000A 090Bh	CTSU	CTSU Channel Transmit/Receive Control Register 0	CTSUCHTRC0	8	8	2 or 3 PCLKB	2 ICLK
000A 090Ch	CTSU	CTSU Channel Transmit/Receive Control Register 1	CTSUCHTRC1	8	8	2 or 3 PCLKB	2 ICLK
000A 090Dh	CTSU	CTSU Channel Transmit/Receive Control Register 2	CTSUCHTRC2	8	8	2 or 3 PCLKB	2 ICLK
000A 090Eh	CTSU	CTSU Channel Transmit/Receive Control Register 3	CTSUCHTRC3	8	8	2 or 3 PCLKB	2 ICLK
000A 090Fh	CTSU	CTSU Channel Transmit/Receive Control Register 4	CTSUCHTRC4	8	8	2 or 3 PCLKB	2 ICLK
000A 0910h	CTSU	CTSU High-Pass Noise Reduction Control Register	CTSUDCLKC	8	8	2 or 3 PCLKB	2 ICLK
000A 0911h	CTSU	CTSU Status Register	CTSUST	8	8	2 or 3 PCLKB	2 ICLK
000A 0912h	CTSU	CTSU High-Pass Noise Reduction Spectrum Diffusion Control Register	CTSUSSC	16	16	2 or 3 PCLKB	2 ICLK
000A 0914h	CTSU	CTSU Sensor Offset Register 0	CTSUSO0	16	16	2 or 3 PCLKB	2 ICLK
000A 0916h	CTSU	CTSU Sensor Offset Register 1	CTSUSO1	16	16	2 or 3 PCLKB	2 ICLK
000A 0918h	CTSU	CTSU Sensor Counter	CTSUSC	16	16	2 or 3 PCLKB	2 ICLK
000A 091Ah	CTSU	CTSU Reference Counter	CTSURC	16	16	2 or 3 PCLKB	2 ICLK
000A 091Ch	CTSU	CTSU Error Status Register	CTSUERRS	16	16	2 or 3 PCLKB	2 ICLK
000A 8300h	RSCAN0	Bit Configuration Register L	CFGL	16	16	2 or 3 PCLKB	2 ICLK
000A 8302h	RSCAN0	Bit Configuration Register H	CFGH	16	16	2 or 3 PCLKB	2 ICLK
000A 8304h	RSCAN0	Control Register L	CTRL	16	16	2 or 3 PCLKB	2 ICLK
000A 8306h	RSCAN0	Control Register H	CTRH	16	16	2 or 3 PCLKB	2 ICLK
000A 8308h	RSCAN0	Status Register L	STSL	16	16	2 or 3 PCLKB	2 ICLK
000A 830Ah	RSCAN0	Status Register H	STSH	16	16	2 or 3 PCLKB	2 ICLK
000A 830Ch	RSCAN0	Error Flag Register L	ERFLL	16	16	2 or 3 PCLKB	2 ICLK
000A 830Eh	RSCAN0	Error Flag Register H	ERFLH	16	16	2 or 3 PCLKB	2 ICLK
000A 8322h	RSCAN	Global Configuration Register L	GCFGFL	16	16	2 or 3 PCLKB	2 ICLK
000A 8324h	RSCAN	Global Configuration Register H	GCFGH	16	16	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (25/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
000A 83AAh	RSCAN	Receive Rule Entry Register 0CH	GAFLPH0	16	16	2 or 3 PCLKB	2 ICLK
000A 83AAh	RSCAN	Receive Buffer Register 0CH	RMDF10	16	16	2 or 3 PCLKB	2 ICLK
000A 83ACh	RSCAN	Receive Rule Entry Register 1AL	GAFLIDL1	16	16	2 or 3 PCLKB	2 ICLK
000A 83ACh	RSCAN	Receive Buffer Register 0DL	RMDF20	16	16	2 or 3 PCLKB	2 ICLK
000A 83AEh	RSCAN	Receive Rule Entry Register 1AH	GAFLIDH1	16	16	2 or 3 PCLKB	2 ICLK
000A 83AEh	RSCAN	Receive Buffer Register 0DH	RMDF30	16	16	2 or 3 PCLKB	2 ICLK
000A 83B0h	RSCAN	Receive Rule Entry Register 1BL	GAFLML1	16	16	2 or 3 PCLKB	2 ICLK
000A 83B0h	RSCAN	Receive Buffer Register 1AL	RMIDL1	16	16	2 or 3 PCLKB	2 ICLK
000A 83B2h	RSCAN	Receive Rule Entry Register 1BH	GAFLMH1	16	16	2 or 3 PCLKB	2 ICLK
000A 83B2h	RSCAN	Receive Buffer Register 1AH	RMIDH1	16	16	2 or 3 PCLKB	2 ICLK
000A 83B4h	RSCAN	Receive Rule Entry Register 1CL	GAFLPL1	16	16	2 or 3 PCLKB	2 ICLK
000A 83B4h	RSCAN	Receive Buffer Register 1BL	RMTS1	16	16	2 or 3 PCLKB	2 ICLK
000A 83B6h	RSCAN	Receive Rule Entry Register 1CH	GAFLPH1	16	16	2 or 3 PCLKB	2 ICLK
000A 83B6h	RSCAN	Receive Buffer Register 1BH	RMPTR1	16	16	2 or 3 PCLKB	2 ICLK
000A 83B8h	RSCAN	Receive Rule Entry Register 2AL	GAFLIDL2	16	16	2 or 3 PCLKB	2 ICLK
000A 83B8h	RSCAN	Receive Buffer Register 1CL	RMDF01	16	16	2 or 3 PCLKB	2 ICLK
000A 83BAh	RSCAN	Receive Rule Entry Register 2AH	GAFLIDH2	16	16	2 or 3 PCLKB	2 ICLK
000A 83BAh	RSCAN	Receive Buffer Register 1CH	RMDF11	16	16	2 or 3 PCLKB	2 ICLK
000A 83BCh	RSCAN	Receive Rule Entry Register 2BL	GAFLML2	16	16	2 or 3 PCLKB	2 ICLK
000A 83BCh	RSCAN	Receive Buffer Register 1DL	RMDF21	16	16	2 or 3 PCLKB	2 ICLK
000A 83BEh	RSCAN	Receive Rule Entry Register 2BH	GAFLMH2	16	16	2 or 3 PCLKB	2 ICLK
000A 83BEh	RSCAN	Receive Buffer Register 1DH	RMDF31	16	16	2 or 3 PCLKB	2 ICLK
000A 83C0h	RSCAN	Receive Rule Entry Register 2CL	GAFLPL2	16	16	2 or 3 PCLKB	2 ICLK
000A 83C0h	RSCAN	Receive Buffer Register 2AL	RMIDL2	16	16	2 or 3 PCLKB	2 ICLK
000A 83C2h	RSCAN	Receive Rule Entry Register 2CH	GAFLPH2	16	16	2 or 3 PCLKB	2 ICLK
000A 83C2h	RSCAN	Receive Buffer Register 2AH	RMIDH2	16	16	2 or 3 PCLKB	2 ICLK
000A 83C4h	RSCAN	Receive Rule Entry Register 3AL	GAFLIDL3	16	16	2 or 3 PCLKB	2 ICLK
000A 83C4h	RSCAN	Receive Buffer Register 2BL	RMTS2	16	16	2 or 3 PCLKB	2 ICLK
000A 83C6h	RSCAN	Receive Rule Entry Register 3AH	GAFLIDH3	16	16	2 or 3 PCLKB	2 ICLK
000A 83C6h	RSCAN	Receive Buffer Register 2BH	RMPTR2	16	16	2 or 3 PCLKB	2 ICLK
000A 83C8h	RSCAN	Receive Rule Entry Register 3BL	GAFLML3	16	16	2 or 3 PCLKB	2 ICLK
000A 83C8h	RSCAN	Receive Buffer Register 2CL	RMDF02	16	16	2 or 3 PCLKB	2 ICLK
000A 83CAh	RSCAN	Receive Rule Entry Register 3BH	GAFLMH3	16	16	2 or 3 PCLKB	2 ICLK
000A 83CAh	RSCAN	Receive Buffer Register 2CH	RMDF12	16	16	2 or 3 PCLKB	2 ICLK
000A 83CCh	RSCAN	Receive Rule Entry Register 3CL	GAFLPL3	16	16	2 or 3 PCLKB	2 ICLK
000A 83CCh	RSCAN	Receive Buffer Register 2DL	RMDF22	16	16	2 or 3 PCLKB	2 ICLK
000A 83CEh	RSCAN	Receive Rule Entry Register 3CH	GAFLPH3	16	16	2 or 3 PCLKB	2 ICLK
000A 83CEh	RSCAN	Receive Buffer Register 2DH	RMDF32	16	16	2 or 3 PCLKB	2 ICLK
000A 83D0h	RSCAN	Receive Rule Entry Register 4AL	GAFLIDL4	16	16	2 or 3 PCLKB	2 ICLK
000A 83D0h	RSCAN	Receive Buffer Register 3AL	RMIDL3	16	16	2 or 3 PCLKB	2 ICLK
000A 83D2h	RSCAN	Receive Rule Entry Register 4AH	GAFLIDH4	16	16	2 or 3 PCLKB	2 ICLK
000A 83D2h	RSCAN	Receive Buffer Register 3AH	RMIDH3	16	16	2 or 3 PCLKB	2 ICLK
000A 83D4h	RSCAN	Receive Rule Entry Register 4BL	GAFLML4	16	16	2 or 3 PCLKB	2 ICLK
000A 83D4h	RSCAN	Receive Buffer Register 3BL	RMTS3	16	16	2 or 3 PCLKB	2 ICLK
000A 83D6h	RSCAN	Receive Rule Entry Register 4BH	GAFLMH4	16	16	2 or 3 PCLKB	2 ICLK
000A 83D6h	RSCAN	Receive Buffer Register 3BH	RMPTR3	16	16	2 or 3 PCLKB	2 ICLK
000A 83D8h	RSCAN	Receive Rule Entry Register 4CL	GAFLPL4	16	16	2 or 3 PCLKB	2 ICLK
000A 83D8h	RSCAN	Receive Buffer Register 3CL	RMDF03	16	16	2 or 3 PCLKB	2 ICLK
000A 83DAh	RSCAN	Receive Rule Entry Register 4CH	GAFLPH4	16	16	2 or 3 PCLKB	2 ICLK
000A 83DAh	RSCAN	Receive Buffer Register 3CH	RMDF13	16	16	2 or 3 PCLKB	2 ICLK
000A 83DCh	RSCAN	Receive Rule Entry Register 5AL	GAFLIDL5	16	16	2 or 3 PCLKB	2 ICLK
000A 83DCh	RSCAN	Receive Buffer Register 3DL	RMDF23	16	16	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (26/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
000A 83DEh	RSCAN	Receive Rule Entry Register 5AH	GAFLIDH5	16	16	2 or 3 PCLKB	2 ICLK
000A 83DEh	RSCAN	Receive Buffer Register 3DH	RMDF33	16	16	2 or 3 PCLKB	2 ICLK
000A 83E0h	RSCAN	Receive Rule Entry Register 5BL	GAFLML5	16	16	2 or 3 PCLKB	2 ICLK
000A 83E0h	RSCAN	Receive Buffer Register 4AL	RMIDL4	16	16	2 or 3 PCLKB	2 ICLK
000A 83E2h	RSCAN	Receive Rule Entry Register 5BH	GAFLMH5	16	16	2 or 3 PCLKB	2 ICLK
000A 83E2h	RSCAN	Receive Buffer Register 4AH	RMIDH4	16	16	2 or 3 PCLKB	2 ICLK
000A 83E4h	RSCAN	Receive Rule Entry Register 5CL	GAFLPL5	16	16	2 or 3 PCLKB	2 ICLK
000A 83E4h	RSCAN	Receive Buffer Register 4BL	RMTS4	16	16	2 or 3 PCLKB	2 ICLK
000A 83E6h	RSCAN	Receive Rule Entry Register 5CH	GAFLPH5	16	16	2 or 3 PCLKB	2 ICLK
000A 83E6h	RSCAN	Receive Buffer Register 4BH	RMPTR4	16	16	2 or 3 PCLKB	2 ICLK
000A 83E8h	RSCAN	Receive Rule Entry Register 6AL	GAFLIDL6	16	16	2 or 3 PCLKB	2 ICLK
000A 83E8h	RSCAN	Receive Buffer Register 4CL	RMDF04	16	16	2 or 3 PCLKB	2 ICLK
000A 83EAh	RSCAN	Receive Rule Entry Register 6AH	GAFLIDH6	16	16	2 or 3 PCLKB	2 ICLK
000A 83EAh	RSCAN	Receive Buffer Register 4CH	RMDF14	16	16	2 or 3 PCLKB	2 ICLK
000A 83ECh	RSCAN	Receive Rule Entry Register 6BL	GAFLML6	16	16	2 or 3 PCLKB	2 ICLK
000A 83ECh	RSCAN	Receive Buffer Register 4DL	RMDF24	16	16	2 or 3 PCLKB	2 ICLK
000A 83EEh	RSCAN	Receive Rule Entry Register 6BH	GAFLMH6	16	16	2 or 3 PCLKB	2 ICLK
000A 83EEh	RSCAN	Receive Buffer Register 4DH	RMDF34	16	16	2 or 3 PCLKB	2 ICLK
000A 83F0h	RSCAN	Receive Rule Entry Register 6CL	GAFLPL6	16	16	2 or 3 PCLKB	2 ICLK
000A 83F0h	RSCAN	Receive Buffer Register 5AL	RMIDL5	16	16	2 or 3 PCLKB	2 ICLK
000A 83F2h	RSCAN	Receive Rule Entry Register 6CH	GAFLPH6	16	16	2 or 3 PCLKB	2 ICLK
000A 83F2h	RSCAN	Receive Buffer Register 5AH	RMIDH5	16	16	2 or 3 PCLKB	2 ICLK
000A 83F4h	RSCAN	Receive Rule Entry Register 7AL	GAFLIDL7	16	16	2 or 3 PCLKB	2 ICLK
000A 83F4h	RSCAN	Receive Buffer Register 5BL	RMTS5	16	16	2 or 3 PCLKB	2 ICLK
000A 83F6h	RSCAN	Receive Rule Entry Register 7AH	GAFLIDH7	16	16	2 or 3 PCLKB	2 ICLK
000A 83F6h	RSCAN	Receive Buffer Register 5BH	RMPTR5	16	16	2 or 3 PCLKB	2 ICLK
000A 83F8h	RSCAN	Receive Rule Entry Register 7BL	GAFLML7	16	16	2 or 3 PCLKB	2 ICLK
000A 83F8h	RSCAN	Receive Buffer Register 5CL	RMDF05	16	16	2 or 3 PCLKB	2 ICLK
000A 83FAh	RSCAN	Receive Rule Entry Register 7BH	GAFLMH7	16	16	2 or 3 PCLKB	2 ICLK
000A 83FAh	RSCAN	Receive Buffer Register 5CH	RMDF15	16	16	2 or 3 PCLKB	2 ICLK
000A 83FCh	RSCAN	Receive Rule Entry Register 7CL	GAFLPL7	16	16	2 or 3 PCLKB	2 ICLK
000A 83FCh	RSCAN	Receive Buffer Register 5DL	RMDF25	16	16	2 or 3 PCLKB	2 ICLK
000A 83FEh	RSCAN	Receive Rule Entry Register 7CH	GAFLPH7	16	16	2 or 3 PCLKB	2 ICLK
000A 83FEh	RSCAN	Receive Buffer Register 5DH	RMDF35	16	16	2 or 3 PCLKB	2 ICLK
000A 8400h	RSCAN	Receive Rule Entry Register 8AL	GAFLIDL8	16	16	2 or 3 PCLKB	2 ICLK
000A 8400h	RSCAN	Receive Buffer Register 6AL	RMIDL6	16	16	2 or 3 PCLKB	2 ICLK
000A 8402h	RSCAN	Receive Rule Entry Register 8AH	GAFLIDH8	16	16	2 or 3 PCLKB	2 ICLK
000A 8402h	RSCAN	Receive Buffer Register 6AH	RMIDH6	16	16	2 or 3 PCLKB	2 ICLK
000A 8404h	RSCAN	Receive Rule Entry Register 8BL	GAFLML8	16	16	2 or 3 PCLKB	2 ICLK
000A 8404h	RSCAN	Receive Buffer Register 6BL	RMTS6	16	16	2 or 3 PCLKB	2 ICLK
000A 8406h	RSCAN	Receive Rule Entry Register 8BH	GAFLMH8	16	16	2 or 3 PCLKB	2 ICLK
000A 8406h	RSCAN	Receive Buffer Register 6BH	RMPTR6	16	16	2 or 3 PCLKB	2 ICLK
000A 8408h	RSCAN	Receive Rule Entry Register 8CL	GAFLPL8	16	16	2 or 3 PCLKB	2 ICLK
000A 8408h	RSCAN	Receive Buffer Register 6CL	RMDF06	16	16	2 or 3 PCLKB	2 ICLK
000A 840Ah	RSCAN	Receive Rule Entry Register 8CH	GAFLPH8	16	16	2 or 3 PCLKB	2 ICLK
000A 840Ah	RSCAN	Receive Buffer Register 6CH	RMDF16	16	16	2 or 3 PCLKB	2 ICLK
000A 840Ch	RSCAN	Receive Rule Entry Register 9AL	GAFLIDL9	16	16	2 or 3 PCLKB	2 ICLK
000A 840Ch	RSCAN	Receive Buffer Register 6DL	RMDF26	16	16	2 or 3 PCLKB	2 ICLK
000A 840Eh	RSCAN	Receive Rule Entry Register 9AH	GAFLIDH9	16	16	2 or 3 PCLKB	2 ICLK
000A 840Eh	RSCAN	Receive Buffer Register 6DH	RMDF36	16	16	2 or 3 PCLKB	2 ICLK
000A 8410h	RSCAN	Receive Rule Entry Register 9BL	GAFLML9	16	16	2 or 3 PCLKB	2 ICLK
000A 8410h	RSCAN	Receive Buffer Register 7AL	RMIDL7	16	16	2 or 3 PCLKB	2 ICLK

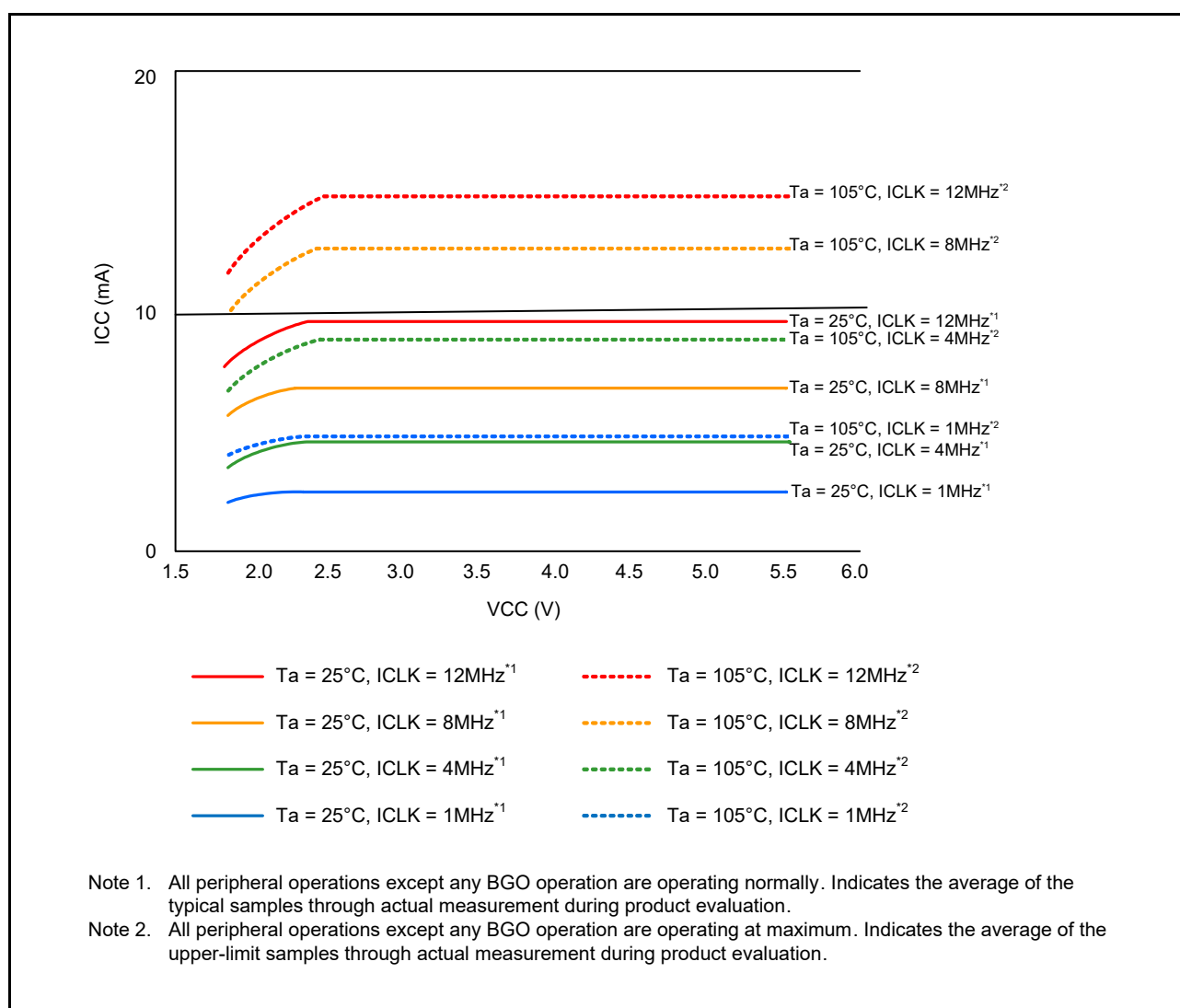


Figure 5.2 Voltage Dependency in Middle-Speed Operating Mode (Reference Data)

Table 5.18 Output Values of Voltage (1)Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} = AV_{CC0} < 2.7\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40$ to $+105^\circ\text{C}$

Item				Symbol	Min.	Max.	Unit	Test Conditions
Output low	All output ports	Normal output mode		V _{OL}	—	0.3	V	I _{OL} = 0.5 mA
		High-drive output mode			—	0.3		I _{OL} = 1.0 mA
Output high	All output ports	Normal output mode	Ports 03, 05, 07, Ports 40 to 47	V _{OH}	AVCC0 – 0.3	—	V	I _{OH} = –0.5 mA
			Ports other than above		VCC – 0.3	—		
		High-drive output mode				VCC – 0.3		—

Table 5.19 Output Values of Voltage (2)Conditions: $2.7\text{ V} \leq V_{CC} = V_{CC_USB} = AV_{CC0} < 4.0\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40$ to $+105^\circ\text{C}$

Item				Symbol	Min.	Max.	Unit	Test Conditions
Output low	All output ports (except for RIIC)	Normal output mode		V _{OL}	—	0.5	V	I _{OL} = 1.0 mA
		High-drive output mode			—	0.5		I _{OL} = 2.0 mA
	RIIC pins	Standard mode (Normal output mode)			—	0.4		I _{OL} = 3.0 mA
		Fast mode (High-drive output mode)			—	0.6		I _{OL} = 6.0 mA
Output high	All output ports	Normal output mode	Ports 03, 05, 07, Ports 40 to 47	V _{OH}	AVCC0 – 0.5	—	V	I _{OH} = –1.0 mA
			Ports other than above		VCC – 0.5			
		High-drive output mode			VCC – 0.5	—		I _{OH} = –2.0 mA

Table 5.20 Output Values of Voltage (3)Conditions: $4.0\text{ V} \leq V_{CC} = V_{CC_USB} = AV_{CC0} \leq 5.5\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40$ to $+105^\circ\text{C}$

Item				Symbol	Min.	Max.	Unit	Test Conditions
Output low	All output ports (except for RIIC)	Normal output mode		V_{OL}	—	0.8	V	$I_{OL} = 2.0\text{ mA}$
		High-drive output mode			—	0.8		$I_{OL} = 4.0\text{ mA}$
	RIIC pins	Standard mode(Normal output mode)			—	0.4		$I_{OL} = 3.0\text{ mA}$
		Fast mode (High-drive output mode)			—	0.6		$I_{OL} = 6.0\text{ mA}$
Output high	All output ports	Normal output mode	Ports 03, 05, 07, Ports 40 to 47	V_{OH}	$AVCC0 - 0.8$	—	V	$I_{OH} = -2.0\text{ mA}$
			Ports other than above		$VCC - 0.8$	—		
		High-drive output mode			$VCC - 0.8$	—		$I_{OH} = -4.0\text{ mA}$

5.2.1 Normal I/O Pin Output Characteristics (1)

Figure 5.8 to Figure 5.12 show the characteristics when normal output is selected by the drive capacity control register.

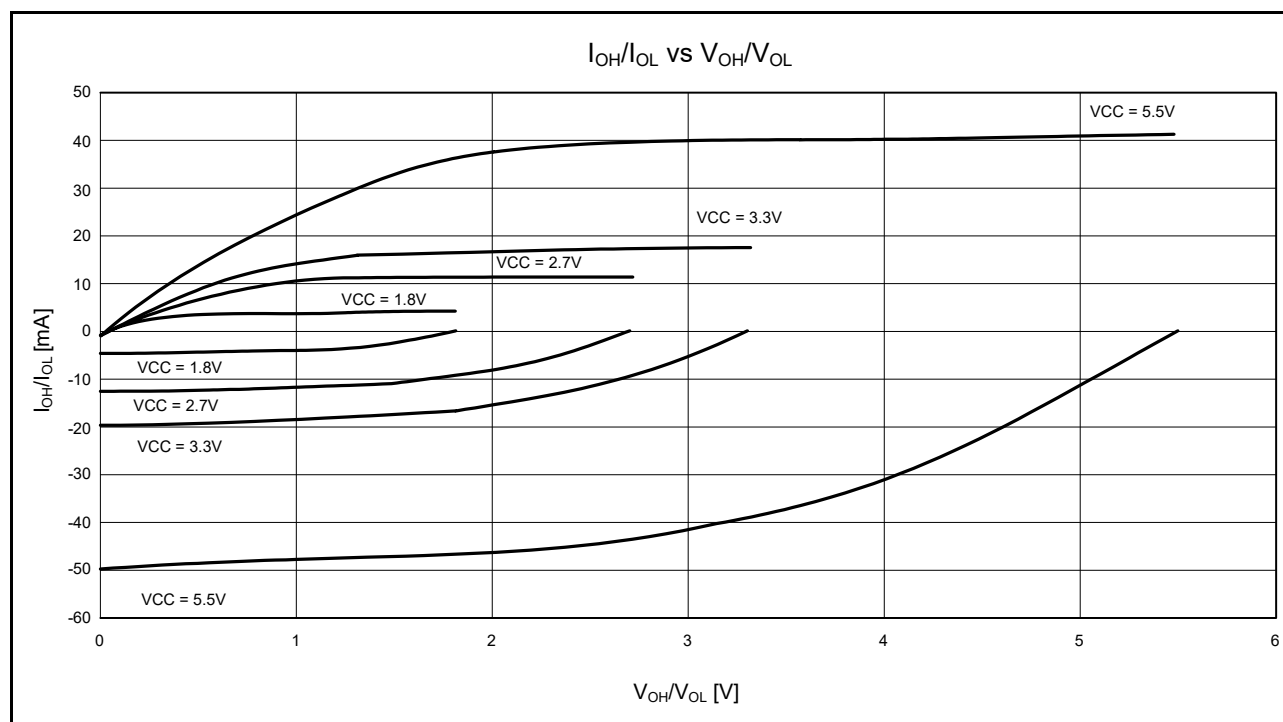


Figure 5.8 V_{OH}/V_{OL} and I_{OH}/I_{OL} Voltage Characteristics at $T_a = 25^\circ\text{C}$ When Normal Output is Selected (Reference Data)

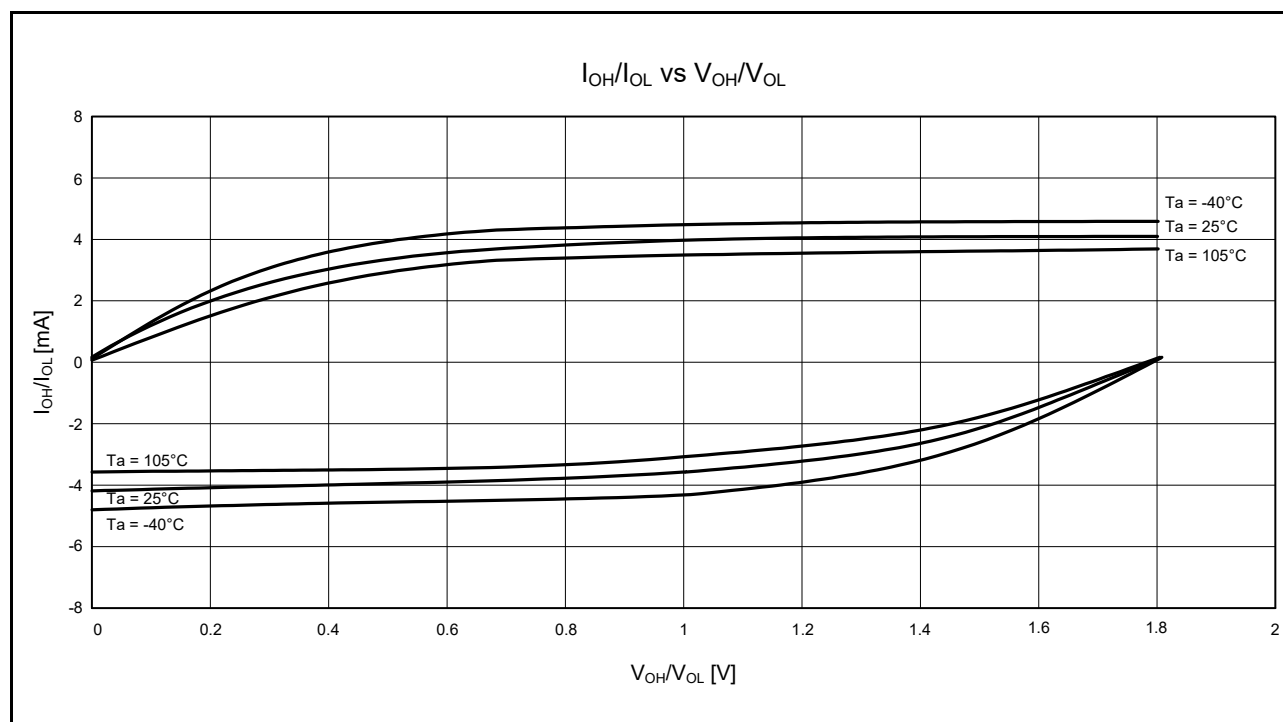


Figure 5.9 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at $V_{CC} = 1.8\text{ V}$ When Normal Output is Selected (Reference Data)

Table 5.39 Timing of On-Chip Peripheral Modules (2)

Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} = AV_{CC0} \leq 5.5\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$, $C = 30\text{ pF}$,
when high-drive output is selected by the drive capacity control register

Item				Symbol	Min.	Max.	Unit	Test Conditions
RSPI	RSPCK clock cycle	Master		t_{SPCyc}	2	4096	t_{Pcyc}^{*1}	Figure 5.54
		Slave			8	4096		
	RSPCK clock high pulse width	Master		t_{SPCKWH}	$(t_{SPCyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
		Slave			$(t_{SPCyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock low pulse width	Master		t_{SPCKWL}	$(t_{SPCyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
		Slave			$(t_{SPCyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock rise/fall time	Output	2.7 V or above	t_{SPCKr} , t_{SPCKf}	—	10	ns	
			1.8 V or above		—	15		
		Input			—	1	μs	
	Data input setup time	Master	2.7 V or above	t_{SU}	10	—	ns	Figure 5.55 to Figure 5.58
			1.8 V or above		30	—		
		Slave			$25 - t_{Pcyc}$	—		
	Data input hold time	Master	RSPCK set to a division ratio other than PCLKB divided by 2	t_H	t_{Pcyc}	—	ns	
			RSPCK set to PCLKB divided by 2	t_{HF}	0	—		
		Slave		t_H	$20 + 2 \times t_{Pcyc}$	—		
	SSL setup time	Master		t_{LEAD}	$-30 + N^2 \times t_{SPcyc}$	—	ns	
		Slave			2	—	t_{Pcyc}	
	SSL hold time	Master		t_{LAG}	$-30 + N^3 \times t_{SPcyc}$	—	ns	
		Slave			2	—	t_{Pcyc}	
	Data output delay time	Master	2.7 V or above	t_{OD}	—	14	ns	
1.8 V or above			—		30			
Slave		2.7 V or above	—		$3 \times t_{Pcyc} + 65$			
		1.8 V or above	—		$3 \times t_{Pcyc} + 105$			
Data output hold time	Master		t_{OH}	0	—	ns		
	Slave			0	—			
Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns		
	Slave			$4 \times t_{Pcyc}$	—			
MOSI and MISO rise/fall time	Output	2.7 V or above	t_{Dr} , t_{Df}	—	10	ns		
		1.8 V or above		—	15			
	Input			—	1	μs		
SSL rise/fall time	Output	2.7 V or above	t_{SSLr} , t_{SSLf}	—	10	ns		
		1.8 V or above		—	15	ns		
	Input			—	1	μs		
Slave access time		2.7 V or above	t_{SA}	—	6	t_{Pcyc}	Figure 5.57, Figure 5.58	
		1.8 V or above		—	7			
Slave output release time		2.7 V or above	t_{REL}	—	5	t_{Pcyc}		
		1.8 V or above		—	6			

Note 1. t_{Pcyc} : PCLK cycle

Note 2. N: An integer from 1 to 8 that can be set by the RSPI clock delay register (SPCKD)

Note 3. N: An integer from 1 to 8 that can be set by the RSPI slave select negation delay register (SSLND)

Table 5.41 Timing of On-Chip Peripheral Modules (4)

Conditions: $2.7\text{ V} \leq V_{CC} = V_{CC_USB} = AV_{CC0} \leq 5.5\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$, $f_{PCLKB} \leq 32\text{ MHz}$,
 $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Symbol	Min.*1, *2	Max.	Unit	Test Conditions
RIIC (Standard mode, SMBus)	SCL cycle time	t _{SCL}	6 (12) × t _{IICcyc} + 1300	—	ns	Figure 5.59
	SCL high pulse width	t _{SCLH}	3 (6) × t _{IICcyc} + 300	—	ns	
	SCL low pulse width	t _{SCLL}	3 (6) × t _{IICcyc} + 300	—	ns	
	SCL, SDA rise time	t _{Sr}	—	1000	ns	
	SCL, SDA fall time	t _{Sf}	—	300	ns	
	SCL, SDA spike pulse removal time	t _{SP}	0	1 (4) × t _{IICcyc}	ns	
	SDA bus free time	t _{BUF}	3 (6) × t _{IICcyc} + 300	—	ns	
	START condition hold time	t _{STAH}	t _{IICcyc} + 300	—	ns	
	Repeated START condition setup time	t _{STAS}	1000	—	ns	
	STOP condition setup time	t _{STOS}	1000	—	ns	
	Data setup time	t _{SDAS}	t _{IICcyc} + 50	—	ns	
	Data hold time	t _{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C _b	—	400	pF	
RIIC (Fast mode)	SCL cycle time	t _{SCL}	6 (12) × t _{IICcyc} + 600	—	ns	Figure 5.59
	SCL high pulse width	t _{SCLH}	3 (6) × t _{IICcyc} + 300	—	ns	
	SCL low pulse width	t _{SCLL}	3 (6) × t _{IICcyc} + 300	—	ns	
	SCL, SDA rise time	t _{Sr}	—	300	ns	
	SCL, SDA fall time	t _{Sf}	—	300	ns	
	SCL, SDA spike pulse removal time	t _{SP}	0	1 (4) × t _{IICcyc}	ns	
	SDA bus free time	t _{BUF}	3 (6) × t _{IICcyc} + 300	—	ns	
	START condition hold time	t _{STAH}	t _{IICcyc} + 300	—	ns	
	Repeated START condition setup time	t _{STAS}	300	—	ns	
	STOP condition setup time	t _{STOS}	300	—	ns	
	Data setup time	t _{SDAS}	t _{IICcyc} + 50	—	ns	
	Data hold time	t _{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C _b	—	400	pF	

Note: t_{IICcyc} : RIIC internal reference clock (IICφ) cycle

Note 1. The value in parentheses is used when the ICMR3.NF[1:0] bits are set to 11b while a digital filter is enabled with the ICFER.NFE bit = 1.

Note 2. C_b is the total capacitance of the bus lines.

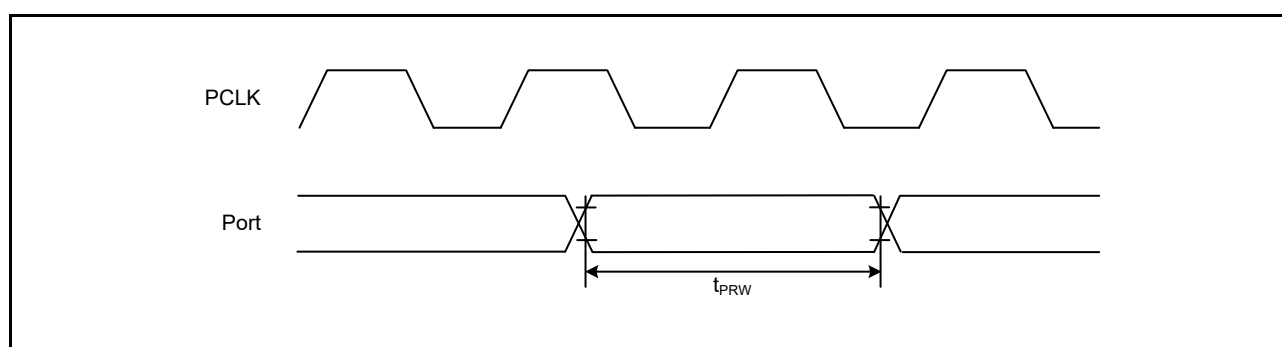


Figure 5.45 I/O Port Input Timing

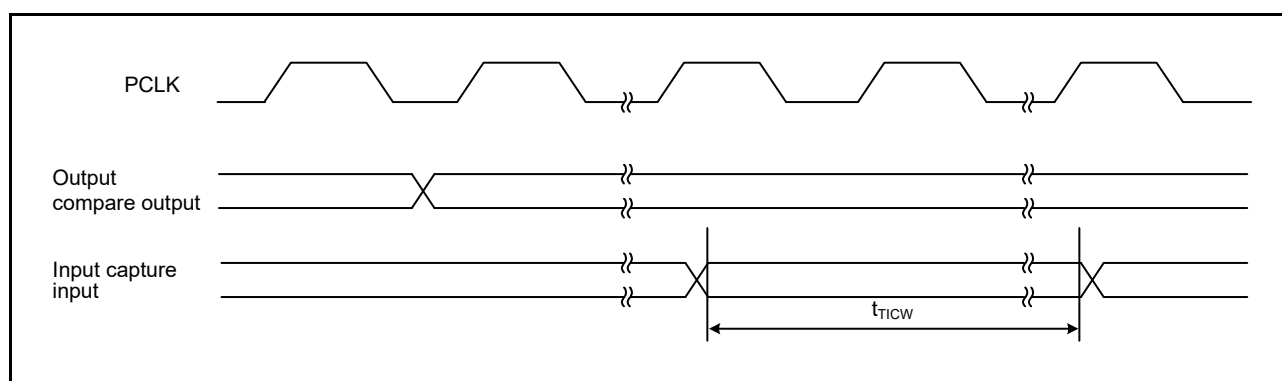


Figure 5.46 MTU2 Input/Output Timing

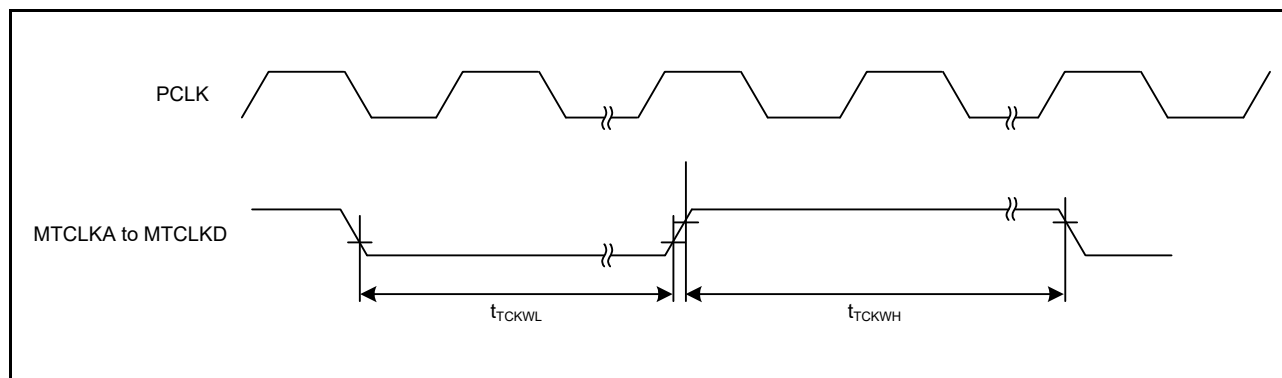


Figure 5.47 MTU2 Clock Input Timing

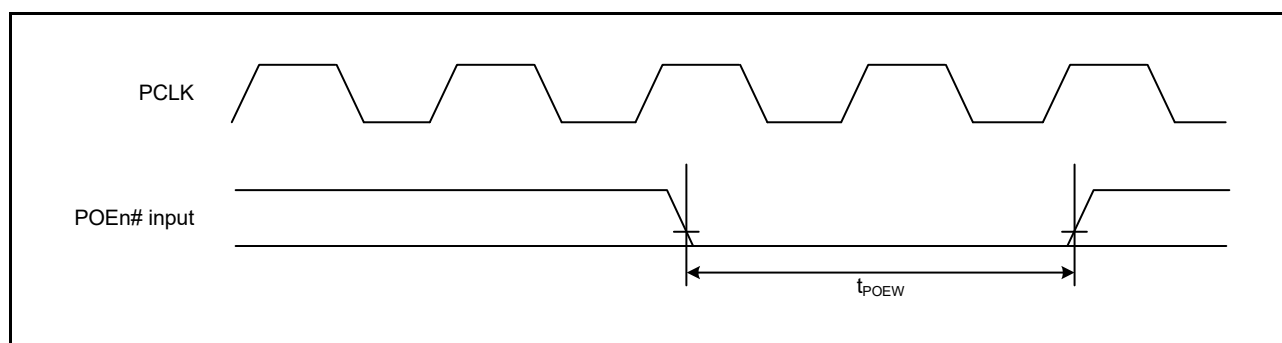


Figure 5.48 POE# Input Timing

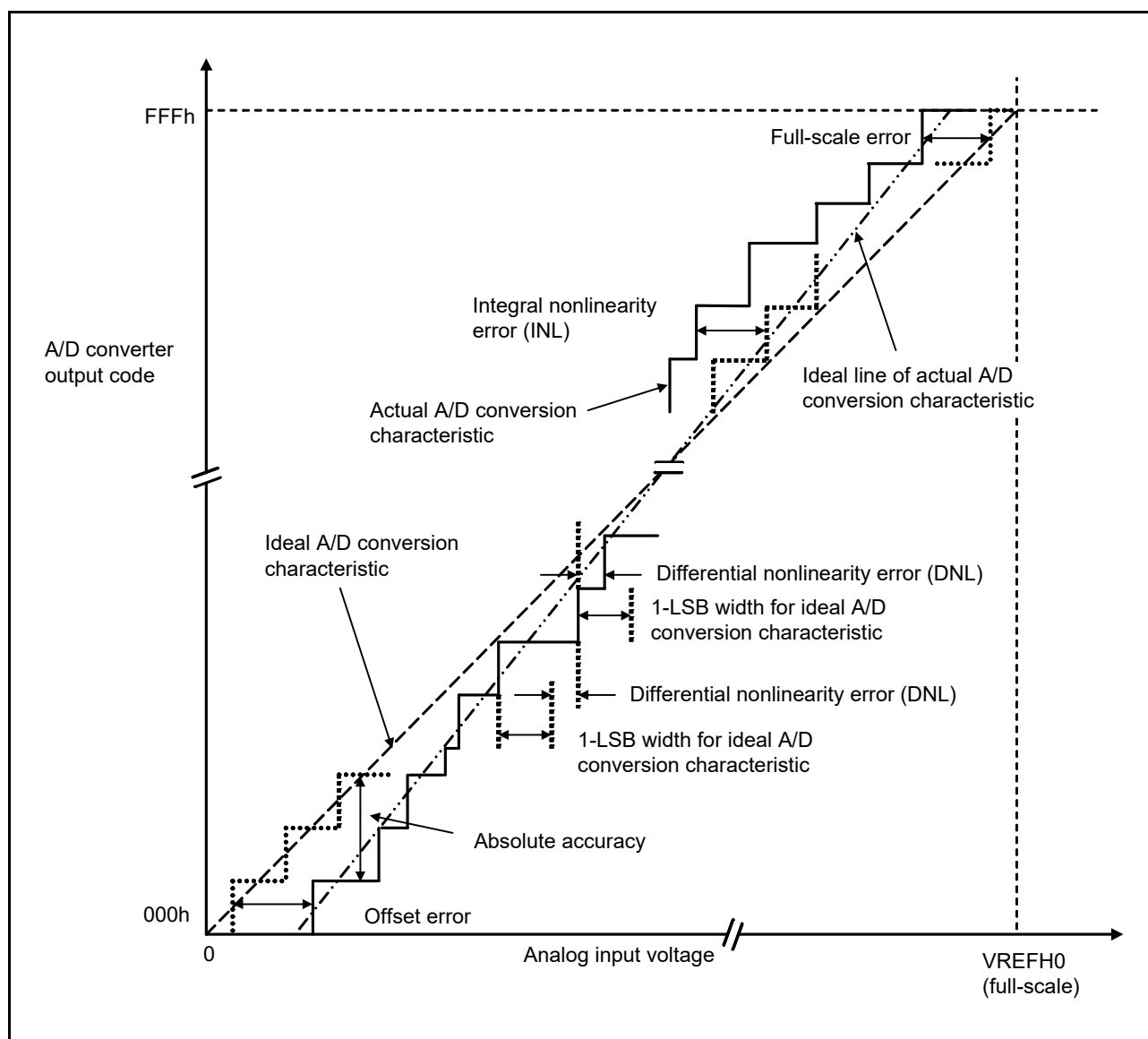


Figure 5.69 Illustration of A/D Converter Characteristic Terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of analog input voltage (1-LSB width), that can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 12-bit resolution is used and if reference voltage ($V_{REFH0} = 3.072\text{ V}$), then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, 1.5 mV, ... are used as analog input voltages.

If analog input voltage is 6 mV, absolute accuracy = $\pm 5\text{ LSB}$ means that the actual A/D conversion result is in the range of 003h to 00Dh, although an output code, 008h, can be expected from the theoretical A/D conversion characteristics.

Integral non-linearity error (INL)

The integral non-linearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HWQFN64-9x9-0.50	PWQN0064KC-A	P64K8-50-6B4-5	0.21

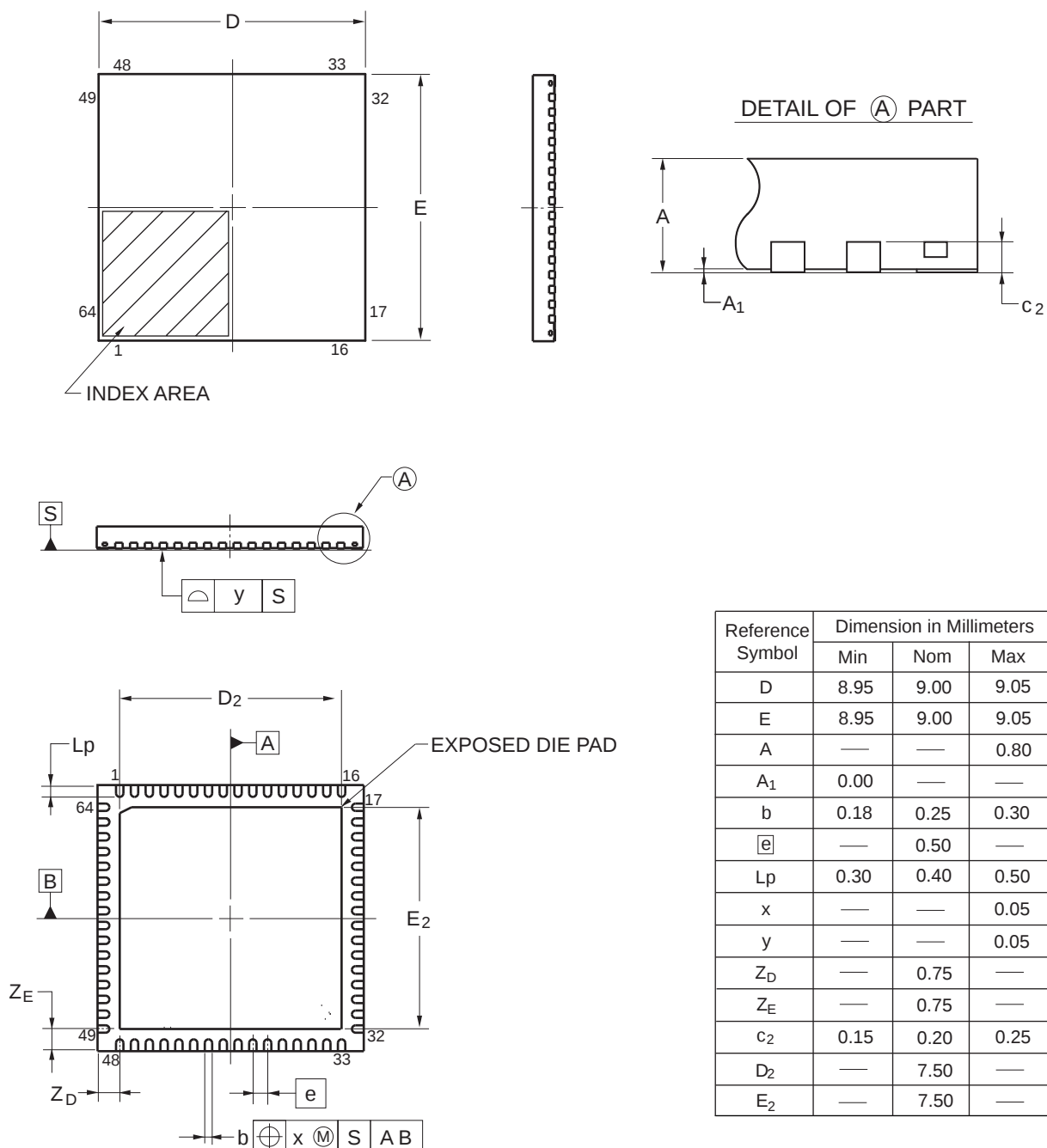


Figure D 64-Pin HWQFN (PWQN0064KC-A)