Renesas Electronics America Inc - R5F52315CDFP#30 Datasheet

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Applications of "Embedded - Microcontrollers"

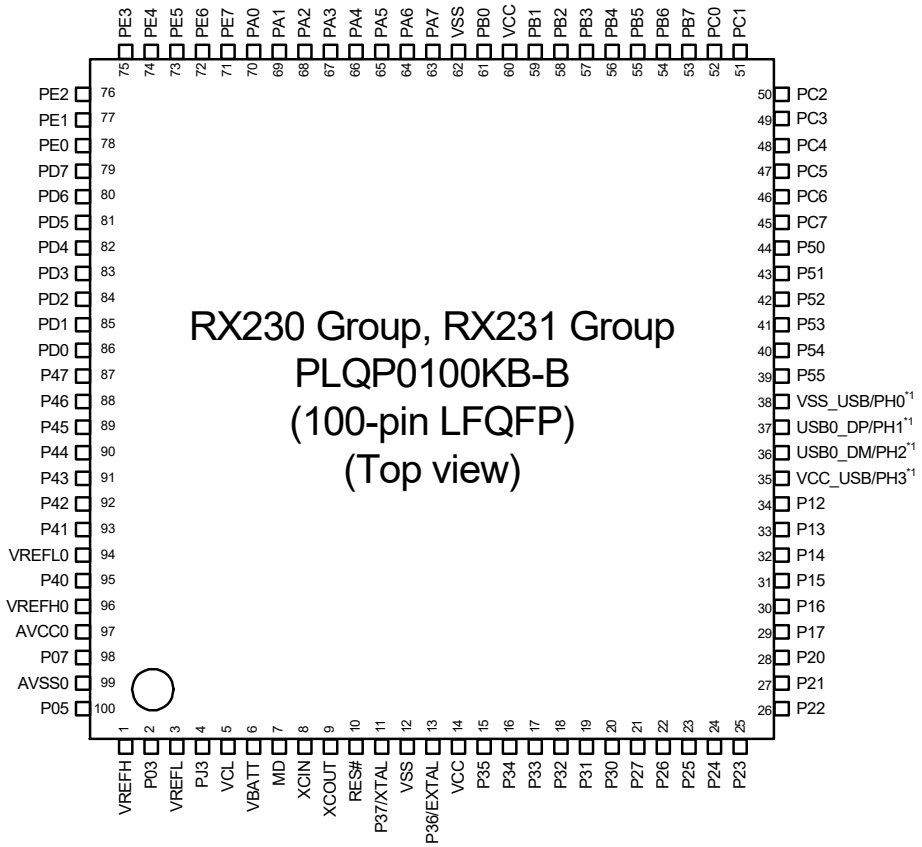
Details	
Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	54MHz
Connectivity	EBI/EMI, I²C, IrDA, SCI, SD/SDIO, SPI, SSI, USB OTG
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	79
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f52315cdfp-30

Table 1.1 Outline of Specifications (4/4)

Classification	Module/Function	Description
Communication functions	Serial Sound Interface (SSI)	• 1 channel • Capable of duplex communications • Various serial audio formats supported • Master/slave function supported • Programmable word clock or bit clock generation function • 8/16/18/20/22/24/32-bit data formats supported • On-chip 8-stage FIFO for transmission/reception • Supports WS continue mode in which the SSIWS signal is not stopped.
	SD Host Interface (SDHIa)	• 1 channel • Transfer speed : Default speed mode (8MB/s) • SD memory card interface (1 bit / 4bits SD bus) • MMC, eMMC Backward-compatible are supported. • SD Specifications Part 1: Compliant with Physical Layer Specification Ver.3.01 (Not support DDR) Part E1: SDIO Specification Ver. 3.00 • Error check function: CRC7 (command), CRC16 (data) • Interrupt Source: Card access interrupt, SDIO access interrupt, Card detection interrupt, SD buffer access interrupt • DMA transfer sources: SD_BUF write, SD_BUF read • Card detection, Write protection
Encryption functions	Trusted Secure IP (TSIP-Lite)	• Access management circuit • Encryption engine 128- or 256-bit key sizes of AES Block cipher mode of operation: GCM, ECB, CBC, CMAC, XTS, CTR, GCTR • Hash function • True random number generator • Prevention from illicit copying of a key
12-bit A/D converter (S12ADE)		• 12 bits (24 channels × 1 unit) • 12-bit resolution • Minimum conversion time: 0.83 µs per channel when the ADCLK is operating at 54 MHz • Operating modes Scan mode (single scan mode, continuous scan mode, and group scan mode) Group A priority control (only for group scan mode) • Sampling variable Sampling time can be set up for each channel. • Self-diagnostic function • Double trigger mode (A/D conversion data duplicated) • Detection of analog input disconnection • A/D conversion start conditions A software trigger, a trigger from a timer (MTU, TPU), an external trigger signal, or ELC • Event linking by the ELC
Temperature sensor (TEMPSA)		• 1 channel • The voltage output from the temperature sensor is converted into a digital value by the 12-bit A/D converter.
12-bit D/A converter (R12DAA)		• 2 channels • 12-bit resolution • Output voltage: 0.4 to AVCC0-0.5V
CRC calculator (CRC)		• CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$ • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable.
Comparator B (CMPBa)		• 2 channels × 2 units • Function to compare the reference voltage and the analog input voltage • Window comparator operation or standard comparator operation is selectable
Capacitive touch sensing unit (CTSU)		Detection pin: 24 channels
Data operation circuit (DOC)		Comparison, addition, and subtraction of 16-bit data
Power supply voltages/Operating frequencies		VCC = 1.8 to 2.4 V: 8 MHz, VCC = 2.4 to 2.7 V: 16 MHz, VCC = 2.7 to 5.5 V: 54 MHz
Operating temperature range		D version: –40 to +85°C, G version: –40 to +105°C
Packages		100-pin TFLGA (PTLG0100KA-A) 5.5 × 5.5 mm, 0.5 mm pitch 100-pin LFQFP (PLQP0100KB-B) 14 × 14 mm, 0.5 mm pitch 64-pin WFLGA (PWLG0064KA-A) 5 × 5 mm, 0.5 mm pitch 64-pin HWQFN (PWQN0064KC-A) 9 × 9 mm, 0.5 mm pitch 64-pin LFQFP (PLQP0064KB-C) 10 × 10 mm, 0.5 mm pitch 48-pin HWQFN (PWQN0048KB-A) 7 × 7 mm, 0.5 mm pitch 48-pin LFQFP (PLQP0048KB-B) 7 × 7 mm, 0.5 mm pitch
Debugging interfaces		FINE interface

Table 1.3 List of Products: D Version (T_a = –40 to +85°C) (2/2)

Group	Part No.	Order Part No.	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency	Security Function	SDHI	CAN	Operating Temperature
RX231	R5F52316ADFL	R5F52316ADFL#30	PLQP0048KB-B	256 Kbytes	32 Kbytes	8 Kbytes	54 MHz	Not available	Not available	Available	–40 to +85°C
	R5F52316CDFL	R5F52316CDFL#30						Not available	Not available	Not available	
	R5F52315ADLA	R5F52315ADLA#20	PTLG0100KA-A	128 Kbytes	32 Kbytes	8 Kbytes	54 MHz	Not available	Not available	Available	–40 to +85°C
	R5F52315CDLA	R5F52315CDLA#20						Not available	Not available	Not available	
	R5F52315ADFP	R5F52315ADFP#30	PLQP0100KB-B					Not available	Not available	Available	
	R5F52315CDFP	R5F52315CDFP#30						Not available	Not available	Not available	
	R5F52315CDLF	R5F52315CDLF#20	PWLG0064KA-A					Not available	Not available	Not available	
	R5F52315ADND	R5F52315ADND#U0	PWQN0064KC-A					Not available	Not available	Available	
	R5F52315CDND	R5F52315CDND#U0						Not available	Not available	Not available	
	R5F52315ADFM	R5F52315ADFM#30	PLQP0064KB-C					Not available	Not available	Available	
	R5F52315CDFM	R5F52315CDFM#30						Not available	Not available	Not available	
	R5F52315ADNE	R5F52315ADNE#U0	PWQN0048KB-A					Not available	Not available	Available	
	R5F52315CDNE	R5F52315CDNE#U0						Not available	Not available	Not available	
	R5F52315ADFL	R5F52315ADFL#30	PLQP0048KB-B					Not available	Not available	Available	
	R5F52315CDFL	R5F52315CDFL#30						Not available	Not available	Not available	
RX230	R5F52306ADLA	R5F52306ADLA#20	PTLG0100KA-A	256 Kbytes	32 Kbytes	8 Kbytes	54 MHz	Not available	Not available	Not available	–40 to +85°C
	R5F52306ADFP	R5F52306ADFP#30	PLQP0100KB-B					Not available	Not available	Not available	
	R5F52306ADLF	R5F52306ADLF#20	PWLG0064KA-A					Not available	Not available	Not available	
	R5F52306ADND	R5F52306ADND#U0	PWQN0064KC-A					Not available	Not available	Not available	
	R5F52306ADFM	R5F52306ADFM#30	PLQP0064KB-C					Not available	Not available	Not available	
	R5F52306ADNE	R5F52306ADNE#U0	PWQN0048KB-A					Not available	Not available	Not available	
	R5F52306ADFL	R5F52306ADFL#30	PLQP0048KB-B					Not available	Not available	Not available	
	R5F52305ADLA	R5F52305ADLA#20	PTLG0100KA-A	128 Kbytes				Not available	Not available	Not available	
	R5F52305ADFP	R5F52305ADFP#30	PLQP0100KB-B					Not available	Not available	Not available	
	R5F52305ADLF	R5F52305ADLF#20	PWLG0064KA-A					Not available	Not available	Not available	
	R5F52305ADND	R5F52305ADND#U0	PWQN0064KC-A					Not available	Not available	Not available	
	R5F52305ADFM	R5F52305ADFM#30	PLQP0064KB-C					Not available	Not available	Not available	
	R5F52305ADNE	R5F52305ADNE#U0	PWQN0048KB-A					Not available	Not available	Not available	
	R5F52305ADFL	R5F52305ADFL#30	PLQP0048KB-B					Not available	Not available	Not available	



Note: This figure indicates the power supply pins and I/O port pins.
For the pin configuration, see the table “List of Pins and Pin Functions (100-Pin LFQFP)”.

Note 1. RX230: PH0, PH1, PH2, PH3
RX231: VSS_USB, USB0_DP, USB0_DM, VCC_USB

Figure 1.4 Pin Assignments of the 100-Pin LFQFP

Table 1.6 List of Pins and Pin Functions (100-Pin TFLGA) (1/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCI, RSPI, RIIC, RSCAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
A1		P05						DA1
A2	VREFH							
A3		P07						ADTRG0#
A4	VREFL0							
A5		P43						AN003
A6		PD0	D0[A0/D0]					IRQ0/AN024
A7		PD4	D4[A4/D4]	POE3#				IRQ4/AN028
A8		PE0	D8[A8/D8]		SCK12			AN016
A9		PE1	D9[A9/D9]	MTIOC4C	TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12			AN017/ CMPB0
A10		PE2	D10[A10/D10]	MTIOC4A	RXD12/RXDX12/ SMISO12/SSCL12			IRQ7/AN018/ CVREFB0
B1		P03						DA0
B2	AVSS0							
B3	AVCC0							
B4		P40						AN000
B5		P44						AN004
B6		PD1	D1[A1/D1]	MTIOC4B				IRQ1/AN025
B7		PD3	D3[A3/D3]	POE8#				IRQ3/AN027
B8		PD6	D6[A6/D6]	MTIC5V/POE1#				IRQ6/AN030
B9		PD7	D7[A7/D7]	MTIC5U/POE0#				IRQ7/AN031
B10		PE3	D11[A11/D11]	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#/ AUDIO_MCLK			AN019/ CLKOUT
C1	VCL							
C2	VREFL							
C3		PJ3		MTIOC3C	CTS6#/RTS6#/SS6#			
C4	VREFH0							
C5		P42						AN002
C6		P47						AN007
C7		PD2	D2[A2/D2]	MTIOC4D				IRQ2/AN026
C8		PD5	D5[A5/D5]	MTIC5W/POE2#				IRQ5/AN029
C9		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B				IRQ5/AN021/ CMPOB0
C10		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A				AN020/ CMPA2/ CLKOUT
D1	XCIN							
D2	XCOUT							
D3	MD							FINED
D4	VBATT							
D5		P45						AN005
D6		P46						AN006
D7		PE6	D14[A14/D14]					IRQ6/AN022
D8		PE7	D15[A15/D15]					IRQ7/AN023
D9		PA1	A1	MTIOC0B/MTCLKC/ TIOCB0	SCK5/SSLA2/SSISCK0			
D10		PA0	A0/BC0#	MTIOC4A/TIOCA0	SSLA1			CACREF
E1	XTAL	P37						
E2	VSS							
E3	RES#							
E4		P34		MTIOC0A/TMCI3/POE2#	SCK6		TS0	IRQ4
E5		P41						AN001
E6		PA2	A2		RXD5/SMISO5/SSCL5/ SSLA3/IRRXD5			
E7		PA6	A6	MTIC5V/MTCLKB/TMCI3/ POE2#/TIOCA2	CTS5#/RTS5#/SS5#/ MOSIA/SSIWS0			

Table 1.7 List of Pins and Pin Functions (100-Pin LFQFP) (1/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCI, RSPI, RIIC, RSCAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
1	VREFH							
2		P03						DA0
3	VREFL							
4		PJ3		MTIOC3C	CTS6#/RTS6#/SS6#			
5	VCL							
6	VBATT							
7	MD							FINED
8	XCIN							
9	XCOUT							
10	RES#							
11	XTAL	P37						
12	VSS							
13	EXTAL	P36						
14	VCC							
15	UPSEL	P35						NMI
16		P34		MTIOC0A/TMCI3/POE2#	SCK6		TS0	IRQ4
17		P33		MTIOC0D/TMRI3/POE3#/ TIOCD0	RXD6/SMISO6/SSCL6		TS1	IRQ3
18		P32		MTIOC0C/TMO3/TIOCC0/ RTCOUT/RTCIC2	TXD6/SMOSI6/SSDA6/ USB0_VBUSEN			IRQ2
19		P31		MTIOC4D/TMCI2/RTCIC1	CTS1#/RTS1#/SS1#/ SSISCK0			IRQ1
20		P30		MTIOC4B/TMRI3/POE8#/ RTCIC0	RXD1/SMISO1/SSCL1/ AUDIO_MCLK			IRQ0/ CMPOB3
21		P27	CS3#	MTIOC2B/TMCI3	SCK1/ SSIWS0		TS2	CVREFB3
22		P26	CS2#	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1/ SSIRXD0		TS3	CMPB3
23		P25	CS1#	MTIOC4C/MTCLKB/ TIOCA4			TS4	ADTRG0#
24		P24	CS0#	MTIOC4A/MTCLKA/TMRI1/ TIOCB4	USB0_VBUSEN		TS5	
25		P23		MTIOC3D/MTCLKD/ TIOCD3	CTS0#/RTS0#/SS0#/ SSISCK0		TS6	
26		P22		MTIOC3B/MTCLKC/TMO0/ TIOCC3	SCK0/ USB0_OVRCURB/ AUDIO_MCLK		TS7	
27		P21		MTIOC1B/TMCI0/TIOCA3	RXD0/SMISO0/SSCL0/ USB0_EXICEN/SSIWS0		TS8	
28		P20		MTIOC1A/TMRI0/TIOCB3	TXD0/SMOSI0/SSDA0/ USB0_ID/SSIRXD0		TS9	
29		P17		MTIOC3A/MTIOC3B/TMO1/ POE8#/TIOCB0/TCLKD	SCK1/MISOA/SDA/ SSITXD0			IRQ7/ CMPOB2
30		P16		MTIOC3C/MTIOC3D/ TMO2/TIOCB1/TCLKC/ RTCOUT	TXD1/SMOSI1/SSDA1/ MOSIA/SCL/USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB			IRQ6/ ADTRG0#
31		P15		MTIOC0B/MTCLKB/TMCI2/ TIOCB2/TCLKB	RXD1/SMISO1/SSCL1/ CRXD0		TS12	IRQ5/CMPB2
32		P14		MTIOC3A/MTCLKA/TMRI2/ TIOCB5/TCLKA	CTS1#/RTS1#/SS1#/ CTXD0/USB0_OVRCURA		TS13	IRQ4/ CVREFB2
33		P13		MTIOC0B/TMO3/TIOCA5	SDA			IRQ3
34		P12		TMCI1	SCL			IRQ2
35	VCC_USB*1	PH3*1		TMCI0*1				
36		PH2*1		TMRI0*1	USB0_DM*1			IRQ1*1
37		PH1*1		TMO0*1	USB0_DP*1			IRQ0*1
38	VSS_USB*1	PH0*1						CACREF*1
39		P55	WAIT#	MTIOC4D/TMO3	CRXD0		TS15	
40		P54	ALE	MTIOC4B/TMCI1	CTXD0		TS16	
41	BCLK	P53					TS17	

Table 1.8 List of Pins and Pin Functions (64-Pin WFLGA) (2/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCI, RSPI, RIIC, RSCAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
F4		PC5	MTIOC3B/MTCLKD/TMRI2	SCK8/RSPCKA/USB0_ID			TS23
F5		P15	MTIOC0B/MTCLKB/TMCI2/ TIOCB2/TCLKB	RXD1/SMISO1/SSCL1/CRXD0		TS12	IRQ5/CMPB2
F6		PB1	MTIOC0C/MTIOC4C/TMCI0/ TIOCB3	TXD6/SMOSI6/SSDA6	SDHI_CLK		IRQ4/ CMPOB1
F7		PB5	MTIOC2A/MTIOC1B/TMRI1/ POE1#/TIOCB4	SCK9/USB0_VBUS	SDHI_CD		
F8		PB3	MTIOC0A/MTIOC4A/TMO0/ POE3#/TIOCD3/TCLKD	SCK6	SDHI_WP		
G1	EXTAL	P36					
G2		P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1/ USB0_VBUSEN/SSIRXD0		TS3	CMPB3
G3	VCC_USB*1	PH3*1	TMCI0*1				
G4	VSS_USB*1	PH0*1					CACREF*1
G5	UB	PC7	MTIOC3A/MTCLKB/TMO2	TXD8/SMOSI8/SSDA8/MISOA			CACREF
G6		PC6	MTIOC3C/MTCLKA/TMCI2	RXD8/SMISO8/SSCL8/MOSIA/ USB0_EXICEN		TS22	
G7		PC3	MTIOC4D/TCLKB	TXD5/SMOSI5/SSDA5/IRTXD5	SDHI_D0	TS27	
G8		PB6/PC0	MTIOC3D/TIOCA5	RXD9/SMISO9/SSCL9	SDHI_D1		
H1	XTAL	P37					
H2		P17	MTIOC3A/MTIOC3B/TMO1/ POE8#/TIOCB0/TCLKD	SCK1/MISOA/SDA/SSITXD0			IRQ7/ CMPOB2
H3		PH2*1	TMRI0*1	USB0_DM*1			IRQ1*1
H4		PH1*1	TMO0*1	USB0_DP*1			IRQ0*1
H5		P55	MTIOC4D/TMO3	CRXD0		TS15	
H6		P54	MTIOC4B/TMCI1	CTXD0		TS16	
H7		PC2	MTIOC4B/TCLKA	RXD5/SMISO5/SSCL5/SSLA3/ IRRXD5	SDHI_D3	TS30	
H8		PB7/PC1	MTIOC3B/TIOCB5	TXD9/SMOSI9/SSDA9	SDHI_D2		

Note 1. RX230: PH0/CACREF, PH1/IRQ0/TMO0, PH2/IRQ1/TMRI0, PH3/TMCI0
RX231: VSS_USB, USB0_DP, USB0_DM, VCC_USB

2. CPU

Figure 2.1 shows register set of the CPU.

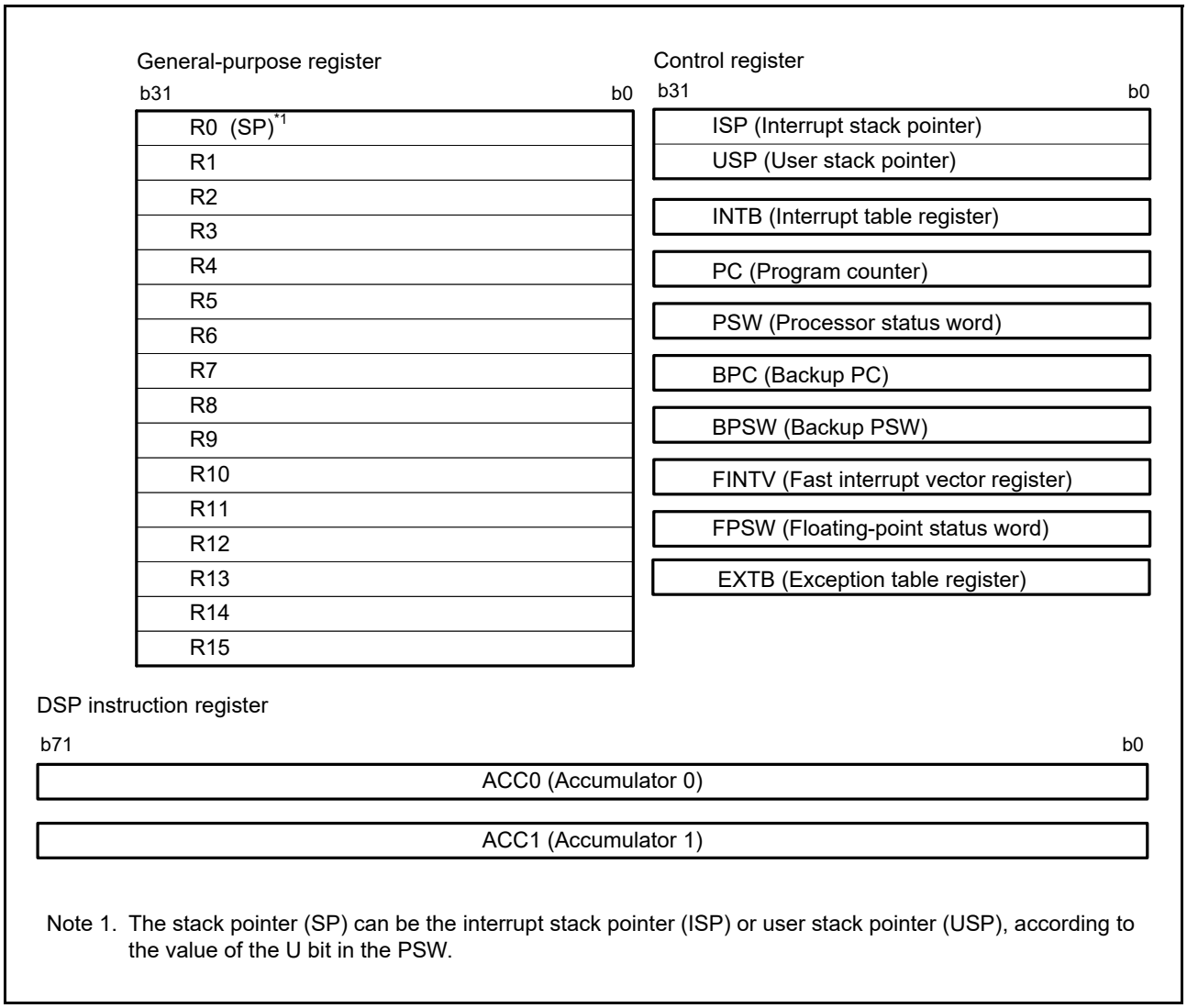


Figure 2.1 Register Set of the CPU

4.1 I/O Register Addresses (Address Order)

Table 4.1 List of I/O Registers (Address Order) (1/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK <PCLK
0008 0000h	SYSTEM	Mode Monitor Register	MDMONR	16	16	3 ICLK	
0008 0006h	SYSTEM	System Control Register 0	SYSCR0	16	16	3 ICLK	
0008 0008h	SYSTEM	System Control Register 1	SYSCR1	16	16	3 ICLK	
0008 000Ch	SYSTEM	Standby Control Register	SBYCR	16	16	3 ICLK	
0008 0010h	SYSTEM	Module Stop Control Register A	MSTPCRA	32	32	3 ICLK	
0008 0014h	SYSTEM	Module Stop Control Register B	MSTPCRB	32	32	3 ICLK	
0008 0018h	SYSTEM	Module Stop Control Register C	MSTPCRC	32	32	3 ICLK	
0008 001Ch	SYSTEM	Module Stop Control Register D	MSTPCRD	32	32	3 ICLK	
0008 0020h	SYSTEM	System Clock Control Register	SCKCR	32	32	3 ICLK	
0008 0026h	SYSTEM	System Clock Control Register 3	SCKCR3	16	16	3 ICLK	
0008 0028h	SYSTEM	PLL Control Register	PLLCR	16	16	3 ICLK	
0008 002Ah	SYSTEM	PLL Control Register 2	PLLCR2	8	8	3 ICLK	
0008 002Ch	SYSTEM	USB-dedicated PLL Control Register	UPLLCR	16	16	3 ICLK	
0008 002Eh	SYSTEM	USB-dedicated PLL Control Register 2	UPLLCR2	8	8	3 ICLK	
0008 0030h	SYSTEM	External Bus Clock Control Register	BCKCR	8	8	3 ICLK	
0008 0031h	SYSTEM	Memory Wait Cycle Setting Register	MEMWAIT	8	8	3 ICLK	
0008 0032h	SYSTEM	Main Clock Oscillator Control Register	MOSCCR	8	8	3 ICLK	
0008 0033h	SYSTEM	Sub-Clock Oscillator Control Register	SOSCCR	8	8	3 ICLK	
0008 0034h	SYSTEM	Low-Speed On-Chip Oscillator Control Register	LOCOCR	8	8	3 ICLK	
0008 0035h	SYSTEM	IWDT-Dedicated On-Chip Oscillator Control Register	ILOCOCR	8	8	3 ICLK	
0008 0036h	SYSTEM	High-Speed On-Chip Oscillator Control Register	HOCOCR	8	8	3 ICLK	
0008 0037h	SYSTEM	High-Speed On-Chip Oscillator Control Register 2	HOCOCR2	8	8	3 ICLK	
0008 003Ch	SYSTEM	Oscillation Stabilization Flag Register	OSCOVFSR	8	8	3 ICLK	
0008 003Eh	SYSTEM	CLKOUT Output Control Register	CKOCR	16	16	3 ICLK	
0008 0040h	SYSTEM	Oscillation Stop Detection Control Register	OSTDCR	8	8	3 ICLK	
0008 0041h	SYSTEM	Oscillation Stop Detection Status Register	OSTDSR	8	8	3 ICLK	
0008 0060h	SYSTEM	Low-Speed On-Chip Oscillator Trimming Register	LOCOTRR	8	8	3 ICLK	
0008 0064h	SYSTEM	IWDT-Dedicated On-Chip Oscillator Trimming Register	ILOCOTRR	8	8	3 ICLK	
0008 0068h	SYSTEM	High-Speed On-Chip Oscillator Trimming Register 0	HOCOTRR0	8	8	3 ICLK	
0008 006Bh	SYSTEM	High-Speed On-Chip Oscillator Trimming Register 3	HOCOTRR3	8	8	3 ICLK	
0008 00A0h	SYSTEM	Operating Power Control Register	OPCCR	8	8	3 ICLK	
0008 00A1h	SYSTEM	Sleep Mode Return Clock Source Switching Register	RSTCKCR	8	8	3 ICLK	
0008 00A2h	SYSTEM	Main Clock Oscillator Wait Control Register	MOSCWTCR	8	8	3 ICLK	
0008 00AAh	SYSTEM	Sub Operating Power Control Register	SOPCCR	8	8	3 ICLK	
0008 00B0h	LPT	Low-Power Timer Control Register 1	LPTCR1	8	8	3 ICLK	
0008 00B1h	LPT	Low-Power Timer Control Register 2	LPTCR2	8	8	3 ICLK	
0008 00B2h	LPT	Low-Power Timer Control Register 3	LPTCR3	8	8	3 ICLK	
0008 00B4h	LPT	Low-Power Timer Cycle Setting Register	LPTPRD	16	16	3 ICLK	
0008 00B8h	LPT	Low-Power Timer Compare Register 0	LPCMR0	16	16	3 ICLK	
0008 00BCh	LPT	Low-Power Timer Standby Return Enable Register	LPWUCR	16	16	3 ICLK	
0008 00C0h	SYSTEM	Reset Status Register 2	RSTSR2	8	8	3 ICLK	
0008 00C2h	SYSTEM	Software Reset Register	SWRR	16	16	3 ICLK	
0008 00E0h	SYSTEM	Voltage Monitoring 1 Circuit Control Register 1	LVD1CR1	8	8	3 ICLK	
0008 00E1h	SYSTEM	Voltage Monitoring 1 Circuit Status Register	LVD1SR	8	8	3 ICLK	
0008 00E2h	SYSTEM	Voltage Monitoring 2 Circuit Control Register 1	LVD2CR1	8	8	3 ICLK	
0008 00E3h	SYSTEM	Voltage Monitoring 2 Circuit Status Register	LVD2SR	8	8	3 ICLK	
0008 03FEh	SYSTEM	Protect Register	PRCR	16	16	3 ICLK	
0008 1300h	BSC	Bus Error Status Clear Register	BERCLR	8	8	2 ICLK	
0008 1304h	BSC	Bus Error Monitoring Enable Register	BEREN	8	8	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (6/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK <PCLK
0008 8158h	TPU4	Timer General Register A	TGRA	16	16	2 or 3 PCLKB	2 ICLK
0008 815Ah	TPU4	Timer General Register B	TGRB	16	16	2 or 3 PCLKB	2 ICLK
0008 8160h	TPU5	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8161h	TPU5	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB	2 ICLK
0008 8162h	TPU5	Timer I/O Control Register	TIOR	8	8	2 or 3 PCLKB	2 ICLK
0008 8164h	TPU5	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB	2 ICLK
0008 8165h	TPU5	Timer Status Register	TSR	8	8	2 or 3 PCLKB	2 ICLK
0008 8166h	TPU5	Timer Counter	TCNT	16	16	2 or 3 PCLKB	2 ICLK
0008 8168h	TPU5	Timer General Register A	TGRA	16	16	2 or 3 PCLKB	2 ICLK
0008 816Ah	TPU5	Timer General Register B	TGRB	16	16	2 or 3 PCLKB	2 ICLK
0008 8200h	TMR0	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8201h	TMR1	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8202h	TMR0	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB	2 ICLK
0008 8203h	TMR1	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB	2 ICLK
0008 8204h	TMR0	Time Constant Register A	TCORA	8	8	2 or 3 PCLKB	2 ICLK
0008 8205h	TMR1	Time Constant Register A	TCORA	8	8*1	2 or 3 PCLKB	2 ICLK
0008 8206h	TMR0	Time Constant Register B	TCORB	8	8	2 or 3 PCLKB	2 ICLK
0008 8207h	TMR1	Time Constant Register B	TCORB	8	8*1	2 or 3 PCLKB	2 ICLK
0008 8208h	TMR0	Timer Counter	TCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 8209h	TMR1	Timer Counter	TCNT	8	8*1	2 or 3 PCLKB	2 ICLK
0008 820Ah	TMR0	Timer Counter Control Register	TCCR	8	8	2 or 3 PCLKB	2 ICLK
0008 820Bh	TMR1	Timer Counter Control Register	TCCR	8	8*1	2 or 3 PCLKB	2 ICLK
0008 820Ch	TMR0	Timer Count Start Register	TCSTR	8	8	2 or 3 PCLKB	2 ICLK
0008 8210h	TMR2	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8211h	TMR3	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8212h	TMR2	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB	2 ICLK
0008 8213h	TMR3	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB	2 ICLK
0008 8214h	TMR2	Time Constant Register A	TCORA	8	8	2 or 3 PCLKB	2 ICLK
0008 8215h	TMR3	Time Constant Register A	TCORA	8	8*1	2 or 3 PCLKB	2 ICLK
0008 8216h	TMR2	Time Constant Register B	TCORB	8	8	2 or 3 PCLKB	2 ICLK
0008 8217h	TMR3	Time Constant Register B	TCORB	8	8*1	2 or 3 PCLKB	2 ICLK
0008 8218h	TMR2	Timer Counter	TCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 8219h	TMR3	Timer Counter	TCNT	8	8*1	2 or 3 PCLKB	2 ICLK
0008 821Ah	TMR2	Timer Counter Control Register	TCCR	8	8	2 or 3 PCLKB	2 ICLK
0008 821Bh	TMR3	Timer Counter Control Register	TCCR	8	8*1	2 or 3 PCLKB	2 ICLK
0008 821Ch	TMR2	Timer Count Start Register	TCSTR	8	8	2 or 3 PCLKB	2 ICLK
0008 8280h	CRC	CRC Control Register	CRCCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8281h	CRC	CRC Data Input Register	CRCDIR	8	8	2 or 3 PCLKB	2 ICLK
0008 8282h	CRC	CRC Data Output Register	CRCDOR	16	16	2 or 3 PCLKB	2 ICLK
0008 8300h	RIIC0	I^2C-Bus Control Register 1	ICCR1	8	8	2 or 3 PCLKB	2 ICLK
0008 8301h	RIIC0	I^2C-Bus Control Register 2	ICCR2	8	8	2 or 3 PCLKB	2 ICLK
0008 8302h	RIIC0	I^2C-Bus Mode Register 1	ICMR1	8	8	2 or 3 PCLKB	2 ICLK
0008 8303h	RIIC0	I^2C-Bus Mode Register 2	ICMR2	8	8	2 or 3 PCLKB	2 ICLK
0008 8304h	RIIC0	I^2C-Bus Mode Register 3	ICMR3	8	8	2 or 3 PCLKB	2 ICLK
0008 8305h	RIIC0	I^2C-Bus Function Enable Register	ICFER	8	8	2 or 3 PCLKB	2 ICLK
0008 8306h	RIIC0	I^2C-Bus Status Enable Register	ICSER	8	8	2 or 3 PCLKB	2 ICLK
0008 8307h	RIIC0	I^2C-Bus Interrupt Enable Register	ICIER	8	8	2 or 3 PCLKB	2 ICLK
0008 8308h	RIIC0	I^2C-Bus Status Register 1	ICSR1	8	8	2 or 3 PCLKB	2 ICLK
0008 8309h	RIIC0	I^2C-Bus Status Register 2	ICSR2	8	8	2 or 3 PCLKB	2 ICLK
0008 830Ah	RIIC0	Slave Address Register L0	SARL0	8	8	2 or 3 PCLKB	2 ICLK
0008 830Bh	RIIC0	Slave Address Register U0	SARU0	8	8	2 or 3 PCLKB	2 ICLK
0008 830Ch	RIIC0	Slave Address Register L1	SARL1	8	8	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (19/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK <PCLK
0008 C1B3h	MPC	PE3 Pin Function Control Register	PE3PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1B4h	MPC	PE4 Pin Function Control Register	PE4PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1B5h	MPC	PE5 Pin Function Control Register	PE5PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1B6h	MPC	PE6 Pin Function Control Register	PE6PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1B7h	MPC	PE7 Pin Function Control Register	PE7PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1C8h	MPC	PH0 Pin Function Control Register	PH0PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1C9h	MPC	PH1 Pin Function Control Register	PH1PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1CAh	MPC	PH2 Pin Function Control Register	PH2PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1CBh	MPC	PH3 Pin Function Control Register	PH3PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1D3h	MPC	PJ3 Pin Function Control Register	PJ3PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C290h	SYSTEM	Reset Status Register 0	RSTSR0	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C291h	SYSTEM	Reset Status Register 1	RSTSR1	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C293h	SYSTEM	Main Clock Oscillator Forced Oscillation Control Register	MOFCR	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C297h	SYSTEM	Voltage Monitoring Circuit Control Register	LVCMPCR	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C298h	SYSTEM	Voltage Detection Level Select Register	LVDLVLR	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C29Ah	SYSTEM	Voltage Monitoring 1 Circuit Control Register 0	LVD1CR0	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C29Bh	SYSTEM	Voltage Monitoring 2 Circuit Control Register 0	LVD2CR0	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C29Dh	SYSTEM	VBATT Control Register	VBATTCR	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C29Eh	SYSTEM	VBATT Status Register	VBATTSR	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C29Fh	SYSTEM	VBATT Pin Voltage Drop Detection Interrupt Control Register	VBTLVDICR	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C400h	RTC	64-Hz Counter	R64CNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C402h	RTC	Second Counter	RSECCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C402h	RTC	Binary Counter 0	BCNT0	8	8	2 or 3 PCLKB	2 ICLK
0008 C404h	RTC	Minute Counter	RMINCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C404h	RTC	Binary Counter 1	BCNT1	8	8	2 or 3 PCLKB	2 ICLK
0008 C406h	RTC	Hour Counter	RHRCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C406h	RTC	Binary Counter 2	BCNT2	8	8	2 or 3 PCLKB	2 ICLK
0008 C408h	RTC	Day-of-Week Counter	RWKCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C408h	RTC	Binary Counter 3	BCNT3	8	8	2 or 3 PCLKB	2 ICLK
0008 C40Ah	RTC	Date Counter	RDAYCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C40Ch	RTC	Month Counter	RMONCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C40Eh	RTC	Year Counter	RYRCNT	16	16	2 or 3 PCLKB	2 ICLK
0008 C410h	RTC	Second Alarm Register	RSECAR	8	8	2 or 3 PCLKB	2 ICLK
0008 C410h	RTC	Binary Counter 0 Alarm Register	BCNT0AR	8	8	2 or 3 PCLKB	2 ICLK
0008 C412h	RTC	Minute Alarm Register	RMINAR	8	8	2 or 3 PCLKB	2 ICLK
0008 C412h	RTC	Binary Counter 1 Alarm Register	BCNT1AR	8	8	2 or 3 PCLKB	2 ICLK
0008 C414h	RTC	Hour Alarm Register	RHRAR	8	8	2 or 3 PCLKB	2 ICLK
0008 C414h	RTC	Binary Counter 2 Alarm Register	BCNT2AR	8	8	2 or 3 PCLKB	2 ICLK
0008 C416h	RTC	Day-of-Week Alarm Register	RWKAR	8	8	2 or 3 PCLKB	2 ICLK
0008 C416h	RTC	Binary Counter 3 Alarm Register	BCNT3AR	8	8	2 or 3 PCLKB	2 ICLK
0008 C418h	RTC	Date Alarm Register	RDAYAR	8	8	2 or 3 PCLKB	2 ICLK
0008 C418h	RTC	Binary Counter 0 Alarm Enable Register	BCNT0AER	8	8	2 or 3 PCLKB	2 ICLK
0008 C41Ah	RTC	Month Alarm Register	RMONAR	8	8	2 or 3 PCLKB	2 ICLK
0008 C41Ah	RTC	Binary Counter 1 Alarm Enable Register	BCNT1AER	8	8	2 or 3 PCLKB	2 ICLK
0008 C41Ch	RTC	Year Alarm Register	RYRAR	16	16	2 or 3 PCLKB	2 ICLK
0008 C41Ch	RTC	Binary Counter 2 Alarm Enable Register	BCNT2AER	16	16	2 or 3 PCLKB	2 ICLK
0008 C41Eh	RTC	Year Alarm Enable Register	RYRAREN	8	8	2 or 3 PCLKB	2 ICLK
0008 C41Eh	RTC	Binary Counter 3 Alarm Enable Register	BCNT3AER	8	8	2 or 3 PCLKB	2 ICLK
0008 C422h	RTC	RTC Control Register 1	RCR1	8	8	2 or 3 PCLKB	2 ICLK
0008 C424h	RTC	RTC Control Register 2	RCR2	8	8	2 or 3 PCLKB	2 ICLK
0008 C426h	RTC	RTC Control Register 3	RCR3	8	8	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (23/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK <PCLK
000A 00B0h	USB0	BC Control Register 0	USBBCCTRL0	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 00CCh	USB0	USB Module Control Register	USBMC	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 00D0h	USB0	Device Address 0 Configuration Register	DEVADD0	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 00D2h	USB0	Device Address 1 Configuration Register	DEVADD1	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 00D4h	USB0	Device Address 2 Configuration Register	DEVADD2	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 00D6h	USB0	Device Address 3 Configuration Register	DEVADD3	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 00D8h	USB0	Device Address 4 Configuration Register	DEVADD4	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 00DAh	USB0	Device Address 5 Configuration Register	DEVADD5	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 0900h	CTSU	CTSU Control Register 0	CTSUCR0	8	8	2 or 3 PCLKB	2 ICLK
000A 0901h	CTSU	CTSU Control Register 1	CTSUCR1	8	8	2 or 3 PCLKB	2 ICLK
000A 0902h	CTSU	CTSU Synchronous Noise Reduction Setting Register	CTSUSDPRS	8	8	2 or 3 PCLKB	2 ICLK
000A 0903h	CTSU	CTSU Sensor Stabilization Wait Control Register	CTSUSST	8	8	2 or 3 PCLKB	2 ICLK
000A 0904h	CTSU	CTSU Measurement Channel Register 0	CTSUMCH0	8	8	2 or 3 PCLKB	2 ICLK
000A 0905h	CTSU	CTSU Measurement Channel Register 1	CTSUMCH1	8	8	2 or 3 PCLKB	2 ICLK
000A 0906h	CTSU	CTSU Channel Enable Control Register 0	CTSUCHAC0	8	8	2 or 3 PCLKB	2 ICLK
000A 0907h	CTSU	CTSU Channel Enable Control Register 1	CTSUCHAC1	8	8	2 or 3 PCLKB	2 ICLK
000A 0908h	CTSU	CTSU Channel Enable Control Register 2	CTSUCHAC2	8	8	2 or 3 PCLKB	2 ICLK
000A 0909h	CTSU	CTSU Channel Enable Control Register 3	CTSUCHAC3	8	8	2 or 3 PCLKB	2 ICLK
000A 090Ah	CTSU	CTSU Channel Enable Control Register 4	CTSUCHAC4	8	8	2 or 3 PCLKB	2 ICLK
000A 090Bh	CTSU	CTSU Channel Transmit/Receive Control Register 0	CTSUCHTRC0	8	8	2 or 3 PCLKB	2 ICLK
000A 090Ch	CTSU	CTSU Channel Transmit/Receive Control Register 1	CTSUCHTRC1	8	8	2 or 3 PCLKB	2 ICLK
000A 090Dh	CTSU	CTSU Channel Transmit/Receive Control Register 2	CTSUCHTRC2	8	8	2 or 3 PCLKB	2 ICLK
000A 090Eh	CTSU	CTSU Channel Transmit/Receive Control Register 3	CTSUCHTRC3	8	8	2 or 3 PCLKB	2 ICLK
000A 090Fh	CTSU	CTSU Channel Transmit/Receive Control Register 4	CTSUCHTRC4	8	8	2 or 3 PCLKB	2 ICLK
000A 0910h	CTSU	CTSU High-Pass Noise Reduction Control Register	CTSUDCLKC	8	8	2 or 3 PCLKB	2 ICLK
000A 0911h	CTSU	CTSU Status Register	CTSUST	8	8	2 or 3 PCLKB	2 ICLK
000A 0912h	CTSU	CTSU High-Pass Noise Reduction Spectrum Diffusion Control Register	CTSUSSC	16	16	2 or 3 PCLKB	2 ICLK
000A 0914h	CTSU	CTSU Sensor Offset Register 0	CTSUSO0	16	16	2 or 3 PCLKB	2 ICLK
000A 0916h	CTSU	CTSU Sensor Offset Register 1	CTSUSO1	16	16	2 or 3 PCLKB	2 ICLK
000A 0918h	CTSU	CTSU Sensor Counter	CTSUSC	16	16	2 or 3 PCLKB	2 ICLK
000A 091Ah	CTSU	CTSU Reference Counter	CTSURC	16	16	2 or 3 PCLKB	2 ICLK
000A 091Ch	CTSU	CTSU Error Status Register	CTSUERRS	16	16	2 or 3 PCLKB	2 ICLK
000A 8300h	RSCAN0	Bit Configuration Register L	CFGL	16	16	2 or 3 PCLKB	2 ICLK
000A 8302h	RSCAN0	Bit Configuration Register H	CFGH	16	16	2 or 3 PCLKB	2 ICLK
000A 8304h	RSCAN0	Control Register L	CTRL	16	16	2 or 3 PCLKB	2 ICLK
000A 8306h	RSCAN0	Control Register H	CTRH	16	16	2 or 3 PCLKB	2 ICLK
000A 8308h	RSCAN0	Status Register L	STSL	16	16	2 or 3 PCLKB	2 ICLK
000A 830Ah	RSCAN0	Status Register H	STSH	16	16	2 or 3 PCLKB	2 ICLK
000A 830Ch	RSCAN0	Error Flag Register L	ERFLL	16	16	2 or 3 PCLKB	2 ICLK
000A 830Eh	RSCAN0	Error Flag Register H	ERFLH	16	16	2 or 3 PCLKB	2 ICLK
000A 8322h	RSCAN	Global Configuration Register L	GCFGL	16	16	2 or 3 PCLKB	2 ICLK
000A 8324h	RSCAN	Global Configuration Register H	GCFGH	16	16	2 or 3 PCLKB	2 ICLK

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Conditions: VSS = AVSS0 = VREFL0 = VREFL= VSS_USB = 0 V

Item		Symbol	Value	Unit
Power supply voltage		VCC, VCC_USB	–0.3 to +6.5	V
VBATT power supply voltage		Vbatt	–0.3 to +6.5	V
Input voltage	Ports for 5 V tolerant*1	V_{in}	–0.3 to +6.5	V
	P03, P05, P07, P40 to P47		–0.3 to AVCC0 +0.3	
	Ports other than above		–0.3 to VCC +0.3	
Reference power supply voltage		VREFH0	–0.3 to AVCC0 +0.3	V
		VREFH		
Analog power supply voltage		AVCC0	–0.3 to +6.5	V
Analog input voltage	When AN000 to AN007 are used	V_{AN}	–0.3 to AVCC0 +0.3	V
	When AN016 to AN031 are used		–0.3 to VCC +0.3	
Operating temperature*2		T_{opr}	–40 to +85 –40 to +105	°C
Storage temperature		T_{stg}	–55 to +125	°C

Caution: Permanent damage to the MCU may be caused if absolute maximum ratings are exceeded.

To preclude any malfunctions due to noise interference, insert capacitors with high frequency characteristics between the VCC and VSS pins, between the AVCC0 and AVSS0 pins, between the VCC_USB and VSS_USB pins, between the VREFH0 and VREFL0 pins, and between the VREFH and VREFL pins. Place capacitors of about 0.1 µF as close as possible to every power supply pin and use the shortest and heaviest possible traces.

Connect the VCL pin to a VSS pin via a 4.7 µF capacitor. The capacitor must be placed close to the pin. For details, refer to section 5.15.1, Connecting VCL Capacitor and Bypass Capacitors.

Do not input signals or an I/O pull-up power supply to ports other than 5-V tolerant ports while the device is not powered.

The current injection that results from input of such a signal or I/O pull-up may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Even if –0.3 to +6.5 V is input to 5-V tolerant ports, it will not cause problems such as damage to the MCU.

Note 1. Ports 12, 13, 16, 17, 30, 31, 32, and B5 are 5 V tolerant.

Note 2. The upper limit of operating temperature is 85°C or 105°C, depending on the product. For details, refer to section 1.2, List of Products.

5.2.2 Normal I/O Pin Output Characteristics (2)

Figure 5.13 to Figure 5.17 show the characteristics when high-drive output is selected by the drive capacity control register.

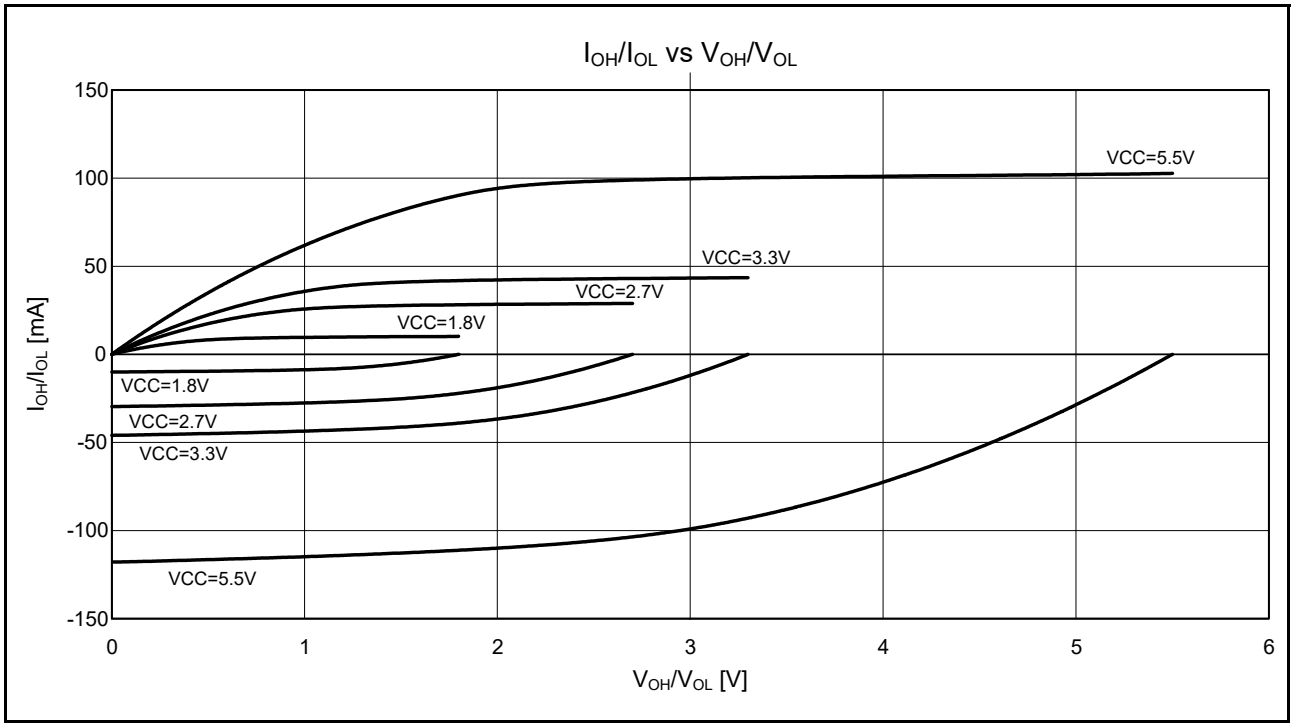


Figure 5.13 V_{OH}/V_{OL} and I_{OH}/I_{OL} Voltage Characteristics at T_a = 25°C When High-Drive Output is Selected (Reference Data)

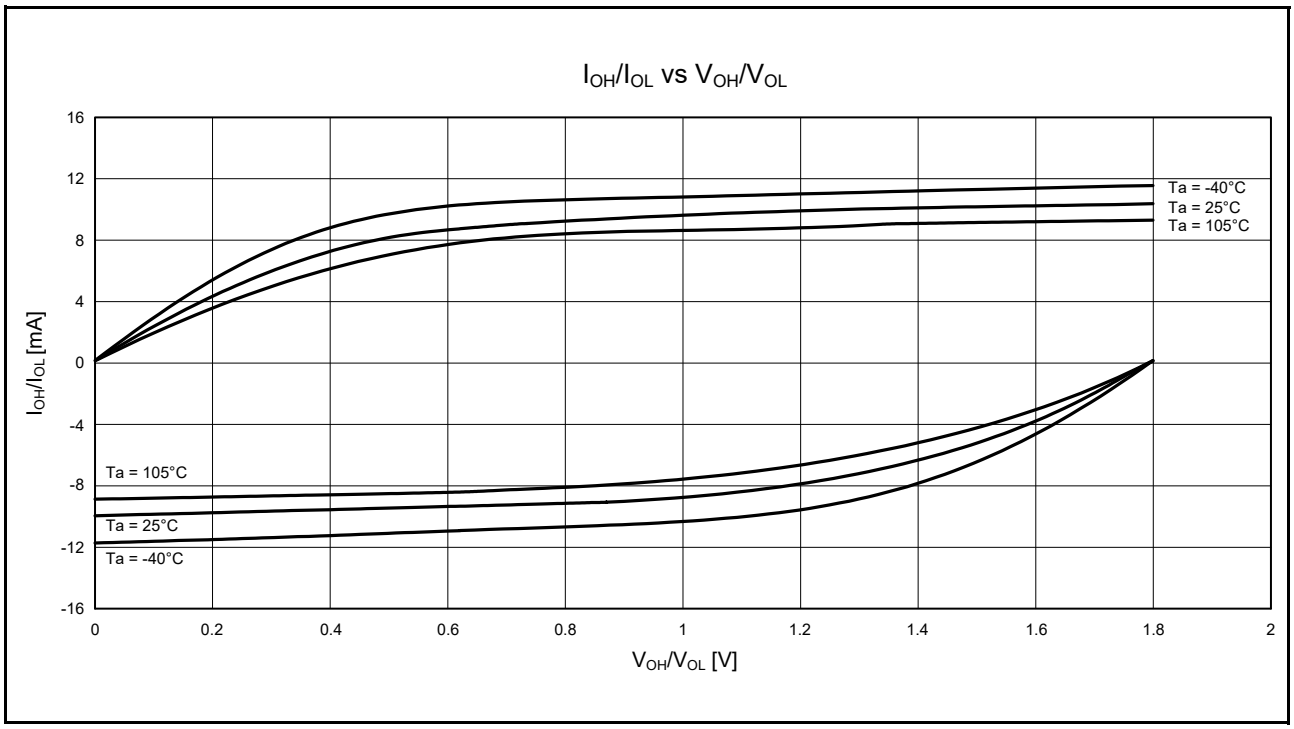


Figure 5.14 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 1.8 V When High-Drive Output is Selected (Reference Data)

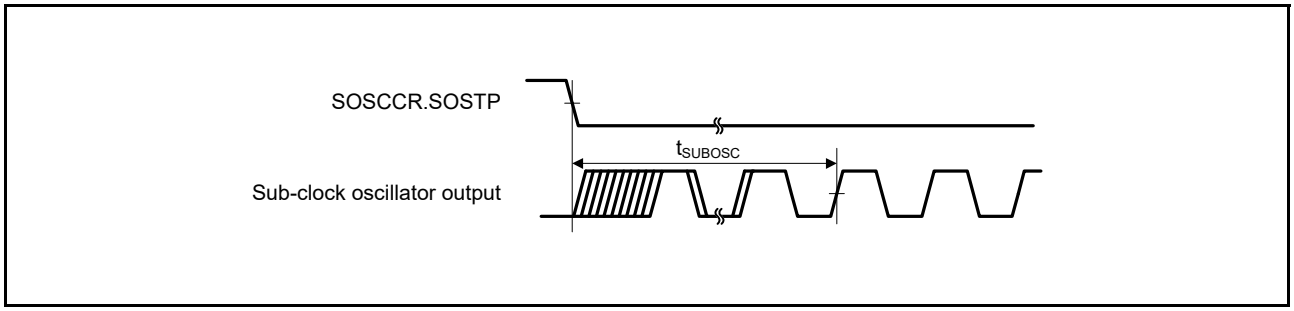


Figure 5.30 Sub-Clock Oscillation Start Timing

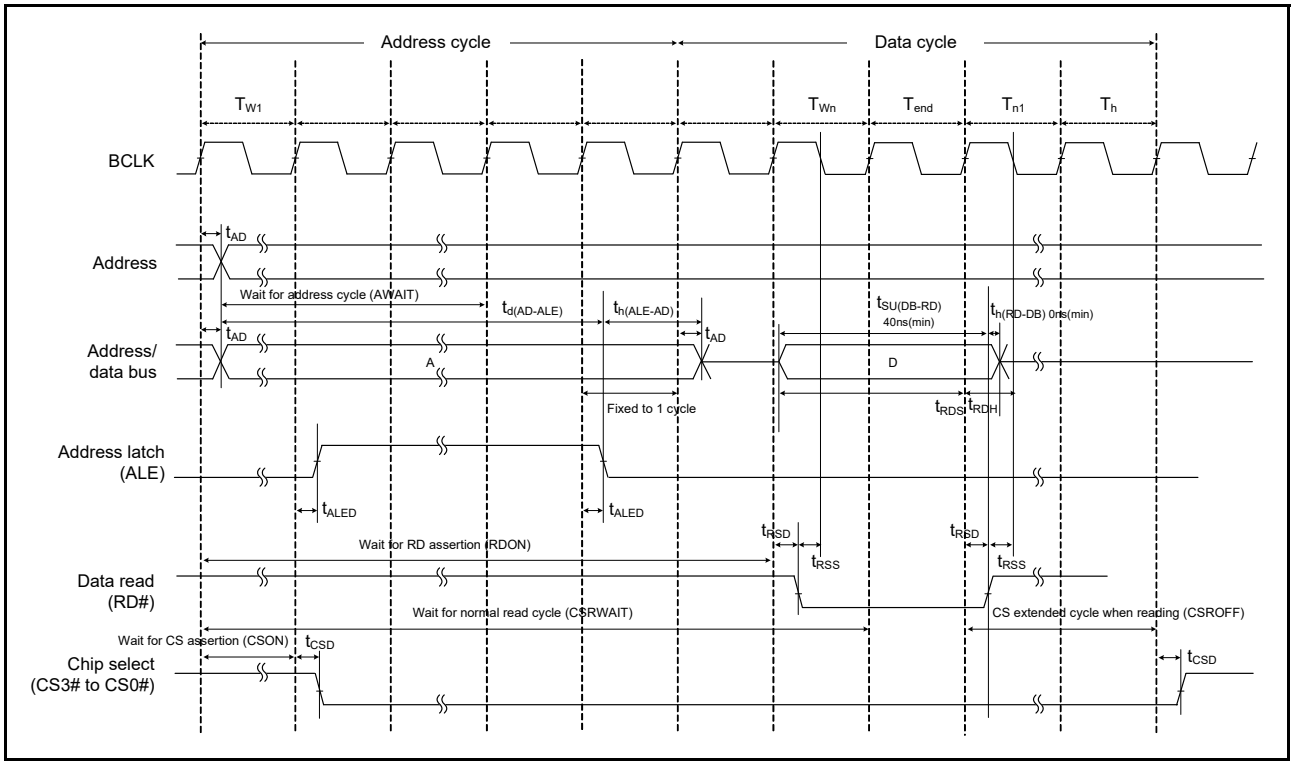


Figure 5.43 External Bus Timing/Read Access Operation Example (Multiplex)

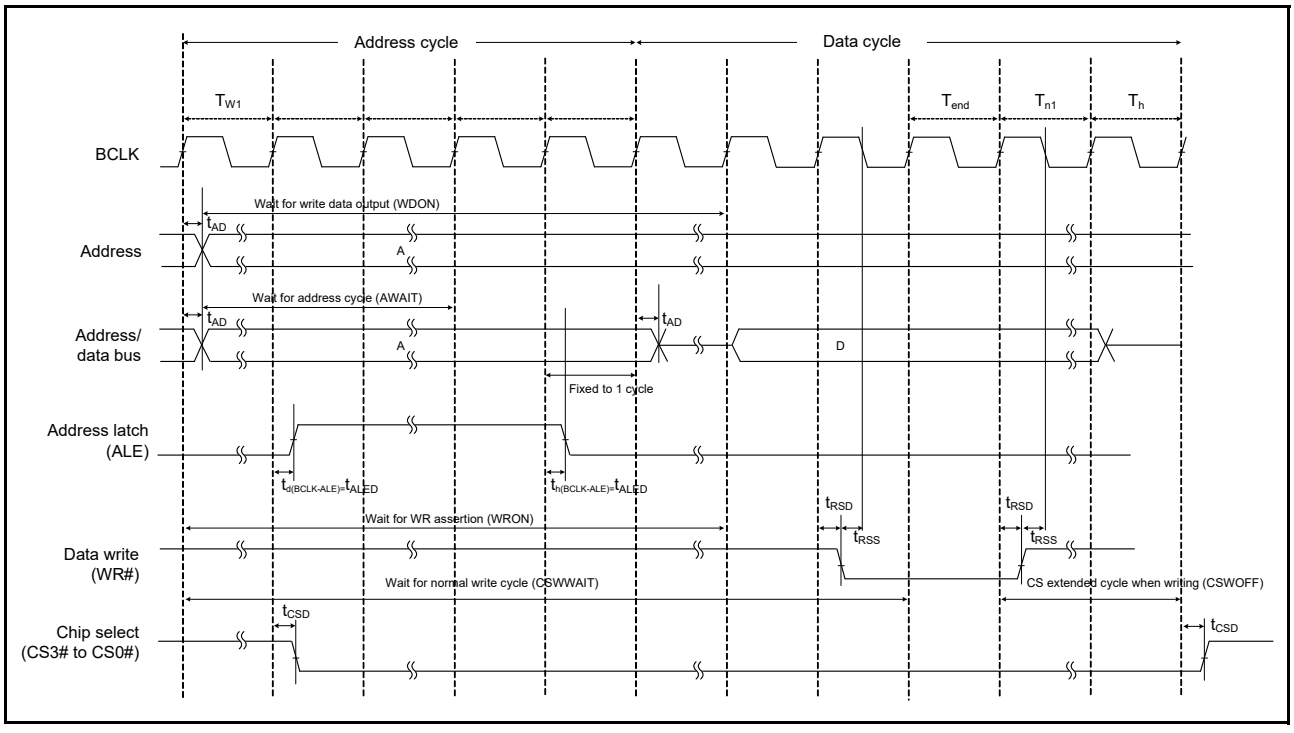


Figure 5.44 External Bus Timing/Write Access Operation Example (Multiplex)

Table 5.39 Timing of On-Chip Peripheral Modules (2)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C, C = 30 pF, when high-drive output is selected by the drive capacity control register

Item				Symbol	Min.	Max.	Unit	Test Conditions
RSPI	RSPCK clock cycle	Master		t_{SPcyc}	2	4096	t_{Pcyc}*1	Figure 5.54
		Slave			8	4096		
	RSPCK clock high pulse width	Master		t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock low pulse width	Master		t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock rise/fall time	Output	2.7 V or above	t_{SPCKr}, t_{SPCKf}	—	10	ns	
			1.8 V or above		—	15		
		Input			—	1	µs	
	Data input setup time	Master	2.7 V or above	t_{SU}	10	—	ns	Figure 5.55 to Figure 5.58
			1.8 V or above		30	—		
		Slave			$25 - t_{Pcyc}$	—		
	Data input hold time	Master	RSPCK set to a division ratio other than PCLKB divided by 2	t_H	t_{Pcyc}	—	ns	
			RSPCK set to PCLKB divided by 2	t_{HF}	0	—		
		Slave		t_H	$20 + 2 \times t_{Pcyc}$	—		
	SSL setup time	Master		t_{LEAD}	$–30 + N^{*2} \times t_{SPcyc}$	—	ns	
		Slave			2	—	t_{Pcyc}	
	SSL hold time	Master		t_{LAG}	$–30 + N^{*3} \times t_{SPcyc}$	—	ns	
		Slave			2	—	t_{Pcyc}	
	Data output delay time	Master	2.7 V or above	t_{OD}	—	14	ns	
			1.8 V or above		—	30		
		Slave	2.7 V or above		—	$3 \times t_{Pcyc} + 65$		
			1.8 V or above		—	$3 \times t_{Pcyc} + 105$		
	Data output hold time	Master		t_{OH}	0	—	ns	
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave			$4 \times t_{Pcyc}$	—		
	MOSI and MISO rise/fall time	Output	2.7 V or above	t_{Dr}, t_{Df}	—	10	ns	
			1.8 V or above		—	15		
		Input			—	1	µs	
	SSL rise/fall time	Output	2.7 V or above	t_{SSLr}, t_{SSLf}	—	10	ns	
			1.8 V or above		—	15	ns	
		Input			—	1	µs	
	Slave access time		2.7 V or above	t_{SA}	—	6	t_{Pcyc}	Figure 5.57, Figure 5.58
			1.8 V or above		—	7		
	Slave output release time		2.7 V or above	t_{REL}	—	5	t_{Pcyc}	
			1.8 V or above		—	6		

Note 1. t_{Pcyc}: PCLK cycle
Note 2. N: An integer from 1 to 8 that can be set by the RSPI clock delay register (SPCKD)
Note 3. N: An integer from 1 to 8 that can be set by the RSPI slave select negation delay register (SSLND)

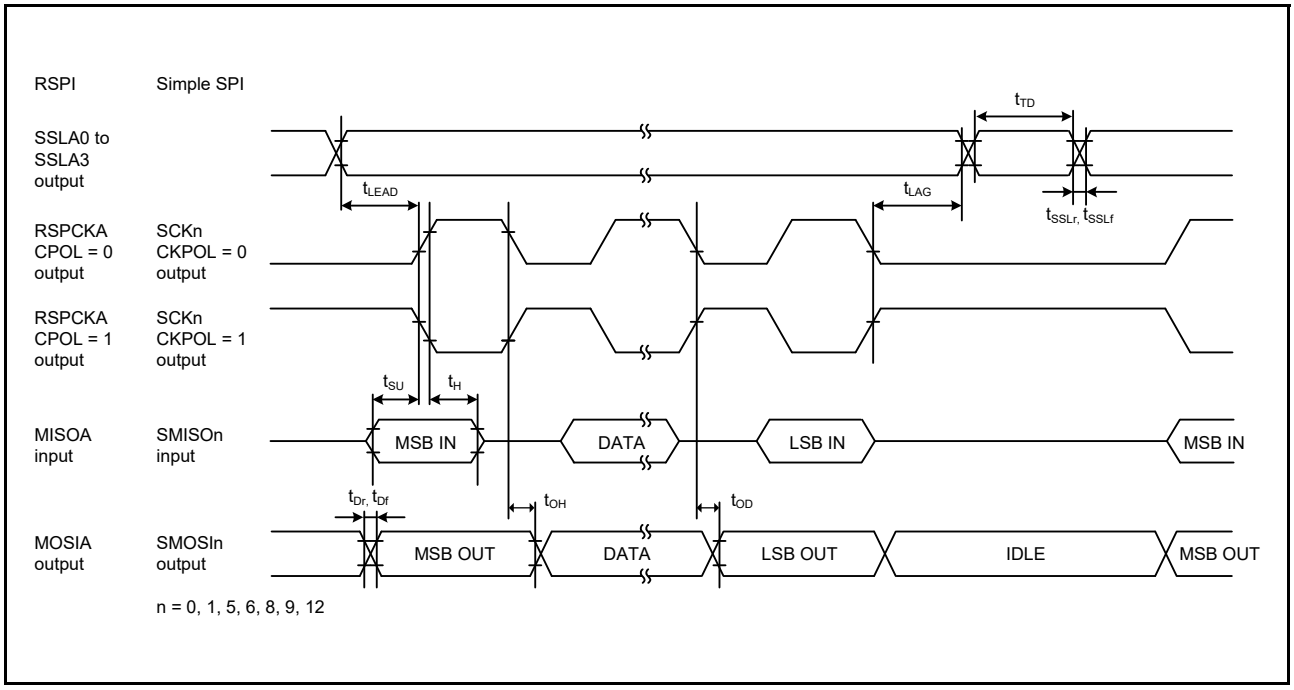


Figure 5.55 RSPI Timing (Master, CPHA = 0) and Simple SPI Clock Timing (Master, CKPH = 1)

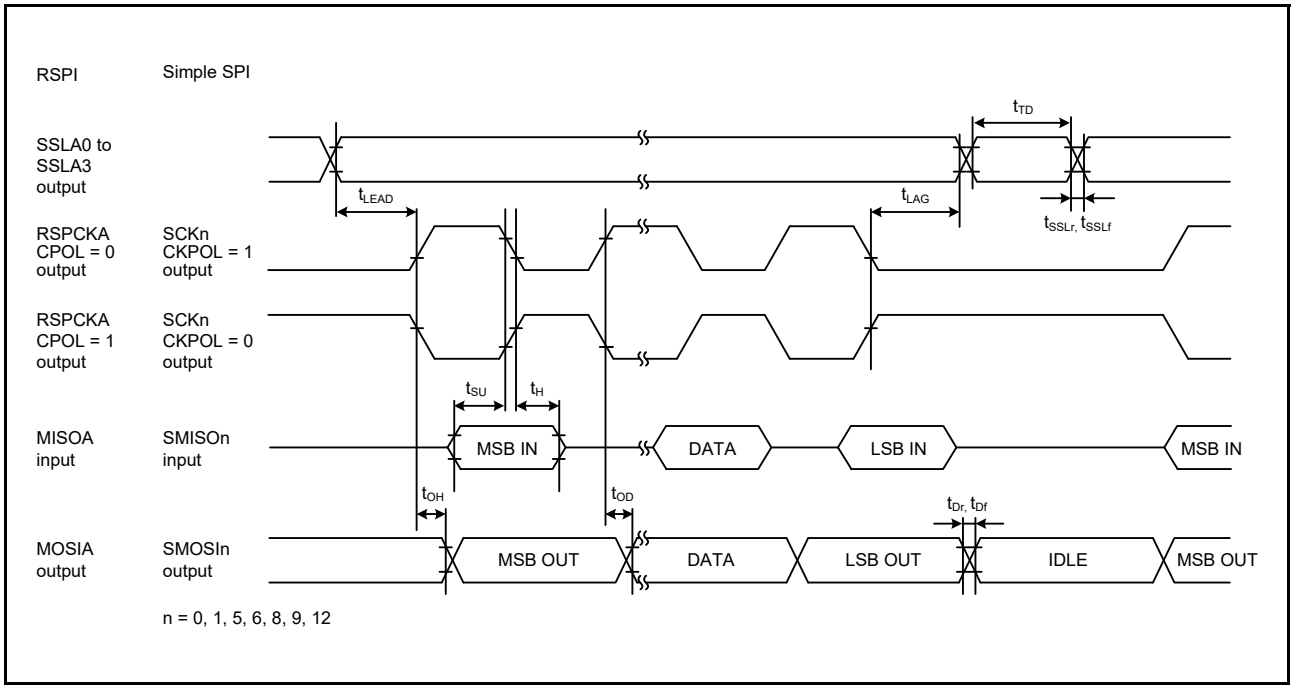


Figure 5.56 RSPI Timing (Master, CPHA = 1) and Simple SPI Clock Timing (Master, CKPH = 0)

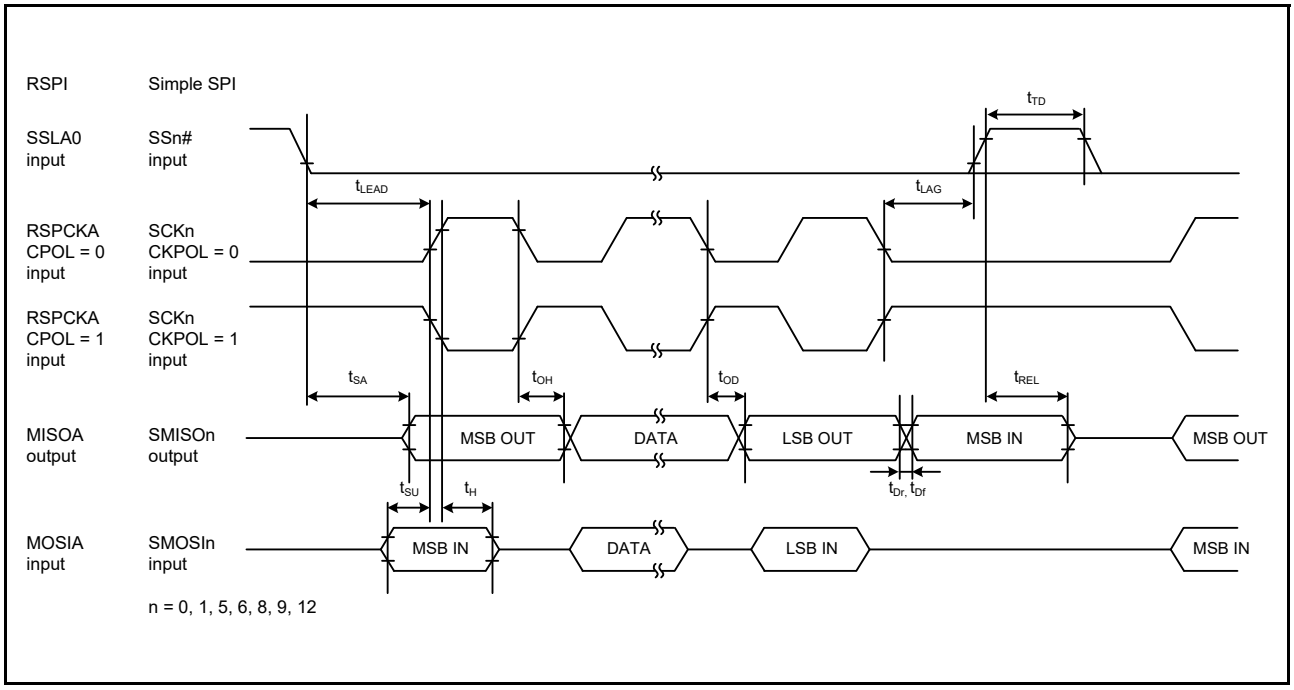


Figure 5.57 RSPI Timing (Slave, CPHA = 0) and Simple SPI Clock Timing (Slave, CKPH = 1)

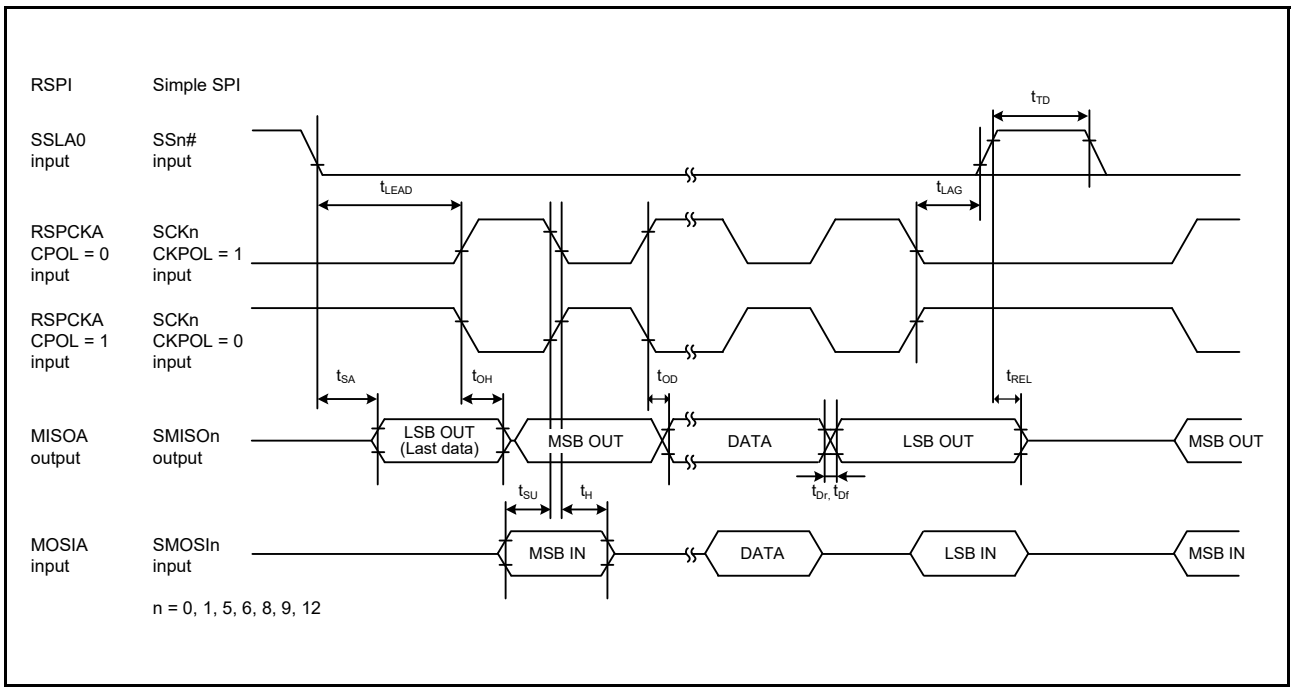


Figure 5.58 RSPI Timing (Slave, CPHA = 1) and Simple SPI Clock Timing (Slave, CKPH = 0)

Table 5.48 A/D Conversion Characteristics (3)

Conditions: 2.7V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5V, 2.7V ≤ VREFH0 ≤ AVCC0, reference voltage = VREFH0 selected,
VSS = AVSS0 = VREFL0 = VSS_USB = 0V, Ta = –40 to +105°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	27	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 27 MHz)	Permissible signal source impedance (Max.) = 1.1 kΩ	2	—	—	μs	High-precision channel The ADCSR.ADHSC bit is 1 The ADSSTRn.SST[7:0] bits are 0Dh
		3	—	—		Normal-precision channel The ADCSR.ADHSC bit is 1 The ADSSTRn.SST[7:0] bits are 28h
Analog input capacitance	Cs	—	—	15	pF	Pin capacitance included Figure 5.68
Analog input resistance	Rs	—	—	2.5	kΩ	Figure 5.68
Offset error		—	±0.5	±4.5	LSB	
Full-scale error		—	±0.75	±4.5	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential non-linearity error		—	±1.0	—	LSB	
INL integral non-linearity error		—	±1.0	±3.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential non-linearity error, and INL integral non-linearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

5.11 Oscillation Stop Detection Timing

Table 5.60 Oscillation Stop Detection Timing

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VREFL0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1	ms	Figure 5.78

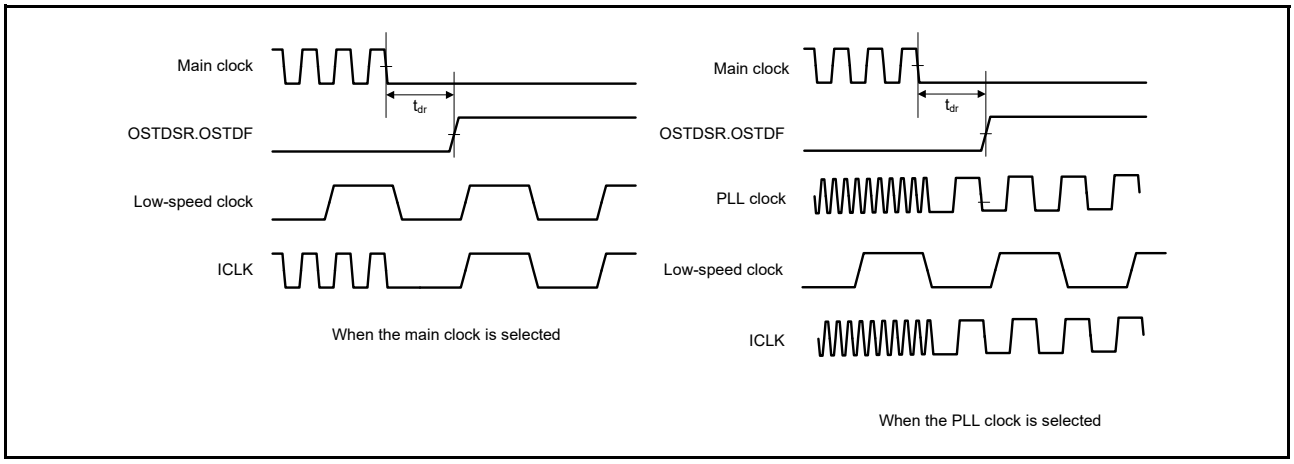


Figure 5.78 Oscillation Stop Detection Timing