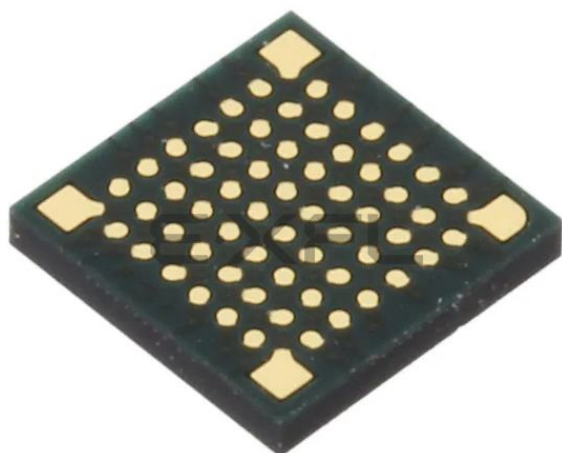




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Details

Product Status	Not For New Designs
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	54MHz
Connectivity	I ² C, IrDA, SCI, SD/SDIO, SPI, SSI, USB OTG
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	43
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-WFLGA
Supplier Device Package	64-FLGA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f52315cdlf-20

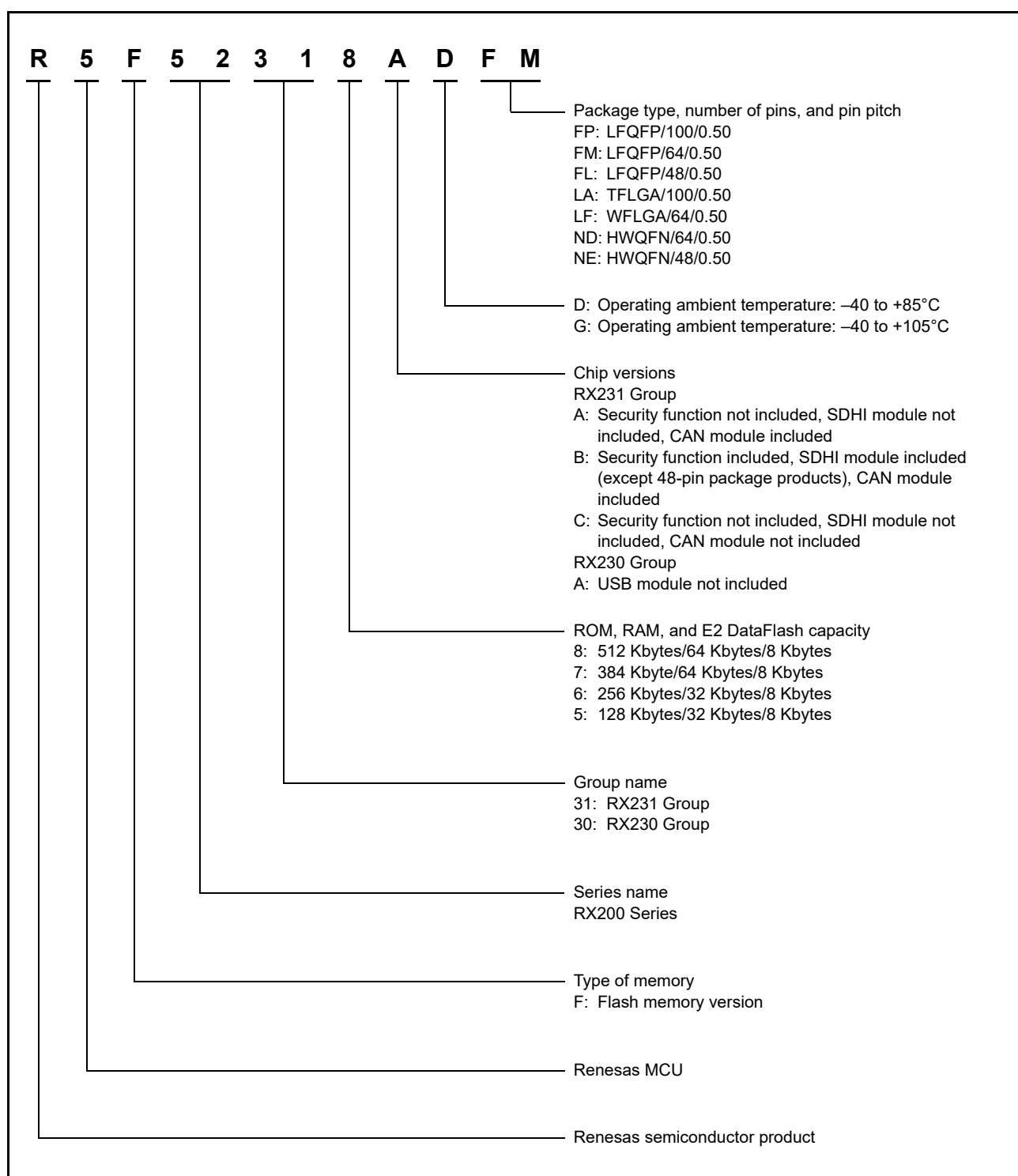


Figure 1.1 How to Read the Product Part Number

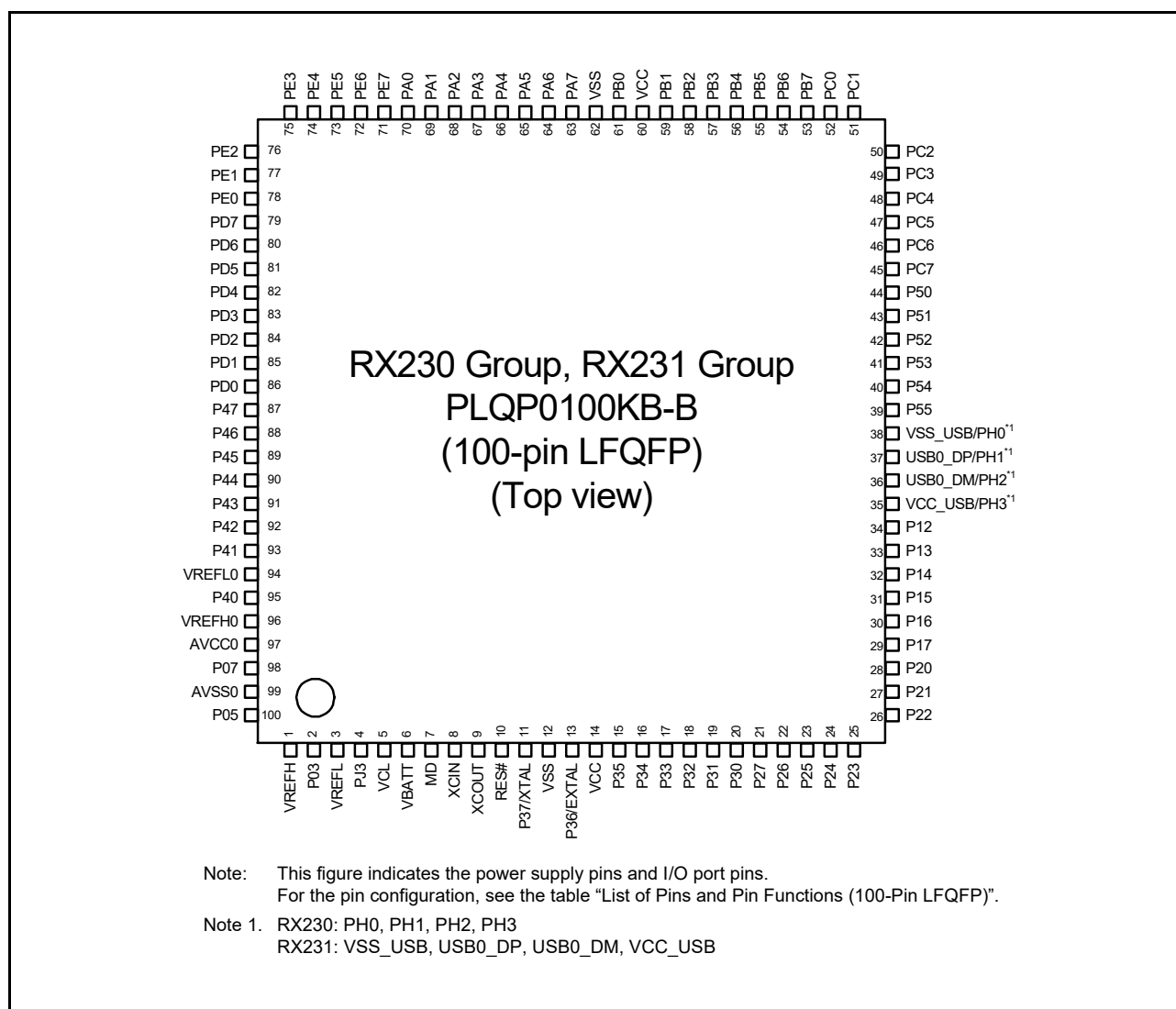
**Figure 1.4 Pin Assignments of the 100-Pin LFQFP**

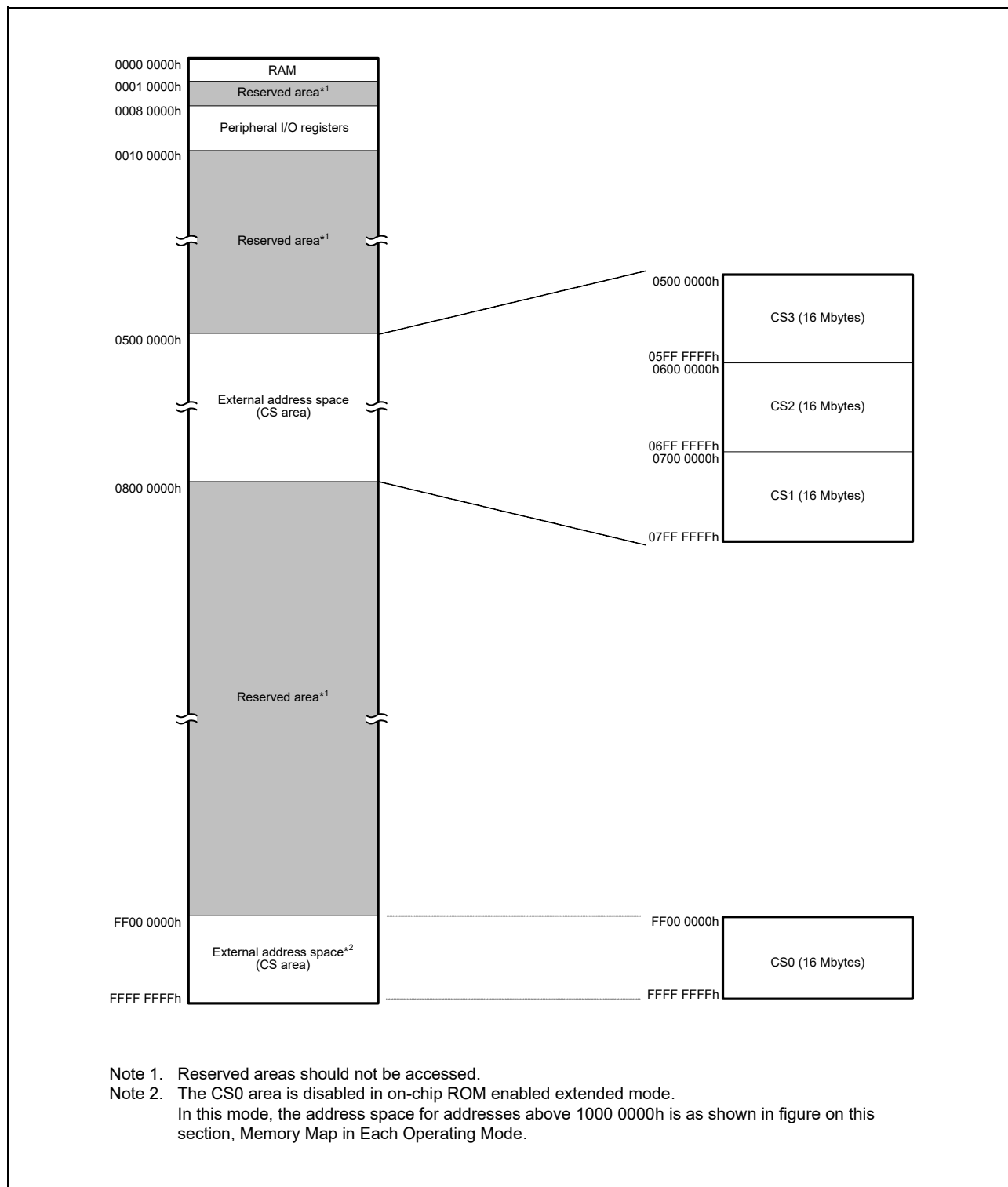
Table 1.9 List of Pins and Pin Functions (64-Pin LFQFP/HWQFN) (2/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCI, RSPI, IIC, RSCAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
42		PA4	MTIC5U/MTCLKA/TMRI0/TIOCA1	TXD5/SMOSI5/SSDA5/SSLA0/SSITXD0/IRTXD5			IRQ5 /CVREFB1
43		PA3	MTIOC0D/MTCLKD/TIOCD0/TCLKB	RXD5/SMISO5/SSCL5/SSIRXD0/IRRXD5			IRQ6 /CMPB1
44		PA1	MTIOC0B/MTCLKC/TIOCB0	SCK5/SSLA2/SSISCK0			
45		PA0	MTIOC4A/TIOCA0	SSLA1			CACREF
46		PE5	MTIOC4C/MTIOC2B				IRQ5/AN021/CMPOB0
47		PE4	MTIOC4D/MTIOC1A				AN020/CMPA2/CLKOUT
48		PE3	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#/AUDIO_MCLK			AN019/CLKOUT
49		PE2	MTIOC4A	RXD12/RXD12/SMISO12/SSCL12			IRQ7/AN018/CVREFB0
50		PE1	MTIOC4C	TXD12/TXD12/SIOX12/SMOSI12/SSDA12			AN017/CMPB0
51		PE0		SCK12			AN016
52	VREFL						
53		P46					AN006
54	VREFH						
55		P44					AN004
56		P43					AN003
57		P42					AN002
58		P41					AN001
59	VREFL0						
60		P40					AN000
61	VREFH0						
62	AVCC0						
63		P05					DA1
64	AVSS0						

Note 1. RX230: PH0/CACREF, PH1/IRQ0/TMO0, PH2/IRQ1/TMRI0, PH3/TMCIO
RX231: VSS_USB, USB_DP, USB_DM, VCC_USB

3.2 External Address Space

The external address space is divided into up to four CS areas (CS0 to CS3), each corresponding to the CSn# signal output from a CSn# (n = 0 to 3) pin. Figure 3.2 shows the address ranges corresponding to the individual CS areas (CS0 to CS3) in on-chip ROM disabled extended mode.



**Figure 3.2 Correspondence between External Address Spaces and CS Areas
(In On-Chip ROM Disabled Extended Mode)**

Table 4.1 List of I/O Registers (Address Order) (7/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
0008 830Dh	RIIC0	Slave Address Register U1	SARU1	8	8	2 or 3 PCLKB	2 ICLK
0008 830Eh	RIIC0	Slave Address Register L2	SARL2	8	8	2 or 3 PCLKB	2 ICLK
0008 830Fh	RIIC0	Slave Address Register U2	SARU2	8	8	2 or 3 PCLKB	2 ICLK
0008 8310h	RIIC0	I ² C-Bus Bit Rate Low-Level Register	ICBRL	8	8	2 or 3 PCLKB	2 ICLK
0008 8311h	RIIC0	I ² C-Bus Bit Rate High-Level Register	ICBRH	8	8	2 or 3 PCLKB	2 ICLK
0008 8312h	RIIC0	I ² C-Bus Transmit Data Register	ICDRT	8	8	2 or 3 PCLKB	2 ICLK
0008 8313h	RIIC0	I ² C-Bus Receive Data Register	ICDRR	8	8	2 or 3 PCLKB	2 ICLK
0008 8380h	RSPI0	RSPI Control Register	SPCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8381h	RSPI0	RSPI Slave Select Polarity Register	SSLP	8	8	2 or 3 PCLKB	2 ICLK
0008 8382h	RSPI0	RSPI Pin Control Register	SPPCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8383h	RSPI0	RSPI Status Register	SPSR	8	8	2 or 3 PCLKB	2 ICLK
0008 8384h	RSPI0	RSPI Data Register	SPDR	32	16, 32	2 or 3 PCLKB	2 ICLK
0008 8388h	RSPI0	RSPI Sequence Control Register	SPSCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8389h	RSPI0	RSPI Sequence Status Register	SPSSR	8	8	2 or 3 PCLKB	2 ICLK
0008 838Ah	RSPI0	RSPI Bit Rate Register	SPBR	8	8	2 or 3 PCLKB	2 ICLK
0008 838Bh	RSPI0	RSPI Data Control Register	SPDCR	8	8	2 or 3 PCLKB	2 ICLK
0008 838Ch	RSPI0	RSPI Clock Delay Register	SPCKD	8	8	2 or 3 PCLKB	2 ICLK
0008 838Dh	RSPI0	RSPI Slave Select Negation Delay Register	SSLND	8	8	2 or 3 PCLKB	2 ICLK
0008 838Eh	RSPI0	RSPI Next-Access Delay Register	SPND	8	8	2 or 3 PCLKB	2 ICLK
0008 838Fh	RSPI0	RSPI Control Register 2	SPCR2	8	8	2 or 3 PCLKB	2 ICLK
0008 8390h	RSPI0	RSPI Command Register 0	SPCMD0	16	16	2 or 3 PCLKB	2 ICLK
0008 8392h	RSPI0	RSPI Command Register 1	SPCMD1	16	16	2 or 3 PCLKB	2 ICLK
0008 8394h	RSPI0	RSPI Command Register 2	SPCMD2	16	16	2 or 3 PCLKB	2 ICLK
0008 8396h	RSPI0	RSPI Command Register 3	SPCMD3	16	16	2 or 3 PCLKB	2 ICLK
0008 8398h	RSPI0	RSPI Command Register 4	SPCMD4	16	16	2 or 3 PCLKB	2 ICLK
0008 839Ah	RSPI0	RSPI Command Register 5	SPCMD5	16	16	2 or 3 PCLKB	2 ICLK
0008 839Ch	RSPI0	RSPI Command Register 6	SPCMD6	16	16	2 or 3 PCLKB	2 ICLK
0008 839Eh	RSPI0	RSPI Command Register 7	SPCMD7	16	16	2 or 3 PCLKB	2 ICLK
0008 8410h	IRDA	IrDA Control Register	IRCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8900h	POE	Input Level Control/Status Register 1	ICSR1	16	8, 16	2 or 3 PCLKB	2 ICLK
0008 8902h	POE	Output Level Control/Status Register 1	OCSR1	16	8, 16	2 or 3 PCLKB	2 ICLK
0008 8908h	POE	Input Level Control/Status Register 2	ICSR2	16	8, 16	2 or 3 PCLKB	2 ICLK
0008 890Ah	POE	Software Port Output Enable Register	SPOER	8	8	2 or 3 PCLKB	2 ICLK
0008 890Bh	POE	Port Output Enable Control Register 1	POECR1	8	8	2 or 3 PCLKB	2 ICLK
0008 890Ch	POE	Port Output Enable Control Register 2	POECR2	8	8	2 or 3 PCLKB	2 ICLK
0008 890Eh	POE	Input Level Control/Status Register 3	ICSR3	16	8, 16	2 or 3 PCLKB	2 ICLK
0008 9000h	S12AD	A/D Control Register	ADCSR	16	16	2 or 3 PCLKB	2 ICLK
0008 9004h	S12AD	A/D Channel Select Register A0	ADANSA0	16	16	2 or 3 PCLKB	2 ICLK
0008 9006h	S12AD	A/D Channel Select Register A1	ADANSA1	16	16	2 or 3 PCLKB	2 ICLK
0008 9008h	S12AD	A/D-Converted Value Addition/Average Function Select Register 0	ADADS0	16	16	2 or 3 PCLKB	2 ICLK
0008 900Ah	S12AD	A/D-Converted Value Addition/Average Function Select Register 1	ADADS1	16	16	2 or 3 PCLKB	2 ICLK
0008 900Ch	S12AD	A/D-Converted Value Addition/Average Count Select Register	ADADC	8	8	2 or 3 PCLKB	2 ICLK
0008 900Eh	S12AD	A/D Control Extended Register	ADCER	16	16	2 or 3 PCLKB	2 ICLK
0008 9010h	S12AD	A/D Conversion Start Trigger Select Register	ADSTRGR	16	16	2 or 3 PCLKB	2 ICLK
0008 9012h	S12AD	A/D Conversion Extended Input Control Register	ADEXICR	16	16	2 or 3 PCLKB	2 ICLK
0008 9014h	S12AD	A/D Channel Select Register B0	ADANSB0	16	16	2 or 3 PCLKB	2 ICLK
0008 9016h	S12AD	A/D Channel Select Register B1	ADANSB1	16	16	2 or 3 PCLKB	2 ICLK
0008 9018h	S12AD	A/D Data Duplication Register	ADBLDR	16	16	2 or 3 PCLKB	2 ICLK
0008 901Ah	S12AD	A/D Temperature Sensor Data Register	ADTSR	16	16	2 or 3 PCLKB	2 ICLK
0008 901Ch	S12AD	A/D Internal Reference Voltage Data Register	ADOCDR	16	16	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (9/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
0008 90AAh	S12AD	A/D Compare Function Window B Upper-Side Level Setting Register	ADWINULB	16	16	2 or 3 PCLKB	2 ICLK
0008 90ACh	S12AD	A/D Compare Function Window B Channel Status Register	ADCMPBSR	8	8	2 or 3 PCLKB	2 ICLK
0008 90B0h	S12AD	A/D Data Storage Buffer Register 0	ADBUF0	16	16	2 or 3 PCLKB	2 ICLK
0008 90B2h	S12AD	A/D Data Storage Buffer Register 1	ADBUF1	16	16	2 or 3 PCLKB	2 ICLK
0008 90B4h	S12AD	A/D Data Storage Buffer Register 2	ADBUF2	16	16	2 or 3 PCLKB	2 ICLK
0008 90B6h	S12AD	A/D Data Storage Buffer Register 3	ADBUF3	16	16	2 or 3 PCLKB	2 ICLK
0008 90B8h	S12AD	A/D Data Storage Buffer Register 4	ADBUF4	16	16	2 or 3 PCLKB	2 ICLK
0008 90BAh	S12AD	A/D Data Storage Buffer Register 5	ADBUF5	16	16	2 or 3 PCLKB	2 ICLK
0008 90BCh	S12AD	A/D Data Storage Buffer Register 6	ADBUF6	16	16	2 or 3 PCLKB	2 ICLK
0008 90BEh	S12AD	A/D Data Storage Buffer Register 7	ADBUF7	16	16	2 or 3 PCLKB	2 ICLK
0008 90C0h	S12AD	A/D Data Storage Buffer Register 8	ADBUF8	16	16	2 or 3 PCLKB	2 ICLK
0008 90C2h	S12AD	A/D Data Storage Buffer Register 9	ADBUF9	16	16	2 or 3 PCLKB	2 ICLK
0008 90C4h	S12AD	A/D Data Storage Buffer Register 10	ADBUF10	16	16	2 or 3 PCLKB	2 ICLK
0008 90C6h	S12AD	A/D Data Storage Buffer Register 11	ADBUF11	16	16	2 or 3 PCLKB	2 ICLK
0008 90C8h	S12AD	A/D Data Storage Buffer Register 12	ADBUF12	16	16	2 or 3 PCLKB	2 ICLK
0008 90CAh	S12AD	A/D Data Storage Buffer Register 13	ADBUF13	16	16	2 or 3 PCLKB	2 ICLK
0008 90CCh	S12AD	A/D Data Storage Buffer Register 14	ADBUF14	16	16	2 or 3 PCLKB	2 ICLK
0008 90CEh	S12AD	A/D Data Storage Buffer Register 15	ADBUF15	16	16	2 or 3 PCLKB	2 ICLK
0008 90D0h	S12AD	A/D Data Storage Buffer Enable Register	ADBUFEN	8	8	2 or 3 PCLKB	2 ICLK
0008 90D2h	S12AD	A/D Data Storage Buffer Pointer Register	ADBUFPTR	8	8	2 or 3 PCLKB	2 ICLK
0008 90DDh	S12AD	A/D Sampling State Register L	ADSSTRL	8	8	2 or 3 PCLKB	2 ICLK
0008 90DEh	S12AD	A/D Sampling State Register T	ADSSTRT	8	8	2 or 3 PCLKB	2 ICLK
0008 90DFh	S12AD	A/D Sampling State Register O	ADSSTRO	8	8	2 or 3 PCLKB	2 ICLK
0008 90E0h	S12AD	A/D Sampling State Register 0	ADSSTR0	8	8	2 or 3 PCLKB	2 ICLK
0008 90E1h	S12AD	A/D Sampling State Register 1	ADSSTR1	8	8	2 or 3 PCLKB	2 ICLK
0008 90E2h	S12AD	A/D Sampling State Register 2	ADSSTR2	8	8	2 or 3 PCLKB	2 ICLK
0008 90E3h	S12AD	A/D Sampling State Register 3	ADSSTR3	8	8	2 or 3 PCLKB	2 ICLK
0008 90E4h	S12AD	A/D Sampling State Register 4	ADSSTR4	8	8	2 or 3 PCLKB	2 ICLK
0008 90E5h	S12AD	A/D Sampling State Register 5	ADSSTR5	8	8	2 or 3 PCLKB	2 ICLK
0008 90E6h	S12AD	A/D Sampling State Register 6	ADSSTR6	8	8	2 or 3 PCLKB	2 ICLK
0008 90E7h	S12AD	A/D Sampling State Register 7	ADSSTR7	8	8	2 or 3 PCLKB	2 ICLK
0008 A000h	SCI0	Serial Mode Register	SMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A001h	SCI0	Bit Rate Register	BRR	8	8	2 or 3 PCLKB	2 ICLK
0008 A002h	SCI0	Serial Control Register	SCR	8	8	2 or 3 PCLKB	2 ICLK
0008 A003h	SCI0	Transmit Data Register	TDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A004h	SCI0	Serial Status Register	SSR	8	8	2 or 3 PCLKB	2 ICLK
0008 A005h	SCI0	Receive Data Register	RDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A006h	SCI0	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A007h	SCI0	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A008h	SCI0	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB	2 ICLK
0008 A009h	SCI0	I ² C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB	2 ICLK
0008 A00Ah	SCI0	I ² C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB	2 ICLK
0008 A00Bh	SCI0	I ² C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB	2 ICLK
0008 A00Ch	SCI0	I ² C Status Register	SISR	8	8	2 or 3 PCLKB	2 ICLK
0008 A00Dh	SCI0	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A00Eh	SCI0	Transmit Data Register HL	TDRHL	16	16	4 or 5 PCLKB	2 ICLK
0008 A00Eh	SCI0	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB	2 ICLK
0008 A00Fh	SCI0	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB	2 ICLK
0008 A010h	SCI0	Receive Data Register HL	RDRHL	16	16	4 or 5 PCLKB	2 ICLK
0008 A010h	SCI0	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB	2 ICLK
0008 A011h	SCI0	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (11/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
0008 A0C9h	SCI6	I ² C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB	2 ICLK
0008 A0CAh	SCI6	I ² C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB	2 ICLK
0008 A0CBh	SCI6	I ² C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB	2 ICLK
0008 A0CCh	SCI6	I ² C Status Register	SISR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0CDh	SCI6	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0CEh	SCI6	Transmit Data Register HL	TDRHL	16	16	4 or 5 PCLKB	2 ICLK
0008 A0CEh	SCI6	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB	2 ICLK
0008 A0CFh	SCI6	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB	2 ICLK
0008 A0D0h	SCI6	Receive Data Register HL	RDRHL	16	16	4 or 5 PCLKB	2 ICLK
0008 A0D0h	SCI6	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB	2 ICLK
0008 A0D1h	SCI6	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB	2 ICLK
0008 A0D2h	SCI6	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A100h	SCI8	Serial Mode Register	SMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A101h	SCI8	Bit Rate Register	BRR	8	8	2 or 3 PCLKB	2 ICLK
0008 A102h	SCI8	Serial Control Register	SCR	8	8	2 or 3 PCLKB	2 ICLK
0008 A103h	SCI8	Transmit Data Register	TDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A104h	SCI8	Serial Status Register	SSR	8	8	2 or 3 PCLKB	2 ICLK
0008 A105h	SCI8	Receive Data Register	RDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A106h	SCI8	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A107h	SCI8	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A108h	SCI8	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB	2 ICLK
0008 A109h	SCI8	I ² C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB	2 ICLK
0008 A10Ah	SCI8	I ² C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB	2 ICLK
0008 A10Bh	SCI8	I ² C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB	2 ICLK
0008 A10Ch	SCI8	I ² C Status Register	SISR	8	8	2 or 3 PCLKB	2 ICLK
0008 A10Dh	SCI8	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A10Eh	SCI8	Transmit Data Register HL	TDRHL	16	16	4 or 5 PCLKB	2 ICLK
0008 A10Eh	SCI8	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB	2 ICLK
0008 A10Fh	SCI8	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB	2 ICLK
0008 A110h	SCI8	Receive Data Register HL	RDRHL	16	16	4 or 5 PCLKB	2 ICLK
0008 A110h	SCI8	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB	2 ICLK
0008 A111h	SCI8	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB	2 ICLK
0008 A112h	SCI8	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A120h	SCI9	Serial Mode Register	SMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A121h	SCI9	Bit Rate Register	BRR	8	8	2 or 3 PCLKB	2 ICLK
0008 A122h	SCI9	Serial Control Register	SCR	8	8	2 or 3 PCLKB	2 ICLK
0008 A123h	SCI9	Transmit Data Register	TDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A124h	SCI9	Serial Status Register	SSR	8	8	2 or 3 PCLKB	2 ICLK
0008 A125h	SCI9	Receive Data Register	RDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A126h	SCI9	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A127h	SCI9	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A128h	SCI9	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB	2 ICLK
0008 A129h	SCI9	I ² C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB	2 ICLK
0008 A12Ah	SCI9	I ² C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB	2 ICLK
0008 A12Bh	SCI9	I ² C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB	2 ICLK
0008 A12Ch	SCI9	I ² C Status Register	SISR	8	8	2 or 3 PCLKB	2 ICLK
0008 A12Dh	SCI9	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A12Eh	SCI9	Transmit Data Register HL	TDRHL	16	16	4 or 5 PCLKB	2 ICLK
0008 A12Eh	SCI9	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB	2 ICLK
0008 A12Fh	SCI9	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB	2 ICLK
0008 A130h	SCI9	Receive Data Register HL	RDRHL	16	16	4 or 5 PCLKB	2 ICLK
0008 A130h	SCI9	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (19/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
0008 C1B3h	MPC	PE3 Pin Function Control Register	PE3PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1B4h	MPC	PE4 Pin Function Control Register	PE4PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1B5h	MPC	PE5 Pin Function Control Register	PE5PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1B6h	MPC	PE6 Pin Function Control Register	PE6PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1B7h	MPC	PE7 Pin Function Control Register	PE7PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1C8h	MPC	PH0 Pin Function Control Register	PH0PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1C9h	MPC	PH1 Pin Function Control Register	PH1PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1CAh	MPC	PH2 Pin Function Control Register	PH2PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1CBh	MPC	PH3 Pin Function Control Register	PH3PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1D3h	MPC	PJ3 Pin Function Control Register	PJ3PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C290h	SYSTEM	Reset Status Register 0	RSTSR0	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C291h	SYSTEM	Reset Status Register 1	RSTSR1	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C293h	SYSTEM	Main Clock Oscillator Forced Oscillation Control Register	MOFCR	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C297h	SYSTEM	Voltage Monitoring Circuit Control Register	LVCMPCR	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C298h	SYSTEM	Voltage Detection Level Select Register	LVDLVL	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C29Ah	SYSTEM	Voltage Monitoring 1 Circuit Control Register 0	LVD1CR0	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C29Bh	SYSTEM	Voltage Monitoring 2 Circuit Control Register 0	LVD2CR0	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C29Dh	SYSTEM	VBATT Control Register	VBATTCT	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C29Eh	SYSTEM	VBATT Status Register	VBATTST	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C29Fh	SYSTEM	VBATT Pin Voltage Drop Detection Interrupt Control Register	VBTLVDICR	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C400h	RTC	64-Hz Counter	R64CNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C402h	RTC	Second Counter	RSECCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C402h	RTC	Binary Counter 0	BCNT0	8	8	2 or 3 PCLKB	2 ICLK
0008 C404h	RTC	Minute Counter	RMINCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C404h	RTC	Binary Counter 1	BCNT1	8	8	2 or 3 PCLKB	2 ICLK
0008 C406h	RTC	Hour Counter	RHRCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C406h	RTC	Binary Counter 2	BCNT2	8	8	2 or 3 PCLKB	2 ICLK
0008 C408h	RTC	Day-of-Week Counter	RWKCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C408h	RTC	Binary Counter 3	BCNT3	8	8	2 or 3 PCLKB	2 ICLK
0008 C40Ah	RTC	Date Counter	RDAYCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C40Ch	RTC	Month Counter	RMONCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C40Eh	RTC	Year Counter	RYRCNT	16	16	2 or 3 PCLKB	2 ICLK
0008 C410h	RTC	Second Alarm Register	RSECAR	8	8	2 or 3 PCLKB	2 ICLK
0008 C410h	RTC	Binary Counter 0 Alarm Register	BCNT0AR	8	8	2 or 3 PCLKB	2 ICLK
0008 C412h	RTC	Minute Alarm Register	RMINAR	8	8	2 or 3 PCLKB	2 ICLK
0008 C412h	RTC	Binary Counter 1 Alarm Register	BCNT1AR	8	8	2 or 3 PCLKB	2 ICLK
0008 C414h	RTC	Hour Alarm Register	RHRAR	8	8	2 or 3 PCLKB	2 ICLK
0008 C414h	RTC	Binary Counter 2 Alarm Register	BCNT2AR	8	8	2 or 3 PCLKB	2 ICLK
0008 C416h	RTC	Day-of-Week Alarm Register	RWKAR	8	8	2 or 3 PCLKB	2 ICLK
0008 C416h	RTC	Binary Counter 3 Alarm Register	BCNT3AR	8	8	2 or 3 PCLKB	2 ICLK
0008 C418h	RTC	Date Alarm Register	RDAYAR	8	8	2 or 3 PCLKB	2 ICLK
0008 C418h	RTC	Binary Counter 0 Alarm Enable Register	BCNT0AER	8	8	2 or 3 PCLKB	2 ICLK
0008 C41Ah	RTC	Month Alarm Register	RMONAR	8	8	2 or 3 PCLKB	2 ICLK
0008 C41Ah	RTC	Binary Counter 1 Alarm Enable Register	BCNT1AER	8	8	2 or 3 PCLKB	2 ICLK
0008 C41Ch	RTC	Year Alarm Register	RYRAR	16	16	2 or 3 PCLKB	2 ICLK
0008 C41Ch	RTC	Binary Counter 2 Alarm Enable Register	BCNT2AER	16	16	2 or 3 PCLKB	2 ICLK
0008 C41Eh	RTC	Year Alarm Enable Register	RYRAREN	8	8	2 or 3 PCLKB	2 ICLK
0008 C41Eh	RTC	Binary Counter 3 Alarm Enable Register	BCNT3AER	8	8	2 or 3 PCLKB	2 ICLK
0008 C422h	RTC	RTC Control Register 1	RCR1	8	8	2 or 3 PCLKB	2 ICLK
0008 C424h	RTC	RTC Control Register 2	RCR2	8	8	2 or 3 PCLKB	2 ICLK
0008 C426h	RTC	RTC Control Register 3	RCR3	8	8	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (30/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK $\geq$ PCLK	ICLK < PCLK
000A 85EAh	RSCAN0	Transmit/Receive FIFO Access Register 0CH	CFDF10	16	16	2 or 3 PCLKB	2 ICLK
000A 85EAh	RSCAN	RAM Test Register 53	RPGACC53	16	16	2 or 3 PCLKB	2 ICLK
000A 85ECh	RSCAN0	Transmit/Receive FIFO Access Register 0DL	CFDF20	16	16	2 or 3 PCLKB	2 ICLK
000A 85ECh	RSCAN	RAM Test Register 54	RPGACC54	16	16	2 or 3 PCLKB	2 ICLK
000A 85EEh	RSCAN0	Transmit/Receive FIFO Access Register 0DH	CFDF30	16	16	2 or 3 PCLKB	2 ICLK
000A 85EEh	RSCAN	RAM Test Register 55	RPGACC55	16	16	2 or 3 PCLKB	2 ICLK
000A 85F0h to 000A 85FEh	RSCAN	RAM Test Register 56 to RAM Test Register 63	RPGACC56 to RPGACC63	16	16	2 or 3 PCLKB	2 ICLK
000A 8600h	RSCAN0	Transmit Buffer Register 0AL	TMIDL0	16	16	2 or 3 PCLKB	2 ICLK
000A 8600h	RSCAN	RAM Test Register 64	RPGACC64	16	16	2 or 3 PCLKB	2 ICLK
000A 8602h	RSCAN0	Transmit Buffer Register 0AH	TMIDH0	16	16	2 or 3 PCLKB	2 ICLK
000A 8602h	RSCAN	RAM Test Register 65	RPGACC65	16	16	2 or 3 PCLKB	2 ICLK
000A 8604h	RSCAN	RAM Test Register 66	RPGACC66	16	16	2 or 3 PCLKB	2 ICLK
000A 8606h	RSCAN0	Transmit Buffer Register 0BH	TMPTR0	16	16	2 or 3 PCLKB	2 ICLK
000A 8606h	RSCAN	RAM Test Register 67	RPGACC67	16	16	2 or 3 PCLKB	2 ICLK
000A 8608h	RSCAN0	Transmit Buffer Register 0CL	TMDF00	16	16	2 or 3 PCLKB	2 ICLK
000A 8608h	RSCAN	RAM Test Register 68	RPGACC68	16	16	2 or 3 PCLKB	2 ICLK
000A 860Ah	RSCAN0	Transmit Buffer Register 0CH	TMDF10	16	16	2 or 3 PCLKB	2 ICLK
000A 860Ah	RSCAN	RAM Test Register 69	RPGACC69	16	16	2 or 3 PCLKB	2 ICLK
000A 860Ch	RSCAN0	Transmit Buffer Register 0DL	TMDF20	16	16	2 or 3 PCLKB	2 ICLK
000A 860Ch	RSCAN	RAM Test Register 70	RPGACC70	16	16	2 or 3 PCLKB	2 ICLK
000A 860Eh	RSCAN0	Transmit Buffer Register 0DH	TMDF30	16	16	2 or 3 PCLKB	2 ICLK
000A 860Eh	RSCAN	RAM Test Register 71	RPGACC71	16	16	2 or 3 PCLKB	2 ICLK
000A 8610h	RSCAN0	Transmit Buffer Register 1AL	TMIDL1	16	16	2 or 3 PCLKB	2 ICLK
000A 8610h	RSCAN	RAM Test Register 72	RPGACC72	16	16	2 or 3 PCLKB	2 ICLK
000A 8612h	RSCAN0	Transmit Buffer Register 1AH	TMIDH1	16	16	2 or 3 PCLKB	2 ICLK
000A 8612h	RSCAN	RAM Test Register 73	RPGACC73	16	16	2 or 3 PCLKB	2 ICLK
000A 8614h	RSCAN	RAM Test Register 74	RPGACC74	16	16	2 or 3 PCLKB	2 ICLK
000A 8616h	RSCAN0	Transmit Buffer Register 1BH	TMPTR1	16	16	2 or 3 PCLKB	2 ICLK
000A 8616h	RSCAN	RAM Test Register 75	RPGACC75	16	16	2 or 3 PCLKB	2 ICLK
000A 8618h	RSCAN0	Transmit Buffer Register 1CL	TMDF01	16	16	2 or 3 PCLKB	2 ICLK
000A 8618h	RSCAN	RAM Test Register 76	RPGACC76	16	16	2 or 3 PCLKB	2 ICLK
000A 861Ah	RSCAN0	Transmit Buffer Register 1CH	TMDF11	16	16	2 or 3 PCLKB	2 ICLK
000A 861Ah	RSCAN	RAM Test Register 77	RPGACC77	16	16	2 or 3 PCLKB	2 ICLK
000A 861Ch	RSCAN0	Transmit Buffer Register 1DL	TMDF21	16	16	2 or 3 PCLKB	2 ICLK
000A 861Ch	RSCAN	RAM Test Register 78	RPGACC78	16	16	2 or 3 PCLKB	2 ICLK
000A 861Eh	RSCAN0	Transmit Buffer Register 1DH	TMDF31	16	16	2 or 3 PCLKB	2 ICLK
000A 861Eh	RSCAN	RAM Test Register 79	RPGACC79	16	16	2 or 3 PCLKB	2 ICLK
000A 8620h	RSCAN0	Transmit Buffer Register 2AL	TMIDL2	16	16	2 or 3 PCLKB	2 ICLK
000A 8620h	RSCAN	RAM Test Register 80	RPGACC80	16	16	2 or 3 PCLKB	2 ICLK
000A 8622h	RSCAN0	Transmit Buffer Register 2AH	TMIDH2	16	16	2 or 3 PCLKB	2 ICLK
000A 8622h	RSCAN	RAM Test Register 81	RPGACC81	16	16	2 or 3 PCLKB	2 ICLK
000A 8624h	RSCAN	RAM Test Register 82	RPGACC82	16	16	2 or 3 PCLKB	2 ICLK
000A 8626h	RSCAN0	Transmit Buffer Register 2BH	TMPTR2	16	16	2 or 3 PCLKB	2 ICLK
000A 8626h	RSCAN	RAM Test Register 83	RPGACC83	16	16	2 or 3 PCLKB	2 ICLK
000A 8628h	RSCAN0	Transmit Buffer Register 2CL	TMDF02	16	16	2 or 3 PCLKB	2 ICLK
000A 8628h	RSCAN	RAM Test Register 84	RPGACC84	16	16	2 or 3 PCLKB	2 ICLK
000A 862Ah	RSCAN0	Transmit Buffer Register 2CH	TMDF12	16	16	2 or 3 PCLKB	2 ICLK
000A 862Ah	RSCAN	RAM Test Register 85	RPGACC85	16	16	2 or 3 PCLKB	2 ICLK
000A 862Ch	RSCAN0	Transmit Buffer Register 2DL	TMDF22	16	16	2 or 3 PCLKB	2 ICLK
000A 862Ch	RSCAN	RAM Test Register 86	RPGACC86	16	16	2 or 3 PCLKB	2 ICLK
000A 862Eh	RSCAN0	Transmit Buffer Register 2DH	TMDF32	16	16	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (32/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK $\geq$ PCLK	ICLK < PCLK
000D 0A34h	MTU	Timer Dead Time Enable Register	TDER	8	8	2 or 3 PCLKA	2 ICLK
000D 0A36h	MTU	Timer Output Level Buffer Register	TOLBR	8	8	2 or 3 PCLKA	2 ICLK
000D 0A38h	MTU3	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	2 or 3 PCLKA	2 ICLK
000D 0A39h	MTU4	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	2 or 3 PCLKA	2 ICLK
000D 0A40h	MTU4	Timer A/D Converter Start Request Control Register	TADCR	16	16	2 or 3 PCLKA	2 ICLK
000D 0A44h	MTU4	Timer A/D Converter Start Request Cycle Set Register A	TADCORA	16	16	2 or 3 PCLKA	2 ICLK
000D 0A46h	MTU4	Timer A/D Converter Start Request Cycle Set Register B	TADCORB	16	16	2 or 3 PCLKA	2 ICLK
000D 0A48h	MTU4	Timer A/D Converter Start Request Cycle Set Buffer Register A	TADCOBRA	16	16	2 or 3 PCLKA	2 ICLK
000D 0A4Ah	MTU4	Timer A/D Converter Start Request Cycle Set Buffer Register B	TADCOBRB	16	16	2 or 3 PCLKA	2 ICLK
000D 0A60h	MTU	Timer Waveform Control Register	TWCR	8	8, 16	2 or 3 PCLKA	2 ICLK
000D 0A80h	MTU	Timer Start Register	TSTR	8	8, 16	2 or 3 PCLKA	2 ICLK
000D 0A81h	MTU	Timer Synchronous Register	TSYR	8	8, 16	2 or 3 PCLKA	2 ICLK
000D 0A84h	MTU	Timer Read/Write Enable Register	TRWER	8	8, 16	2 or 3 PCLKA	2 ICLK
000D 0A90h	MTU0	Noise Filter Control Register	NFCR	8	8, 16	2 or 3 PCLKA	2 ICLK
000D 0A91h	MTU1	Noise Filter Control Register	NFCR	8	8, 16	2 or 3 PCLKA	2 ICLK
000D 0A92h	MTU2	Noise Filter Control Register	NFCR	8	8, 16	2 or 3 PCLKA	2 ICLK
000D 0A93h	MTU3	Noise Filter Control Register	NFCR	8	8, 16	2 or 3 PCLKA	2 ICLK
000D 0A94h	MTU4	Noise Filter Control Register	NFCR	8	8, 16	2 or 3 PCLKA	2 ICLK
000D 0A95h	MTU5	Noise Filter Control Register	NFCR	8	8, 16	2 or 3 PCLKA	2 ICLK
000D 0B00h	MTU0	Timer Control Register	TCR	8	8	2 or 3 PCLKA	2 ICLK
000D 0B01h	MTU0	Timer Mode Register	TMDR	8	8	2 or 3 PCLKA	2 ICLK
000D 0B02h	MTU0	Timer I/O Control Register H	TIORH	8	8	2 or 3 PCLKA	2 ICLK
000D 0B03h	MTU0	Timer I/O Control Register L	TIORL	8	8	2 or 3 PCLKA	2 ICLK
000D 0B04h	MTU0	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKA	2 ICLK
000D 0B05h	MTU0	Timer Status Register	TSR	8	8	2 or 3 PCLKA	2 ICLK
000D 0B06h	MTU0	Timer Counter	TCNT	16	16	2 or 3 PCLKA	2 ICLK
000D 0B08h	MTU0	Timer General Register A	TGRA	16	16	2 or 3 PCLKA	2 ICLK
000D 0B0Ah	MTU0	Timer General Register B	TGRB	16	16	2 or 3 PCLKA	2 ICLK
000D 0B0Ch	MTU0	Timer General Register C	TGRC	16	16	2 or 3 PCLKA	2 ICLK
000D 0B0Eh	MTU0	Timer General Register D	TGRD	16	16	2 or 3 PCLKA	2 ICLK
000D 0B20h	MTU0	Timer General Register E	TGRE	16	16	2 or 3 PCLKA	2 ICLK
000D 0B22h	MTU0	Timer General Register F	TGRF	16	16	2 or 3 PCLKA	2 ICLK
000D 0B24h	MTU0	Timer Interrupt Enable Register 2	TIER2	8	8	2 or 3 PCLKA	2 ICLK
000D 0B26h	MTU0	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	2 or 3 PCLKA	2 ICLK
000D 0B80h	MTU1	Timer Control Register	TCR	8	8	2 or 3 PCLKA	2 ICLK
000D 0B81h	MTU1	Timer Mode Register	TMDR	8	8	2 or 3 PCLKA	2 ICLK
000D 0B82h	MTU1	Timer I/O Control Register	TIOR	8	8	2 or 3 PCLKA	2 ICLK
000D 0B84h	MTU1	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKA	2 ICLK
000D 0B85h	MTU1	Timer Status Register	TSR	8	8	2 or 3 PCLKA	2 ICLK
000D 0B86h	MTU1	Timer Counter	TCNT	16	16	2 or 3 PCLKA	2 ICLK
000D 0B88h	MTU1	Timer General Register A	TGRA	16	16	2 or 3 PCLKA	2 ICLK
000D 0B8Ah	MTU1	Timer General Register B	TGRB	16	16	2 or 3 PCLKA	2 ICLK
000D 0B90h	MTU1	Timer Input Capture Control Register	TICCR	8	8	2 or 3 PCLKA	2 ICLK
000D 0C00h	MTU2	Timer Control Register	TCR	8	8	2 or 3 PCLKA	2 ICLK
000D 0C01h	MTU2	Timer Mode Register	TMDR	8	8	2 or 3 PCLKA	2 ICLK
000D 0C02h	MTU2	Timer I/O Control Register	TIOR	8	8	2 or 3 PCLKA	2 ICLK
000D 0C04h	MTU2	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKA	2 ICLK
000D 0C05h	MTU2	Timer Status Register	TSR	8	8	2 or 3 PCLKA	2 ICLK
000D 0C06h	MTU2	Timer Counter	TCNT	16	16	2 or 3 PCLKA	2 ICLK
000D 0C08h	MTU2	Timer General Register A	TGRA	16	16	2 or 3 PCLKA	2 ICLK
000D 0C0Ah	MTU2	Timer General Register B	TGRB	16	16	2 or 3 PCLKA	2 ICLK

Table 5.8 DC Characteristics (6)Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} = \text{AVCC0} \leq 5.5\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

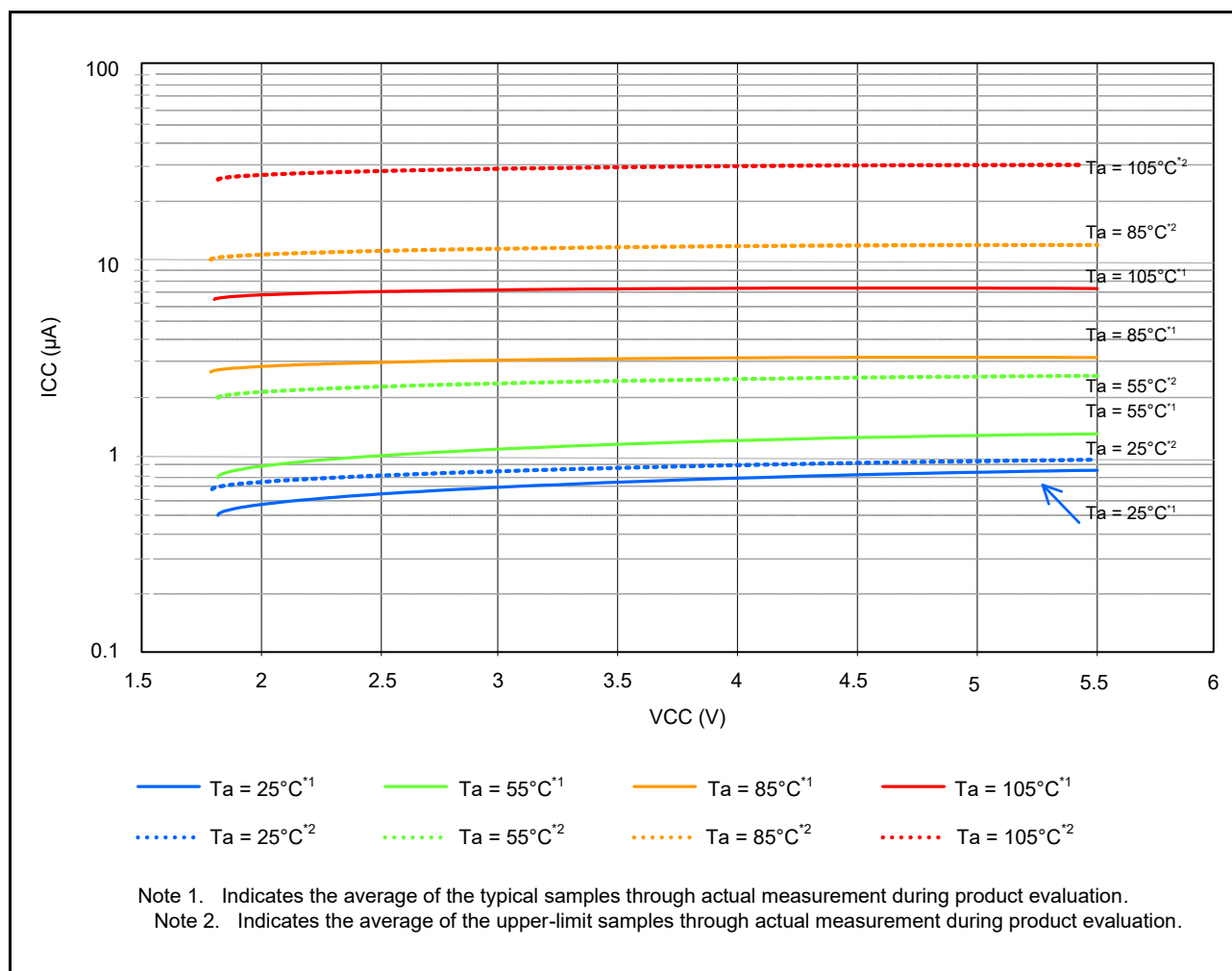
Item			Symbol	Typ.*3	Max.	Unit	Test Conditions
Supply current*1	Software standby mode*2	T _a = 25°C	I _{CC}	0.8	3.7	μA	
		T _a = 55°C		1.2	4.3		
		T _a = 85°C		3.5	18.6		
		T _a = 105°C		7.9	45.2		
	Increment for IWDT operation			0.4	—		Use IWDT-Dedicated On-Chip Oscillator for clock source
	Increment for LPT operation			0.4	—		
	Increment for RTC operation*4			0.4	—		
				1.2	—		RCR3.RTCDV[2:0] set to normal drive capacity

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.

Note 2. The IWDG, LVD, and CMPB are stopped.

Note 3. When VCC is 3.3 V.

Note 4. This increment includes the oscillation circuit.

**Figure 5.4 Voltage Dependency in Software Standby Mode (Reference Data)**

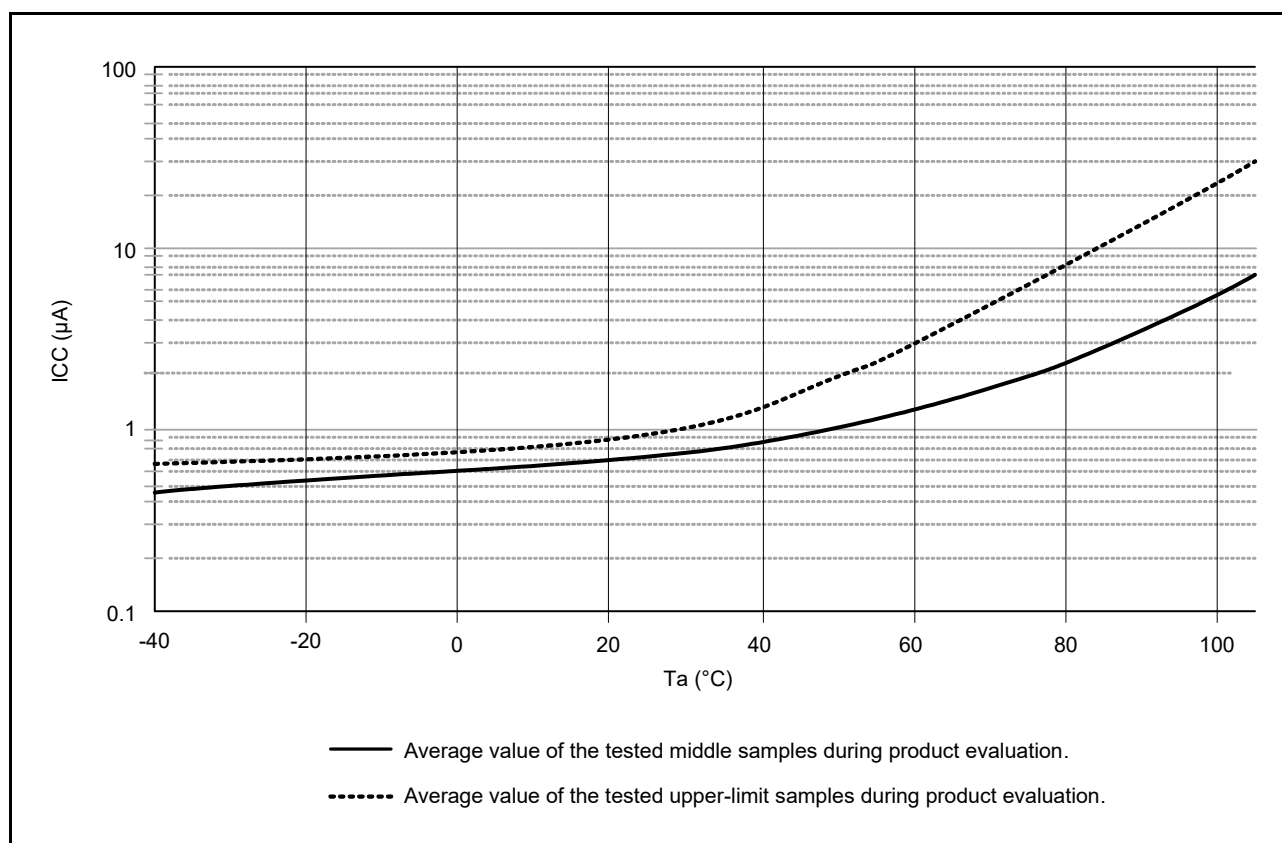


Figure 5.5 Temperature Dependency in Software Standby Mode (Reference Data)

Table 5.9 DC Characteristics (7)

Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} = AV_{CC0} \leq 5.5\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item			Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	RTC operation when VCC is off	T _a = 25°C	I _{CC}	0.8	—	μA	VBATT = 2.0 V RCR3.RTCDV[2:0] set to low drive capacity
		T _a = 55°C		0.9	—		
		T _a = 85°C		1.0	—		
		T _a = 105°C		1.2	—		
		T _a = 25°C		0.9	—		VBATT = 3.3 V RCR3.RTCDV[2:0] set to low drive capacity
		T _a = 55°C		1.0	—		
		T _a = 85°C		1.1	—		
		T _a = 105°C		1.3	—		
		T _a = 25°C		1.5	—		VBATT = 2.0 V RCR3.RTCDV[2:0] set to normal drive capacity
		T _a = 55°C		1.8	—		
		T _a = 85°C		2.1	—		
		T _a = 105°C		2.4	—		
		T _a = 25°C		1.6	—		VBATT = 3.3 V RCR3.RTCDV[2:0] set to normal drive capacity
		T _a = 55°C		1.9	—		
		T _a = 85°C		2.2	—		
		T _a = 105°C		2.5	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

5.2.2 Normal I/O Pin Output Characteristics (2)

Figure 5.13 to Figure 5.17 show the characteristics when high-drive output is selected by the drive capacity control register.

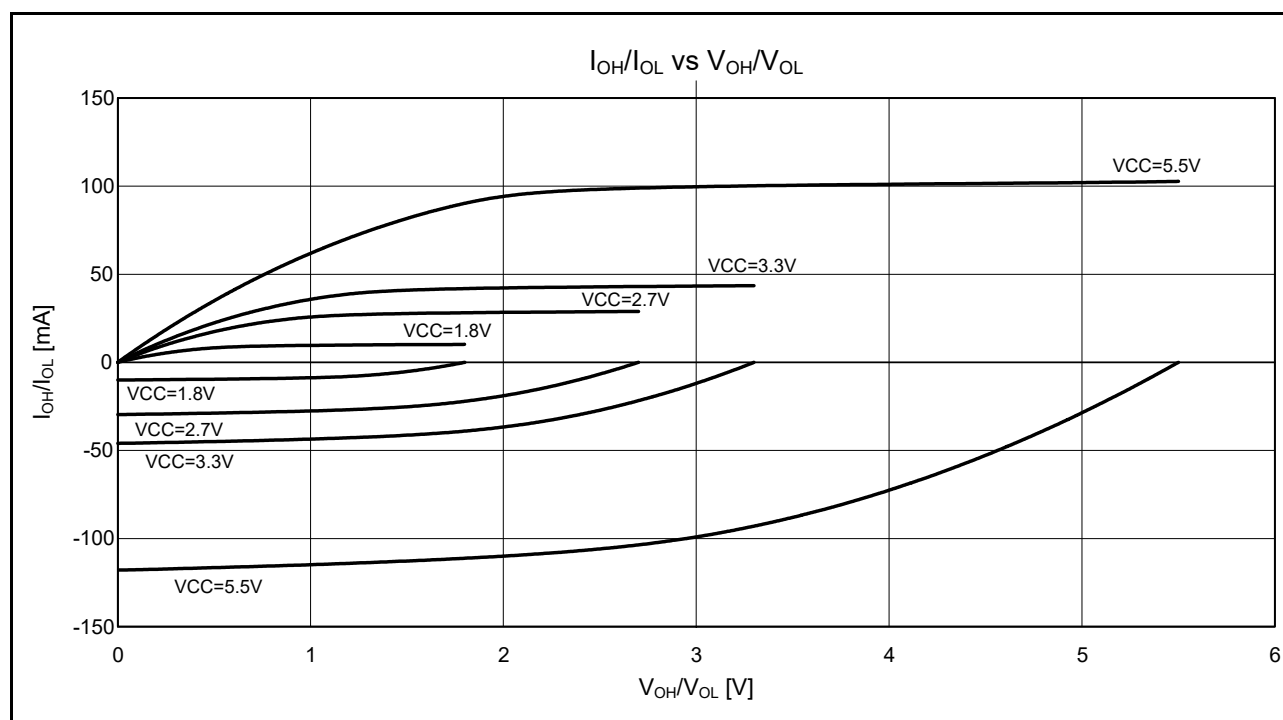


Figure 5.13 V_{OH}/V_{OL} and I_{OH}/I_{OL} Voltage Characteristics at $T_a = 25^\circ\text{C}$ When High-Drive Output is Selected (Reference Data)

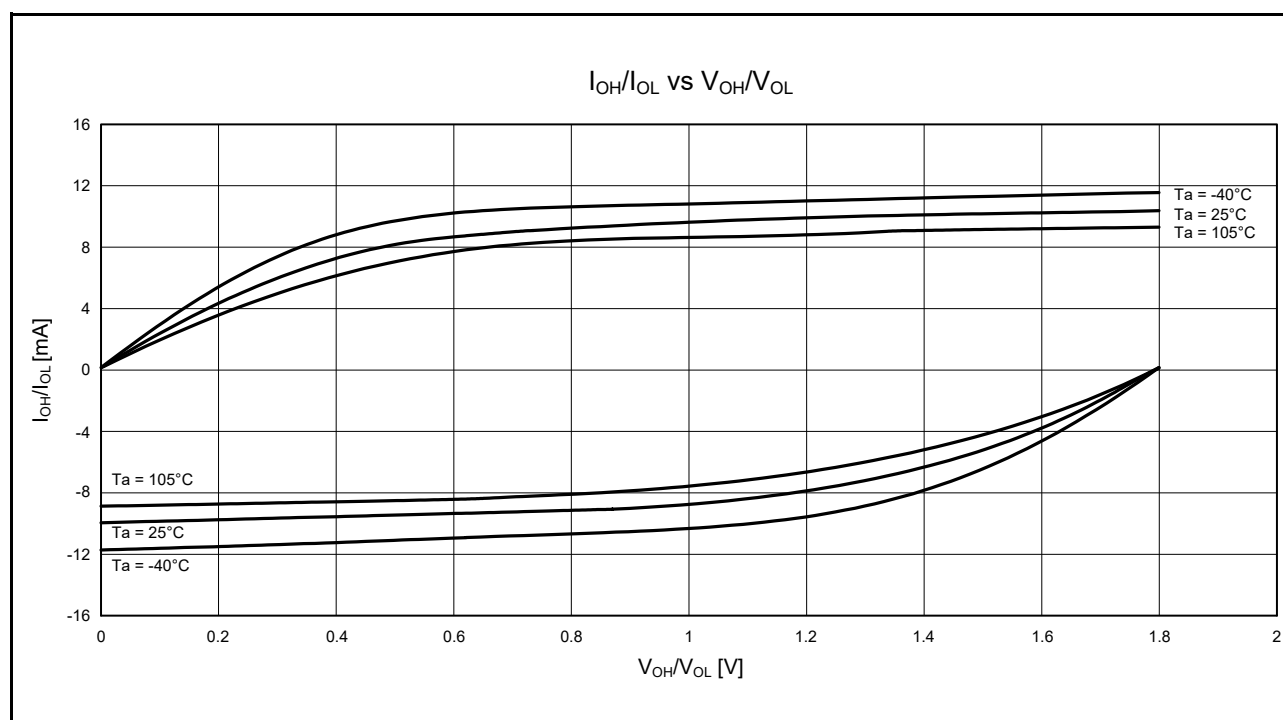


Figure 5.14 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at $V_{CC} = 1.8\text{ V}$ When High-Drive Output is Selected (Reference Data)

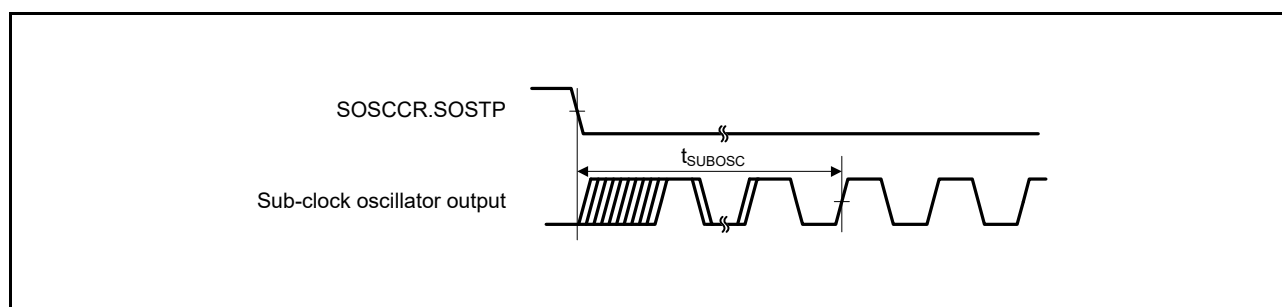


Figure 5.30 Sub-Clock Oscillation Start Timing

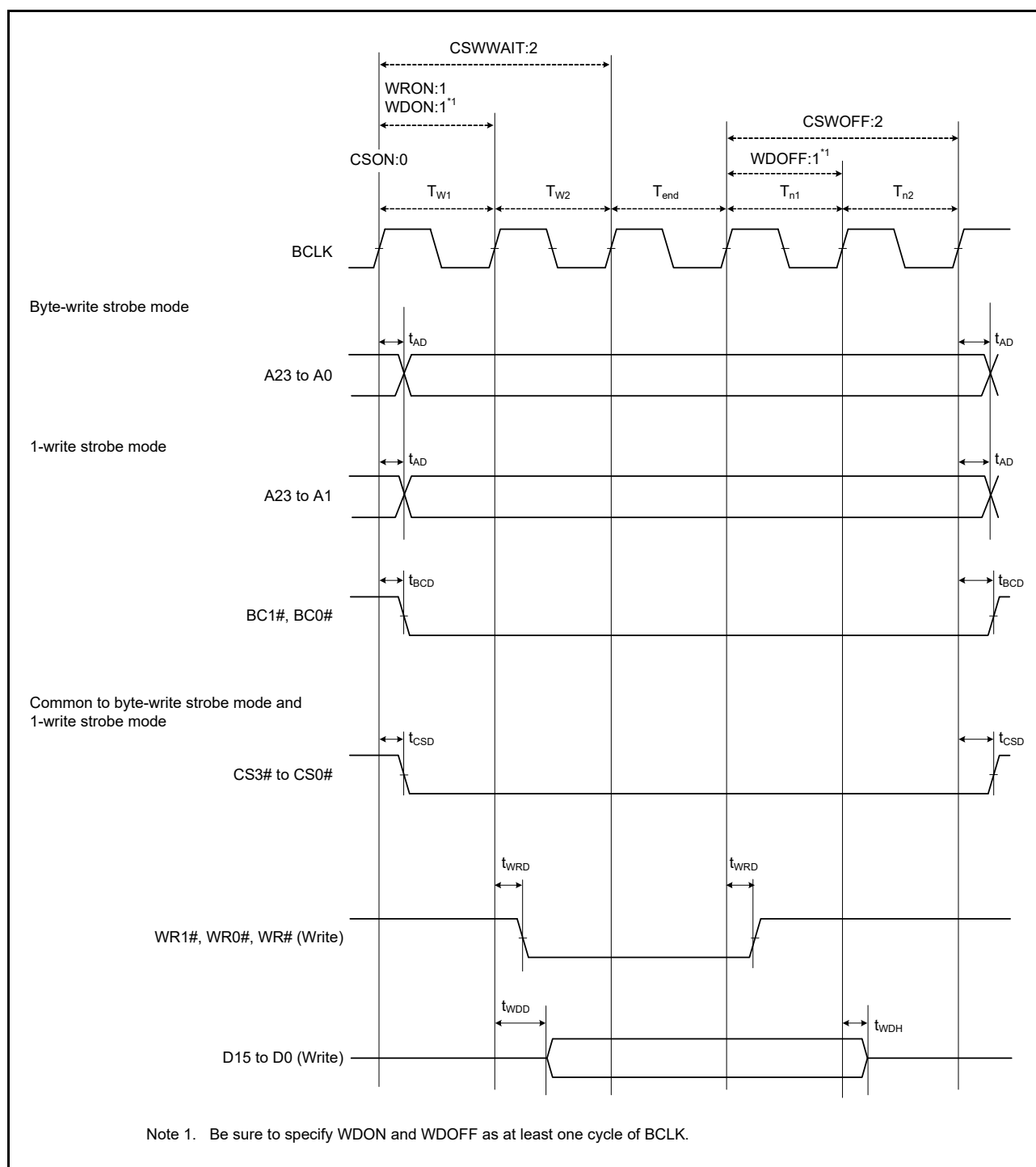


Figure 5.39 External Bus Timing/Normal Write Cycle (Bus Clock Synchronization)

Table 5.40 Timing of On-Chip Peripheral Modules (3)Conditions: $1.8\text{ V} \leq VCC = VCC_USB = AVCC0 \leq 5.5\text{ V}$, $VSS = AVSS0 = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)		t_{SPcyc}	4	65536	t_{Pcyc}	Figure 5.54
	SCK clock cycle input (slave)			6	65536	t_{Pcyc}	
	SCK clock high pulse width		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time		t_{SPCKr} t_{SPCKf}	—	20	ns	
Simple SPI	Data input setup time (master)	2.7 V or above	t_{SU}	65	—	ns	Figure 5.55, Figure 5.56
		1.8 V or above		95	—		
	Data input setup time (slave)			40	—		
	Data input hold time		t_H	40	—	ns	
	SSL input setup time		t_{LEAD}	3	—	t_{SPcyc}	
	SSL input hold time		t_{LAG}	3	—	t_{SPcyc}	
	Data output delay time (master)		t_{OD}	—	40	ns	
	Data output delay time (slave)	2.7 V or above		—	65		
		1.8 V or above		—	100		
	Data output hold time (master)	2.7 V or above	t_{OH}	−10	—	ns	
		1.8 V or above		−20	—		
	Data output hold time (slave)			−10	—		
	Data rise/fall time		t_{Dr} t_{Df}	—	20	ns	
	SSL input rise/fall time		t_{SSLr} t_{SSLf}	—	20	ns	
	Slave access time		t_{SA}	—	6	t_{Pcyc}	Figure 5.57, Figure 5.58
	Slave output release time		t_{REL}	—	6	t_{Pcyc}	

Note 1. t_{Pcyc} : PCLK cycle

Table 5.41 Timing of On-Chip Peripheral Modules (4)

Conditions: $2.7\text{ V} \leq V_{CC} = V_{CC_USB} = AV_{CC0} \leq 5.5\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$, $f_{PCLKB} \leq 32\text{ MHz}$,
 $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Symbol	Min.*1, *2	Max.	Unit	Test Conditions
RIIC (Standard mode, SMBus)	SCL cycle time	t_{SCL}	$6(12) \times t_{IICcyc} + 1300$	—	ns	Figure 5.59
	SCL high pulse width	t_{SCLH}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL low pulse width	t_{SCLL}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL, SDA rise time	t_{Sr}	—	1000	ns	
	SCL, SDA fall time	t_{Sf}	—	300	ns	
	SCL, SDA spike pulse removal time	t_{SP}	0	$1(4) \times t_{IICcyc}$	ns	
	SDA bus free time	t_{BUF}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	START condition hold time	t_{STAH}	$t_{IICcyc} + 300$	—	ns	
	Repeated START condition setup time	t_{STAS}	1000	—	ns	
	STOP condition setup time	t_{STOS}	1000	—	ns	
	Data setup time	t_{SDAS}	$t_{IICcyc} + 50$	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
RIIC (Fast mode)	SCL cycle time	t_{SCL}	$6(12) \times t_{IICcyc} + 600$	—	ns	Figure 5.59
	SCL high pulse width	t_{SCLH}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL low pulse width	t_{SCLL}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL, SDA rise time	t_{Sr}	—	300	ns	
	SCL, SDA fall time	t_{Sf}	—	300	ns	
	SCL, SDA spike pulse removal time	t_{SP}	0	$1(4) \times t_{IICcyc}$	ns	
	SDA bus free time	t_{BUF}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	START condition hold time	t_{STAH}	$t_{IICcyc} + 300$	—	ns	
	Repeated START condition setup time	t_{STAS}	300	—	ns	
	STOP condition setup time	t_{STOS}	300	—	ns	
	Data setup time	t_{SDAS}	$t_{IICcyc} + 50$	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: t_{IICcyc} : RIIC internal reference clock (IICφ) cycle

Note 1. The value in parentheses is used when the ICMR3.NF[1:0] bits are set to 11b while a digital filter is enabled with the ICFER.NFE bit = 1.

Note 2. C_b is the total capacitance of the bus lines.

Differential non-linearity error (DNL)

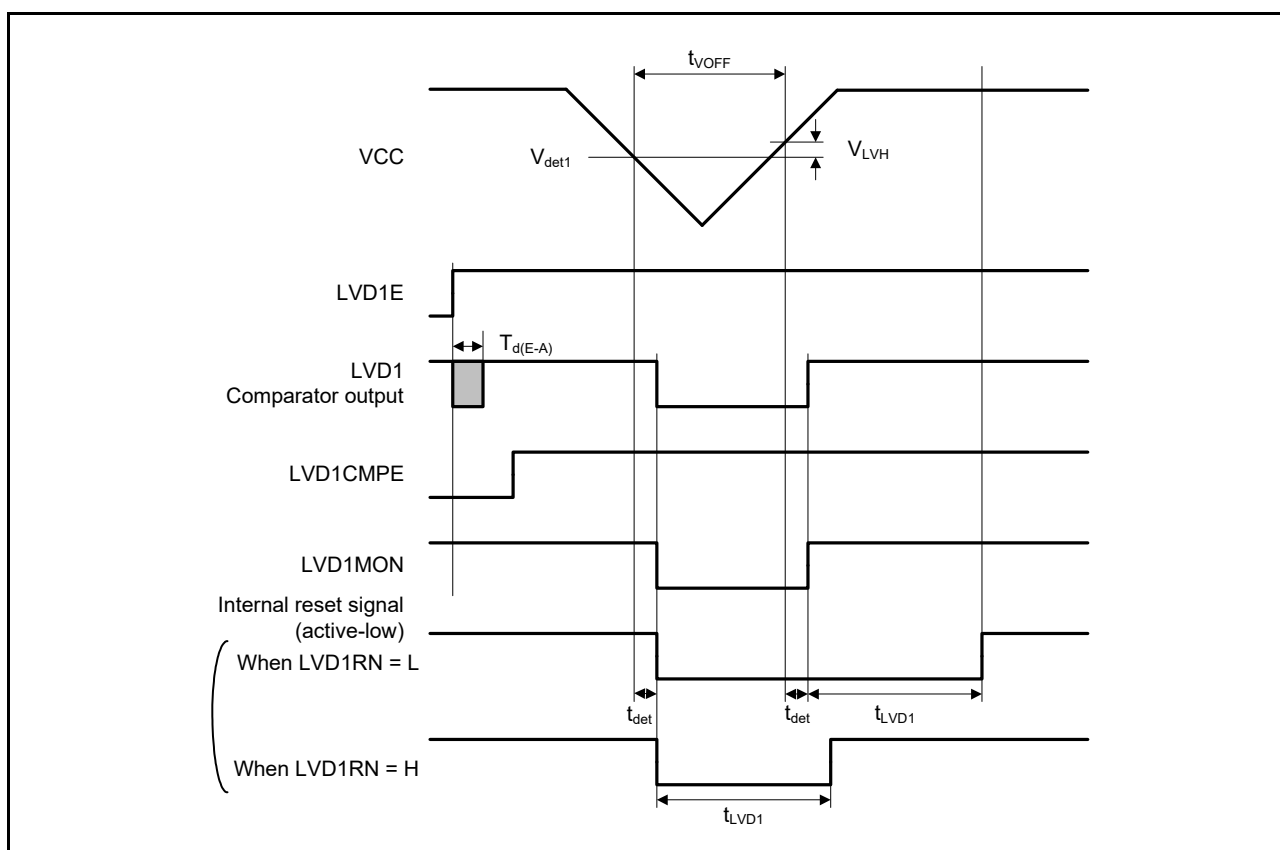
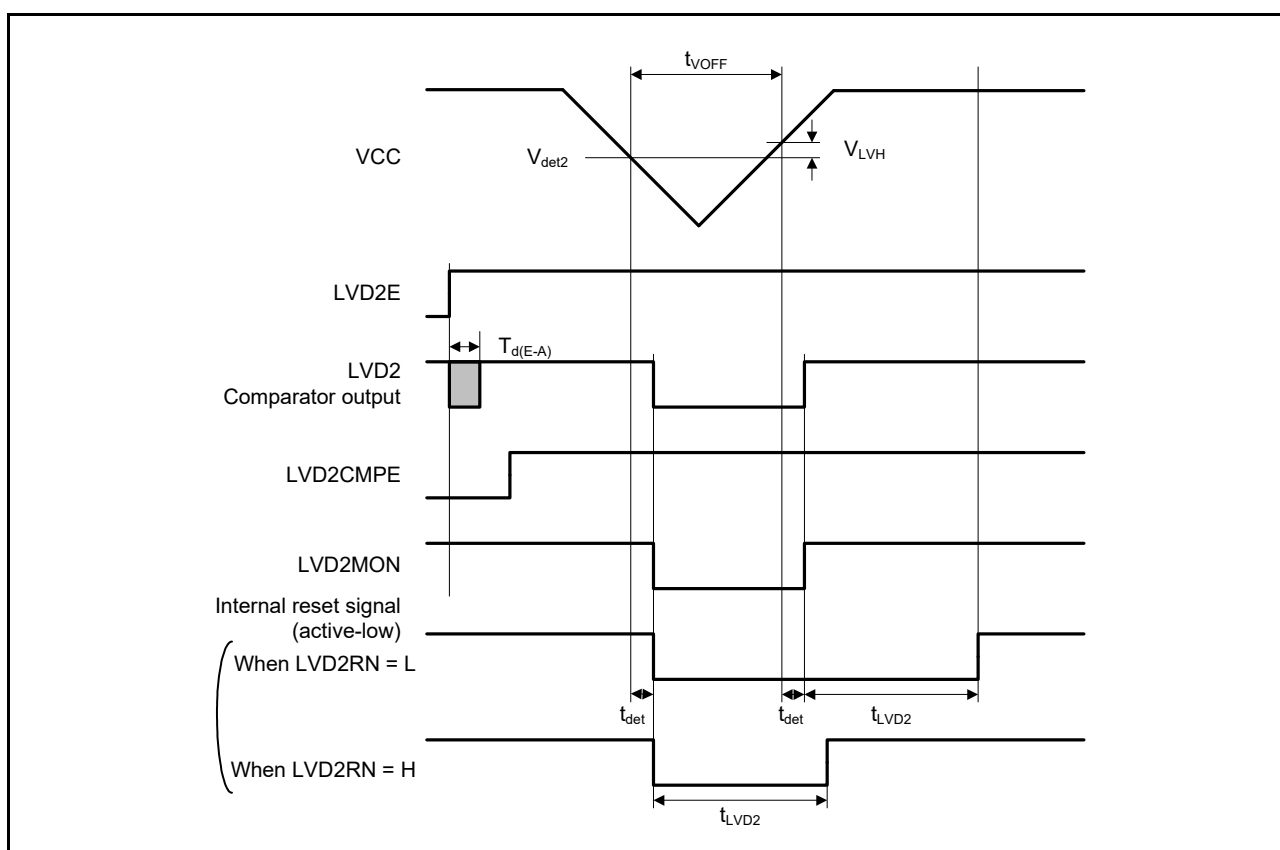
The differential non-linearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

Offset error

An offset error is the difference between a transition point of the ideal first output code and the actual first output code.

Full-scale error

A full-scale error is the difference between a transition point of the ideal last output code and the actual last output code.

Figure 5.76 Voltage Detection Circuit Timing (V_{det1})Figure 5.77 Voltage Detection Circuit Timing (V_{det2})

5.13 ROM (Flash Memory for Code Storage) Characteristics

Table 5.62 ROM (Flash Memory for Code Storage) Characteristics (1)

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Reprogramming/erasure cycle*1	N _{PEC}	1000	—	—	Times	
Data hold time	After 1000 times of N _{PEC} t _{DRP}	20*2, *3	—	—	Year	T _a = +85°C

Note 1. Definition of reprogram/erase cycle: The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 4-byte programming is performed 256 times for different addresses in a 1-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. Characteristic when using the flash memory programmer and the self-programming library provided from Renesas Electronics.

Note 3. This result is obtained from reliability testing.

Table 5.63 ROM (Flash Memory for Code Storage) Characteristics (2) High-Speed Operating Mode

Conditions: 2.7 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VSS_USB = 0 V

Temperature range for the programming/erasure operation: T_a = −40 to +105°C

Item		Symbol	FCLK = 1 MHz			FCLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	8-byte	t _{P8}	—	112	967	—	52.3	491	μs
Erasure time	2-Kbyte	t _{E2K}	—	8.75	278	—	5.50	215	ms
	512-Kbyte (when block erase command is used)	t _{E512K}	—	928	19218	—	72.0	1679	ms
	512-Kbyte (when all-block erase command is used)	t _{EA512K}	—	923	19013	—	66.7	1469	ms
Blank check time	8-byte	t _{BC8}	—	—	55.0	—	—	16.1	μs
	2-Kbyte	t _{BC2K}	—	—	1840	—	—	136	ms
Erasure operation forced stop time		t _{SED}	—	—	18.0	—	—	10.7	μs
Start-up area switching setting time		t _{SAS}	—	12.3	566.5	—	6.2	434	ms
Access window time		t _{AWS}	—	12.3	566.5	—	6.2	434	ms
ROM mode transition wait time 1		t _{DIS}	2.0	—	—	2.0	—	—	μs
ROM mode transition wait time 2		t _{MS}	5.0	—	—	5.0	—	—	μs

Note: The time until each operation of the flash memory is started after instructions are executed by software is not included.

Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: The frequency accuracy of FCLK must be within ±3.5%.