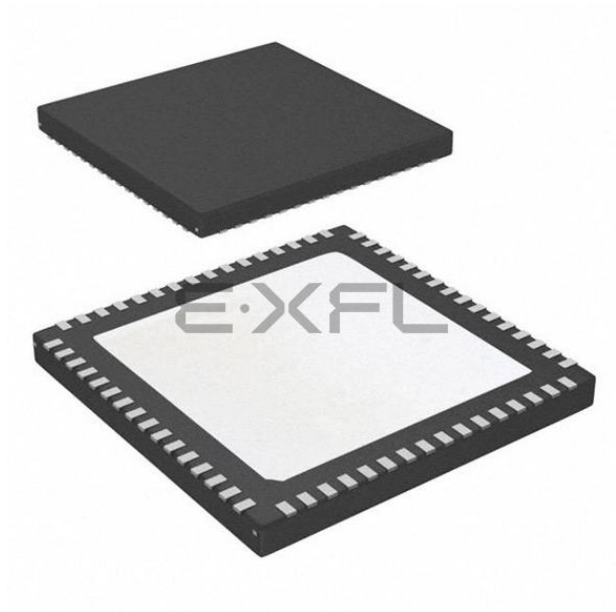
Renesas Electronics America Inc - R5F52316ADND#U0 Datasheet



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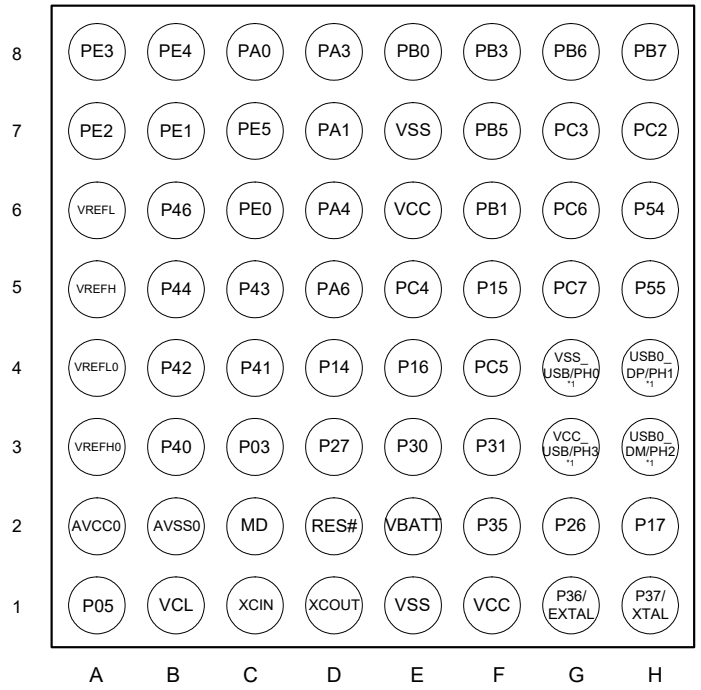
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	54MHz
Connectivity	CANbus, I²C, IrDA, SCI, SD/SDIO, SPI, SSI, USB OTG
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	43
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-WFQFN Exposed Pad
Supplier Device Package	64-HWQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f52316adnd-u0

Table 1.1 Outline of Specifications (4/4)

Classification	Module/Function	Description
Communication functions	Serial Sound Interface (SSI)	• 1 channel • Capable of duplex communications • Various serial audio formats supported • Master/slave function supported • Programmable word clock or bit clock generation function • 8/16/18/20/22/24/32-bit data formats supported • On-chip 8-stage FIFO for transmission/reception • Supports WS continue mode in which the SSIWS signal is not stopped.
	SD Host Interface (SDHIa)	• 1 channel • Transfer speed : Default speed mode (8MB/s) • SD memory card interface (1 bit / 4bits SD bus) • MMC, eMMC Backward-compatible are supported. • SD Specifications Part 1: Compliant with Physical Layer Specification Ver.3.01 (Not support DDR) Part E1: SDIO Specification Ver. 3.00 • Error check function: CRC7 (command), CRC16 (data) • Interrupt Source: Card access interrupt, SDIO access interrupt, Card detection interrupt, SD buffer access interrupt • DMA transfer sources: SD_BUF write, SD_BUF read • Card detection, Write protection
Encryption functions	Trusted Secure IP (TSIP-Lite)	• Access management circuit • Encryption engine 128- or 256-bit key sizes of AES Block cipher mode of operation: GCM, ECB, CBC, CMAC, XTS, CTR, GCTR • Hash function • True random number generator • Prevention from illicit copying of a key
12-bit A/D converter (S12ADE)		• 12 bits (24 channels × 1 unit) • 12-bit resolution • Minimum conversion time: 0.83 µs per channel when the ADCLK is operating at 54 MHz • Operating modes Scan mode (single scan mode, continuous scan mode, and group scan mode) Group A priority control (only for group scan mode) • Sampling variable Sampling time can be set up for each channel. • Self-diagnostic function • Double trigger mode (A/D conversion data duplicated) • Detection of analog input disconnection • A/D conversion start conditions A software trigger, a trigger from a timer (MTU, TPU), an external trigger signal, or ELC • Event linking by the ELC
Temperature sensor (TEMPSA)		• 1 channel • The voltage output from the temperature sensor is converted into a digital value by the 12-bit A/D converter.
12-bit D/A converter (R12DAA)		• 2 channels • 12-bit resolution • Output voltage: 0.4 to AVCC0-0.5V
CRC calculator (CRC)		• CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$ • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable.
Comparator B (CMPBa)		• 2 channels × 2 units • Function to compare the reference voltage and the analog input voltage • Window comparator operation or standard comparator operation is selectable
Capacitive touch sensing unit (CTSU)		Detection pin: 24 channels
Data operation circuit (DOC)		Comparison, addition, and subtraction of 16-bit data
Power supply voltages/Operating frequencies		VCC = 1.8 to 2.4 V: 8 MHz, VCC = 2.4 to 2.7 V: 16 MHz, VCC = 2.7 to 5.5 V: 54 MHz
Operating temperature range		D version: –40 to +85°C, G version: –40 to +105°C
Packages		100-pin TFLGA (PTLG0100KA-A) 5.5 × 5.5 mm, 0.5 mm pitch 100-pin LFQFP (PLQP0100KB-B) 14 × 14 mm, 0.5 mm pitch 64-pin WFLGA (PWLG0064KA-A) 5 × 5 mm, 0.5 mm pitch 64-pin HWQFN (PWQN0064KC-A) 9 × 9 mm, 0.5 mm pitch 64-pin LFQFP (PLQP0064KB-C) 10 × 10 mm, 0.5 mm pitch 48-pin HWQFN (PWQN0048KB-A) 7 × 7 mm, 0.5 mm pitch 48-pin LFQFP (PLQP0048KB-B) 7 × 7 mm, 0.5 mm pitch
Debugging interfaces		FINE interface

RX230 Group, RX231 Group
PWLG0064KA-A
(64-pin WFLGA)
(Upper perspective view)



Note: This figure indicates the power supply pins and I/O port pins.
For the pin configuration, see the table “List of Pins and Pin Functions (64-Pin WFLGA)”.
Note: For the position of A1 pin in the package, see “Package Dimensions”.
Note 1. RX230: PH0, PH1, PH2, PH3
RX231: VSS_USB, USB0_DP, USB0_DM, VCC_USB

Figure 1.5 Pin Assignments of the 64-Pin WFLGA

Table 1.7 List of Pins and Pin Functions (100-Pin LFQFP) (1/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCI, RSPI, RIIC, RSCAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
1	VREFH							
2		P03						DA0
3	VREFL							
4		PJ3		MTIOC3C	CTS6#/RTS6#/SS6#			
5	VCL							
6	VBATT							
7	MD							FINED
8	XCIN							
9	XCOUT							
10	RES#							
11	XTAL	P37						
12	VSS							
13	EXTAL	P36						
14	VCC							
15	UPSEL	P35						NMI
16		P34		MTIOC0A/TMCI3/POE2#	SCK6		TS0	IRQ4
17		P33		MTIOC0D/TMRI3/POE3#/ TIOCD0	RXD6/SMISO6/SSCL6		TS1	IRQ3
18		P32		MTIOC0C/TMO3/TIOCC0/ RTCOUT/RTCIC2	TXD6/SMOSI6/SSDA6/ USB0_VBUSEN			IRQ2
19		P31		MTIOC4D/TMCI2/RTCIC1	CTS1#/RTS1#/SS1#/ SSISCK0			IRQ1
20		P30		MTIOC4B/TMRI3/POE8#/ RTCIC0	RXD1/SMISO1/SSCL1/ AUDIO_MCLK			IRQ0/ CMPOB3
21		P27	CS3#	MTIOC2B/TMCI3	SCK1/ SSIWS0		TS2	CVREFB3
22		P26	CS2#	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1/ SSIRXD0		TS3	CMPB3
23		P25	CS1#	MTIOC4C/MTCLKB/ TIOCA4			TS4	ADTRG0#
24		P24	CS0#	MTIOC4A/MTCLKA/TMRI1/ TIOCB4	USB0_VBUSEN		TS5	
25		P23		MTIOC3D/MTCLKD/ TIOCD3	CTS0#/RTS0#/SS0#/ SSISCK0		TS6	
26		P22		MTIOC3B/MTCLKC/TMO0/ TIOCC3	SCK0/ USB0_OVRCURB/ AUDIO_MCLK		TS7	
27		P21		MTIOC1B/TMCI0/TIOCA3	RXD0/SMISO0/SSCL0/ USB0_EXICEN/SSIWS0		TS8	
28		P20		MTIOC1A/TMRI0/TIOCB3	TXD0/SMOSI0/SSDA0/ USB0_ID/SSIRXD0		TS9	
29		P17		MTIOC3A/MTIOC3B/TMO1/ POE8#/TIOCB0/TCLKD	SCK1/MISOA/SDA/ SSITXD0			IRQ7/ CMPOB2
30		P16		MTIOC3C/MTIOC3D/ TMO2/TIOCB1/TCLKC/ RTCOUT	TXD1/SMOSI1/SSDA1/ MOSIA/SCL/USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB			IRQ6/ ADTRG0#
31		P15		MTIOC0B/MTCLKB/TMCI2/ TIOCB2/TCLKB	RXD1/SMISO1/SSCL1/ CRXD0		TS12	IRQ5/CMPB2
32		P14		MTIOC3A/MTCLKA/TMRI2/ TIOCB5/TCLKA	CTS1#/RTS1#/SS1#/ CTXD0/USB0_OVRCURA		TS13	IRQ4/ CVREFB2
33		P13		MTIOC0B/TMO3/TIOCA5	SDA			IRQ3
34		P12		TMCI1	SCL			IRQ2
35	VCC_USB*1	PH3*1		TMCI0*1				
36		PH2*1		TMRI0*1	USB0_DM*1			IRQ1*1
37		PH1*1		TMO0*1	USB0_DP*1			IRQ0*1
38	VSS_USB*1	PH0*1						CACREF*1
39		P55	WAIT#	MTIOC4D/TMO3	CRXD0		TS15	
40		P54	ALE	MTIOC4B/TMCI1	CTXD0		TS16	
41	BCLK	P53					TS17	

Table 1.8 List of Pins and Pin Functions (64-Pin WFLGA) (1/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCI, RSPI, RIIC, RSCAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
A1		P05					DA1
A2	AVCC0						
A3	VREFH0						
A4	VREFL0						
A5	VREFH						
A6	VREFL						
A7		PE2	MTIOC4A	RXD12/RXDX12/SMISO12/ SSCL12			IRQ7/AN018/ CVREFB0
A8		PE3	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#/ AUDIO_MCLK			AN019/CLKOUT
B1	VCL						
B2	AVSS0						
B3		P40					AN000
B4		P42					AN002
B5		P44					AN004
B6		P46					AN006
B7		PE1	MTIOC4C	TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12			AN017/CMPB0
B8		PE4	MTIOC4D/MTIOC1A				AN020/CMPA2/ CLKOUT
C1	XCIN						
C2	MD						FINED
C3		P03					DA0
C4		P41					AN001
C5		P43					AN003
C6		PE0		SCK12			AN016
C7		PE5	MTIOC4C/MTIOC2B				IRQ5/AN021/ CMPOB0
C8		PA0	MTIOC4A/TIOCA0	SSLA1			CACREF
D1	XCOUT						
D2	RES#						
D3		P27	MTIOC2B/TMCI3	SCK1/ SSIWS0		TS2	CVREFB3
D4		P14	MTIOC3A/MTCLKA/TMRI2/ TIOCB5/TCLKA	CTS1#/RTS1#/SS1#/CTXD0/ USB0_OVRCURA		TS13	IRQ4/CVREFB2
D5		PA6	MTIC5V/MTCLKB/TMCI3/POE2#/ TIOCA2	CTS5#/RTS5#/SS5#/MOSIA/ SSIWS0			
D6		PA4	MTIC5U/MTCLKA/TMRI0/TIOCA1	TXD5/SMOSI5/SSDA5/SSLA0/ SSITXD0/IRTXD5			IRQ5 /CVREFB1
D7		PA1	MTIOC0B/MTCLKC/TIOCB0	SCK5/SSLA2/SSISCK0			
D8		PA3	MTIOC0D/MTCLKD/TIOCD0/ TCLKB	RXD5/SMISO5/SSCL5/SSIRXD0/ IRRXD5			IRQ6 /CMPB1
E1	VSS						
E2	VBATT						
E3		P30	MTIOC4B/TMRI3/POE8#/RTCIC0	RXD1/SMISO1/SSCL1/ AUDIO_MCLK			IRQ0/CMPOB3
E4		P16	MTIOC3C/MTIOC3D/TMO2/ TIOCB1/TCLKC/RTCOUT	TXD1/SMOSI1/SSDA1/MOSIA/ SCL/USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB			IRQ6/ADTRG0#
E5		PC4	MTIOC3D/MTCLKC/TMCI1/ POE0#	SCK5/CTS8#/RTS8#/SS8#/ SSLA0	SDHI_D1	TSCAP	
E6	VCC						
E7	VSS						
E8		PB0	MTIC5W/TIOCA3	RXD6/SMISO6/SSCL6/RSPCKA	SDHI_C MD		
F1	VCC						
F2	UPSEL	P35					NMI
F3		P31	MTIOC4D/TMCI2/RTCIC1	CTS1#/RTS1#/SS1#/SSISCK0			IRQ1

2.1 General-Purpose Registers (R0 to R15)

This CPU has sixteen 32-bit general-purpose registers (R0 to R15). R0 to R15 can be used as data registers or address registers.
R0, a general-purpose register, also functions as the stack pointer (SP).
The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

2.2 Control Registers

(1) Interrupt stack pointer (ISP) and user stack pointer (USP)

The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP). Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).
Set the ISP or USP to a multiple of 4 to reduce the number of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

(2) Exception table register (EXTB)

The exception table register (EXTB) specifies the address where the exception vector table starts.
Set the EXTB to a multiple of 4 to reduce the number of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

(3) Interrupt table register (INTB)

The interrupt table register (INTB) specifies the address where the interrupt vector table starts.
Set the INTB to a multiple of 4 to reduce the number of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

(4) Program counter (PC)

The program counter (PC) indicates the address of the instruction being executed.

(5) Processor status word (PSW)

The processor status word (PSW) indicates the results of instruction execution or the state of the CPU.

(6) Backup PC (BPC)

The backup PC (BPC) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC register.

(7) Backup PSW (BPSW)

The backup PSW (BPSW) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

(8) Fast interrupt vector register (FINTV)

The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.
The FINTV register specifies a branch destination address when a fast interrupt has been generated.

Table 4.1 List of I/O Registers (Address Order) (2/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK <PCLK
0008 1308h	BSC	Bus Error Status Register 1	BERSR1	8	8	2 ICLK	
0008 130Ah	BSC	Bus Error Status Register 2	BERSR2	16	16	2 ICLK	
0008 1310h	BSC	Bus Priority Control Register	BUSPRI	16	16	2 ICLK	
0008 2000h	DMAC0	DMA Source Address Register	DMSAR	32	32	2 ICLK	
0008 2004h	DMAC0	DMA Destination Address Register	DMDAR	32	32	2 ICLK	
0008 2008h	DMAC0	DMA Transfer Count Register	DMCRA	32	32	2 ICLK	
0008 200Ch	DMAC0	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK	
0008 2010h	DMAC0	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK	
0008 2013h	DMAC0	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK	
0008 2014h	DMAC0	DMA Address Mode Register	DMAMD	16	16	2 ICLK	
0008 2018h	DMAC0	DMA Offset Register	DMOFR	32	32	2 ICLK	
0008 201Ch	DMAC0	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK	
0008 201Dh	DMAC0	DMA Software Start Register	DMREQ	8	8	2 ICLK	
0008 201Eh	DMAC0	DMA Status Register	DMSTS	8	8	2 ICLK	
0008 201Fh	DMAC0	DMA Activation Source Flag Control Register	DMCSL	8	8	2 ICLK	
0008 2040h	DMAC1	DMA Source Address Register	DMSAR	32	32	2 ICLK	
0008 2044h	DMAC1	DMA Destination Address Register	DMDAR	32	32	2 ICLK	
0008 2048h	DMAC1	DMA Transfer Count Register	DMCRA	32	32	2 ICLK	
0008 204Ch	DMAC1	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK	
0008 2050h	DMAC1	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK	
0008 2053h	DMAC1	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK	
0008 2054h	DMAC1	DMA Address Mode Register	DMAMD	16	16	2 ICLK	
0008 205Ch	DMAC1	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK	
0008 205Dh	DMAC1	DMA Software Start Register	DMREQ	8	8	2 ICLK	
0008 205Eh	DMAC1	DMA Status Register	DMSTS	8	8	2 ICLK	
0008 205Fh	DMAC1	DMA Activation Source Flag Control Register	DMCSL	8	8	2 ICLK	
0008 2080h	DMAC2	DMA Source Address Register	DMSAR	32	32	2 ICLK	
0008 2084h	DMAC2	DMA Destination Address Register	DMDAR	32	32	2 ICLK	
0008 2088h	DMAC2	DMA Transfer Count Register	DMCRA	32	32	2 ICLK	
0008 208Ch	DMAC2	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK	
0008 2090h	DMAC2	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK	
0008 2093h	DMAC2	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK	
0008 2094h	DMAC2	DMA Address Mode Register	DMAMD	16	16	2 ICLK	
0008 209Ch	DMAC2	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK	
0008 209Dh	DMAC2	DMA Software Start Register	DMREQ	8	8	2 ICLK	
0008 209Eh	DMAC2	DMA Status Register	DMSTS	8	8	2 ICLK	
0008 209Fh	DMAC2	DMA Activation Source Flag Control Register	DMCSL	8	8	2 ICLK	
0008 20C0h	DMAC3	DMA Source Address Register	DMSAR	32	32	2 ICLK	
0008 20C4h	DMAC3	DMA Destination Address Register	DMDAR	32	32	2 ICLK	
0008 20C8h	DMAC3	DMA Transfer Count Register	DMCRA	32	32	2 ICLK	
0008 20CCh	DMAC3	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK	
0008 20D0h	DMAC3	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK	
0008 20D3h	DMAC3	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK	
0008 20D4h	DMAC3	DMA Address Mode Register	DMAMD	16	16	2 ICLK	
0008 20DCh	DMAC3	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK	
0008 20DDh	DMAC3	DMA Software Start Register	DMREQ	8	8	2 ICLK	
0008 20DEh	DMAC3	DMA Status Register	DMSTS	8	8	2 ICLK	
0008 20DFh	DMAC3	DMA Activation Source Flag Control Register	DMCSL	8	8	2 ICLK	
0008 2200h	DMAC	DMA Module Activation Register	DMAST	8	8	2 ICLK	
0008 2400h	DTC	DTC Control Register	DTCCR	8	8	2 ICLK	
0008 2404h	DTC	DTC Vector Base Register	DTCVBR	32	32	2 ICLK	
0008 2408h	DTC	DTC Address Mode Register	DTCADMOD	8	8	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (3/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK <PCLK
0008 240Ch	DTC	DTC Module Start Register	DTCST	8	8	2 ICLK	
0008 240Eh	DTC	DTC Status Register	DTCSTS	16	16	2 ICLK	
0008 3002h	BSC	CS0 Mode Register	CS0MOD	16	16	1 or 2 BCLK	
0008 3004h	BSC	CS0 Wait Control Register 1	CS0WCR1	32	32	1 or 2 BCLK	
0008 3008h	BSC	CS0 Wait Control Register 2	CS0WCR2	32	32	1 or 2 BCLK	
0008 3012h	BSC	CS1 Mode Register	CS1MOD	16	16	1 or 2 BCLK	
0008 3014h	BSC	CS1 Wait Control Register 1	CS1WCR1	32	32	1 or 2 BCLK	
0008 3018h	BSC	CS1 Wait Control Register 2	CS1WCR2	32	32	1 or 2 BCLK	
0008 3022h	BSC	CS2 Mode Register	CS2MOD	16	16	1 or 2 BCLK	
0008 3024h	BSC	CS2 Wait Control Register 1	CS2WCR1	32	32	1 or 2 BCLK	
0008 3028h	BSC	CS2 Wait Control Register 2	CS2WCR2	32	32	1 or 2 BCLK	
0008 3032h	BSC	CS3 Mode Register	CS3MOD	16	16	1 or 2 BCLK	
0008 3034h	BSC	CS3 Wait Control Register 1	CS3WCR1	32	32	1 or 2 BCLK	
0008 3038h	BSC	CS3 Wait Control Register 2	CS3WCR2	32	32	1 or 2 BCLK	
0008 3802h	BSC	CS0 Control Register	CS0CR	16	16	1 or 2 BCLK	
0008 380Ah	BSC	CS0 Recovery Cycle Register	CS0REC	16	16	1 or 2 BCLK	
0008 3812h	BSC	CS1 Control Register	CS1CR	16	16	1 or 2 BCLK	
0008 381Ah	BSC	CS1 Recovery Cycle Register	CS1REC	16	16	1 or 2 BCLK	
0008 3822h	BSC	CS2 Control Register	CS2CR	16	16	1 or 2 BCLK	
0008 382Ah	BSC	CS2 Recovery Cycle Register	CS2REC	16	16	1 or 2 BCLK	
0008 3832h	BSC	CS3 Control Register	CS3CR	16	16	1 or 2 BCLK	
0008 383Ah	BSC	CS3 Recovery Cycle Register	CS3REC	16	16	1 or 2 BCLK	
0008 3880h	BSC	CS Recovery Cycle Insertion Enable Register	CSRECEN	16	16	1 or 2 BCLK	
0008 6400h	MPU	Region-0 Start Page Number Register	RSPAGE0	32	32	1 ICLK	
0008 6404h	MPU	Region-0 End Page Number Register	REPAGE0	32	32	1 ICLK	
0008 6408h	MPU	Region-1 Start Page Number Register	RSPAGE1	32	32	1 ICLK	
0008 640Ch	MPU	Region-1 End Page Number Register	REPAGE1	32	32	1 ICLK	
0008 6410h	MPU	Region-2 Start Page Number Register	RSPAGE2	32	32	1 ICLK	
0008 6414h	MPU	Region-2 End Page Number Register	REPAGE2	32	32	1 ICLK	
0008 6418h	MPU	Region-3 Start Page Number Register	RSPAGE3	32	32	1 ICLK	
0008 641Ch	MPU	Region-3 End Page Number Register	REPAGE3	32	32	1 ICLK	
0008 6420h	MPU	Region-4 Start Page Number Register	RSPAGE4	32	32	1 ICLK	
0008 6424h	MPU	Region-4 End Page Number Register	REPAGE4	32	32	1 ICLK	
0008 6428h	MPU	Region-5 Start Page Number Register	RSPAGE5	32	32	1 ICLK	
0008 642Ch	MPU	Region-5 End Page Number Register	REPAGE5	32	32	1 ICLK	
0008 6430h	MPU	Region-6 Start Page Number Register	RSPAGE6	32	32	1 ICLK	
0008 6434h	MPU	Region-6 End Page Number Register	REPAGE6	32	32	1 ICLK	
0008 6438h	MPU	Region-7 Start Page Number Register	RSPAGE7	32	32	1 ICLK	
0008 643Ch	MPU	Region-7 End Page Number Register	REPAGE7	32	32	1 ICLK	
0008 6500h	MPU	Memory-Protection Enable Register	MPEN	32	32	1 ICLK	
0008 6504h	MPU	Background Access Control Register	MPBAC	32	32	1 ICLK	
0008 6508h	MPU	Memory-Protection Error Status-Clearing Register	MPECLR	32	32	1 ICLK	
0008 650Ch	MPU	Memory-Protection Error Status Register	MPESTS	32	32	1 ICLK	
0008 6514h	MPU	Data Memory-Protection Error Address Register	MPDEA	32	32	1 ICLK	
0008 6520h	MPU	Region Search Address Register	MPSA	32	32	1 ICLK	
0008 6524h	MPU	Region Search Operation Register	MPOPS	16	16	1 ICLK	
0008 6526h	MPU	Region Invalidation Operation Register	MPOPI	16	16	1 ICLK	
0008 6528h	MPU	Instruction-Hit Region Register	MHITI	32	32	1 ICLK	
0008 652Ch	MPU	Data-Hit Region Register	MHITD	32	32	1 ICLK	
0008 7010h to 0008 70FFh	ICU	Interrupt Request Register 016 to Interrupt Request Register 255	IR016 to IR255	8	8	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (11/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK <PCLK
0008 A0C9h	SCI6	I²C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB	2 ICLK
0008 A0CAh	SCI6	I²C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB	2 ICLK
0008 A0CBh	SCI6	I²C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB	2 ICLK
0008 A0CCh	SCI6	I²C Status Register	SISR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0CDh	SCI6	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0CEh	SCI6	Transmit Data Register HL	TDRHL	16	16	4 or 5 PCLKB	2 ICLK
0008 A0CEh	SCI6	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB	2 ICLK
0008 A0CFh	SCI6	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB	2 ICLK
0008 A0D0h	SCI6	Receive Data Register HL	RDRHL	16	16	4 or 5 PCLKB	2 ICLK
0008 A0D0h	SCI6	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB	2 ICLK
0008 A0D1h	SCI6	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB	2 ICLK
0008 A0D2h	SCI6	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A100h	SCI8	Serial Mode Register	SMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A101h	SCI8	Bit Rate Register	BRR	8	8	2 or 3 PCLKB	2 ICLK
0008 A102h	SCI8	Serial Control Register	SCR	8	8	2 or 3 PCLKB	2 ICLK
0008 A103h	SCI8	Transmit Data Register	TDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A104h	SCI8	Serial Status Register	SSR	8	8	2 or 3 PCLKB	2 ICLK
0008 A105h	SCI8	Receive Data Register	RDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A106h	SCI8	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A107h	SCI8	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A108h	SCI8	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB	2 ICLK
0008 A109h	SCI8	I²C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB	2 ICLK
0008 A10Ah	SCI8	I²C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB	2 ICLK
0008 A10Bh	SCI8	I²C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB	2 ICLK
0008 A10Ch	SCI8	I²C Status Register	SISR	8	8	2 or 3 PCLKB	2 ICLK
0008 A10Dh	SCI8	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A10Eh	SCI8	Transmit Data Register HL	TDRHL	16	16	4 or 5 PCLKB	2 ICLK
0008 A10Eh	SCI8	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB	2 ICLK
0008 A10Fh	SCI8	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB	2 ICLK
0008 A110h	SCI8	Receive Data Register HL	RDRHL	16	16	4 or 5 PCLKB	2 ICLK
0008 A110h	SCI8	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB	2 ICLK
0008 A111h	SCI8	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB	2 ICLK
0008 A112h	SCI8	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A120h	SCI9	Serial Mode Register	SMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A121h	SCI9	Bit Rate Register	BRR	8	8	2 or 3 PCLKB	2 ICLK
0008 A122h	SCI9	Serial Control Register	SCR	8	8	2 or 3 PCLKB	2 ICLK
0008 A123h	SCI9	Transmit Data Register	TDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A124h	SCI9	Serial Status Register	SSR	8	8	2 or 3 PCLKB	2 ICLK
0008 A125h	SCI9	Receive Data Register	RDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A126h	SCI9	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A127h	SCI9	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A128h	SCI9	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB	2 ICLK
0008 A129h	SCI9	I²C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB	2 ICLK
0008 A12Ah	SCI9	I²C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB	2 ICLK
0008 A12Bh	SCI9	I²C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB	2 ICLK
0008 A12Ch	SCI9	I²C Status Register	SISR	8	8	2 or 3 PCLKB	2 ICLK
0008 A12Dh	SCI9	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A12Eh	SCI9	Transmit Data Register HL	TDRHL	16	16	4 or 5 PCLKB	2 ICLK
0008 A12Eh	SCI9	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB	2 ICLK
0008 A12Fh	SCI9	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB	2 ICLK
0008 A130h	SCI9	Receive Data Register HL	RDRHL	16	16	4 or 5 PCLKB	2 ICLK
0008 A130h	SCI9	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (20/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK <PCLK
0008 C42Eh	RTC	Time Error Adjustment Register	RADJ	8	8	2 or 3 PCLKB	2 ICLK
0008 C440h	RTC	Time Capture Control Register 0	RTCCR0	8	8	2 or 3 PCLKB	2 ICLK
0008 C442h	RTC	Time Capture Control Register 1	RTCCR1	8	8	2 or 3 PCLKB	2 ICLK
0008 C444h	RTC	Time Capture Control Register 2	RTCCR2	8	8	2 or 3 PCLKB	2 ICLK
0008 C452h	RTC	Second Capture Register 0	RSECCP0	8	8	2 or 3 PCLKB	2 ICLK
0008 C452h	RTC	BCNT0 Capture Register 0	BCNT0CP0	8	8	2 or 3 PCLKB	2 ICLK
0008 C454h	RTC	Minute Capture Register 0	RMINCP0	8	8	2 or 3 PCLKB	2 ICLK
0008 C454h	RTC	BCNT1 Capture Register 0	BCNT1CP0	8	8	2 or 3 PCLKB	2 ICLK
0008 C456h	RTC	Hour Capture Register 0	RHRCP0	8	8	2 or 3 PCLKB	2 ICLK
0008 C456h	RTC	BCNT2 Capture Register 0	BCNT2CP0	8	8	2 or 3 PCLKB	2 ICLK
0008 C45Ah	RTC	Date Capture Register 0	RDAYCP0	8	8	2 or 3 PCLKB	2 ICLK
0008 C45Ah	RTC	BCNT3 Capture Register 0	BCNT3CP0	8	8	2 or 3 PCLKB	2 ICLK
0008 C45Ch	RTC	Month Capture Register 0	RMONCP0	8	8	2 or 3 PCLKB	2 ICLK
0008 C462h	RTC	Second Capture Register 1	RSECCP1	8	8	2 or 3 PCLKB	2 ICLK
0008 C462h	RTC	BCNT0 Capture Register 1	BCNT0CP1	8	8	2 or 3 PCLKB	2 ICLK
0008 C464h	RTC	Minute Capture Register 1	RMINCP1	8	8	2 or 3 PCLKB	2 ICLK
0008 C464h	RTC	BCNT1 Capture Register 1	BCNT1CP1	8	8	2 or 3 PCLKB	2 ICLK
0008 C466h	RTC	Hour Capture Register 1	RHRCP1	8	8	2 or 3 PCLKB	2 ICLK
0008 C466h	RTC	BCNT2 Capture Register 1	BCNT2CP1	8	8	2 or 3 PCLKB	2 ICLK
0008 C46Ah	RTC	Date Capture Register 1	RDAYCP1	8	8	2 or 3 PCLKB	2 ICLK
0008 C46Ah	RTC	BCNT3 Capture Register 1	BCNT3CP1	8	8	2 or 3 PCLKB	2 ICLK
0008 C46Ch	RTC	Month Capture Register 1	RMONCP1	8	8	2 or 3 PCLKB	2 ICLK
0008 C472h	RTC	Second Capture Register 2	RSECCP2	8	8	2 or 3 PCLKB	2 ICLK
0008 C472h	RTC	BCNT0 Capture Register 2	BCNT0CP2	8	8	2 or 3 PCLKB	2 ICLK
0008 C474h	RTC	Minute Capture Register 2	RMINCP2	8	8	2 or 3 PCLKB	2 ICLK
0008 C474h	RTC	BCNT1 Capture Register 2	BCNT1CP2	8	8	2 or 3 PCLKB	2 ICLK
0008 C476h	RTC	Hour Capture Register 2	RHRCP2	8	8	2 or 3 PCLKB	2 ICLK
0008 C476h	RTC	BCNT2 Capture Register 2	BCNT2CP2	8	8	2 or 3 PCLKB	2 ICLK
0008 C47Ah	RTC	Date Capture Register 2	RDAYCP2	8	8	2 or 3 PCLKB	2 ICLK
0008 C47Ah	RTC	BCNT3 Capture Register 2	BCNT3CP2	8	8	2 or 3 PCLKB	2 ICLK
0008 C47Ch	RTC	Month Capture Register 2	RMONCP2	8	8	2 or 3 PCLKB	2 ICLK
0008 C580h	CMPB	Comparator B Control Register 1	CPBCNT1	8	8	2 or 3 PCLKB	2 ICLK
0008 C581h	CMPB	Comparator B Control Register 2	CPBCNT2	8	8	2 or 3 PCLKB	2 ICLK
0008 C582h	CMPB	Comparator B Flag Register	CPBFLG	8	8	2 or 3 PCLKB	2 ICLK
0008 C583h	CMPB	Comparator B Interrupt Control Register	CPBINT	8	8	2 or 3 PCLKB	2 ICLK
0008 C584h	CMPB	Comparator B Filter Select Register	CPBF	8	8	2 or 3 PCLKB	2 ICLK
0008 C585h	CMPB	Comparator B Mode Select Register	CPBMD	8	8	2 or 3 PCLKB	2 ICLK
0008 C586h	CMPB	Comparator B Reference Input Voltage Select Register	CPBREF	8	8	2 or 3 PCLKB	2 ICLK
0008 C587h	CMPB	Comparator B Output Control Register	CPBOCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C5A0h	CMPB	Comparator B1 Control Register 1	CPB1CNT1	8	8	2 or 3 PCLKB	2 ICLK
0008 C5A1h	CMPB	Comparator B1 Control Register 2	CPB1CNT2	8	8	2 or 3 PCLKB	2 ICLK
0008 C5A2h	CMPB	Comparator B1 Flag Register	CPB1FLG	8	8	2 or 3 PCLKB	2 ICLK
0008 C5A3h	CMPB	Comparator B1 Interrupt Control Register	CPB1INT	8	8	2 or 3 PCLKB	2 ICLK
0008 C5A4h	CMPB	Comparator B1 Filter Select Register	CPB1F	8	8	2 or 3 PCLKB	2 ICLK
0008 C5A5h	CMPB	Comparator B1 Mode Select Register	CPB1MD	8	8	2 or 3 PCLKB	2 ICLK
0008 C5A6h	CMPB	Comparator B1 Reference Input Voltage Select Register	CPB1REF	8	8	2 or 3 PCLKB	2 ICLK
0008 C5A7h	CMPB	Comparator B1 Output Control Register	CPB1OCR	8	8	2 or 3 PCLKB	2 ICLK
000A 0000h	USB0	System Configuration Control Register	SYSCFG	16	16	3, 4 PCLKB	2 ICLK
000A 0004h	USB0	System Configuration Status Register 0	SYSSTS0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9 × (frequency ratio of ICLK/PCLKB)*2

Table 4.1 List of I/O Registers (Address Order) (22/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK <PCLK
000A 0060h	USB0	DCP Control Register	DCPCTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 0064h	USB0	Pipe Window Select Register	PIPESEL	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 0068h	USB0	Pipe Configuration Register	PIPECFG	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 006Ch	USB0	Pipe Maximum Packet Size Register	PIPEMAXP	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 006Eh	USB0	Pipe Cycle Control Register	PIPEPERI	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 0070h	USB0	PIPE1 Control Register	PIPE1CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 0072h	USB0	PIPE2 Control Register	PIPE2CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 0074h	USB0	PIPE3 Control Register	PIPE3CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 0076h	USB0	PIPE4 Control Register	PIPE4CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 0078h	USB0	PIPE5 Control Register	PIPE5CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 007Ah	USB0	PIPE6 Control Register	PIPE6CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 007Ch	USB0	PIPE7 Control Register	PIPE7CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 007Eh	USB0	PIPE8 Control Register	PIPE8CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 0080h	USB0	PIPE9 Control Register	PIPE9CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 0090h	USB0	PIPE1 Transaction Counter Enable Register	PIPE1TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 0092h	USB0	PIPE1 Transaction Counter Register	PIPE1TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 0094h	USB0	PIPE2 Transaction Counter Enable Register	PIPE2TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 0096h	USB0	PIPE2 Transaction Counter Register	PIPE2TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 0098h	USB0	PIPE3 Transaction Counter Enable Register	PIPE3TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 009Ah	USB0	PIPE3 Transaction Counter Register	PIPE3TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 009Ch	USB0	PIPE4 Transaction Counter Enable Register	PIPE4TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 009Eh	USB0	PIPE4 Transaction Counter Register	PIPE4TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 00A0h	USB0	PIPE5 Transaction Counter Enable Register	PIPE5TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 00A2h	USB0	PIPE5 Transaction Counter Register	PIPE5TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2

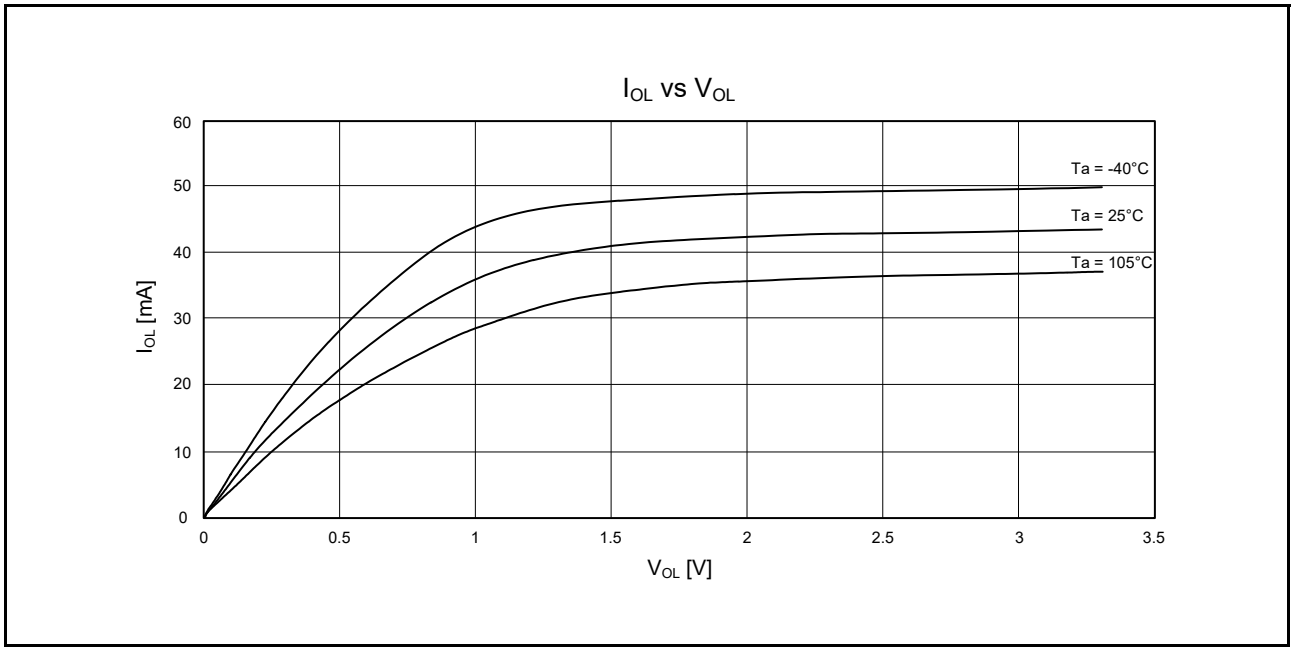


Figure 5.20 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at VCC = 3.3 V (Reference Data)

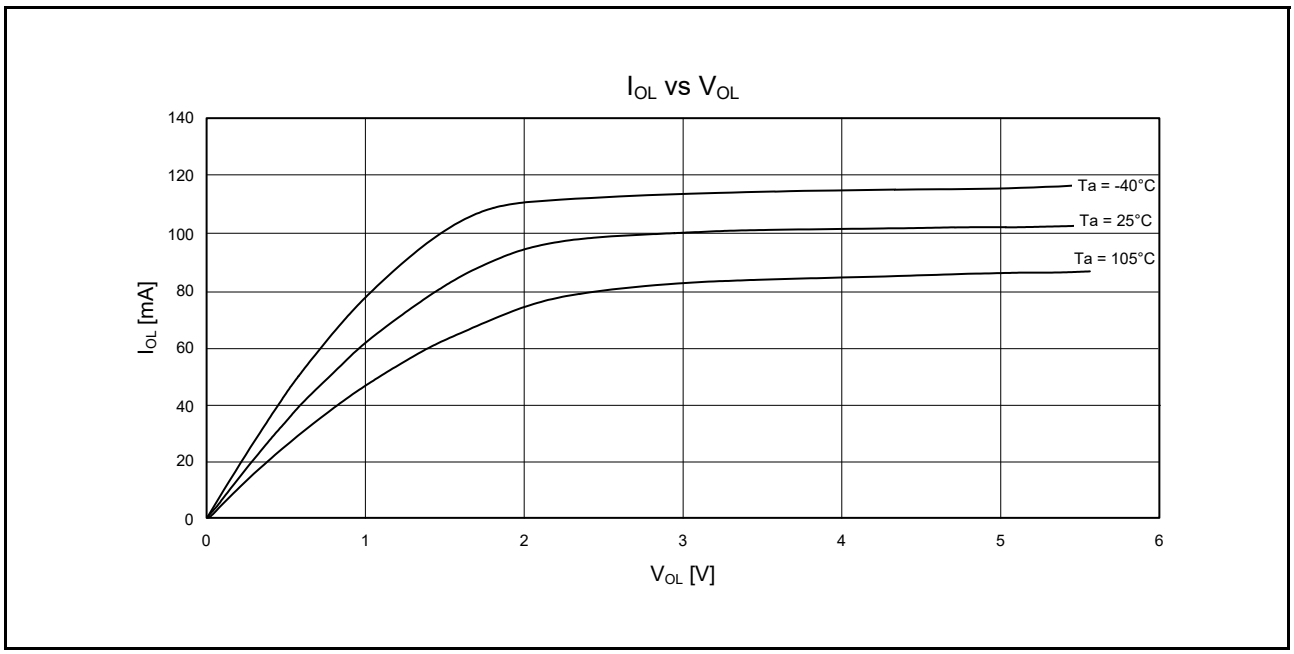


Figure 5.21 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at VCC = 5.5 V (Reference Data)

Table 5.26 Clock Timing

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VREFL0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
EXTAL external clock input cycle time		t_{Xcyc}	50	—	—	ns	Figure 5.23
EXTAL external clock input high pulse width		t_{XH}	20	—	—	ns	
EXTAL external clock input low pulse width		t_{XL}	20	—	—	ns	
EXTAL external clock rise time		t_{Xr}	—	—	5	ns	
EXTAL external clock fall time		t_{Xf}	—	—	5	ns	
EXTAL external clock input wait time*1		t_{XWT}	0.5	—	—	μs	
Main clock oscillator oscillation frequency*2	2.4 ≤ VCC ≤ 5.5	f_{MAIN}	1	—	20	MHz	
	1.8 ≤ VCC < 2.4		1	—	8		
Main clock oscillation stabilization time (crystal)*2		$t_{MAINOSC}$	—	3	—	ms	Figure 5.24
Main clock oscillation stabilization time (ceramic resonator)*2		$t_{MAINOSC}$	—	50	—	μs	
LOCO clock oscillation frequency		f_{LOCO}	3.44	4.0	4.56	MHz	
LOCO clock oscillation stabilization time		t_{LOCO}	—	—	0.5	μs	Figure 5.25
IWDT-dedicated clock oscillation frequency		f_{ILOCO}	12.75	15	17.25	kHz	
IWDT-dedicated clock oscillation stabilization time		t_{ILOCO}	—	—	50	μs	Figure 5.26
HOCO clock oscillation frequency		f_{HOCO} (32 MHz)	31.52	32	32.48	MHz	T_a = –40 to + 85°C
			31.68	32	32.32		T_a = 0 to + 55°C
			31.36	32	32.64		T_a = –40 to +105°C
		f_{HOCO} (54 MHz)	53.19	54	54.81	MHz	T_a = –40 to + 85°C
			53.46	54	54.54		T_a = 0 to + 55°C
			52.92	54	55.08		T_a = –40 to +105°C
HOCO clock oscillation stabilization time		t_{HOCO}	—	—	30	μs	Figure 5.28
PLL input frequency*3		f_{PLLIN}	4	—	12.5	MHz	
PLL circuit oscillation frequency*3		f_{PLL}	24	—	54	MHz	
PLL clock oscillation stabilization time		t_{PLL}	—	—	50	μs	Figure 5.29
PLL free-running oscillation frequency		f_{PLLFR}	—	8	—	MHz	
USBPLL input frequency*5		f_{PLLIN}	—	6, 8*6	—	MHz	
USBPLL circuit oscillation frequency*5		f_{PLL}	—	48*6	—	MHz	
USBPLL clock oscillation stabilization time		t_{PLL}	—	—	50	μs	Figure 5.29
Sub-clock oscillator oscillation frequency*7		f_{SUB}	—	32.768	—	kHz	
Sub-clock oscillation stabilization time*4		t_{SUBOSC}	—	0.5	—	s	Figure 5.30

Note 1. Time until the clock can be used after the main clock oscillator stop bit (MOSCCR.MOSTP) is set to 0 (operating).

Note 2. Reference values when an 8-MHz resonator is used.
When specifying the main clock oscillator stabilization time, set the MOSCWTCR register with a stabilization time value that is equal to or greater than the resonator-manufacturer-recommended value.
After the MOSCCR.MOSTP bit is changed to enable the main clock oscillator, confirm that the OSCOVFSR.MOOVF flag has become 1, and then start using the main clock.

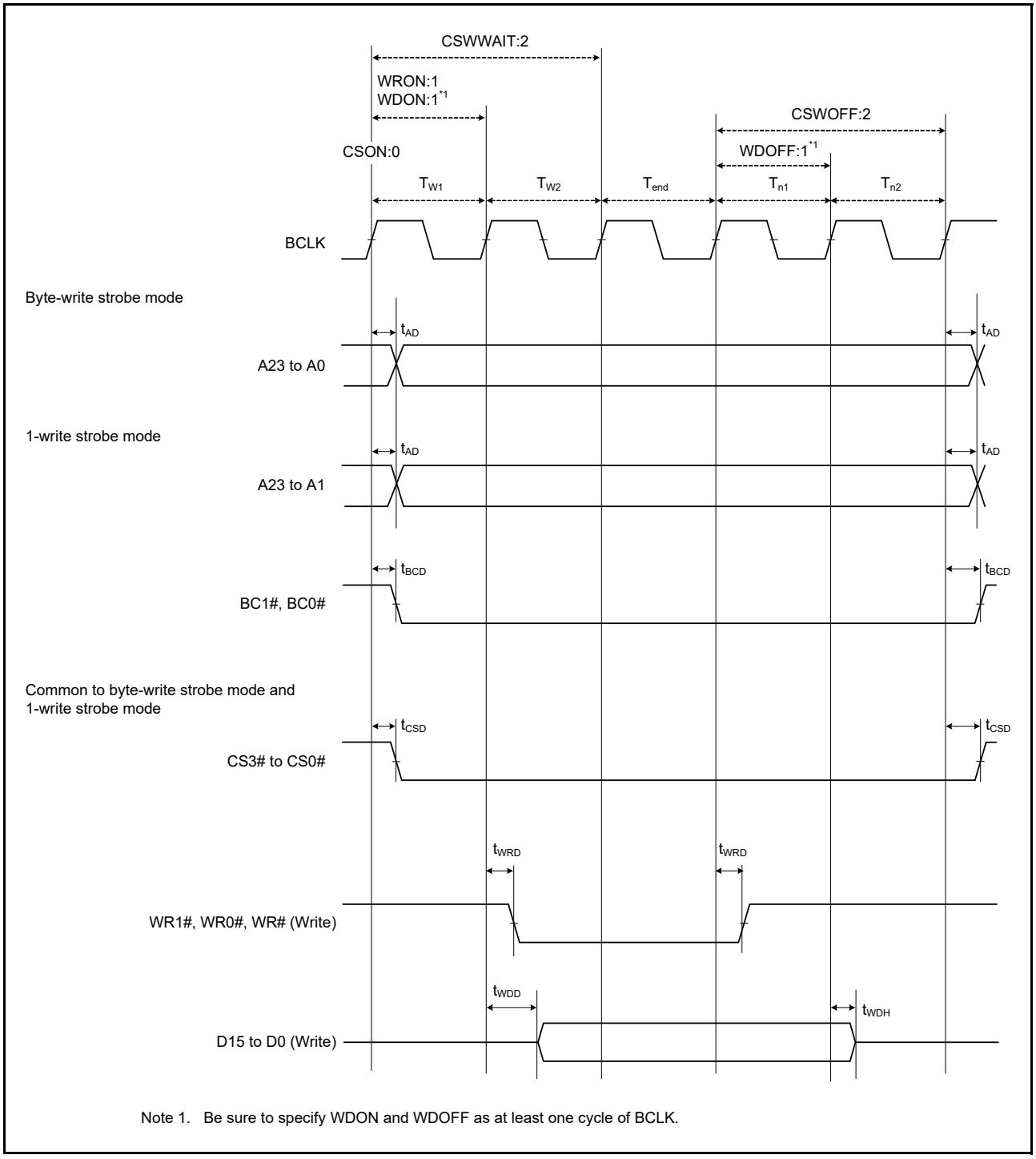
Note 3. The VCC range should be 2.4 to 5.5 V when the PLL is used.

Note 4. Reference values when a 32.768-kHz resonator is used.
After the setting of the SOSCCR.SOSTP bit or RCR3.RTCEN bit is changed to operate the sub-clock oscillator, only start using the sub-clock after the sub-clock oscillation stabilization wait time that is equal to or greater than the oscillator-manufacturer-recommended value has elapsed.

Note 5. The VCC range should be 3.0 to 5.5 V when the USBPLL is used.

Note 6. The input frequency can be set to 6 or 8 MHz and the oscillation frequency can be set to 48 MHz only.

Note 7. Only 32.768 kHz can be used.



Note 1. Be sure to specify WDON and WDOFF as at least one cycle of BCLK.

Figure 5.39 External Bus Timing/Normal Write Cycle (Bus Clock Synchronization)

5.3.6 Timing of On-Chip Peripheral Modules

Table 5.38 Timing of On-Chip Peripheral Modules (1)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit *1	Test Conditions
I/O ports	Input data pulse width		t_{PRW}	1.5	—	t_{Pcyc}	Figure 5.45
MTU2/TPU	Input capture input pulse width	Single-edge setting	t_{TICW}	1.5	—	t_{Pcyc}	Figure 5.46
		Both-edge setting		2.5	—		
	Timer clock pulse width	Single-edge setting	t_{TCKWH}, t_{TCKWL}	1.5	—	t_{Pcyc}	Figure 5.47
		Both-edge setting		2.5	—		
		Phase counting mode		2.5	—		
POE2	POE# input pulse width		t_{POEW}	1.5	—	t_{Pcyc}	Figure 5.48
TMR	Timer clock pulse width	Single-edge setting	t_{TMCWH}, t_{TMCWL}	1.5	—	t_{Pcyc}	Figure 5.49
		Both-edge setting		2.5	—		
SCI	Input clock cycle time	Asynchronous	t_{Scyc}	4	—	t_{Pcyc}	Figure 5.50
		Clock synchronous		6	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	20	ns	
	Input clock fall time		t_{SCKf}	—	20	ns	
	Output clock cycle time	Asynchronous	t_{Scyc}	16	—	t_{Pcyc}	Figure 5.51
		Clock synchronous		4	—		
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		t_{SCKr}	—	20	ns	
	Output clock fall time		t_{SCKf}	—	20	ns	
	Transmit data delay time (master)	Clock synchronous	t_{TXD}	—	40	ns	
	Transmit data delay time (slave)	Clock synchronous, 2.7 V or above		—	65	ns	
		Clock synchronous, 1.8 V or above		—	100	ns	
	Receive data setup time (master)	Clock synchronous, 2.7 V or above	t_{RXS}	65	—	ns	
		Clock synchronous, 1.8 V or above		90	—	ns	
	Receive data setup time (slave)	Clock synchronous		40	—	ns	
	Receive data hold time	Clock synchronous	t_{RXH}	40	—	ns	
A/D converter	Trigger input pulse width		t_{TRGW}	1.5	—	t_{Pcyc}	Figure 5.52
CAC	CACREF input pulse width	$t_{Pcyc} \le t_{cac}$ *2	t_{CACREF}	4.5 t_{cac} + 3 t_{Pcyc}	—	ns	
		$t_{Pcyc} > t_{cac}$ *2		5 t_{cac} + 6.5 t_{Pcyc}			
CLKOUT	CLKOUT pin output cycle*4	VCC = 2.7 V or above	t_{Ccyc}	62.5	—	ns	Figure 5.53
		VCC = 1.8 V or above		125			
	CLKOUT pin high pulse width*3	VCC = 2.7 V or above	t_{CH}	15	—	ns	
		VCC = 1.8 V or above		30			
	CLKOUT pin low pulse width*3	VCC = 2.7 V or above	t_{CL}	15	—	ns	
		VCC = 1.8 V or above		30			
	CLKOUT pin output rise time	VCC = 2.7 V or above	t_{Cr}	—	12	ns	
		VCC = 1.8 V or above			25		
	CLKOUT pin output fall time	VCC = 2.7 V or above	t_{Cf}	—	12	ns	
		VCC = 1.8 V or above			25		

Note 1. t_{Pcyc}: PCLK cycle
Note 2. t_{cac}: CAC count clock source cycle
Note 3. When the LOCO is selected as the clock output source (the CKOCR.CKOSEL[2:0] bits are 000b), set the clock output division ratio selection to divided by 2 (the CKOCR.CKODIV[2:0] bits are 001b).
Note 4. When the EXTAL external clock input or an oscillator is used with divided by 1 (the CKOCR.CKOSEL[2:0] bits are 010b and the CKOCR.CKODIV[2:0] bits are 000b) to output from CLKOUT, the above should be satisfied with an input duty cycle of 45 to 55%.

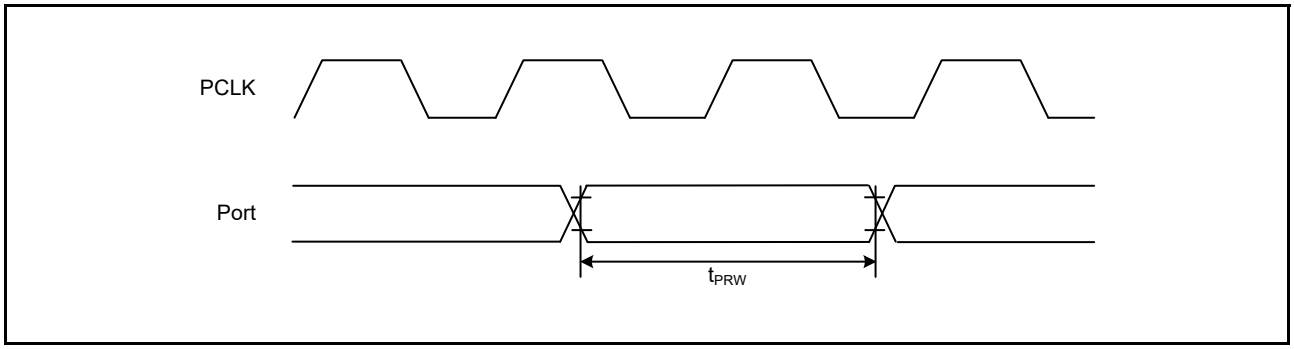


Figure 5.45 I/O Port Input Timing

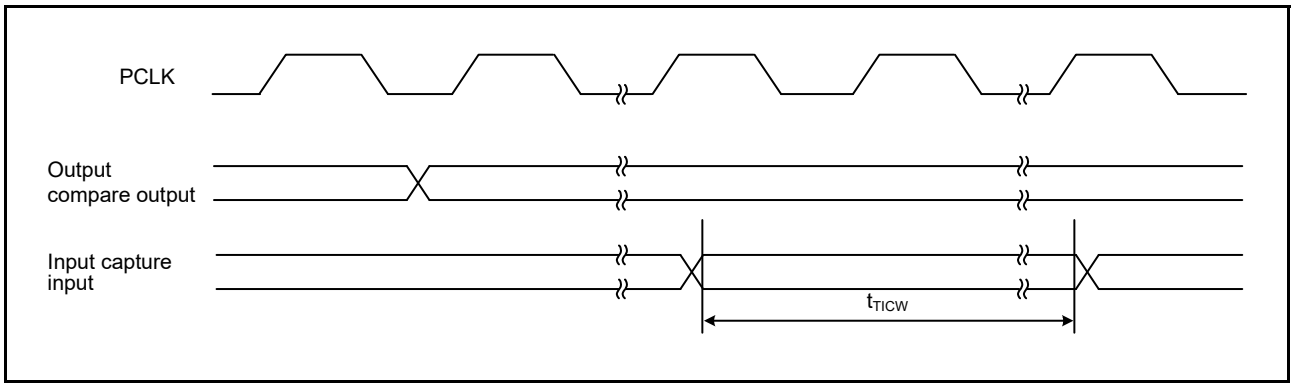


Figure 5.46 MTU2 Input/Output Timing

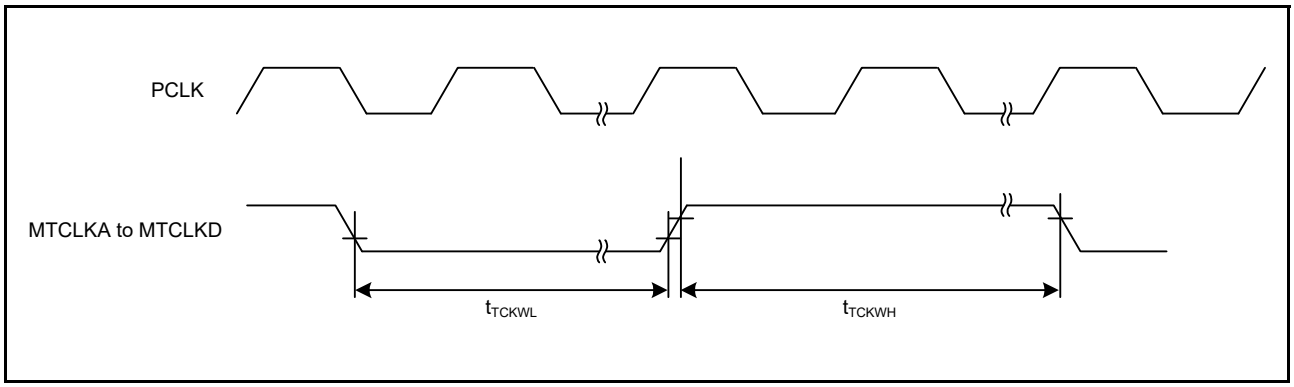


Figure 5.47 MTU2 Clock Input Timing

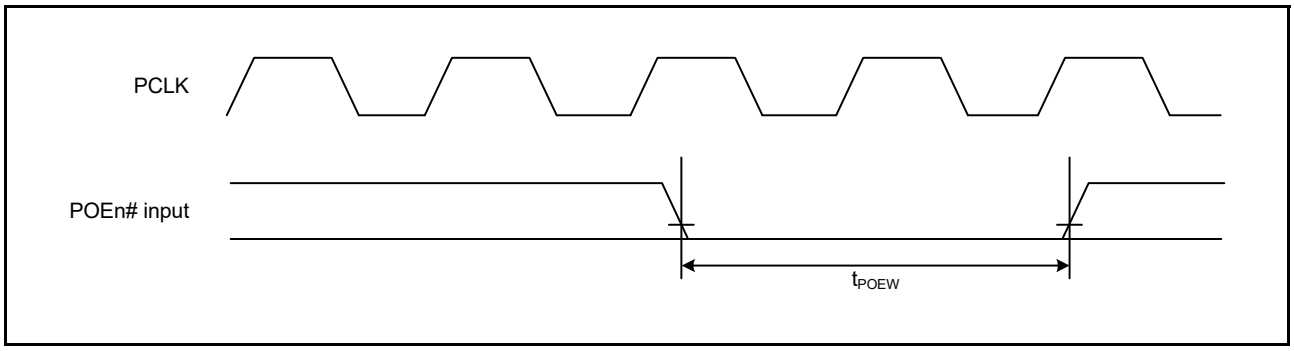
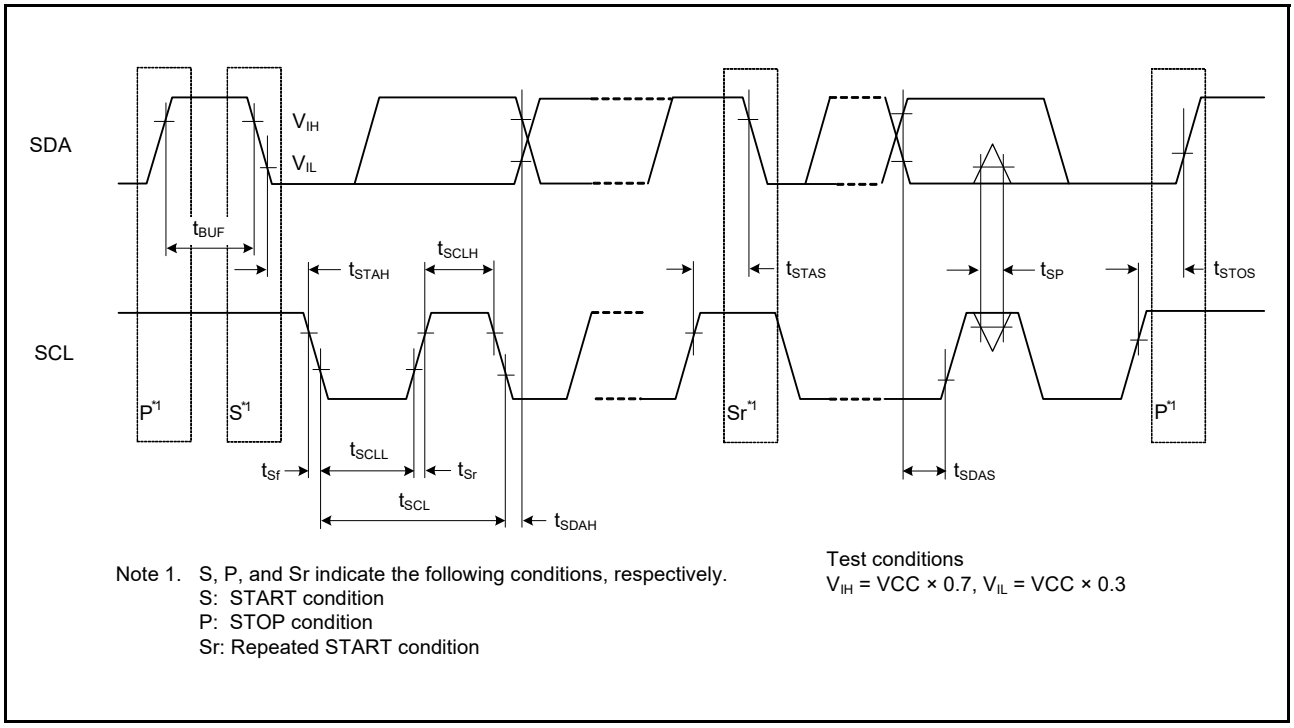


Figure 5.48 POE# Input Timing



Note 1. S, P, and Sr indicate the following conditions, respectively.
S: START condition
P: STOP condition
Sr: Repeated START condition

Figure 5.59 RIIC Bus Interface Input/Output Timing and Simple I²C Bus Interface Input/Output Timing

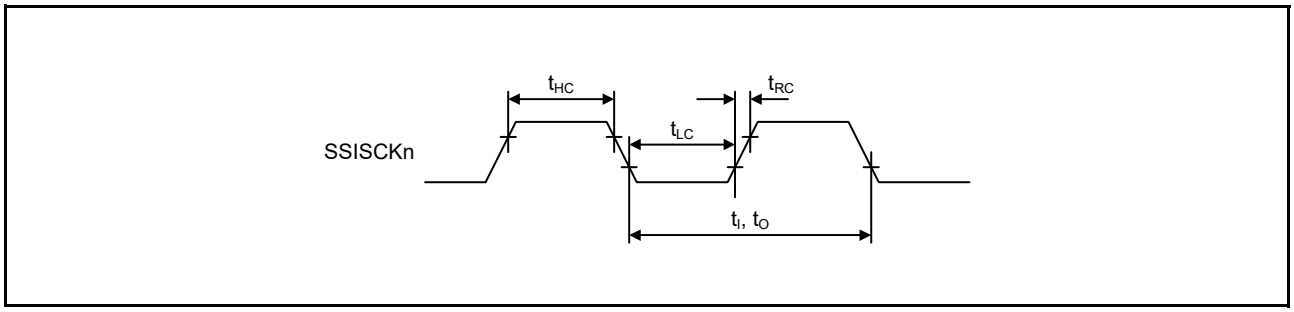


Figure 5.60 SSI Clock Input/Output Timing

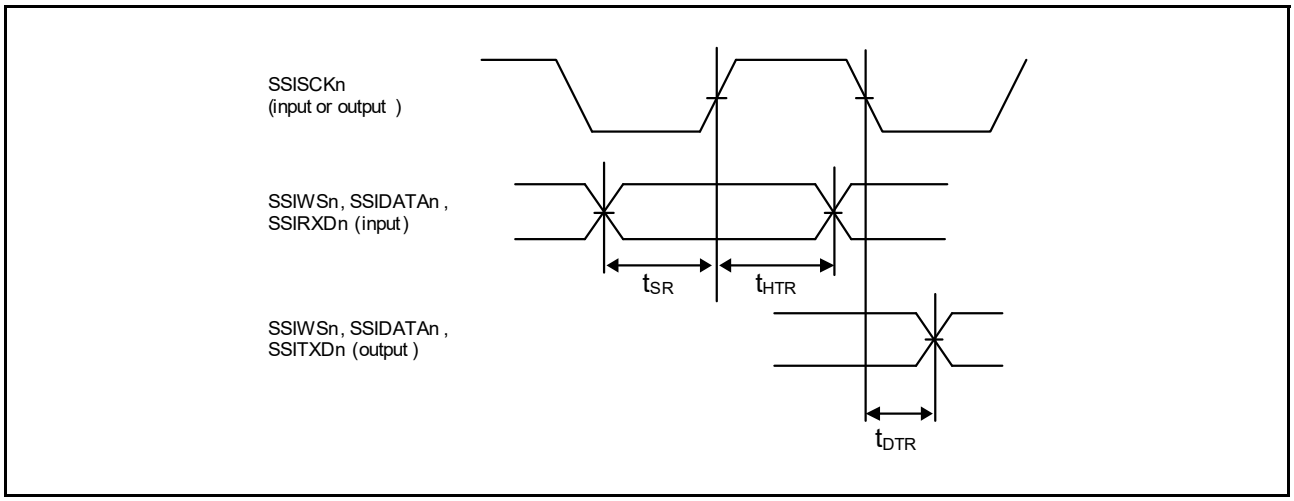


Figure 5.61 SSI Transmission/Reception Timing (SSICR.SCKP=0)

5.4 USB Characteristics

Table 5.45 USB Characteristics (USB0_DP and USB0_DM Pin Characteristics)

Conditions: 3.0 V ≤ VCC = VCC_USB = AVCC < 3.6 V (when a regulator is not in use) or 4.0 V ≤ VCC = AVCC0 < 5.5 V (when a regulator is in use), VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
Input characteristics	Input high level voltage		V_{IH}	2.0	—	V	
	Input low level voltage		V_{IL}	—	0.8	V	
	Differential input sensitivity		V_{DI}	0.2	—	V	| USB0_DP – USB0_DM |
	Differential common mode range		V_{CM}	0.8	2.5	V	
Output characteristics	Output high level voltage		V_{OH}	2.8	VCC_USB	V	I_{OH} = –200 µA
	Output low level voltage		V_{OL}	0.0	0.3	V	I_{OL} = 2 mA
	Cross-over voltage		V_{CRS}	1.3	2.0	V	Figure 5.65, Figure 5.66
	Rise time	FS	t_r	4	20	ns	
		LS		75	300		
	Fall time	FS	t_f	4	20	ns	
		LS		75	300		
	Rise/fall time ratio	FS	t_r/t_f	90	111.11	%	t_r/t_f
		LS		80	125		
	Output resistance		Z_{DRV}	28	44	Ω	(Adjusting the resistance by external elements is not necessary.)
VBUS characteristics	VBUS input voltage		V_{IH}	VCC × 0.8	—	V	
			V_{IL}	—	VCC × 0.2	V	
Pull-up, pull-down	Pull-down resistor		R_{PD}	14.25	24.80	kΩ	
	Pull-up resistor		R_{PUI}	0.9	1.575	kΩ	During idle state
			R_{PUA}	1.425	3.09	kΩ	During reception
Battery Charging Specification Ver 1.2	D+ sink current		I_{DP_SINK}	25	175	µA	
	D- sink current		I_{DM_SINK}	25	175	µA	
	DCD source current		I_{DP_SRC}	7	13	µA	
	Data detection voltage		V_{DAT_REF}	0.25	0.4	V	
	D+ source current		V_{DP_SRC}	0.5	0.7	V	Output current = 250 µA
	D- source current		V_{DM_SRC}	0.5	0.7	V	Output current = 250 µA

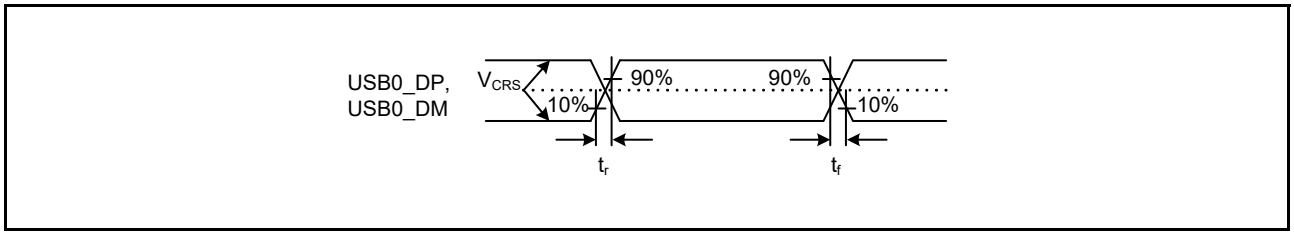


Figure 5.65 USB0_DP and USB0_DM Output Timing

Table 5.50 A/D Conversion Characteristics (5)

Conditions: 1.8V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5V, 1.8V ≤ VREFH0 ≤ AVCC0, VSS = AVSS0 = VSS_USB = 0V, reference voltage = VREFH0 selected, Ta = –40 to +105°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	8	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 8 MHz)	Permissible signal source impedance (Max.) = 5 kΩ	6.75	—	—	µs	High-precision channel The ADCSR.ADHSC bit is 1 The ADSSTRn register is 0Dh
		10.13	—	—		Normal-precision channel The ADCSR.ADHSC bit is 1 The ADSSTRn register is 28h
Analog input capacitance	Cs	—	—	15	pF	Pin capacitance included Figure 5.68
Analog input resistance	Rs	—	—	2.5	kΩ	Figure 5.68
Offset error		—	±1	±7.5	LSB	
Full-scale error		—	±1.5	±7.5	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±3.0	±8.0	LSB	
DNL differential non-linearity error		—	±1.0	—	LSB	
INL integral non-linearity error		—	±1.25	±3.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential non-linearity error, and INL integral non-linearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 5.51 A/D Converter Channel Classification

Classification	Channel	Conditions	Remarks
High-precision channel	AN000 to AN007	AVCC0 = 1.8 to 5.5 V	Pins AN000 to AN007 cannot be used as digital outputs when the A/D converter is in use.
Normal-precision channel	AN016 to AN031		
Internal reference voltage input channel	Internal reference voltage	AVCC0 = 2.0 to 5.5 V	
Temperature sensor input channel	Temperature sensor output	AVCC0 = 2.0 to 5.5 V	

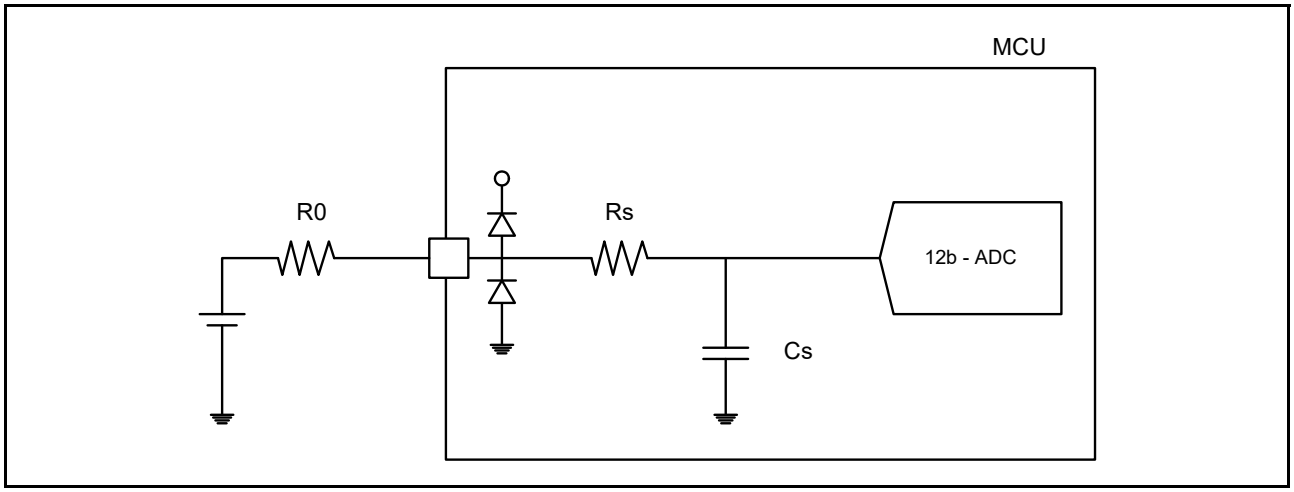


Figure 5.68 Equivalent Circuit

5.7 Temperature Sensor Characteristics

Table 5.55 Temperature Sensor Characteristics

Conditions: 2.0 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Relative accuracy	—	—	±1.5	—	°C	2.4 V or above
		—	±2.0	—		Below 2.4 V
Temperature slope	—	—	–3.65	—	mV/°C	
Output voltage (25°C)	—	—	1.05	—	V	VCC = 3.3 V
Temperature sensor start time	t_{START}	—	—	5	µs	
Sampling time	—	5	—	—	µs	

5.8 Comparator Characteristics

Table 5.56 Comparator Characteristics

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
CVREFB0 to CVREFB3 input reference voltage		VREF	0	—	VCC - 1.4	V	
CMPB0 to CMPB3 input voltage		VI	–0.3	—	VCC + 0.3	V	
Offset	Comparator high-speed mode	—	—	—	50	mV	
	Comparator high-speed mode Window function enabled	—	—	—	60	mV	
	Comparator low-speed mode	—	—	—	40	mV	
Comparator output delay time	Comparator high-speed mode	Td	—	—	1.2	µs	VCC = 3 V, input slew rate ≥ 50 mV/us
	Comparator high-speed mode Window function enabled	Tdw	—	—	2.0	µs	
	Comparator low-speed mode	Td	—	—	5.0	µs	
High-side reference voltage (comparator high-speed mode, window function enabled)		VRFH	—	0.76 VCC	—	V	
Low-side reference voltage (comparator high-speed mode, window function enabled)		VRFL	—	0.24 VCC	—	V	
Operation stabilization wait time		Tcmp	100	—	—	µs	

Rev.	Date	Description		Classification
		Page	Summary	
1.20	Sep 28, 2018	95	Figure 5.12 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 5.5 V When Normal Output is Selected (Reference Data), changed	TN-RX*-A201A/E
		124	Table 5.44 Timing of On-Chip Peripheral Modules (7), added	TN-RX*-A197A/E
		131	Figure 5.64 SD Host Interface Input/Output Signal Timing, added	TN-RX*-A197A/E
		132	Table 5.45 USB Characteristics (USB0_DP and USB0_DM Pin Characteristics) conditions, changed	