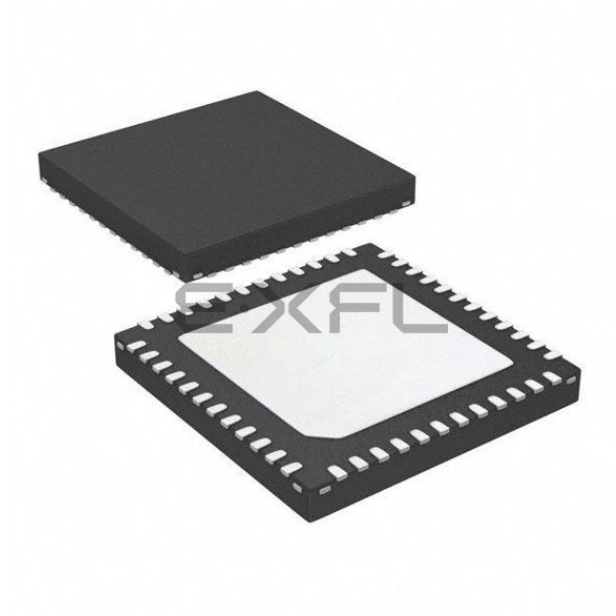
Renesas Electronics America Inc - R5F52316ADNE#U0 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	54MHz
Connectivity	CANbus, I²C, IrDA, SCI, SD/SDIO, SPI, SSI, USB OTG
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	30
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-WFQFN Exposed Pad
Supplier Device Package	48-HWQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f52316adne-u0

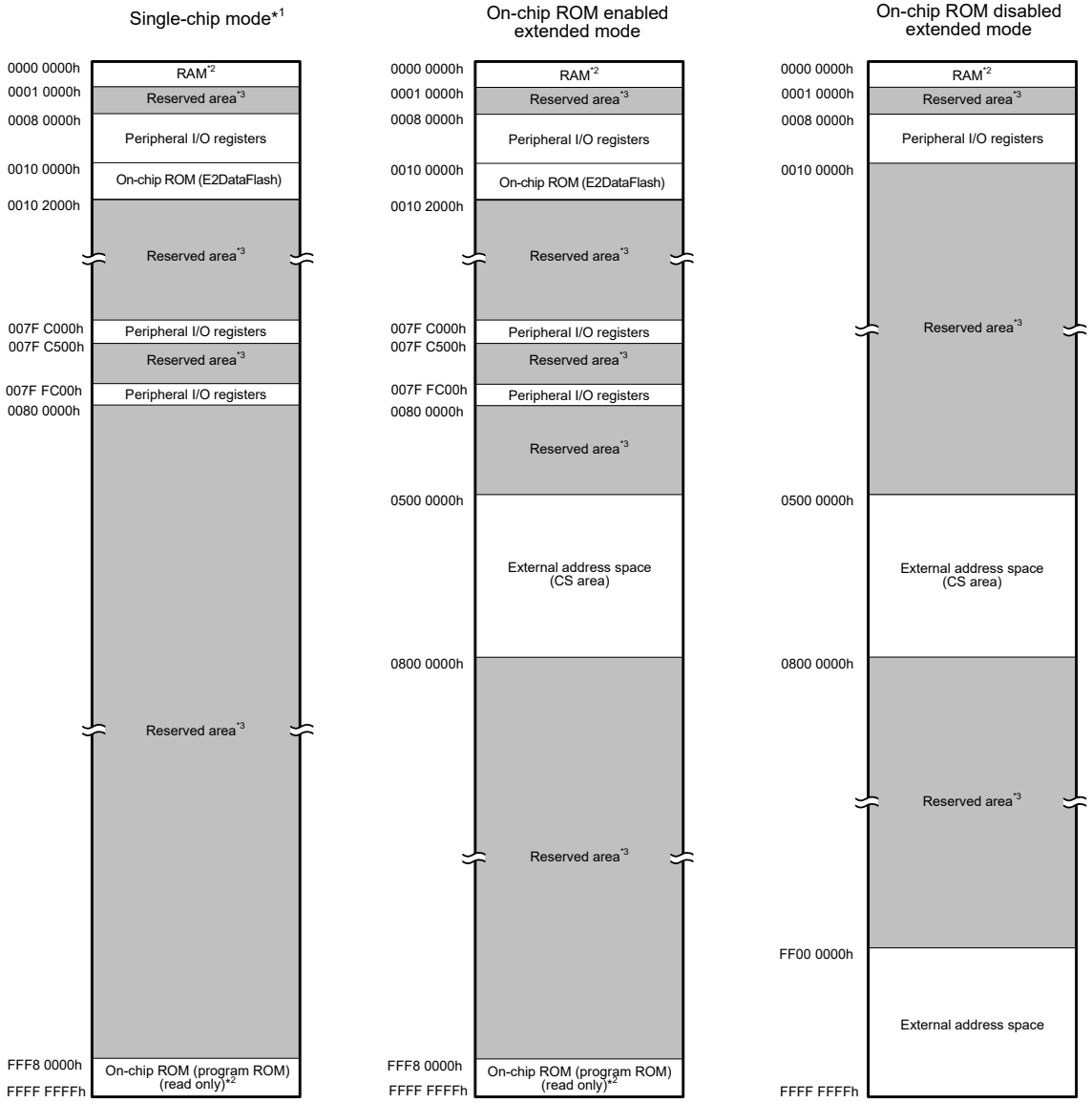
Table 1.7 List of Pins and Pin Functions (100-Pin LFQFP) (3/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCI, RSPI, RIIC, RSCAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
79		PD7	D7[A7/D7]	MTIC5U/POE0#				IRQ7/AN031
80		PD6	D6[A6/D6]	MTIC5V/POE1#				IRQ6/AN030
81		PD5	D5[A5/D5]	MTIC5W/POE2#				IRQ5/AN029
82		PD4	D4[A4/D4]	POE3#				IRQ4/AN028
83		PD3	D3[A3/D3]	POE8#				IRQ3/AN027
84		PD2	D2[A2/D2]	MTIOC4D				IRQ2/AN026
85		PD1	D1[A1/D1]	MTIOC4B				IRQ1/AN025
86		PD0	D0[A0/D0]					IRQ0/AN024
87		P47						AN007
88		P46						AN006
89		P45						AN005
90		P44						AN004
91		P43						AN003
92		P42						AN002
93		P41						AN001
94	VREFL0							
95		P40						AN000
96	VREFH0							
97	AVCC0							
98		P07						ADTRG0#
99	AVSS0							
100		P05						DA1

Note 1. RX230: PH0/CACREF, PH1/IRQ0/TMO0, PH2/IRQ1/TMRI0, PH3/TMCI0
RX231: VSS_USB, USB0_DP, USB0_DM, VCC_USB

Table 1.8 List of Pins and Pin Functions (64-Pin WFLGA) (1/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCI, RSPI, RIIC, RSCAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
A1		P05					DA1
A2	AVCC0						
A3	VREFH0						
A4	VREFL0						
A5	VREFH						
A6	VREFL						
A7		PE2	MTIOC4A	RXD12/RXDX12/SMISO12/ SSCL12			IRQ7/AN018/ CVREFB0
A8		PE3	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#/ AUDIO_MCLK			AN019/CLKOUT
B1	VCL						
B2	AVSS0						
B3		P40					AN000
B4		P42					AN002
B5		P44					AN004
B6		P46					AN006
B7		PE1	MTIOC4C	TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12			AN017/CMPB0
B8		PE4	MTIOC4D/MTIOC1A				AN020/CMPA2/ CLKOUT
C1	XCIN						
C2	MD						FINED
C3		P03					DA0
C4		P41					AN001
C5		P43					AN003
C6		PE0		SCK12			AN016
C7		PE5	MTIOC4C/MTIOC2B				IRQ5/AN021/ CMPOB0
C8		PA0	MTIOC4A/TIOCA0	SSLA1			CACREF
D1	XCOUT						
D2	RES#						
D3		P27	MTIOC2B/TMCI3	SCK1/ SSIWS0		TS2	CVREFB3
D4		P14	MTIOC3A/MTCLKA/TMRI2/ TIOCB5/TCLKA	CTS1#/RTS1#/SS1#/CTXD0/ USB0_OVRCURA		TS13	IRQ4/CVREFB2
D5		PA6	MTIC5V/MTCLKB/TMCI3/POE2#/ TIOCA2	CTS5#/RTS5#/SS5#/MOSIA/ SSIWS0			
D6		PA4	MTIC5U/MTCLKA/TMRI0/TIOCA1	TXD5/SMOSI5/SSDA5/SSLA0/ SSITXD0/IRTXD5			IRQ5 /CVREFB1
D7		PA1	MTIOC0B/MTCLKC/TIOCB0	SCK5/SSLA2/SSISCK0			
D8		PA3	MTIOC0D/MTCLKD/TIOCD0/ TCLKB	RXD5/SMISO5/SSCL5/SSIRXD0/ IRRXD5			IRQ6 /CMPB1
E1	VSS						
E2	VBATT						
E3		P30	MTIOC4B/TMRI3/POE8#/RTCIC0	RXD1/SMISO1/SSCL1/ AUDIO_MCLK			IRQ0/CMPOB3
E4		P16	MTIOC3C/MTIOC3D/TMO2/ TIOCB1/TCLKC/RTCOUT	TXD1/SMOSI1/SSDA1/MOSIA/ SCL/USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB			IRQ6/ADTRG0#
E5		PC4	MTIOC3D/MTCLKC/TMCI1/ POE0#	SCK5/CTS8#/RTS8#/SS8#/ SSLA0	SDHI_D1	TSCAP	
E6	VCC						
E7	VSS						
E8		PB0	MTIC5W/TIOCA3	RXD6/SMISO6/SSCL6/RSPCKA	SDHI_C MD		
F1	VCC						
F2	UPSEL	P35					NMI
F3		P31	MTIOC4D/TMCI2/RTCIC1	CTS1#/RTS1#/SS1#/SSISCK0			IRQ1



Note 1. The address space in boot mode and USB boot mode is the same as the address space in single-chip mode.
Note 2. The capacity of ROM/RAM differs depending on the products.

ROM (bytes)		RAM (bytes)	
Capacity	**Address**	**Capacity**	**Address**
512 Kbytes	FFF8 0000h to FFFF FFFFh	64 Kbytes	0000 0000h to 0000 FFFFh
384 Kbytes	FFFA 0000h to FFFF FFFFh		
256 Kbytes	FFFC 0000h to FFFF FFFFh	32 Kbytes	0000 0000h to 0000 7FFFh
128 Kbytes	FFFE 0000h to FFFF FFFFh		

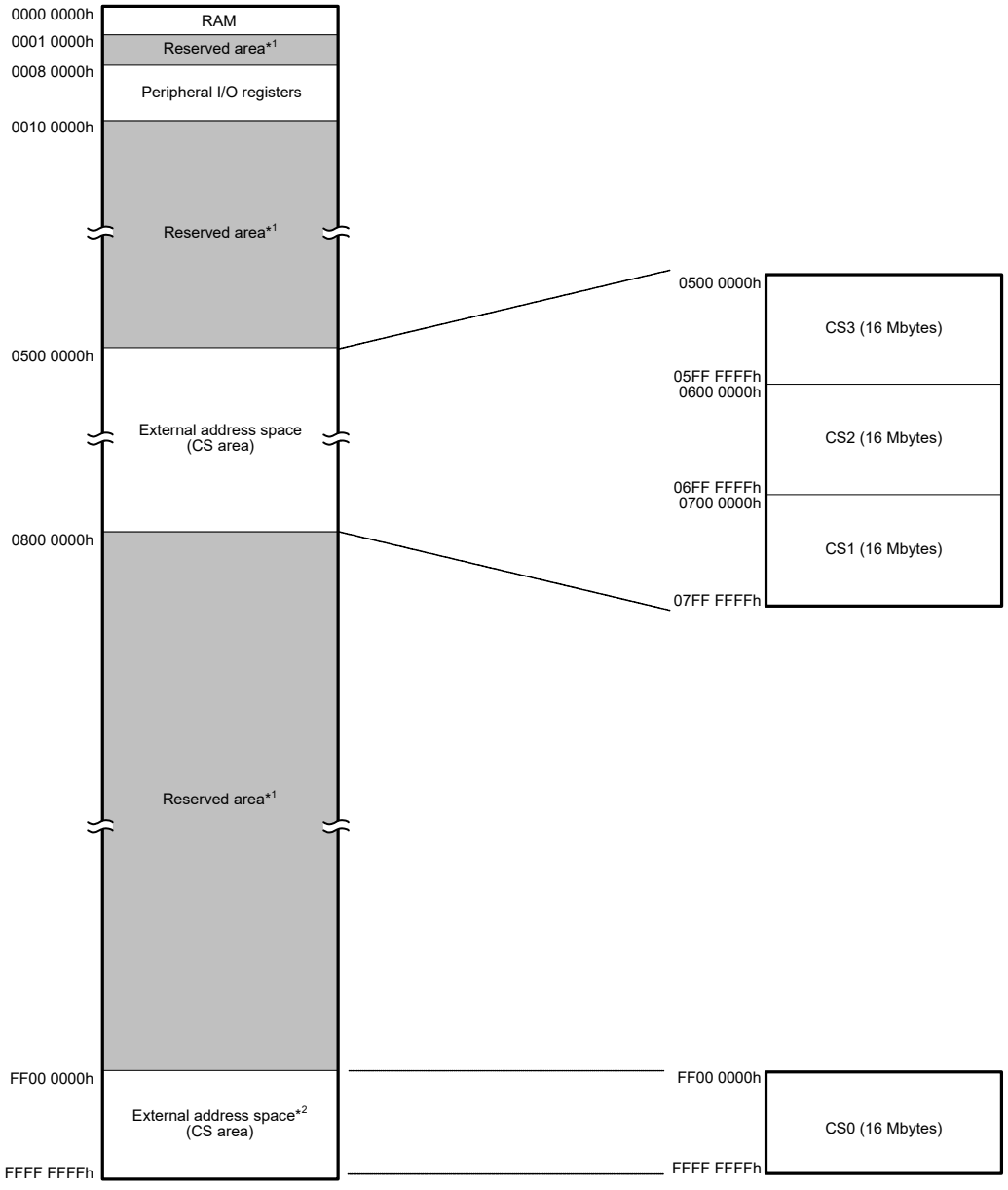
Note: See Table 1.3 and Table 1.4 List of Products, for the product type name.

Note 3. Reserved areas should not be accessed.

Figure 3.1 Memory Map in Each Operating Mode

3.2 External Address Space

The external address space is divided into up to four CS areas (CS0 to CS3), each corresponding to the CSn# signal output from a CSn# (n = 0 to 3) pin. Figure 3.2 shows the address ranges corresponding to the individual CS areas (CS0 to CS3) in on-chip ROM disabled extended mode.



Note 1. Reserved areas should not be accessed.
Note 2. The CS0 area is disabled in on-chip ROM enabled extended mode.
In this mode, the address space for addresses above 1000 0000h is as shown in figure on this section, Memory Map in Each Operating Mode.

Figure 3.2 Correspondence between External Address Spaces and CS Areas (In On-Chip ROM Disabled Extended Mode)

Table 4.1 List of I/O Registers (Address Order) (8/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK <PCLK
0008 901Eh	S12AD	A/D Self-Diagnosis Data Register	ADRD	16	16	2 or 3 PCLKB	2 ICLK
0008 9020h	S12AD	A/D Data Register 0	ADDR0	16	16	2 or 3 PCLKB	2 ICLK
0008 9022h	S12AD	A/D Data Register 1	ADDR1	16	16	2 or 3 PCLKB	2 ICLK
0008 9024h	S12AD	A/D Data Register 2	ADDR2	16	16	2 or 3 PCLKB	2 ICLK
0008 9026h	S12AD	A/D Data Register 3	ADDR3	16	16	2 or 3 PCLKB	2 ICLK
0008 9028h	S12AD	A/D Data Register 4	ADDR4	16	16	2 or 3 PCLKB	2 ICLK
0008 902Ah	S12AD	A/D Data Register 5	ADDR5	16	16	2 or 3 PCLKB	2 ICLK
0008 902Ch	S12AD	A/D Data Register 6	ADDR6	16	16	2 or 3 PCLKB	2 ICLK
0008 902Eh	S12AD	A/D Data Register 7	ADDR7	16	16	2 or 3 PCLKB	2 ICLK
0008 9040h	S12AD	A/D Data Register 16	ADDR16	16	16	2 or 3 PCLKB	2 ICLK
0008 9042h	S12AD	A/D Data Register 17	ADDR17	16	16	2 or 3 PCLKB	2 ICLK
0008 9044h	S12AD	A/D Data Register 18	ADDR18	16	16	2 or 3 PCLKB	2 ICLK
0008 9046h	S12AD	A/D Data Register 19	ADDR19	16	16	2 or 3 PCLKB	2 ICLK
0008 9048h	S12AD	A/D Data Register 20	ADDR20	16	16	2 or 3 PCLKB	2 ICLK
0008 904Ah	S12AD	A/D Data Register 21	ADDR21	16	16	2 or 3 PCLKB	2 ICLK
0008 904Ch	S12AD	A/D Data Register 22	ADDR22	16	16	2 or 3 PCLKB	2 ICLK
0008 904Eh	S12AD	A/D Data Register 23	ADDR23	16	16	2 or 3 PCLKB	2 ICLK
0008 9050h	S12AD	A/D Data Register 24	ADDR24	16	16	2 or 3 PCLKB	2 ICLK
0008 9052h	S12AD	A/D Data Register 25	ADDR25	16	16	2 or 3 PCLKB	2 ICLK
0008 9055h	S12AD	A/D Data Register 26	ADDR26	16	16	2 or 3 PCLKB	2 ICLK
0008 9056h	S12AD	A/D Data Register 27	ADDR27	16	16	2 or 3 PCLKB	2 ICLK
0008 9058h	S12AD	A/D Data Register 28	ADDR28	16	16	2 or 3 PCLKB	2 ICLK
0008 905Ah	S12AD	A/D Data Register 29	ADDR29	16	16	2 or 3 PCLKB	2 ICLK
0008 905Ch	S12AD	A/D Data Register 30	ADDR30	16	16	2 or 3 PCLKB	2 ICLK
0008 905Eh	S12AD	A/D Data Register 31	ADDR31	16	16	2 or 3 PCLKB	2 ICLK
0008 907Ah	S12AD	A/D Disconnection Detection Control Register	ADDISCR	8	8	2 or 3 PCLKB	2 ICLK
0008 907Dh	S12AD	A/D Event Link Control Register	ADELCCR	8	8	2 or 3 PCLKB	2 ICLK
0008 9080h	S12AD	A/D Group Scan Priority Control Register	ADGSPCR	16	16	2 or 3 PCLKB	2 ICLK
0008 908Ah	S12AD	A/D High-Side/Low-Side Reference Voltage Control Register	ADHVREFCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 908Ch	S12AD	A/D Compare Function Window A/B Status Monitor Register	ADWINMON	8	8	2 or 3 PCLKB	2 ICLK
0008 9090h	S12AD	A/D Compare Function Control Register	ADCMPCR	16	16	2 or 3 PCLKB	2 ICLK
0008 9092h	S12AD	A/D Compare Function Window A Extended Input Select Register	ADCMPANSER	8	8	2 or 3 PCLKB	2 ICLK
0008 9093h	S12AD	A/D Compare Function Window A Extended Input Comparison Condition Setting Register	ADCMPLER	8	8	2 or 3 PCLKB	2 ICLK
0008 9094h	S12AD	A/D Compare Function Window A Channel Select Register 0	ADCMPANSR0	16	16	2 or 3 PCLKB	2 ICLK
0008 9096h	S12AD	A/D Compare Function Window A Channel Select Register 1	ADCMPANSR1	16	16	2 or 3 PCLKB	2 ICLK
0008 9098h	S12AD	A/D Compare Function Window A Comparison Condition Setting Register 0	ADCMPLR0	16	16	2 or 3 PCLKB	2 ICLK
0008 909Ah	S12AD	A/D Compare Function Window A Comparison Condition Setting Register 1	ADCMPLR1	16	16	2 or 3 PCLKB	2 ICLK
0008 909Ch	S12AD	A/D Compare Function Window A Lower-Side Level Setting Register	ADCMPDR0	16	16	2 or 3 PCLKB	2 ICLK
0008 909Eh	S12AD	A/D Compare Function Window A Upper-Side Level Setting Register	ADCMPDR1	16	16	2 or 3 PCLKB	2 ICLK
0008 90A0h	S12AD	A/D Compare Function Window A Channel Status Register 0	ADCMPSR0	16	16	2 or 3 PCLKB	2 ICLK
0008 90A2h	S12AD	A/D Compare Function Window A Channel Status Register 1	ADCMPSR1	16	16	2 or 3 PCLKB	2 ICLK
0008 90A4h	S12AD	A/D Compare Function Window A Extended Input Channel Status Register	ADCMPSER	16	16	2 or 3 PCLKB	2 ICLK
0008 90A6h	S12AD	A/D Compare Function Window B Channel Select Register	ADCMPBNSR	8	8	2 or 3 PCLKB	2 ICLK
0008 90A8h	S12AD	A/D Compare Function Window B Lower-Side Level Setting Register	ADWINLLB	16	16	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (9/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK <PCLK
0008 90AAh	S12AD	A/D Compare Function Window B Upper-Side Level Setting Register	ADWINULB	16	16	2 or 3 PCLKB	2 ICLK
0008 90ACh	S12AD	A/D Compare Function Window B Channel Status Register	ADCMPBSR	8	8	2 or 3 PCLKB	2 ICLK
0008 90B0h	S12AD	A/D Data Storage Buffer Register 0	ADBUF0	16	16	2 or 3 PCLKB	2 ICLK
0008 90B2h	S12AD	A/D Data Storage Buffer Register 1	ADBUF1	16	16	2 or 3 PCLKB	2 ICLK
0008 90B4h	S12AD	A/D Data Storage Buffer Register 2	ADBUF2	16	16	2 or 3 PCLKB	2 ICLK
0008 90B6h	S12AD	A/D Data Storage Buffer Register 3	ADBUF3	16	16	2 or 3 PCLKB	2 ICLK
0008 90B8h	S12AD	A/D Data Storage Buffer Register 4	ADBUF4	16	16	2 or 3 PCLKB	2 ICLK
0008 90BAh	S12AD	A/D Data Storage Buffer Register 5	ADBUF5	16	16	2 or 3 PCLKB	2 ICLK
0008 90BCh	S12AD	A/D Data Storage Buffer Register 6	ADBUF6	16	16	2 or 3 PCLKB	2 ICLK
0008 90BEh	S12AD	A/D Data Storage Buffer Register 7	ADBUF7	16	16	2 or 3 PCLKB	2 ICLK
0008 90C0h	S12AD	A/D Data Storage Buffer Register 8	ADBUF8	16	16	2 or 3 PCLKB	2 ICLK
0008 90C2h	S12AD	A/D Data Storage Buffer Register 9	ADBUF9	16	16	2 or 3 PCLKB	2 ICLK
0008 90C4h	S12AD	A/D Data Storage Buffer Register 10	ADBUF10	16	16	2 or 3 PCLKB	2 ICLK
0008 90C6h	S12AD	A/D Data Storage Buffer Register 11	ADBUF11	16	16	2 or 3 PCLKB	2 ICLK
0008 90C8h	S12AD	A/D Data Storage Buffer Register 12	ADBUF12	16	16	2 or 3 PCLKB	2 ICLK
0008 90CAh	S12AD	A/D Data Storage Buffer Register 13	ADBUF13	16	16	2 or 3 PCLKB	2 ICLK
0008 90CCh	S12AD	A/D Data Storage Buffer Register 14	ADBUF14	16	16	2 or 3 PCLKB	2 ICLK
0008 90CEh	S12AD	A/D Data Storage Buffer Register 15	ADBUF15	16	16	2 or 3 PCLKB	2 ICLK
0008 90D0h	S12AD	A/D Data Storage Buffer Enable Register	ADBUFEN	8	8	2 or 3 PCLKB	2 ICLK
0008 90D2h	S12AD	A/D Data Storage Buffer Pointer Register	ADBUFPTR	8	8	2 or 3 PCLKB	2 ICLK
0008 90DDh	S12AD	A/D Sampling State Register L	ADSSTRL	8	8	2 or 3 PCLKB	2 ICLK
0008 90DEh	S12AD	A/D Sampling State Register T	ADSSTRT	8	8	2 or 3 PCLKB	2 ICLK
0008 90DFh	S12AD	A/D Sampling State Register O	ADSSTRO	8	8	2 or 3 PCLKB	2 ICLK
0008 90E0h	S12AD	A/D Sampling State Register 0	ADSSTR0	8	8	2 or 3 PCLKB	2 ICLK
0008 90E1h	S12AD	A/D Sampling State Register 1	ADSSTR1	8	8	2 or 3 PCLKB	2 ICLK
0008 90E2h	S12AD	A/D Sampling State Register 2	ADSSTR2	8	8	2 or 3 PCLKB	2 ICLK
0008 90E3h	S12AD	A/D Sampling State Register 3	ADSSTR3	8	8	2 or 3 PCLKB	2 ICLK
0008 90E4h	S12AD	A/D Sampling State Register 4	ADSSTR4	8	8	2 or 3 PCLKB	2 ICLK
0008 90E5h	S12AD	A/D Sampling State Register 5	ADSSTR5	8	8	2 or 3 PCLKB	2 ICLK
0008 90E6h	S12AD	A/D Sampling State Register 6	ADSSTR6	8	8	2 or 3 PCLKB	2 ICLK
0008 90E7h	S12AD	A/D Sampling State Register 7	ADSSTR7	8	8	2 or 3 PCLKB	2 ICLK
0008 A000h	SCI0	Serial Mode Register	SMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A001h	SCI0	Bit Rate Register	BRR	8	8	2 or 3 PCLKB	2 ICLK
0008 A002h	SCI0	Serial Control Register	SCR	8	8	2 or 3 PCLKB	2 ICLK
0008 A003h	SCI0	Transmit Data Register	TDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A004h	SCI0	Serial Status Register	SSR	8	8	2 or 3 PCLKB	2 ICLK
0008 A005h	SCI0	Receive Data Register	RDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A006h	SCI0	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A007h	SCI0	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A008h	SCI0	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB	2 ICLK
0008 A009h	SCI0	I^2C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB	2 ICLK
0008 A00Ah	SCI0	I^2C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB	2 ICLK
0008 A00Bh	SCI0	I^2C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB	2 ICLK
0008 A00Ch	SCI0	I^2C Status Register	SISR	8	8	2 or 3 PCLKB	2 ICLK
0008 A00Dh	SCI0	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A00Eh	SCI0	Transmit Data Register HL	TDRHL	16	16	4 or 5 PCLKB	2 ICLK
0008 A00Eh	SCI0	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB	2 ICLK
0008 A00Fh	SCI0	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB	2 ICLK
0008 A010h	SCI0	Receive Data Register HL	RDRHL	16	16	4 or 5 PCLKB	2 ICLK
0008 A010h	SCI0	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB	2 ICLK
0008 A011h	SCI0	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (23/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK <PCLK
000A 00B0h	USB0	BC Control Register 0	USBBCCTRL0	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 00CCh	USB0	USB Module Control Register	USBMC	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 00D0h	USB0	Device Address 0 Configuration Register	DEVADD0	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 00D2h	USB0	Device Address 1 Configuration Register	DEVADD1	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 00D4h	USB0	Device Address 2 Configuration Register	DEVADD2	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 00D6h	USB0	Device Address 3 Configuration Register	DEVADD3	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 00D8h	USB0	Device Address 4 Configuration Register	DEVADD4	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 00DAh	USB0	Device Address 5 Configuration Register	DEVADD5	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 0900h	CTSU	CTSU Control Register 0	CTSUCR0	8	8	2 or 3 PCLKB	2 ICLK
000A 0901h	CTSU	CTSU Control Register 1	CTSUCR1	8	8	2 or 3 PCLKB	2 ICLK
000A 0902h	CTSU	CTSU Synchronous Noise Reduction Setting Register	CTSUSDPRS	8	8	2 or 3 PCLKB	2 ICLK
000A 0903h	CTSU	CTSU Sensor Stabilization Wait Control Register	CTSUSST	8	8	2 or 3 PCLKB	2 ICLK
000A 0904h	CTSU	CTSU Measurement Channel Register 0	CTSUMCH0	8	8	2 or 3 PCLKB	2 ICLK
000A 0905h	CTSU	CTSU Measurement Channel Register 1	CTSUMCH1	8	8	2 or 3 PCLKB	2 ICLK
000A 0906h	CTSU	CTSU Channel Enable Control Register 0	CTSUCHAC0	8	8	2 or 3 PCLKB	2 ICLK
000A 0907h	CTSU	CTSU Channel Enable Control Register 1	CTSUCHAC1	8	8	2 or 3 PCLKB	2 ICLK
000A 0908h	CTSU	CTSU Channel Enable Control Register 2	CTSUCHAC2	8	8	2 or 3 PCLKB	2 ICLK
000A 0909h	CTSU	CTSU Channel Enable Control Register 3	CTSUCHAC3	8	8	2 or 3 PCLKB	2 ICLK
000A 090Ah	CTSU	CTSU Channel Enable Control Register 4	CTSUCHAC4	8	8	2 or 3 PCLKB	2 ICLK
000A 090Bh	CTSU	CTSU Channel Transmit/Receive Control Register 0	CTSUCHTRC0	8	8	2 or 3 PCLKB	2 ICLK
000A 090Ch	CTSU	CTSU Channel Transmit/Receive Control Register 1	CTSUCHTRC1	8	8	2 or 3 PCLKB	2 ICLK
000A 090Dh	CTSU	CTSU Channel Transmit/Receive Control Register 2	CTSUCHTRC2	8	8	2 or 3 PCLKB	2 ICLK
000A 090Eh	CTSU	CTSU Channel Transmit/Receive Control Register 3	CTSUCHTRC3	8	8	2 or 3 PCLKB	2 ICLK
000A 090Fh	CTSU	CTSU Channel Transmit/Receive Control Register 4	CTSUCHTRC4	8	8	2 or 3 PCLKB	2 ICLK
000A 0910h	CTSU	CTSU High-Pass Noise Reduction Control Register	CTSUDCLKC	8	8	2 or 3 PCLKB	2 ICLK
000A 0911h	CTSU	CTSU Status Register	CTSUST	8	8	2 or 3 PCLKB	2 ICLK
000A 0912h	CTSU	CTSU High-Pass Noise Reduction Spectrum Diffusion Control Register	CTSUSSC	16	16	2 or 3 PCLKB	2 ICLK
000A 0914h	CTSU	CTSU Sensor Offset Register 0	CTSUSO0	16	16	2 or 3 PCLKB	2 ICLK
000A 0916h	CTSU	CTSU Sensor Offset Register 1	CTSUSO1	16	16	2 or 3 PCLKB	2 ICLK
000A 0918h	CTSU	CTSU Sensor Counter	CTSUSC	16	16	2 or 3 PCLKB	2 ICLK
000A 091Ah	CTSU	CTSU Reference Counter	CTSURC	16	16	2 or 3 PCLKB	2 ICLK
000A 091Ch	CTSU	CTSU Error Status Register	CTSUERRS	16	16	2 or 3 PCLKB	2 ICLK
000A 8300h	RSCAN0	Bit Configuration Register L	CFGL	16	16	2 or 3 PCLKB	2 ICLK
000A 8302h	RSCAN0	Bit Configuration Register H	CFGH	16	16	2 or 3 PCLKB	2 ICLK
000A 8304h	RSCAN0	Control Register L	CTRL	16	16	2 or 3 PCLKB	2 ICLK
000A 8306h	RSCAN0	Control Register H	CTRH	16	16	2 or 3 PCLKB	2 ICLK
000A 8308h	RSCAN0	Status Register L	STSL	16	16	2 or 3 PCLKB	2 ICLK
000A 830Ah	RSCAN0	Status Register H	STSH	16	16	2 or 3 PCLKB	2 ICLK
000A 830Ch	RSCAN0	Error Flag Register L	ERFLL	16	16	2 or 3 PCLKB	2 ICLK
000A 830Eh	RSCAN0	Error Flag Register H	ERFLH	16	16	2 or 3 PCLKB	2 ICLK
000A 8322h	RSCAN	Global Configuration Register L	GCFGL	16	16	2 or 3 PCLKB	2 ICLK
000A 8324h	RSCAN	Global Configuration Register H	GCFGH	16	16	2 or 3 PCLKB	2 ICLK

Table 5.7 DC Characteristics (5)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item					Symbol	Typ. *4	Max.	Unit	Test Conditions
Supply current *1	High-speed operating mode	Normal operating mode	No peripheral operation*2	ICLK = 54 MHz	I_{CC}	6.5	—	mA	
				ICLK = 32 MHz		4.1	—		
				ICLK = 16 MHz		2.9	—		
				ICLK = 8 MHz		2.2	—		
				ICLK = 4 MHz		1.9	—		
			All peripheral operation: Normal	ICLK = 54 MHz*11		26.5	—		
				ICLK = 32 MHz*3		21.0	—		
				ICLK = 16 MHz*3		11.8	—		
				ICLK = 8 MHz*3		6.6	—		
				ICLK = 4 MHz*3		4.2	—		
			All peripheral operation: Max.	ICLK = 54 MHz*11		—	53.3		
				ICLK = 32 MHz*3		—	40.8		
			Increase due to operation of the Trusted Secure IP	PCLKB = 32 MHz		—	2		
		Sleep mode	No peripheral operation*2	ICLK = 54 MHz		3.5	—		
				ICLK = 32 MHz		2.4	—		
				ICLK = 16 MHz		1.9	—		
				ICLK = 8 MHz		1.6	—		
				ICLK = 4 MHz		1.5	—		
			All peripheral operation: Normal	ICLK = 54 MHz*11		13.4	—		
				ICLK = 32 MHz*3		12.5	—		
				ICLK = 16 MHz*3		7.3	—		
				ICLK = 8 MHz*3		4.6	—		
				ICLK = 4 MHz*3		3.3	—		
		Deep sleep mode	No peripheral operation*2	ICLK = 54 MHz		2.3	—		
				ICLK = 32 MHz		1.5	—		
				ICLK = 16 MHz		1.3	—		
				ICLK = 8 MHz		1.2	—		
				ICLK = 4 MHz		1.1	—		
			All peripheral operation: Normal	ICLK = 54 MHz*11		10.6	—		
				ICLK = 32 MHz*3		9.9	—		
				ICLK = 16 MHz*3		5.9	—		
				ICLK = 8 MHz*3		3.8	—		
				ICLK = 4 MHz*3		2.7	—		
		Increase during BGO operation*5				2.5	—		
	Middle-speed operating mode	Normal operating mode	No peripheral operation*6	ICLK = 12 MHz	I_{CC}	2.7	—	mA	
				ICLK = 8 MHz		1.8	—		
				ICLK = 4 MHz		1.4	—		
				ICLK = 1 MHz		1.1	—		
			All peripheral operation: Normal*7	ICLK = 12 MHz		9.6	—		
				ICLK = 8 MHz		6.2	—		
				ICLK = 4 MHz		3.8	—		
				ICLK = 1 MHz		2.3	—		

Table 5.13 DC Characteristics (11)

Conditions: 0 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Power-on VCC rising gradient	At normal startup*1	SrVCC	0.02	—	20	ms/V	
	During fast startup time*2		0.02	—	2		
	Voltage monitoring 0 reset enabled at startup*3, *4		0.02	—	—		

Note 1. When OFS1.(FASTSTUP, LVDAS) bits are 11b.
Note 2. When OFS1.(FASTSTUP, LVDAS) bits are 01b.
Note 3. When OFS1.LVDAS bit is 0.
Note 4. Turn on the power supply voltage according to the normal startup rising gradient because the settings in the OFS1 register are not read in boot mode.

Table 5.14 DC Characteristics (12)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

The ripple voltage must meet the allowable ripple frequency $f_{r\,(VCC)}$ within the range between the VCC upper limit and lower limit. When VCC change exceeds VCC ±10%, the allowable voltage change rising/falling gradient dt/dVCC must be met.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Allowable ripple frequency	$f_{r\,(VCC)}$	—	—	10	kHz	Figure 5.7 $V_{r\,(VCC)}$ ≤ VCC × 0.2
		—	—	1	MHz	Figure 5.7 $V_{r\,(VCC)}$ ≤ VCC × 0.08
		—	—	10	MHz	Figure 5.7 $V_{r\,(VCC)}$ ≤ VCC × 0.06
Allowable voltage change rising/falling gradient	dt/dVCC	1.0	—	—	ms/V	When VCC change exceeds VCC ±10%

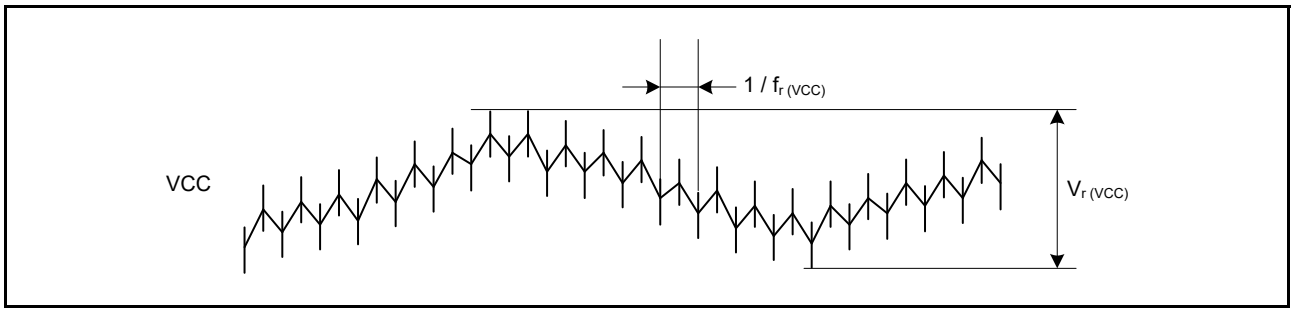


Figure 5.7 Ripple Waveform

Table 5.15 DC Characteristics (13)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Permissible error of VCL pin external capacitance	C_{VCL}	1.4	4.7	7.0	µF	

Note: The recommended capacitance is 4.7 µF. Variations in connected capacitors should be within the above range.

5.2.1 Normal I/O Pin Output Characteristics (1)

Figure 5.8 to Figure 5.12 show the characteristics when normal output is selected by the drive capacity control register.

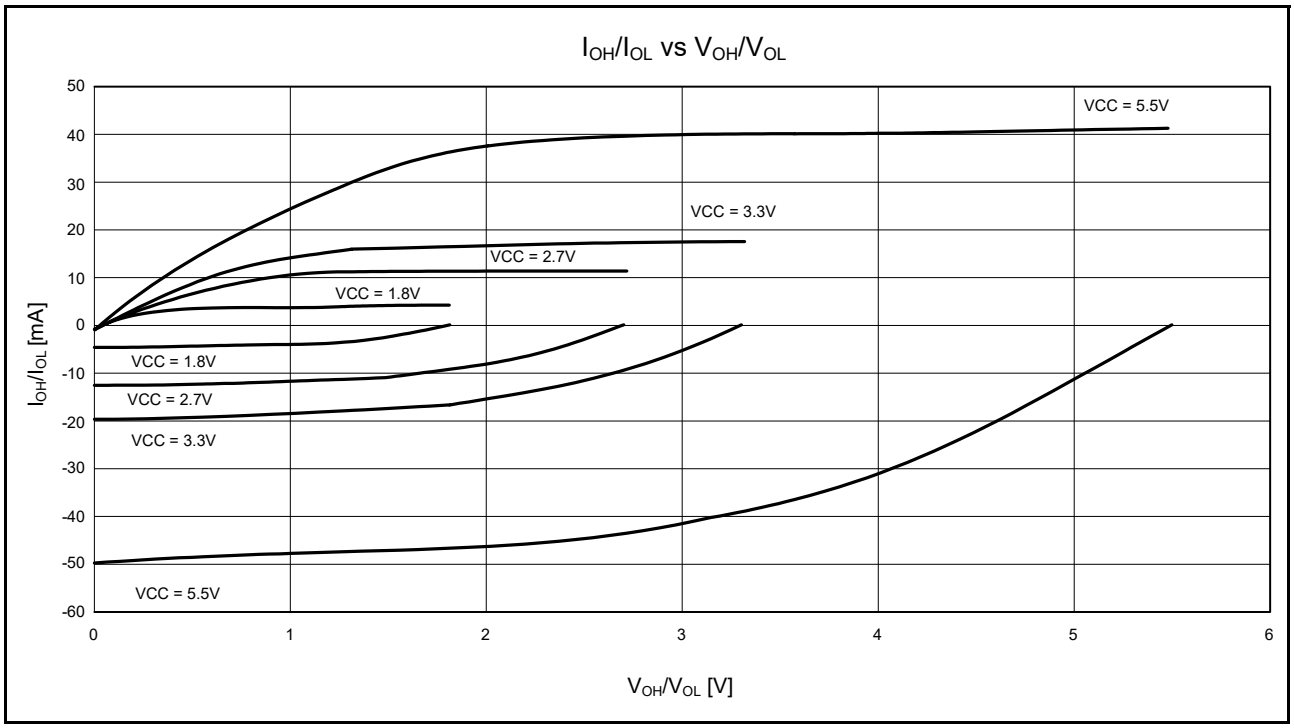


Figure 5.8 V_{OH}/V_{OL} and I_{OH}/I_{OL} Voltage Characteristics at T_a = 25°C When Normal Output is Selected (Reference Data)

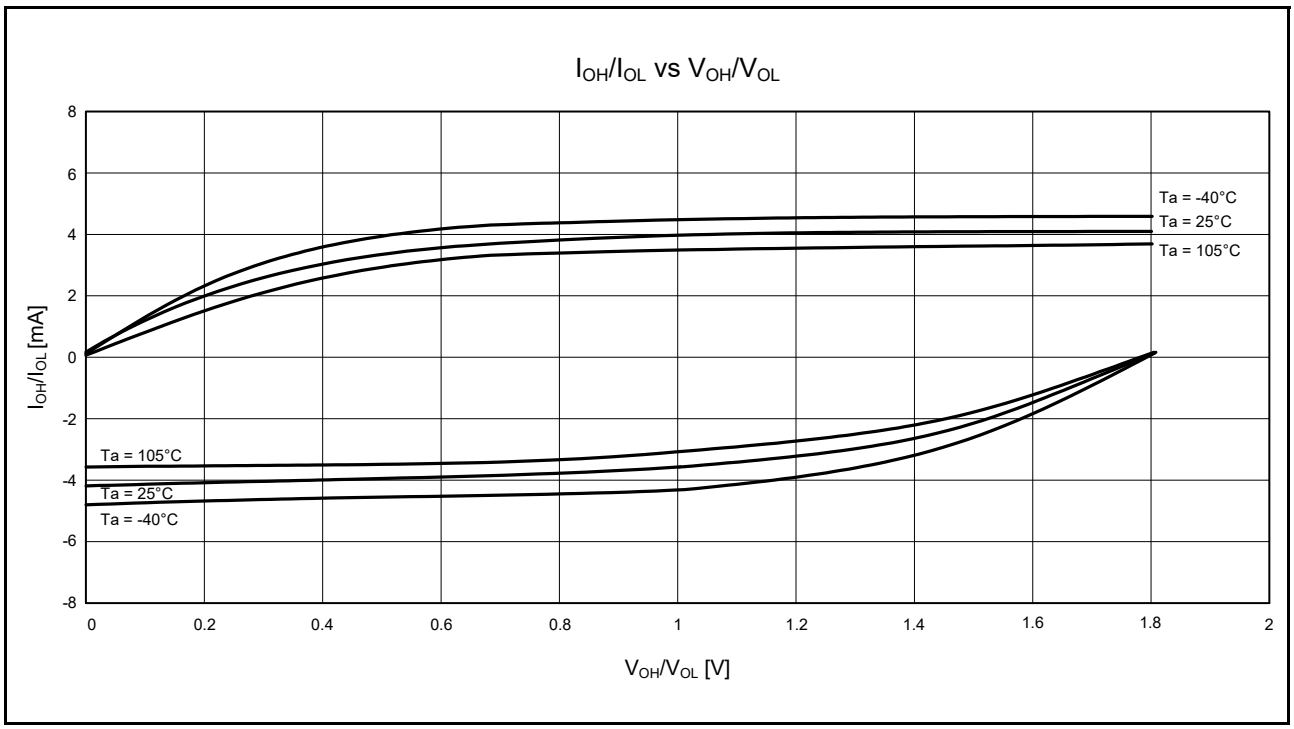


Figure 5.9 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 1.8 V When Normal Output is Selected (Reference Data)

5.2.3 Normal I/O Pin Output Characteristics (3)

Figure 5.18 to Figure 5.21 show the characteristics of the RIIC output pin.

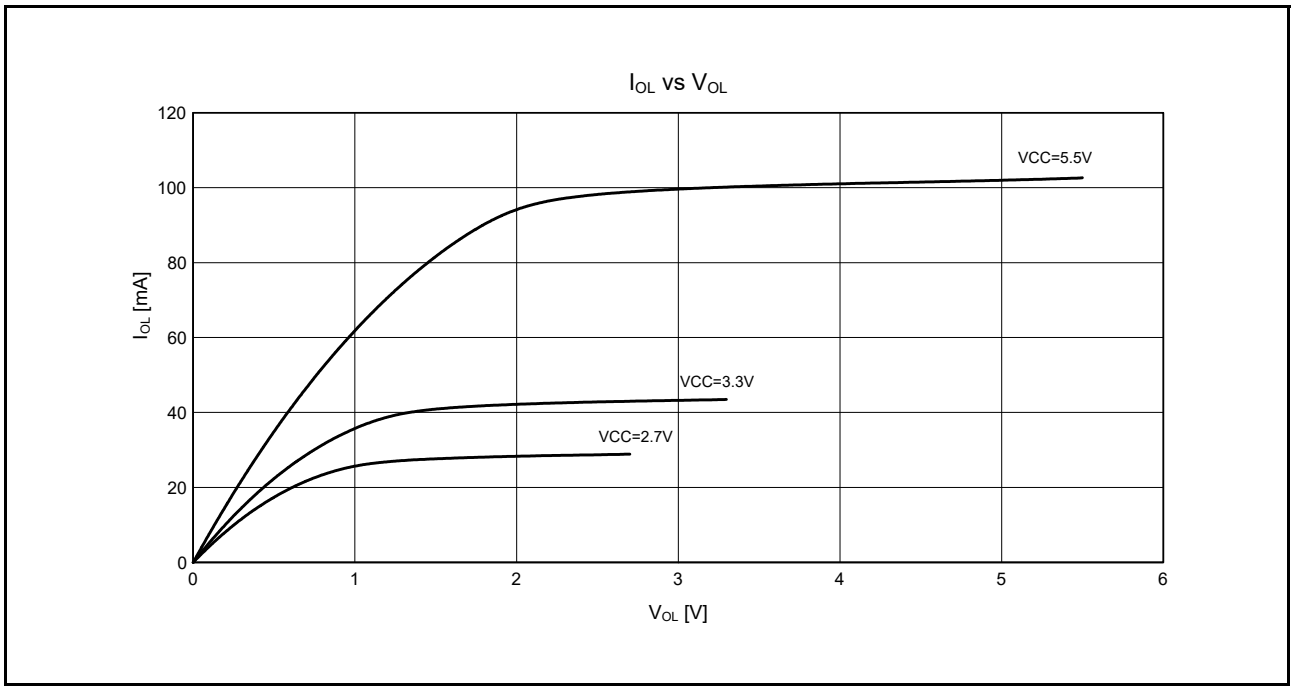


Figure 5.18 V_{OL} and I_{OL} Voltage Characteristics of RIIC Output Pin at T_a = 25°C (Reference Data)

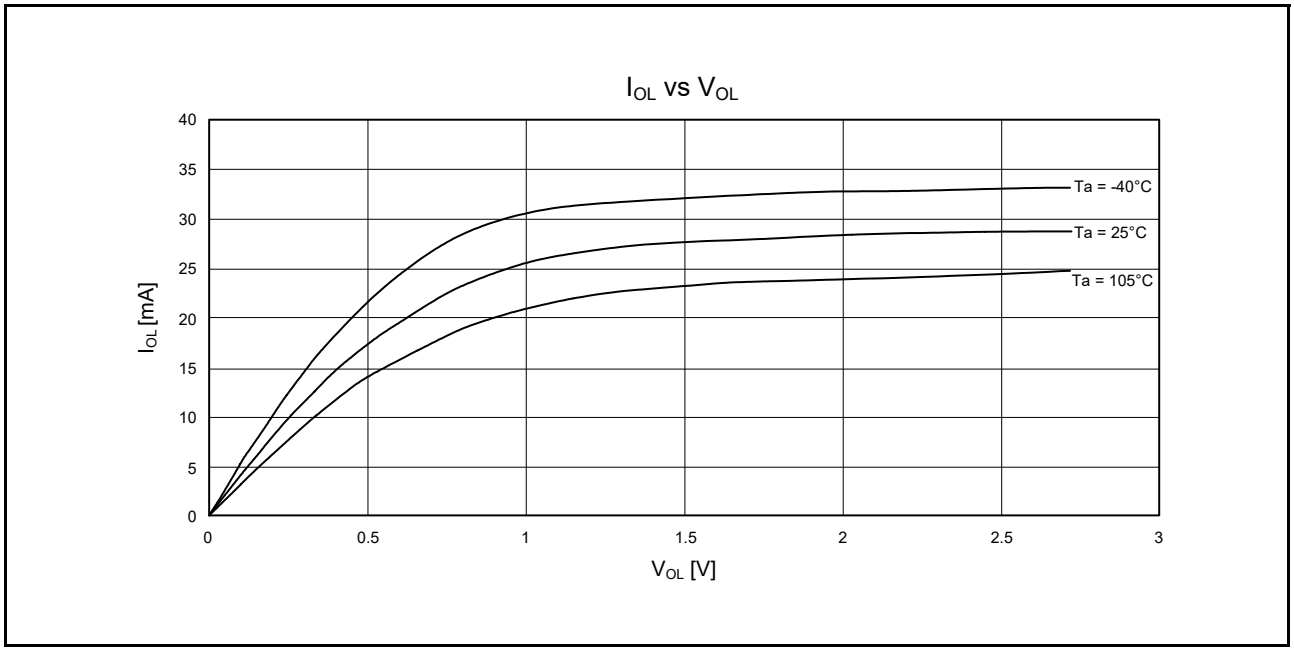


Figure 5.19 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at VCC = 2.7 V (Reference Data)

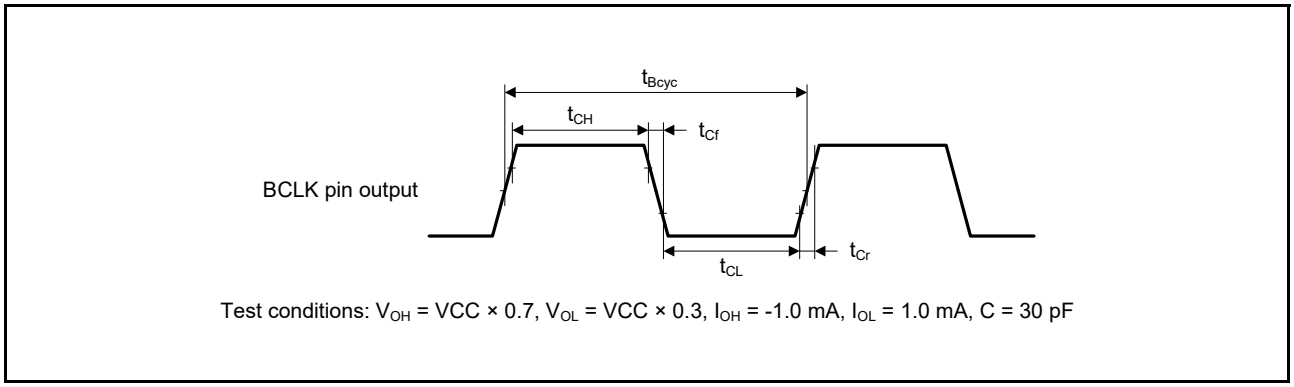


Figure 5.22 BCLK Pin Output Timing

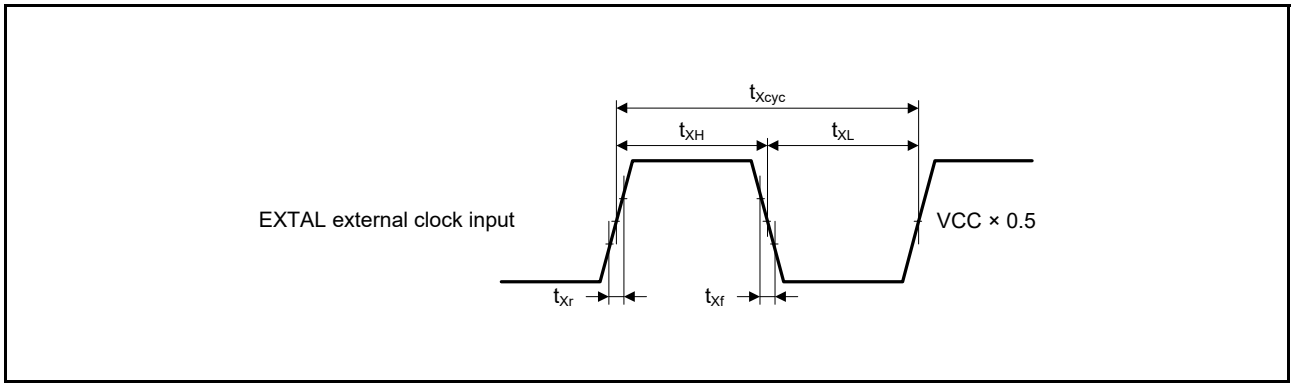


Figure 5.23 EXTAL External Clock Input Timing

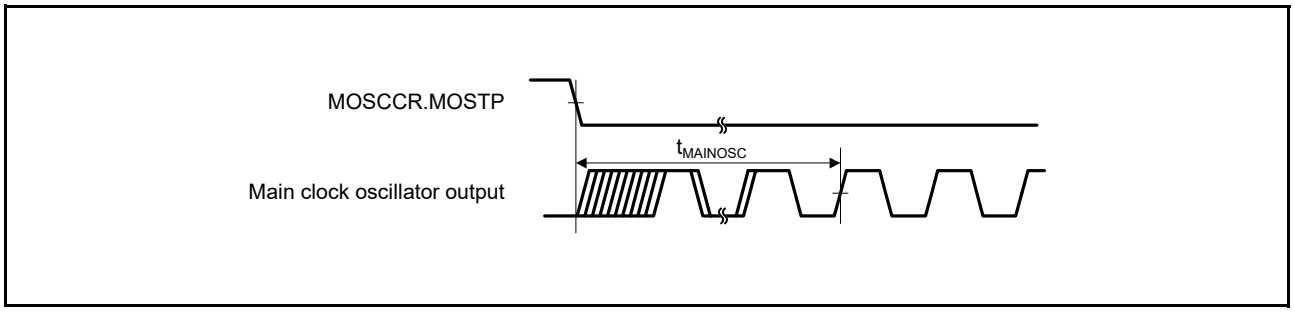


Figure 5.24 Main Clock Oscillation Start Timing

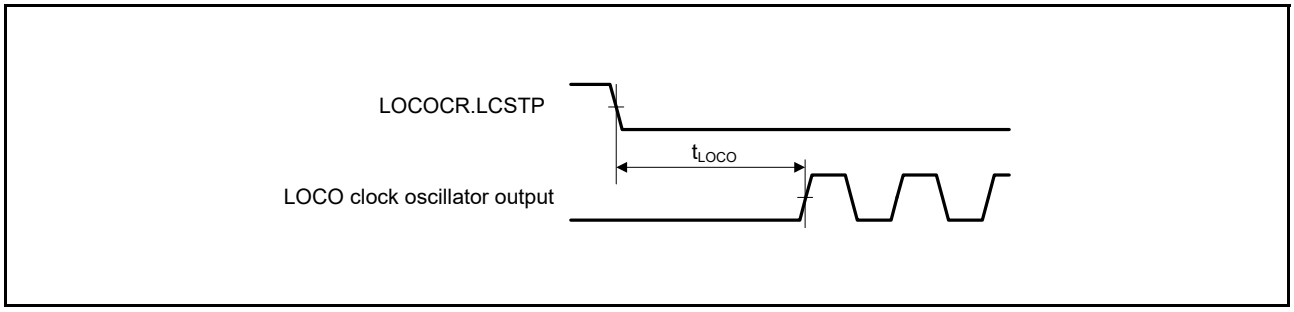


Figure 5.25 LOCO Clock Oscillation Start Timing

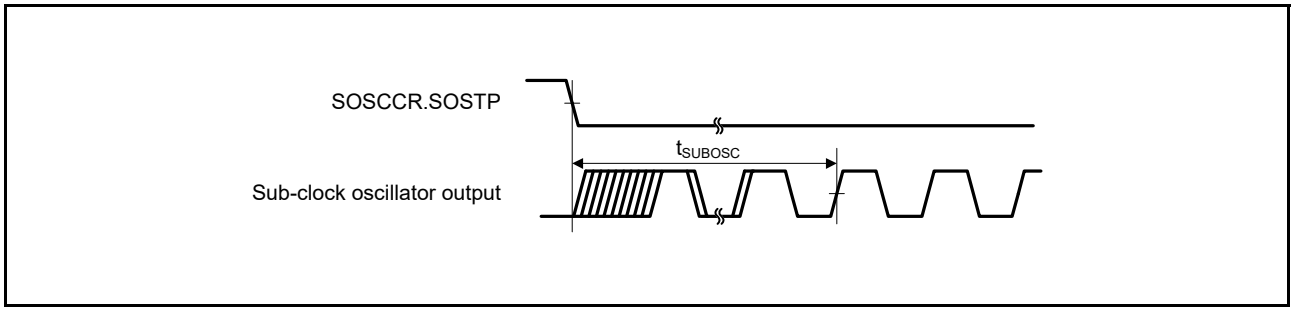


Figure 5.30 Sub-Clock Oscillation Start Timing

Table 5.30 Timing of Recovery from Low Power Consumption Modes (3)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VREFL0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from software standby mode*1	Low-speed mode	Sub-clock oscillator operating	t_{SBYSC}	—	600	750	µs	Figure 5.34

Note 1. The sub-clock continues oscillating in software standby mode during low-speed mode.

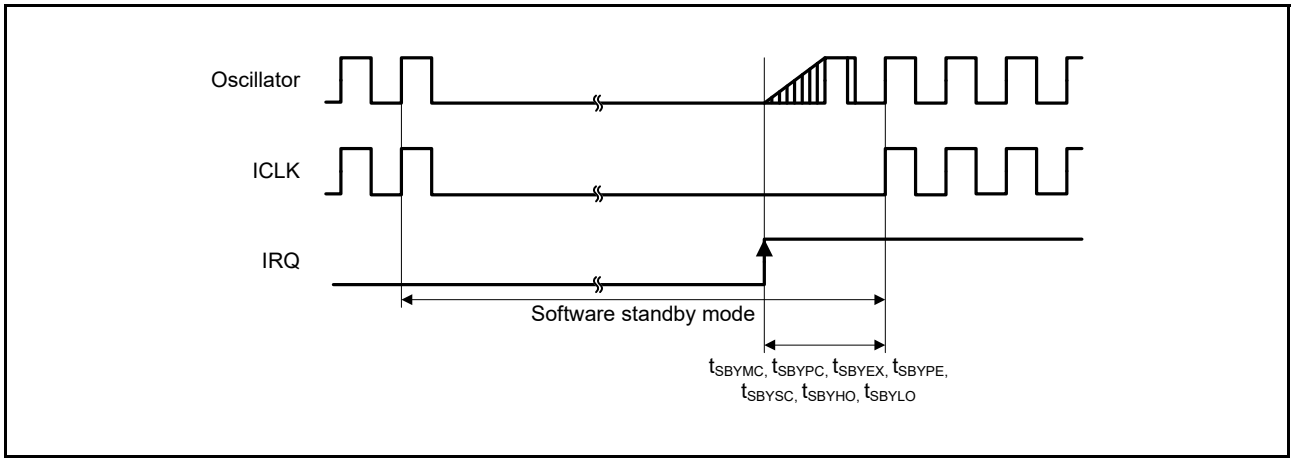


Figure 5.34 Software Standby Mode Recovery Timing

Table 5.31 Timing of Recovery from Low Power Consumption Modes (4)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VREFL0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from deep sleep mode*1	High-speed mode*2	t_{DSLP}	—	2	3.5	µs	Figure 5.35
	Middle-speed mode*3	t_{DSLP}	—	3	4	µs	
	Low-speed mode*4	t_{DSLP}	—	400	500	µs	

Note 1. Oscillators continue oscillating in deep sleep mode.
Note 2. When the frequency of the system clock is 32 MHz.
Note 3. When the frequency of the system clock is 12 MHz.
Note 4. When the frequency of the system clock is 32 kHz.

5.4 USB Characteristics

Table 5.45 USB Characteristics (USB0_DP and USB0_DM Pin Characteristics)

Conditions: 3.0 V ≤ VCC = VCC_USB = AVCC < 3.6 V (when a regulator is not in use) or 4.0 V ≤ VCC = AVCC0 < 5.5 V (when a regulator is in use), VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
Input characteristics	Input high level voltage		V_{IH}	2.0	—	V	
	Input low level voltage		V_{IL}	—	0.8	V	
	Differential input sensitivity		V_{DI}	0.2	—	V	| USB0_DP – USB0_DM |
	Differential common mode range		V_{CM}	0.8	2.5	V	
Output characteristics	Output high level voltage		V_{OH}	2.8	VCC_USB	V	I_{OH} = –200 µA
	Output low level voltage		V_{OL}	0.0	0.3	V	I_{OL} = 2 mA
	Cross-over voltage		V_{CRS}	1.3	2.0	V	Figure 5.65, Figure 5.66
	Rise time	FS	t_r	4	20	ns	
		LS		75	300		
	Fall time	FS	t_f	4	20	ns	
		LS		75	300		
	Rise/fall time ratio	FS	t_r/t_f	90	111.11	%	t_r/t_f
		LS		80	125		
	Output resistance		Z_{DRV}	28	44	Ω	(Adjusting the resistance by external elements is not necessary.)
VBUS characteristics	VBUS input voltage		V_{IH}	VCC × 0.8	—	V	
			V_{IL}	—	VCC × 0.2	V	
Pull-up, pull-down	Pull-down resistor		R_{PD}	14.25	24.80	kΩ	
	Pull-up resistor		R_{PUI}	0.9	1.575	kΩ	During idle state
			R_{PUA}	1.425	3.09	kΩ	During reception
Battery Charging Specification Ver 1.2	D+ sink current		I_{DP_SINK}	25	175	µA	
	D- sink current		I_{DM_SINK}	25	175	µA	
	DCD source current		I_{DP_SRC}	7	13	µA	
	Data detection voltage		V_{DAT_REF}	0.25	0.4	V	
	D+ source current		V_{DP_SRC}	0.5	0.7	V	Output current = 250 µA
	D- source current		V_{DM_SRC}	0.5	0.7	V	Output current = 250 µA

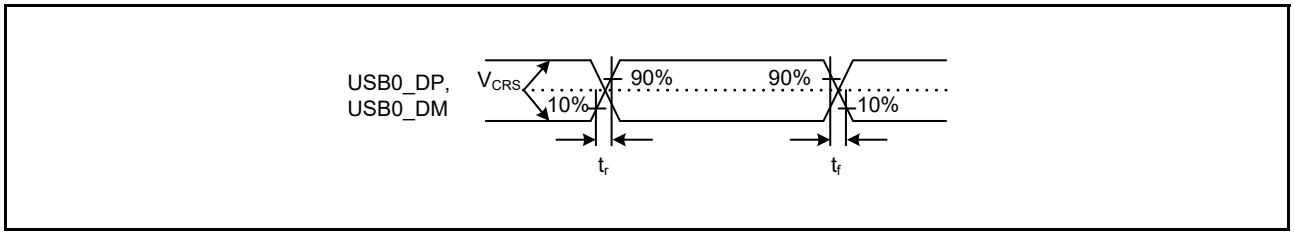


Figure 5.65 USB0_DP and USB0_DM Output Timing

Table 5.47 A/D Conversion Characteristics (2)

Conditions: 2.4 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, 2.4 V ≤ VREFH0 ≤ AVCC0, reference voltage = VREFH0 selected, VSS = AVSS0 = VREFL0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	32	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 32 MHz)	Permissible signal source impedance (Max.) = 1.3 kΩ	1.41	—	—	μs	High-precision channel The ADCSR.ADHSC bit is 0 The ADSSTRn register is 0Dh
		2.25	—	—		Normal-precision channel The ADCSR.ADHSC bit is 0 The ADSSTRn register is 28h
Analog input capacitance	Cs	—	—	15	pF	Pin capacitance included Figure 5.68
Analog input resistance	Rs	—	—	2.5	kΩ	Figure 5.68
Offset error		—	±0.5	±4.5	LSB	
Full-scale error		—	±0.75	±4.5	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential non-linearity error		—	±1.0	—	LSB	
INL integral non-linearity error		—	±1.0	±4.5	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential non-linearity error, and INL integral non-linearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

5.9 CTSU Characteristics

Table 5.57 CTSU Characteristics

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
External capacitance connected to TSCAP pin	C_{tscap}	9	10	11	nF	
TS pin capacitive load	C_{base}	—	—	50	pF	
Permissible output high current	ΣI_{OH}	—	—	–24	mA	When the mutual capacitance method is applied

5.10 Characteristics of Power-On Reset Circuit and Voltage Detection Circuit

Table 5.58 Characteristics of Power-On Reset Circuit and Voltage Detection Circuit (1)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V_{POR}	1.35	1.50	1.65	V	Figure 5.73, Figure 5.74
	Voltage detection circuit (LVD0)*1	V_{det0_0}	3.67	3.84	3.97	V	Figure 5.75 At falling edge VCC
		V_{det0_1}	2.70	2.82	3.00		
		V_{det0_2}	2.37	2.51	2.67		
		V_{det0_3}	1.80	1.90	1.99		
	Voltage detection circuit (LVD1)*2	V_{det1_0}	4.12	4.29	4.42	V	Figure 5.76 At falling edge VCC
		V_{det1_1}	3.98	4.14	4.28		
		V_{det1_2}	3.86	4.02	4.16		
		V_{det1_3}	3.68	3.84	3.98		
		V_{det1_4}	2.99	3.10	3.29		
		V_{det1_5}	2.89	3.00	3.19		
		V_{det1_6}	2.79	2.90	3.09		
		V_{det1_7}	2.68	2.79	2.98		
		V_{det1_8}	2.57	2.68	2.87		
		V_{det1_9}	2.47	2.58	2.67		
		V_{det1_A}	2.37	2.48	2.57		
		V_{det1_B}	2.10	2.20	2.30		
		V_{det1_C}	1.86	1.96	2.06		
		V_{det1_D}	1.80	1.86	1.96		
	Voltage detection circuit (LVD2)*3	V_{det2_0}	4.08	4.29	4.48	V	Figure 5.77 At falling edge VCC
		V_{det2_1}	3.95	4.14	4.35		
		V_{det2_2}	3.82	4.02	4.22		
		V_{det2_3}	3.62	3.84	4.02		

Note: These characteristics apply when noise is not superimposed on the power supply. When a setting is made so that the voltage detection level overlaps with that of the voltage detection circuit (LVD2), it cannot be specified which of LVD1 and LVD2 is used for voltage detection.

Note 1. n in the symbol Vdet0_n denotes the value of the OFS1.VDSEL[1:0] bits.

Note 2. n in the symbol Vdet1_n denotes the value of the LVDLVLR.LVD1LVL[3:0] bits.

Note 3. n in the symbol Vdet2_n denotes the value of the LVDLVLR.LVD2LVL[1:0] bits.

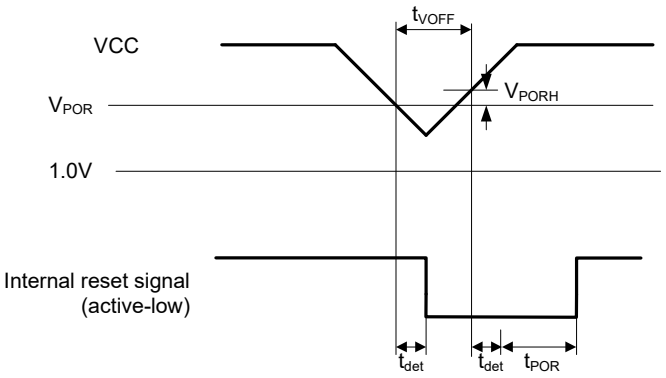
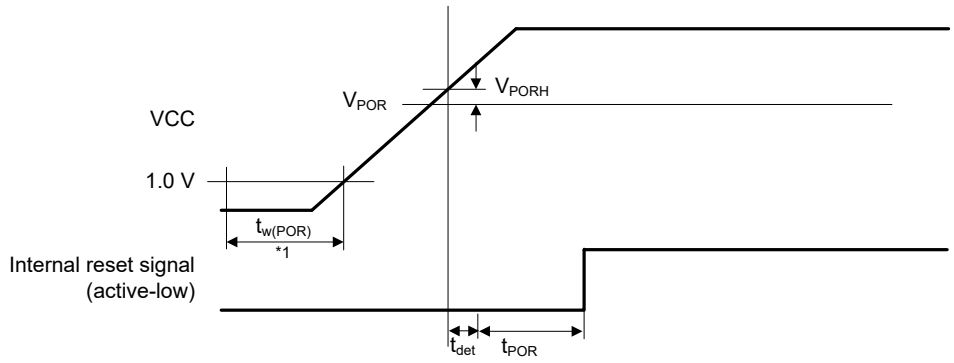


Figure 5.73 Voltage Detection Reset Timing



Note 1. $t_{w(POR)}$ is the time required for a power-on reset to be enabled while the external power VCC is being held below the valid voltage (1.0 V).
When turning the VCC on, maintain a voltage below 1.0V for at least 1.0ms.

Figure 5.74 Power-On Reset Timing

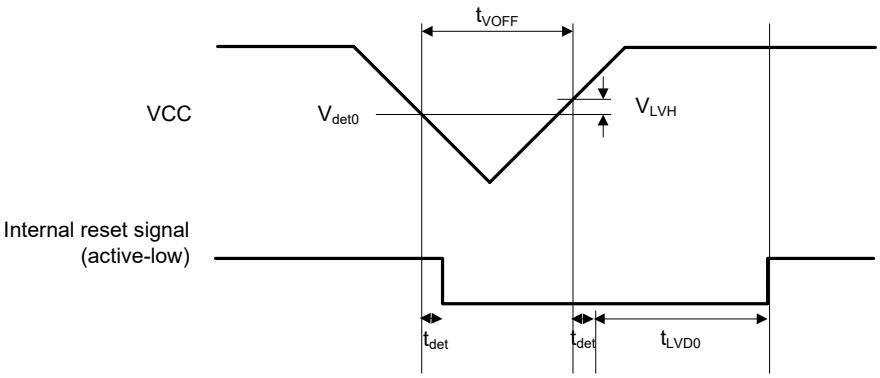
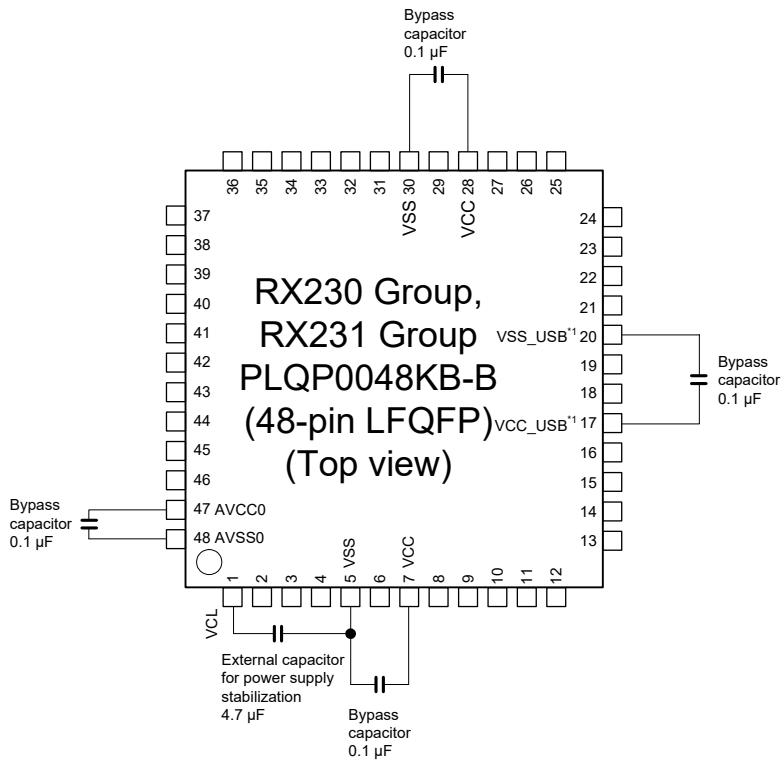


Figure 5.75 Voltage Detection Circuit Timing (Vdet0)

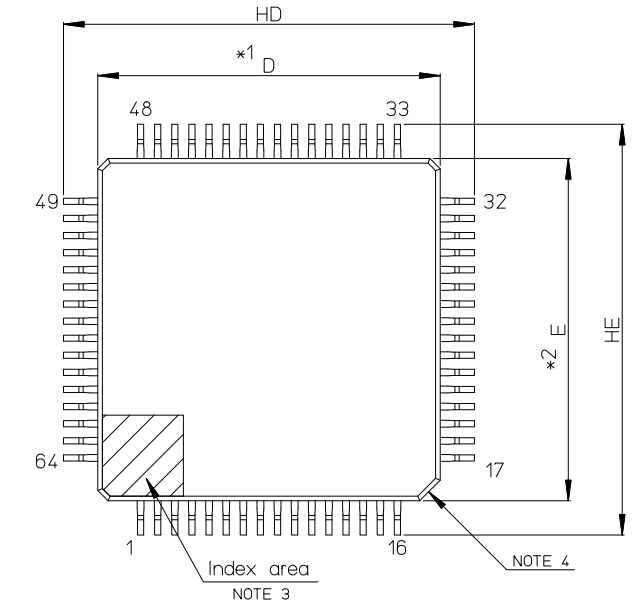


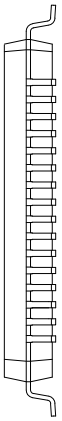
Note: Do not apply the power supply voltage to the VCL pin.
Use a 4.7-µF multilayer ceramic capacitor for the VCL pin and place it close to the pin.
A recommended value is shown for the capacitance of the bypass capacitors.

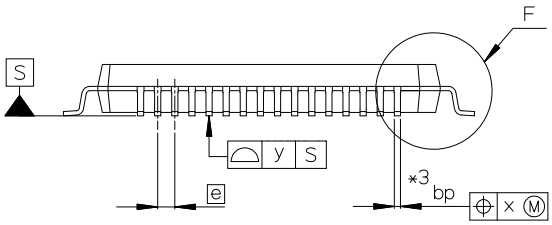
Note 1. As the products of the RX230 group do not have VCC_USB or VSS_USB, a bypass capacitor is not required.

Figure 5.82 Connecting Capacitors (48 Pins)

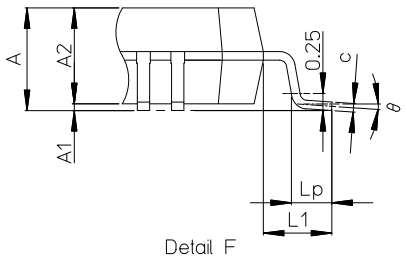
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP64-10x10-0.50	PLQP0064KB-C	——	0.3g







NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL; SIZE MAY VARY.



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A2	——	1.4	——
HD	11.8	12.0	12.2
HE	11.8	12.0	12.2
A	——	——	1.7
A1	0.05	——	0.15
bp	0.15	0.20	0.27
c	0.09	——	0.20
θ	0°	3.5°	8°
e	——	0.5	——
x	——	——	0.08
y	——	——	0.08
Lp	0.45	0.6	0.75
L1	——	1.0	——

Figure E 64 -Pin LFQFP (PLQP0064KB-C)