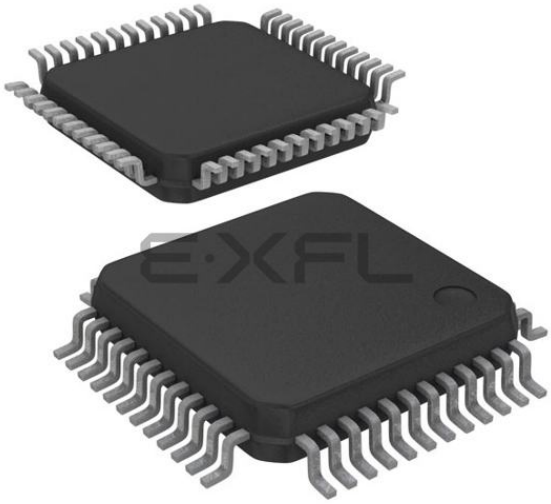

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

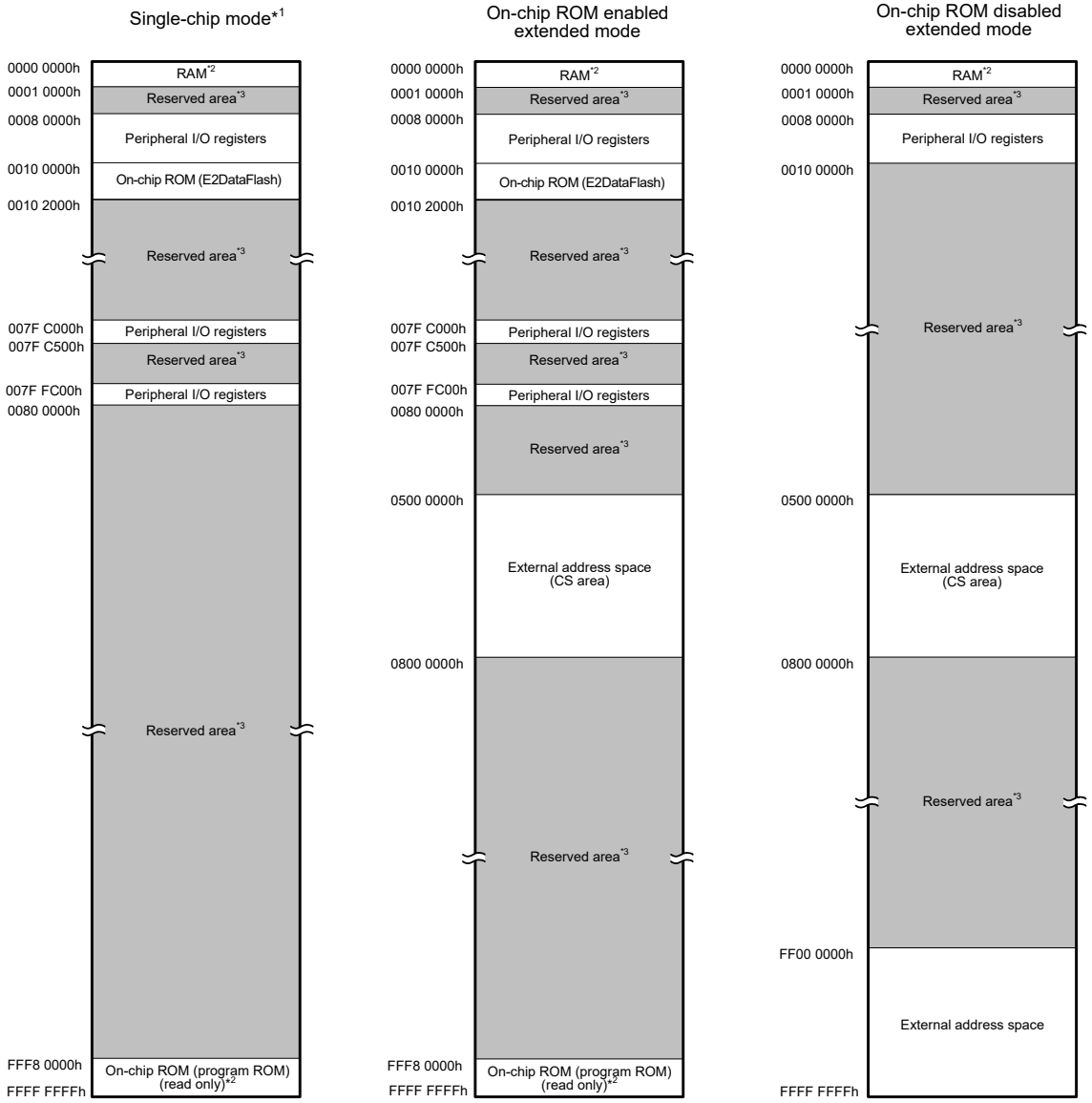
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	54MHz
Connectivity	I²C, IrDA, SCI, SD/SDIO, SPI, SSI, USB OTG
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	30
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LFQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f52316cdfl-30

Table 1.7 List of Pins and Pin Functions (100-Pin LFQFP) (3/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCI, RSPI, RIIC, RSCAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
79		PD7	D7[A7/D7]	MTIC5U/POE0#				IRQ7/AN031
80		PD6	D6[A6/D6]	MTIC5V/POE1#				IRQ6/AN030
81		PD5	D5[A5/D5]	MTIC5W/POE2#				IRQ5/AN029
82		PD4	D4[A4/D4]	POE3#				IRQ4/AN028
83		PD3	D3[A3/D3]	POE8#				IRQ3/AN027
84		PD2	D2[A2/D2]	MTIOC4D				IRQ2/AN026
85		PD1	D1[A1/D1]	MTIOC4B				IRQ1/AN025
86		PD0	D0[A0/D0]					IRQ0/AN024
87		P47						AN007
88		P46						AN006
89		P45						AN005
90		P44						AN004
91		P43						AN003
92		P42						AN002
93		P41						AN001
94	VREFL0							
95		P40						AN000
96	VREFH0							
97	AVCC0							
98		P07						ADTRG0#
99	AVSS0							
100		P05						DA1

Note 1. RX230: PH0/CACREF, PH1/IRQ0/TMO0, PH2/IRQ1/TMRI0, PH3/TMCI0
RX231: VSS_USB, USB0_DP, USB0_DM, VCC_USB



Note 1. The address space in boot mode and USB boot mode is the same as the address space in single-chip mode.
Note 2. The capacity of ROM/RAM differs depending on the products.

ROM (bytes)		RAM (bytes)	
Capacity	**Address**	**Capacity**	**Address**
512 Kbytes	FFF8 0000h to FFFF FFFFh	64 Kbytes	0000 0000h to 0000 FFFFh
384 Kbytes	FFFA 0000h to FFFF FFFFh		
256 Kbytes	FFFC 0000h to FFFF FFFFh	32 Kbytes	0000 0000h to 0000 7FFFh
128 Kbytes	FFFE 0000h to FFFF FFFFh		

Note: See Table 1.3 and Table 1.4 List of Products, for the product type name.

Note 3. Reserved areas should not be accessed.

Figure 3.1 Memory Map in Each Operating Mode

Table 4.1 List of I/O Registers (Address Order) (7/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK <PCLK
0008 830Dh	RIIC0	Slave Address Register U1	SARU1	8	8	2 or 3 PCLKB	2 ICLK
0008 830Eh	RIIC0	Slave Address Register L2	SARL2	8	8	2 or 3 PCLKB	2 ICLK
0008 830Fh	RIIC0	Slave Address Register U2	SARU2	8	8	2 or 3 PCLKB	2 ICLK
0008 8310h	RIIC0	I²C-Bus Bit Rate Low-Level Register	ICBRL	8	8	2 or 3 PCLKB	2 ICLK
0008 8311h	RIIC0	I²C-Bus Bit Rate High-Level Register	ICBRH	8	8	2 or 3 PCLKB	2 ICLK
0008 8312h	RIIC0	I²C-Bus Transmit Data Register	ICDRT	8	8	2 or 3 PCLKB	2 ICLK
0008 8313h	RIIC0	I²C-Bus Receive Data Register	ICDRR	8	8	2 or 3 PCLKB	2 ICLK
0008 8380h	RSPI0	RSPI Control Register	SPCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8381h	RSPI0	RSPI Slave Select Polarity Register	SSLP	8	8	2 or 3 PCLKB	2 ICLK
0008 8382h	RSPI0	RSPI Pin Control Register	SPPCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8383h	RSPI0	RSPI Status Register	SPSR	8	8	2 or 3 PCLKB	2 ICLK
0008 8384h	RSPI0	RSPI Data Register	SPDR	32	16, 32	2 or 3 PCLKB	2 ICLK
0008 8388h	RSPI0	RSPI Sequence Control Register	SPSCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8389h	RSPI0	RSPI Sequence Status Register	SPSSR	8	8	2 or 3 PCLKB	2 ICLK
0008 838Ah	RSPI0	RSPI Bit Rate Register	SPBR	8	8	2 or 3 PCLKB	2 ICLK
0008 838Bh	RSPI0	RSPI Data Control Register	SPDCR	8	8	2 or 3 PCLKB	2 ICLK
0008 838Ch	RSPI0	RSPI Clock Delay Register	SPCKD	8	8	2 or 3 PCLKB	2 ICLK
0008 838Dh	RSPI0	RSPI Slave Select Negation Delay Register	SSLND	8	8	2 or 3 PCLKB	2 ICLK
0008 838Eh	RSPI0	RSPI Next-Access Delay Register	SPND	8	8	2 or 3 PCLKB	2 ICLK
0008 838Fh	RSPI0	RSPI Control Register 2	SPCR2	8	8	2 or 3 PCLKB	2 ICLK
0008 8390h	RSPI0	RSPI Command Register 0	SPCMD0	16	16	2 or 3 PCLKB	2 ICLK
0008 8392h	RSPI0	RSPI Command Register 1	SPCMD1	16	16	2 or 3 PCLKB	2 ICLK
0008 8394h	RSPI0	RSPI Command Register 2	SPCMD2	16	16	2 or 3 PCLKB	2 ICLK
0008 8396h	RSPI0	RSPI Command Register 3	SPCMD3	16	16	2 or 3 PCLKB	2 ICLK
0008 8398h	RSPI0	RSPI Command Register 4	SPCMD4	16	16	2 or 3 PCLKB	2 ICLK
0008 839Ah	RSPI0	RSPI Command Register 5	SPCMD5	16	16	2 or 3 PCLKB	2 ICLK
0008 839Ch	RSPI0	RSPI Command Register 6	SPCMD6	16	16	2 or 3 PCLKB	2 ICLK
0008 839Eh	RSPI0	RSPI Command Register 7	SPCMD7	16	16	2 or 3 PCLKB	2 ICLK
0008 8410h	IRDA	IrDA Control Register	IRCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8900h	POE	Input Level Control/Status Register 1	ICSR1	16	8, 16	2 or 3 PCLKB	2 ICLK
0008 8902h	POE	Output Level Control/Status Register 1	OCSR1	16	8, 16	2 or 3 PCLKB	2 ICLK
0008 8908h	POE	Input Level Control/Status Register 2	ICSR2	16	8, 16	2 or 3 PCLKB	2 ICLK
0008 890Ah	POE	Software Port Output Enable Register	SPOER	8	8	2 or 3 PCLKB	2 ICLK
0008 890Bh	POE	Port Output Enable Control Register 1	POECR1	8	8	2 or 3 PCLKB	2 ICLK
0008 890Ch	POE	Port Output Enable Control Register 2	POECR2	8	8	2 or 3 PCLKB	2 ICLK
0008 890Eh	POE	Input Level Control/Status Register 3	ICSR3	16	8, 16	2 or 3 PCLKB	2 ICLK
0008 9000h	S12AD	A/D Control Register	ADCSR	16	16	2 or 3 PCLKB	2 ICLK
0008 9004h	S12AD	A/D Channel Select Register A0	ADANSA0	16	16	2 or 3 PCLKB	2 ICLK
0008 9006h	S12AD	A/D Channel Select Register A1	ADANSA1	16	16	2 or 3 PCLKB	2 ICLK
0008 9008h	S12AD	A/D-Converted Value Addition/Average Function Select Register 0	ADADS0	16	16	2 or 3 PCLKB	2 ICLK
0008 900Ah	S12AD	A/D-Converted Value Addition/Average Function Select Register 1	ADADS1	16	16	2 or 3 PCLKB	2 ICLK
0008 900Ch	S12AD	A/D-Converted Value Addition/Average Count Select Register	ADADC	8	8	2 or 3 PCLKB	2 ICLK
0008 900Eh	S12AD	A/D Control Extended Register	ADCER	16	16	2 or 3 PCLKB	2 ICLK
0008 9010h	S12AD	A/D Conversion Start Trigger Select Register	ADSTRGR	16	16	2 or 3 PCLKB	2 ICLK
0008 9012h	S12AD	A/D Conversion Extended Input Control Register	ADEXICR	16	16	2 or 3 PCLKB	2 ICLK
0008 9014h	S12AD	A/D Channel Select Register B0	ADANSB0	16	16	2 or 3 PCLKB	2 ICLK
0008 9016h	S12AD	A/D Channel Select Register B1	ADANSB1	16	16	2 or 3 PCLKB	2 ICLK
0008 9018h	S12AD	A/D Data Duplication Register	ADDBLDR	16	16	2 or 3 PCLKB	2 ICLK
0008 901Ah	S12AD	A/D Temperature Sensor Data Register	ADTSDR	16	16	2 or 3 PCLKB	2 ICLK
0008 901Ch	S12AD	A/D Internal Reference Voltage Data Register	ADOCDR	16	16	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (9/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK <PCLK
0008 90AAh	S12AD	A/D Compare Function Window B Upper-Side Level Setting Register	ADWINULB	16	16	2 or 3 PCLKB	2 ICLK
0008 90ACh	S12AD	A/D Compare Function Window B Channel Status Register	ADCMPBSR	8	8	2 or 3 PCLKB	2 ICLK
0008 90B0h	S12AD	A/D Data Storage Buffer Register 0	ADBUF0	16	16	2 or 3 PCLKB	2 ICLK
0008 90B2h	S12AD	A/D Data Storage Buffer Register 1	ADBUF1	16	16	2 or 3 PCLKB	2 ICLK
0008 90B4h	S12AD	A/D Data Storage Buffer Register 2	ADBUF2	16	16	2 or 3 PCLKB	2 ICLK
0008 90B6h	S12AD	A/D Data Storage Buffer Register 3	ADBUF3	16	16	2 or 3 PCLKB	2 ICLK
0008 90B8h	S12AD	A/D Data Storage Buffer Register 4	ADBUF4	16	16	2 or 3 PCLKB	2 ICLK
0008 90BAh	S12AD	A/D Data Storage Buffer Register 5	ADBUF5	16	16	2 or 3 PCLKB	2 ICLK
0008 90BCh	S12AD	A/D Data Storage Buffer Register 6	ADBUF6	16	16	2 or 3 PCLKB	2 ICLK
0008 90BEh	S12AD	A/D Data Storage Buffer Register 7	ADBUF7	16	16	2 or 3 PCLKB	2 ICLK
0008 90C0h	S12AD	A/D Data Storage Buffer Register 8	ADBUF8	16	16	2 or 3 PCLKB	2 ICLK
0008 90C2h	S12AD	A/D Data Storage Buffer Register 9	ADBUF9	16	16	2 or 3 PCLKB	2 ICLK
0008 90C4h	S12AD	A/D Data Storage Buffer Register 10	ADBUF10	16	16	2 or 3 PCLKB	2 ICLK
0008 90C6h	S12AD	A/D Data Storage Buffer Register 11	ADBUF11	16	16	2 or 3 PCLKB	2 ICLK
0008 90C8h	S12AD	A/D Data Storage Buffer Register 12	ADBUF12	16	16	2 or 3 PCLKB	2 ICLK
0008 90CAh	S12AD	A/D Data Storage Buffer Register 13	ADBUF13	16	16	2 or 3 PCLKB	2 ICLK
0008 90CCh	S12AD	A/D Data Storage Buffer Register 14	ADBUF14	16	16	2 or 3 PCLKB	2 ICLK
0008 90CEh	S12AD	A/D Data Storage Buffer Register 15	ADBUF15	16	16	2 or 3 PCLKB	2 ICLK
0008 90D0h	S12AD	A/D Data Storage Buffer Enable Register	ADBUFEN	8	8	2 or 3 PCLKB	2 ICLK
0008 90D2h	S12AD	A/D Data Storage Buffer Pointer Register	ADBUFPTR	8	8	2 or 3 PCLKB	2 ICLK
0008 90DDh	S12AD	A/D Sampling State Register L	ADSSTRL	8	8	2 or 3 PCLKB	2 ICLK
0008 90DEh	S12AD	A/D Sampling State Register T	ADSSTRT	8	8	2 or 3 PCLKB	2 ICLK
0008 90DFh	S12AD	A/D Sampling State Register O	ADSSTRO	8	8	2 or 3 PCLKB	2 ICLK
0008 90E0h	S12AD	A/D Sampling State Register 0	ADSSTR0	8	8	2 or 3 PCLKB	2 ICLK
0008 90E1h	S12AD	A/D Sampling State Register 1	ADSSTR1	8	8	2 or 3 PCLKB	2 ICLK
0008 90E2h	S12AD	A/D Sampling State Register 2	ADSSTR2	8	8	2 or 3 PCLKB	2 ICLK
0008 90E3h	S12AD	A/D Sampling State Register 3	ADSSTR3	8	8	2 or 3 PCLKB	2 ICLK
0008 90E4h	S12AD	A/D Sampling State Register 4	ADSSTR4	8	8	2 or 3 PCLKB	2 ICLK
0008 90E5h	S12AD	A/D Sampling State Register 5	ADSSTR5	8	8	2 or 3 PCLKB	2 ICLK
0008 90E6h	S12AD	A/D Sampling State Register 6	ADSSTR6	8	8	2 or 3 PCLKB	2 ICLK
0008 90E7h	S12AD	A/D Sampling State Register 7	ADSSTR7	8	8	2 or 3 PCLKB	2 ICLK
0008 A000h	SCI0	Serial Mode Register	SMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A001h	SCI0	Bit Rate Register	BRR	8	8	2 or 3 PCLKB	2 ICLK
0008 A002h	SCI0	Serial Control Register	SCR	8	8	2 or 3 PCLKB	2 ICLK
0008 A003h	SCI0	Transmit Data Register	TDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A004h	SCI0	Serial Status Register	SSR	8	8	2 or 3 PCLKB	2 ICLK
0008 A005h	SCI0	Receive Data Register	RDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A006h	SCI0	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A007h	SCI0	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A008h	SCI0	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB	2 ICLK
0008 A009h	SCI0	I^2C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB	2 ICLK
0008 A00Ah	SCI0	I^2C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB	2 ICLK
0008 A00Bh	SCI0	I^2C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB	2 ICLK
0008 A00Ch	SCI0	I^2C Status Register	SISR	8	8	2 or 3 PCLKB	2 ICLK
0008 A00Dh	SCI0	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A00Eh	SCI0	Transmit Data Register HL	TDRHL	16	16	4 or 5 PCLKB	2 ICLK
0008 A00Eh	SCI0	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB	2 ICLK
0008 A00Fh	SCI0	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB	2 ICLK
0008 A010h	SCI0	Receive Data Register HL	RDRHL	16	16	4 or 5 PCLKB	2 ICLK
0008 A010h	SCI0	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB	2 ICLK
0008 A011h	SCI0	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (31/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK <PCLK
000A 862Eh	RSCAN	RAM Test Register 87	RPGACC87	16	16	2 or 3 PCLKB	2 ICLK
000A 8630h	RSCAN0	Transmit Buffer Register 3AL	TMIDL3	16	16	2 or 3 PCLKB	2 ICLK
000A 8630h	RSCAN	RAM Test Register 88	RPGACC88	16	16	2 or 3 PCLKB	2 ICLK
000A 8632h	RSCAN0	Transmit Buffer Register 3AH	TMIDH3	16	16	2 or 3 PCLKB	2 ICLK
000A 8632h	RSCAN	RAM Test Register 89	RPGACC89	16	16	2 or 3 PCLKB	2 ICLK
000A 8634h	RSCAN	RAM Test Register 90	RPGACC90	16	16	2 or 3 PCLKB	2 ICLK
000A 8636h	RSCAN0	Transmit Buffer Register 3BH	TMPTR3	16	16	2 or 3 PCLKB	2 ICLK
000A 8636h	RSCAN	RAM Test Register 91	RPGACC91	16	16	2 or 3 PCLKB	2 ICLK
000A 8638h	RSCAN0	Transmit Buffer Register 3CL	TMDF03	16	16	2 or 3 PCLKB	2 ICLK
000A 8638h	RSCAN	RAM Test Register 92	RPGACC92	16	16	2 or 3 PCLKB	2 ICLK
000A 863Ah	RSCAN0	Transmit Buffer Register 3CH	TMDF13	16	16	2 or 3 PCLKB	2 ICLK
000A 863Ah	RSCAN	RAM Test Register 93	RPGACC93	16	16	2 or 3 PCLKB	2 ICLK
000A 863Ch	RSCAN0	Transmit Buffer Register 3DL	TMDF23	16	16	2 or 3 PCLKB	2 ICLK
000A 863Ch	RSCAN	RAM Test Register 94	RPGACC94	16	16	2 or 3 PCLKB	2 ICLK
000A 863Eh	RSCAN0	Transmit Buffer Register 3DH	TMDF33	16	16	2 or 3 PCLKB	2 ICLK
000A 863Eh	RSCAN	RAM Test Register 95	RPGACC95	16	16	2 or 3 PCLKB	2 ICLK
000A 8640h to 000A 867Eh	RSCAN	RAM Test Register 96 to RAM Test Register 127	RPGACC96 to RPGACC127	16	16	2 or 3 PCLKB	2 ICLK
000A 8680h	RSCAN0	Transmit History Buffer Access Register	THLACC0	16	16	2 or 3 PCLKB	2 ICLK
000D 0A00h	MTU3	Timer Control Register	TCR	8	8	2 or 3 PCLKA	2 ICLK
000D 0A01h	MTU4	Timer Control Register	TCR	8	8	2 or 3 PCLKA	2 ICLK
000D 0A02h	MTU3	Timer Mode Register	TMDR	8	8	2 or 3 PCLKA	2 ICLK
000D 0A03h	MTU4	Timer Mode Register	TMDR	8	8	2 or 3 PCLKA	2 ICLK
000D 0A04h	MTU3	Timer I/O Control Register H	TIORH	8	8	2 or 3 PCLKA	2 ICLK
000D 0A05h	MTU3	Timer I/O Control Register L	TIORL	8	8	2 or 3 PCLKA	2 ICLK
000D 0A06h	MTU4	Timer I/O Control Register H	TIORH	8	8	2 or 3 PCLKA	2 ICLK
000D 0A07h	MTU4	Timer I/O Control Register L	TIORL	8	8	2 or 3 PCLKA	2 ICLK
000D 0A08h	MTU3	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKA	2 ICLK
000D 0A09h	MTU4	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKA	2 ICLK
000D 0A0Ah	MTU	Timer Output Master Enable Register	TOER	8	8	2 or 3 PCLKA	2 ICLK
000D 0A0Dh	MTU	Timer Gate Control Register	TGCR	8	8	2 or 3 PCLKA	2 ICLK
000D 0A0Eh	MTU	Timer Output Control Register 1	TOCR1	8	8	2 or 3 PCLKA	2 ICLK
000D 0A0Fh	MTU	Timer Output Control Register 2	TOCR2	8	8	2 or 3 PCLKA	2 ICLK
000D 0A10h	MTU3	Timer Counter	TCNT	16	16	2 or 3 PCLKA	2 ICLK
000D 0A12h	MTU4	Timer Counter	TCNT	16	16	2 or 3 PCLKA	2 ICLK
000D 0A14h	MTU	Timer Cycle Data Register	TCDR	16	16	2 or 3 PCLKA	2 ICLK
000D 0A16h	MTU	Timer Dead Time Data Register	TDDR	16	16	2 or 3 PCLKA	2 ICLK
000D 0A18h	MTU3	Timer General Register A	TGRA	16	16	2 or 3 PCLKA	2 ICLK
000D 0A1Ah	MTU3	Timer General Register B	TGRB	16	16	2 or 3 PCLKA	2 ICLK
000D 0A1Ch	MTU4	Timer General Register A	TGRA	16	16	2 or 3 PCLKA	2 ICLK
000D 0A1Eh	MTU4	Timer General Register B	TGRB	16	16	2 or 3 PCLKA	2 ICLK
000D 0A20h	MTU	Timer Subcounters	TCNTS	16	16	2 or 3 PCLKA	2 ICLK
000D 0A22h	MTU	Timer Cycle Buffer Register	TCBR	16	16	2 or 3 PCLKA	2 ICLK
000D 0A24h	MTU3	Timer General Register C	TGRC	16	16	2 or 3 PCLKA	2 ICLK
000D 0A26h	MTU3	Timer General Register D	TGRD	16	16	2 or 3 PCLKA	2 ICLK
000D 0A28h	MTU4	Timer General Register C	TGRC	16	16	2 or 3 PCLKA	2 ICLK
000D 0A2Ah	MTU4	Timer General Register D	TGRD	16	16	2 or 3 PCLKA	2 ICLK
000D 0A2Ch	MTU3	Timer Status Register	TSR	8	8	2 or 3 PCLKA	2 ICLK
000D 0A2Dh	MTU4	Timer Status Register	TSR	8	8	2 or 3 PCLKA	2 ICLK
000D 0A30h	MTU	Timer Interrupt Skipping Set Register	TITCR	8	8	2 or 3 PCLKA	2 ICLK
000D 0A31h	MTU	Timer Interrupt Skipping Counters	TITCNT	8	8	2 or 3 PCLKA	2 ICLK
000D 0A32h	MTU	Timer Buffer Transfer Set Register	TBTER	8	8	2 or 3 PCLKA	2 ICLK

Table 5.2 Recommended Operating Voltage Conditions

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltages	VCC*1, *2	When USB is not used	1.8	—	5.5	V
		When USB is used When USB regulator is not used	3.0	—	3.6	
		When USB is used When USB regulator is used	4.0	—	5.5	
	VSS		—	0	—	
USB power supply voltages	VCC_USB	When USB regulator is not used	—	VCC	—	V
	VSS_USB		—	0	—	
VBATT power supply voltage	VBATT		1.8	—	5.5	V
Analog power supply voltages	AVCC0*1, *2		1.8	—	5.5	V
	AVSS0		—	0	—	
	VREFH0		1.8	—	AVCC0	
	VREFL0		—	0	—	
	VREFH		1.8	—	AVCC0	
	VREFL		—	0	—	

Note 1. Use AVCC0 and VCC under the following conditions:
AVCC0 and VCC can be set individually within the operating range when VCC ≥ 2.0 V
AVCC0 = VCC when VCC < 2.0 V
Note 2. When powering on the VCC and AVCC0 pins, power them on at the same time or the VCC pin first and then the AVCC0 pin.

Table 5.16 Permissible Output Currents (1)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +85°C

Item			Symbol	Max.	Unit
Permissible output low current (average value per pin)	Ports 40 to 47, ports 03, 05, 07, port 36, 37		I_{OL}	4.0	mA
	Ports other than above	Normal output mode		4.0	
		High-drive output mode		8.0	
Permissible output low current (maximum value per pin)	Ports 40 to 47, ports 03, 05, 07, ports 36, 37			4.0	
	Ports other than above	Normal output mode		4.0	
		High-drive output mode		8.0	
Permissible output low current	Total of ports 40 to 47, ports 03, 05, 07		ΣI_{OL}	40	
	Total of ports 12 to 17, ports 20 to 27, ports 30 to 37, port PJ3			40	
	Total of ports 50 to 55, ports C0 to C7, ports B0 to B7			40	
	Total of ports E0 to E7, ports A0 to A7, ports D0 to D4			40	
	Total of all output pins			80	
Permissible output high current (average value per pin)	Ports 40 to 47, ports 03, 05, 07, ports 36, 37		I_{OH}	–4.0	
	Ports other than above	Normal output mode		–4.0	
		High-drive output mode		–8.0	
Permissible output high current (maximum value per pin)	Ports 40 to 47, ports 03, 05, 07, ports 36, 37			–4.0	
	Ports other than above	Normal output mode		–4.0	
		High-drive output mode		–8.0	
Permissible output high current	Total of ports 40 to 47, ports 03, 05, 07		ΣI_{OH}	–40	
	Total of ports 12 to 17, ports 20 to 27, ports 30 to 37, port PJ3			–40	
	Total of ports 50 to 55, ports C0 to C7, ports B0 to B7			–40	
	Total of ports E0 to E7, ports A0 to A7, ports D0 to D4			–40	
	Total of all output pins			–80	

Note: Do not exceed the permissible total supply current.

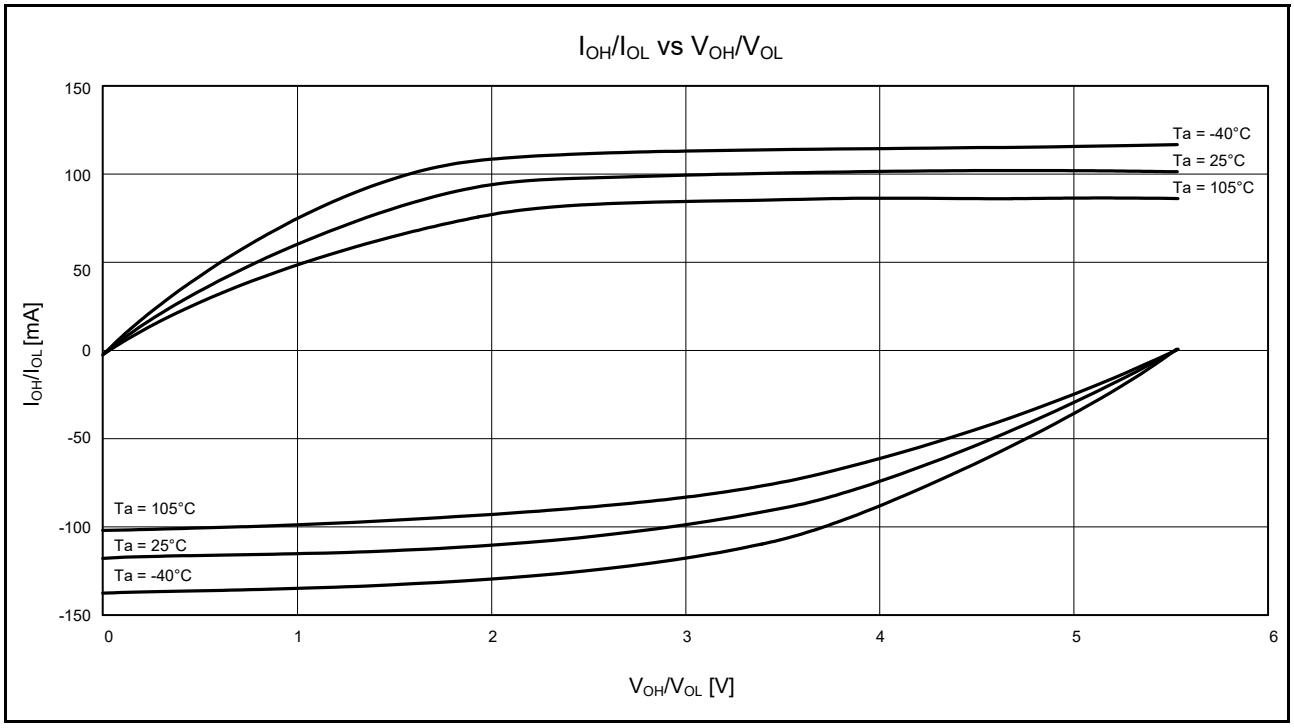


Figure 5.17 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 5.5 V When High-Drive Output is Selected (Reference Data)

5.3 AC Characteristics

5.3.1 Clock Timing

Table 5.21 Operating Frequency Value (High-Speed Operating Mode)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VREFL0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC				Unit
			1.8 V ≤ VCC < 2.4 V	2.4 V ≤ VCC < 2.7 V	2.7 V ≤ VCC ≤ 5.5 V	When USB is in Use*3	
Maximum operating frequency*4	System clock (ICLK)	f_{max}	8	16	54	54	MHz
	FlashIF clock (FCLK)*1, *2		8	16	32	32	
	Peripheral module clock (PCLKA)		8	16	54	54	
	Peripheral module clock (PCLKB)		8	16	32	32	
	Peripheral module clock (PCLKD)		8	32	54	54	
	External bus clock (BCLK)		8	16	32	32	
	BCLK pin output		8	8	16	16	
	USB clock (UCLK)	f_{usb}	—	—	—	48	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When FCLK is in use at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK must be within ±3.5%.
Note 3. The VCC_USB range is 3.0 to 5.5 V when the USB clock is in use.
Note 4. The maximum operating frequency listed above does not include errors of the external oscillator and internal oscillator. For details on the range for the guaranteed operation, see Table 5.26, Clock Timing.

Table 5.22 Operating Frequency Value (Middle-Speed Operating Mode)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VREFL0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC				Unit
			1.8 V ≤ VCC < 2.4 V	2.4 V ≤ VCC < 2.7 V	2.7 V ≤ VCC ≤ 5.5 V	When USB is in Use*3	
Maximum operating frequency*4	System clock (ICLK)	f_{max}	8	12	12	12	MHz
	FlashIF clock (FCLK)*1, *2		8	12	12	12	
	Peripheral module clock (PCLKA)		8	12	12	12	
	Peripheral module clock (PCLKB)		8	12	12	12	
	Peripheral module clock (PCLKD)		8	12	12	12	
	External bus clock (BCLK)		8	12	12	12	
	BCLK pin output		8	8	12	12	
	USB clock (UCLK)	f_{usb}	—	—	—	48	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK must be within ±3.5%.
Note 3. The VCC_USB range is 3.0 to 5.5 V when the USB clock is in use.
Note 4. The maximum operating frequency listed above does not include errors of the external oscillator and internal oscillator. For details on the range for the guaranteed operation, see Table 5.26, Clock Timing.

Table 5.23 Operating Frequency Value (Low-Speed Operating Mode)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VREFL0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC			Unit
			1.8 V ≤ VCC < 2.4 V	2.4 V ≤ VCC < 2.7 V	2.7 V ≤ VCC ≤ 5.5 V	
Maximum operating frequency*3	System clock (ICLK)	f_{max}	32.768			kHz
	FlashIF clock (FCLK)*1		32.768			
	Peripheral module clock (PCLKA)		32.768			
	Peripheral module clock (PCLKB)		32.768			
	Peripheral module clock (PCLKD)*2		32.768			
	External bus clock (BCLK)		32.768			
	BCLK pin output		32.768			

Note 1. Programming and erasing the flash memory is impossible.
Note 2. The A/D converter cannot be used.
Note 3. The maximum operating frequency listed above does not include errors of the external oscillator. For details on the range for the guaranteed operation, see Table 5.26, Clock Timing.

Table 5.24 BCLK Clock Timing (1)

Conditions: 2.7 V ≤ VCC= VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VREFL0 = VSS_USB = 0 V,
fBCLK ≤ 32 MHz (BCLK pin output frequency ≤ 16 MHz), T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BCLK pin output cycle time	t_{Bcyc}	62.5	—	—	ns	Figure 5.22
BCLK pin output high pulse width	t_{CH}	15	—	—	ns	
BCLK pin output low pulse width	t_{CL}	15	—	—	ns	
BCLK pin output rise time	t_{Cr}	—	—	12	ns	
BCLK pin output fall time	t_{Cf}	—	—	12	ns	

Table 5.25 BCLK Clock Timing (2)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 < 2.7 V, VSS = AVSS0 = VREFL0 = VSS_USB = 0 V,
fBCLK ≤ 16 MHz (BCLK pin output frequency ≤ 8 MHz), T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BCLK pin output cycle time	t_{Bcyc}	125	—	—	ns	Figure 5.22
BCLK pin output high pulse width	t_{CH}	30	—	—	ns	
BCLK pin output low pulse width	t_{CL}	30	—	—	ns	
BCLK pin output rise time	t_{Cr}	—	—	25	ns	
BCLK pin output fall time	t_{Cf}	—	—	25	ns	

Table 5.30 Timing of Recovery from Low Power Consumption Modes (3)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VREFL0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from software standby mode*1	Low-speed mode	Sub-clock oscillator operating	t_{SBYSC}	—	600	750	µs	Figure 5.34

Note 1. The sub-clock continues oscillating in software standby mode during low-speed mode.

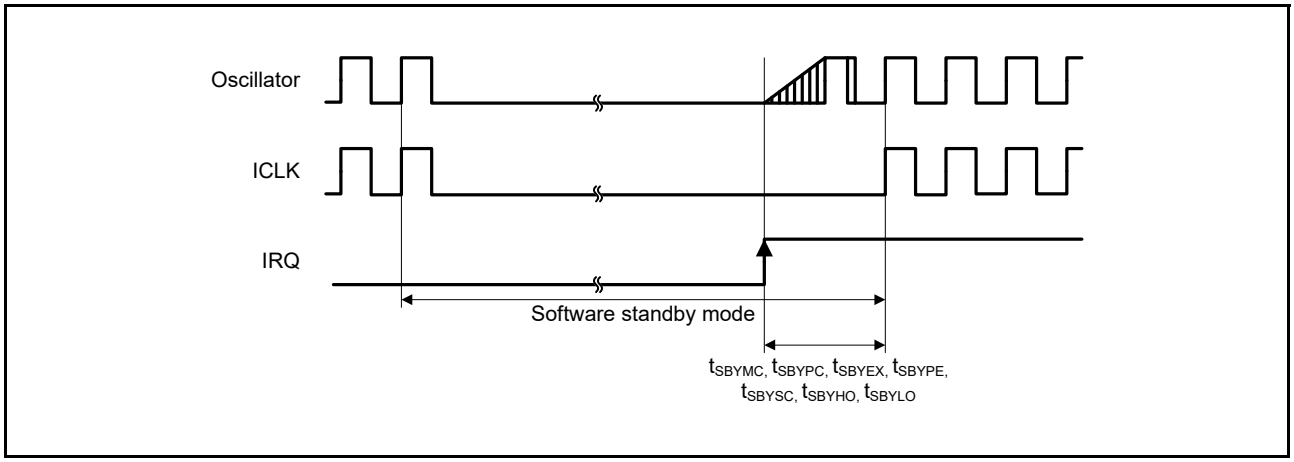


Figure 5.34 Software Standby Mode Recovery Timing

Table 5.31 Timing of Recovery from Low Power Consumption Modes (4)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VREFL0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from deep sleep mode*1	High-speed mode*2	t_{DSLP}	—	2	3.5	µs	Figure 5.35
	Middle-speed mode*3	t_{DSLP}	—	3	4	µs	
	Low-speed mode*4	t_{DSLP}	—	400	500	µs	

Note 1. Oscillators continue oscillating in deep sleep mode.
Note 2. When the frequency of the system clock is 32 MHz.
Note 3. When the frequency of the system clock is 12 MHz.
Note 4. When the frequency of the system clock is 32 kHz.

5.3.4 Control Signal Timing

Table 5.33 Control Signal Timing

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
NMI pulse width	t_{NMIW}	200	—	—	ns	NMI digital filter is disabled (NMIFLTE.NFLTEN = 0)	t_{Pcyc} × 2 ≤ 200 ns
		t_{Pcyc} × 2*1	—	—			t_{Pcyc} × 2 > 200 ns
		200	—	—		NMI digital filter is enabled (NMIFLTE.NFLTEN = 1)	t_{NMICK} × 3 ≤ 200 ns
		t_{NMICK} × 3.5*2	—	—			t_{NMICK} × 3 > 200 ns
IRQ pulse width	t_{IRQW}	200	—	—	ns	IRQ digital filter is disabled (IRQFLTE0.FLTENi = 0)	t_{Pcyc} × 2 ≤ 200 ns
		t_{Pcyc} × 2*1	—	—			t_{Pcyc} × 2 > 200 ns
		200	—	—		IRQ digital filter is enabled (IRQFLTE0.FLTENi = 1)	t_{IRQCK} × 3 ≤ 200 ns
		t_{IRQCK} × 3.5*3	—	—			t_{IRQCK} × 3 > 200 ns

Note: 200 ns minimum in software standby mode.
Note 1. t_{Pcyc} indicates the cycle of PCLKB.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 7).

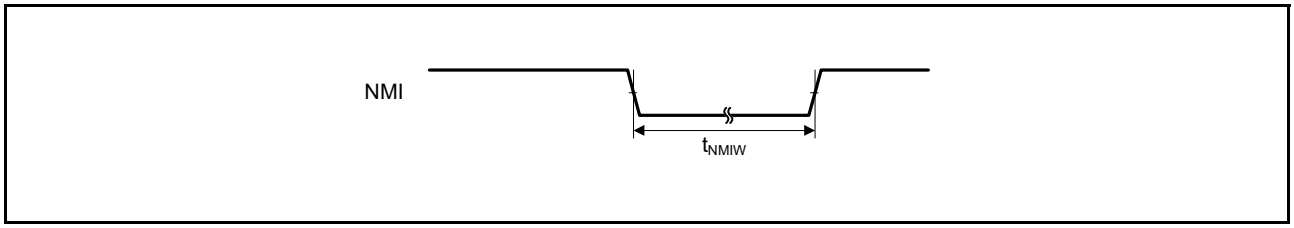


Figure 5.36 NMI Interrupt Input Timing

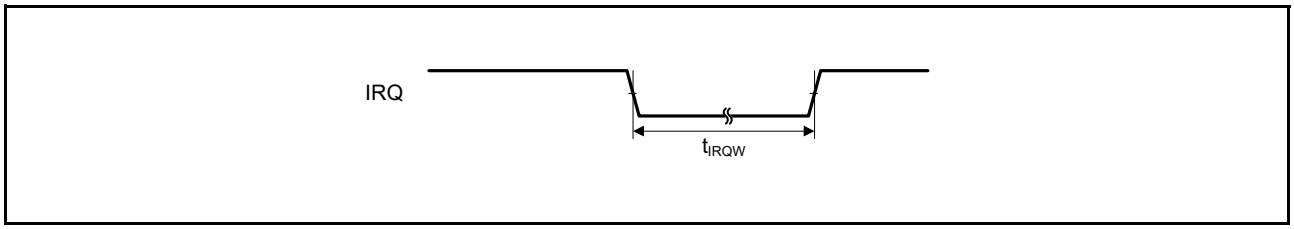


Figure 5.37 IRQ Interrupt Input Timing

Table 5.44 Timing of On-Chip Peripheral Modules (7)

Conditions: 2.7 V ≤ VCC = VCC_USB = AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, fPCLKB ≤ 32 MHz,
T_a = –40 to +105°C,
when high-drive output is selected by the drive capacity control register

Item		Symbol	Min.	Max.	Unit	Test Conditions
SDHI	SDHI_CLK pin output cycle time	$t_{PP(SD)}$	62.5	—	ns	Figure 5.64
	SDHI_CLK pin output high pulse width	$t_{WH(SD)}$	18.25	—	ns	
	SDHI_CLK pin output low pulse width	$t_{WL(SD)}$	18.25	—	ns	
	SDHI_CLK pin output rise time	$t_{TLH(SD)}$	—	10	ns	
	SDHI_CLK pin output fall time	$t_{THL(SD)}$	—	10	ns	
	Output data delay time (data transfer mode) for SDHI_CMD and SDHI_D0 to SDHI_D3 pins	$t_{ODLY(SD)}$	–18.25	18.25	ns	
	Input data setup time for SDHI_CMD and SDHI_D0 to SDHI_D3 pins	$t_{ISU(SD)}$	9.25	—	ns	
	Input data hold time for SDHI_CMD and SDHI_D0 to SDHI_D3 pins	$t_{IH(SD)}$	8.3	—	ns	

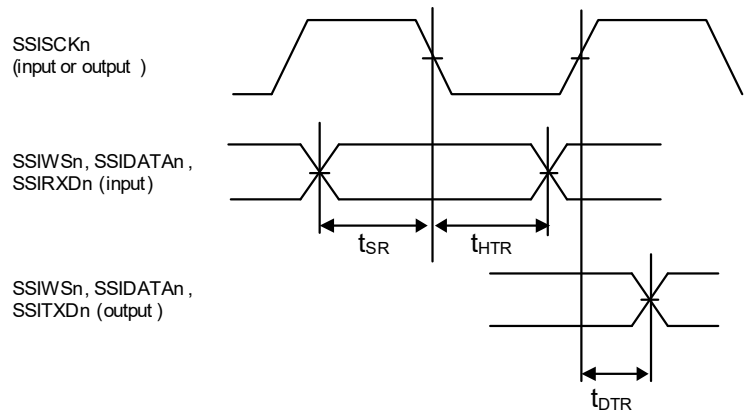
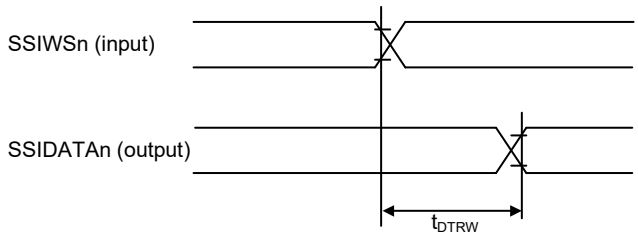


Figure 5.62 SSI Transmission/Reception Timing (SSICR.SCKP=1)



Note. Timing to output the MSB bit during slave transmission from SSIWSn
when DEL = 1 and SDTA = 0 or DEL = 1, SDTA = 1, and SWL[2:0] = DWL[2:0]

Figure 5.63 SSIDATA Output Delay After SSIWSn Changing Edge

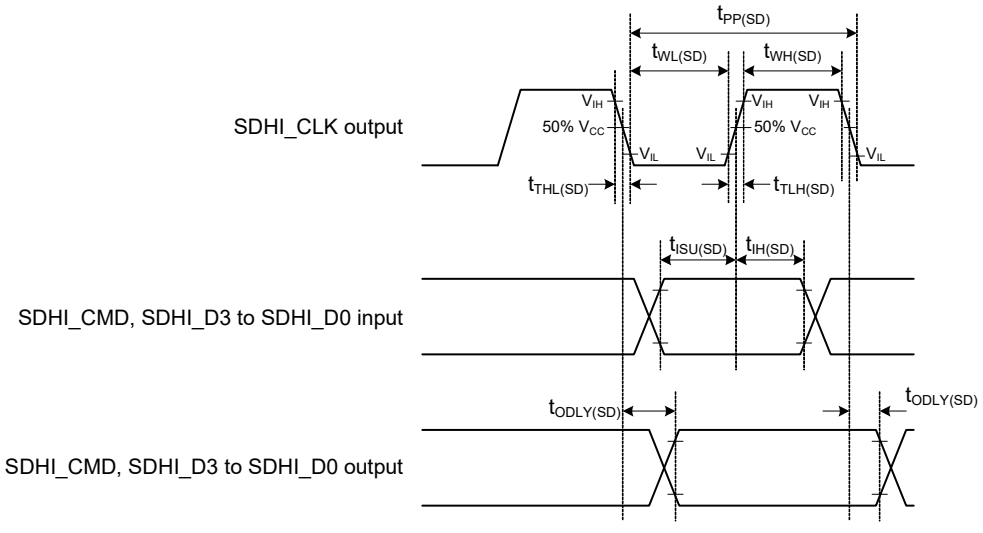


Figure 5.64 SD Host Interface Input/Output Signal Timing

Differential non-linearity error (DNL)

The differential non-linearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

Offset error

An offset error is the difference between a transition point of the ideal first output code and the actual first output code.

Full-scale error

A full-scale error is the difference between a transition point of the ideal last output code and the actual last output code.

5.6 D/A Conversion Characteristics

Table 5.52 D/A Conversion Characteristics (1)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C
Reference voltage = VREFH or VREFL selected

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	—	—	12	Bit	
Resistive load	30	—	—	kΩ	
Capacitive load	—	—	50	pF	
Output voltage range	0.35	—	AVCC0 - 0.47	V	
DNL differential non-linearity error	—	±0.5	±1.0	LSB	
INL integral non-linearity error	—	±2.0	±8.0	LSB	
Offset error	—	—	±20	mV	
Full-scale error	—	—	±20	mV	
Output resistance	—	5	—	Ω	
Conversion time	—	—	30	μs	

Table 5.53 D/A Conversion Characteristics (2)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VREFL = VSS_USB = 0 V, T_a = –40 to +105°C
Reference voltage = AVCC0 or AVSS0 selected

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	—	—	12	Bit	
Resistive load	30	—	—	kΩ	
Capacitive load	—	—	50	pF	
Output voltage range	0.35	—	AVCC0 - 0.47	V	
DNL differential non-linearity error	—	±0.5	±2.0	LSB	
INL integral non-linearity error	—	±2.0	±8.0	LSB	
Offset error	—	—	±30	mV	
Full-scale error	—	—	±30	mV	
Output resistance	—	5	—	Ω	
Conversion time	—	—	30	μs	

Table 5.54 D/A Conversion Characteristics (3)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C
Reference voltage = internal reference voltage selected

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	—	—	12	Bit	
Internal reference voltage (Vbgr)	1.36	1.43	1.50	V	
Resistive load	30	—	—	kΩ	
Capacitive load	—	—	50	pF	
Output voltage range	0.35	—	Vbgr	V	
DNL differential non-linearity error	—	±2.0	±16.0	LSB	
INL integral non-linearity error	—	±8.0	±16.0	LSB	
Offset error	—	—	30	mV	
Output resistance	—	5	—	Ω	
Conversion time	—	—	30	μs	

5.7 Temperature Sensor Characteristics

Table 5.55 Temperature Sensor Characteristics

Conditions: 2.0 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Relative accuracy	—	—	±1.5	—	°C	2.4 V or above
		—	±2.0	—		Below 2.4 V
Temperature slope	—	—	–3.65	—	mV/°C	
Output voltage (25°C)	—	—	1.05	—	V	VCC = 3.3 V
Temperature sensor start time	t_{START}	—	—	5	µs	
Sampling time	—	5	—	—	µs	

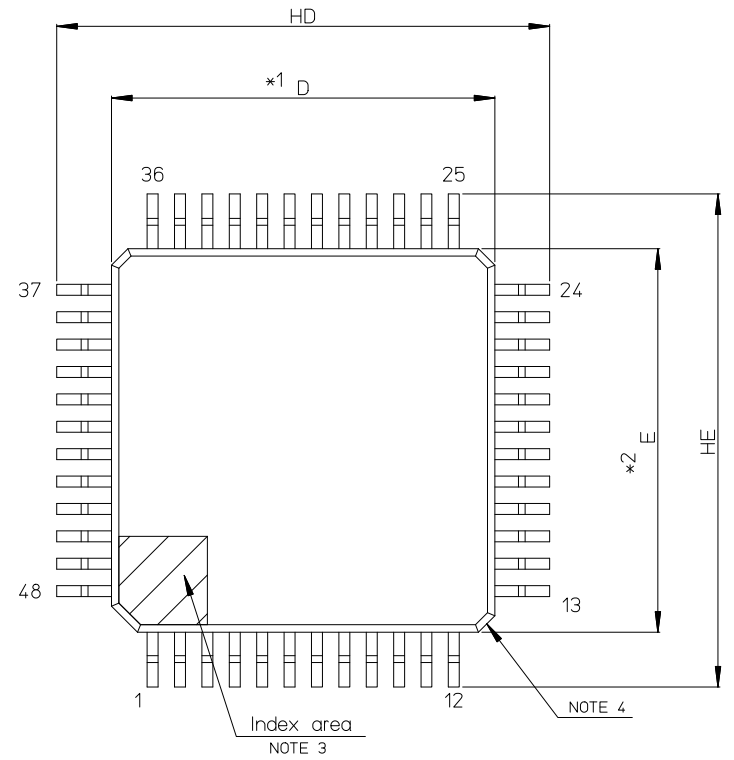
5.8 Comparator Characteristics

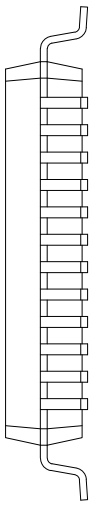
Table 5.56 Comparator Characteristics

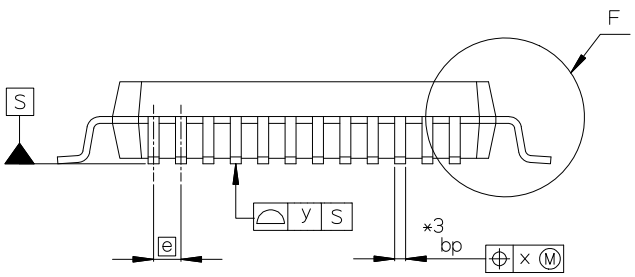
Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

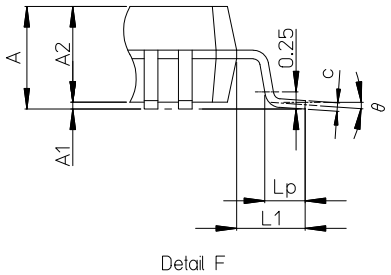
Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
CVREFB0 to CVREFB3 input reference voltage		VREF	0	—	VCC - 1.4	V	
CMPB0 to CMPB3 input voltage		VI	–0.3	—	VCC + 0.3	V	
Offset	Comparator high-speed mode	—	—	—	50	mV	
	Comparator high-speed mode Window function enabled	—	—	—	60	mV	
	Comparator low-speed mode	—	—	—	40	mV	
Comparator output delay time	Comparator high-speed mode	Td	—	—	1.2	µs	VCC = 3 V, input slew rate ≥ 50 mV/us
	Comparator high-speed mode Window function enabled	Tdw	—	—	2.0	µs	
	Comparator low-speed mode	Td	—	—	5.0	µs	
High-side reference voltage (comparator high-speed mode, window function enabled)		VRFH	—	0.76 VCC	—	V	
Low-side reference voltage (comparator high-speed mode, window function enabled)		VRFL	—	0.24 VCC	—	V	
Operation stabilization wait time		Tcmp	100	—	—	µs	

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP48-7x7-0.50	PLQP0048KB-B	——	0.2g









Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A2	——	1.4	——
HD	8.8	9.0	9.2
HE	8.8	9.0	9.2
A	——	——	1.7
A1	0.05	——	0.15
bp	0.17	0.20	0.27
c	0.09	——	0.20
θ	0°	3.5°	8°
e	——	0.5	——
x	——	——	0.08
y	——	——	0.08
Lp	0.45	0.6	0.75
L1	——	1.0	——

Figure G 48 -Pin LFQFP (PLQP0048KB-B)

NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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