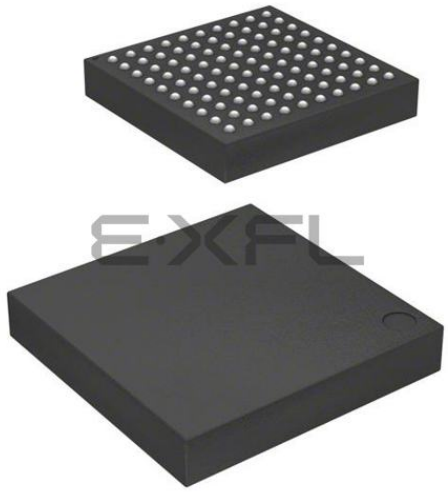

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Details	
Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	54MHz
Connectivity	EBI/EMI, I²C, IrDA, SCI, SD/SDIO, SPI, SSI, USB OTG
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	79
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFLGA
Supplier Device Package	100-TFLGA (5.5x5.5)
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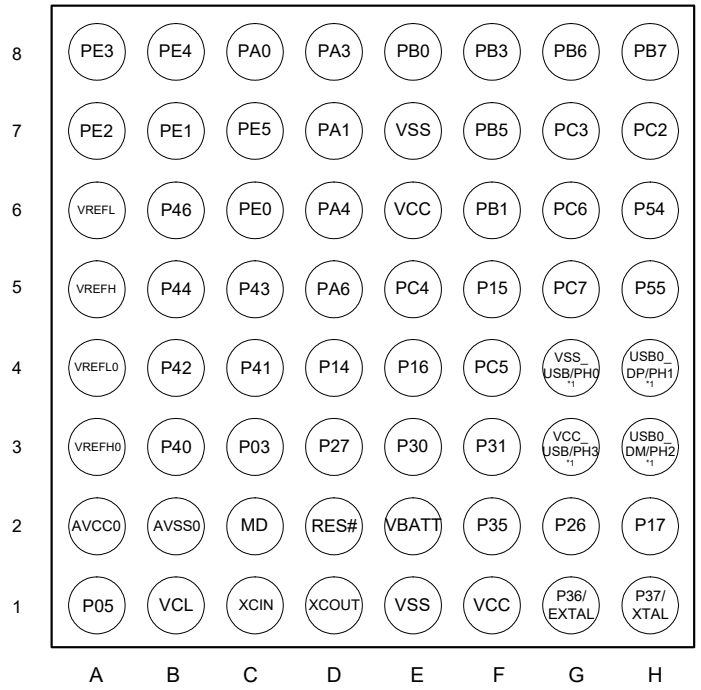
1.4 Pin Functions

Table 1.5 lists the pin functions.

Table 1.5 Pin Functions (1/4)

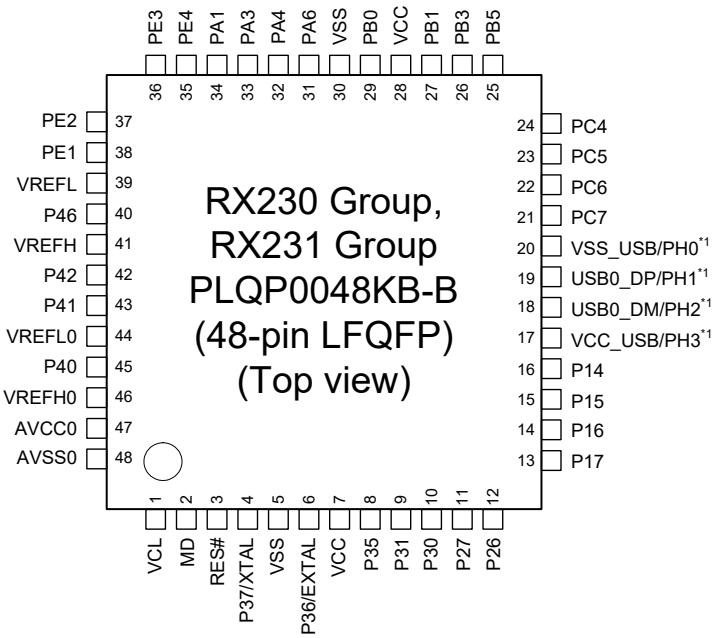
Classifications	Pin Name	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply.
	VCL	—	Connect this pin to the VSS pin via a 4.7 μF smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
	VBATT	Input	Backup power pin
Clock	XTAL	Output	Pins for connecting a crystal. An external clock can be input through the EXTAL pin.
	EXTAL	Input	
	BCLK	Output	Outputs the external bus clock for external devices.
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal between XCIN and XCOUT.
	XCOUT	Output	
	CLKOUT	Output	Clock output pin.
Operating mode control	MD	Input	Pin for setting the operating mode. The signal levels on this pin must not be changed during operation.
	UB	Input	Pin used for boot mode (USB interface).
	UPSEL	Input	Pin used for boot mode (USB interface).
System control	RES#	Input	Reset pin. This MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Input pin for the clock frequency accuracy measurement circuit.
On-chip emulator	FINED	I/O	FINE interface pin.
Address bus	A0 to A23	Output	Output pins for the address.
Data bus	D0 to D15	I/O	Input and output pins for the bidirectional data bus.
Multiplexed bus	A0/D0 to A15/D15	I/O	Address/data multiplexed bus
Bus control	RD#	Output	Strobe signal which indicates that reading from the external bus interface space is in progress.
	WR#	Output	Strobe signal which indicates that writing to the external bus interface space is in progress, in single-write strobe mode.
	WR0#, WR1#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0, and D15 to D8) is valid in writing to the external bus interface space, in byte strobe mode.
	BC0#, BC1#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0 and D15 to D8) is valid in access to the external bus interface space, in single-write strobe mode.
	CS0# to CS3#	Output	Select signals for areas 0 to 3.
	WAIT#	Input	Input pin for wait request signals in access to the external space.
	ALE	Output	Address latch signal when address/data multiplexed bus is selected.
LVD	CMPA2	Input	Detection target voltage pin for voltage detection 2.
Interrupts	NMI	Input	Non-maskable interrupt request pin.
	IRQ0 to IRQ7	Input	Interrupt request pins.

RX230 Group, RX231 Group
PWLG0064KA-A
(64-pin WFLGA)
(Upper perspective view)



Note: This figure indicates the power supply pins and I/O port pins.
For the pin configuration, see the table “List of Pins and Pin Functions (64-Pin WFLGA)”.
Note: For the position of A1 pin in the package, see “Package Dimensions”.
Note 1. RX230: PH0, PH1, PH2, PH3
RX231: VSS_USB, USB0_DP, USB0_DM, VCC_USB

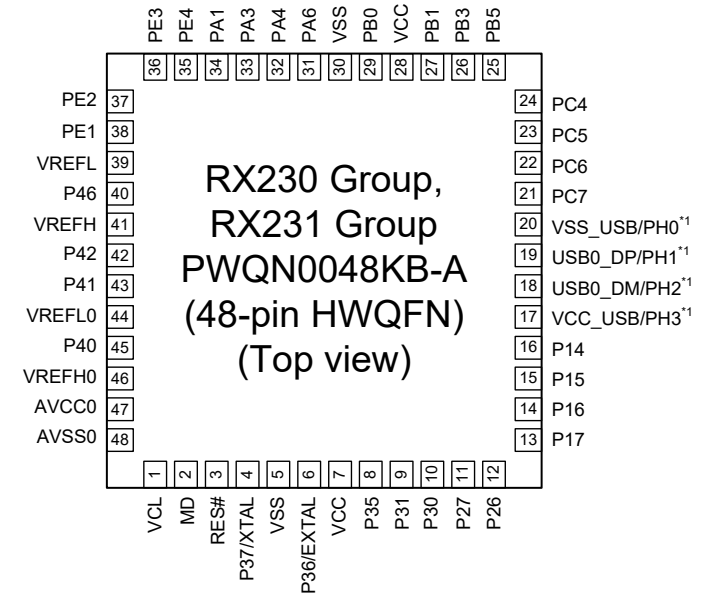
Figure 1.5 Pin Assignments of the 64-Pin WFLGA



Note: This figure indicates the power supply pins and I/O port pins.
For the pin configuration, see the table “List of Pins and Pin Functions (48-Pin LFQFP/HWQFN)”.

Note 1. RX230: PH0, PH1, PH2, PH3
RX231: VSS_USB, USB0_DP, USB0_DM, VCC_USB

Figure 1.8 Pin Assignments of the 48-Pin LFQFP



Note: It is recommended to connect an exposed die pad to VSS.

Note: This figure indicates the power supply pins and I/O port pins.
For the pin configuration, see the table “List of Pins and Pin Functions (48-Pin LFQFP/HWQFN)”.

Note 1. RX230: PH0, PH1, PH2, PH3
RX231: VSS_USB, USB0_DP, USB0_DM, VCC_USB

Figure 1.9 Pin Assignments of the 48-Pin HWQFN

Table 1.10 List of Pins and Pin Functions (48-Pin LFQFP/HWQFN) (1/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCI, RSPI, RIIC, RSCAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
1	VCL						
2	MD						FINED
3	RES#						
4	XTAL	P37					
5	VSS						
6	EXTAL	P36					
7	VCC						
8	UPSEL	P35					NMI
9		P31	MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#/SSISCK0			IRQ1
10		P30	MTIOC4B/TMRI3/POE8#	RXD1/SMISO1/SSCL1/ AUDIO_MCLK			IRQ0/CMPOB3
11		P27	MTIOC2B/TMCI3	SCK1/SSIWS0		TS2	CVREFB3
12		P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1/ USB0_VBUSEN/SSIRXD0		TS3	CMPB3
13		P17	MTIOC3A/MTIOC3B/TMO1/ POE8#/TIOCB0/TCLKD	SCK1/MISOA/SDA/ SSITXD0			IRQ7/ CMPOB2
14		P16	MTIOC3C/MTIOC3D/TMO2/ TIOCB1/TCLKC	TXD1/SMOSI1/SSDA1/MOSIA/ SCL/USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB			IRQ6/ADTRG0#
15		P15	MTIOC0B/MTCLKB/TMCI2/ TIOCB2/TCLKB	RXD1/SMISO1/SSCL1/CRXD0		TS12	IRQ5/CMPB2
16		P14	MTIOC3A/MTCLKA/TMRI2/ TIOCB5/TCLKA	CTS1#/RTS1#/SS1#/CTXD0/ USB0_OVRCURA		TS13	IRQ4/CVREFB2
17	VCC_USB*1	PH3*1	TMCI0*1				
18		PH2*1	TMRI0*1	USB0_DM*1			IRQ1*1
19		PH1*1	TMO0*1	USB0_DP*1			IRQ0*1
20	VSS_USB*1	PH0*1					CACREF*1
21	UB	PC7	MTIOC3A/MTCLKB/TMO2	TXD8/SMOSI8/SSDA8/MISOA			CACREF
22		PC6	MTIOC3C/MTCLKA/TMCI2	RXD8/SMISO8/SSCL8/MOSIA/ USB0_EXICEN		TS22	
23		PC5	MTIOC3B/MTCLKD/TMRI2	SCK8/RSPCKA/USB0_ID		TS23	
24		PC4	MTIOC3D/MTCLKC/TMCI1/ POE0#	SCK5/CTS8#/RTS8#/SS8#/ SSLA0		TSCAP	
25		PB5/PC3	MTIOC2A/MTIOC1B/TMRI1/ POE1#/TIOCB4	USB0_VBUS			
26		PB3/PC2	MTIOC0A/MTIOC4A/TMO0/ POE3#/TIOCD3/TCLKD	SCK6			
27		PB1/PC1	MTIOC0C/MTIOC4C/TMCI0/ TIOCB3	TXD6/SMOSI6/SSDA6			IRQ4/ CMPOB1
28	VCC						
29		PB0/PC0	MTIC5W/TIOCA3	RXD6/SMISO6/SSCL6/RSPCKA			
30	VSS						
31		PA6	MTIC5V/MTCLKB/TMCI3/POE2#/ TIOCA2	CTS5#/RTS5#/SS5#/MOSIA/ SSIWS0			
32		PA4	MTIC5U/MTCLKA/TMRI0/TIOCA1	TXD5/SMOSI5/SSDA5/SSLA0/ SSITXD0/IRTXD5			IRQ5 /CVREFB1
33		PA3	MTIOC0D/MTCLKD/TIOCD0/ TCLKB	RXD5/SMISO5/SSCL5/SSIRXD0/ IRRXD5			IRQ6 /CMPB1
34		PA1	MTIOC0B/MTCLKC/TIOCB0	SCK5/SSLA2/SSISCK0			
35		PE4	MTIOC4D/MTIOC1A				AN020/CMPA2/ CLKOUT
36		PE3	MTIOC4B/POE8#	CTS12#/RTS12#/AUDIO_MCLK			AN019/CLKOUT
37		PE2	MTIOC4A	RXD12/RXDX12/SSCL12			IRQ7/AN018/ CVREFB0
38		PE1	MTIOC4C	TXD12/TXDX12/SIOX12/SSDA12			AN017/CMPB0
39	VREFL						
40		P46					AN006
41	VREFH						

3. Address Space

3.1 Address Space

This LSI has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.
Figure 3.1 shows the memory maps in the respective operating modes. Accessible areas will differ according to the operating mode and states of control bits.

Table 4.1 List of I/O Registers (Address Order) (6/33)

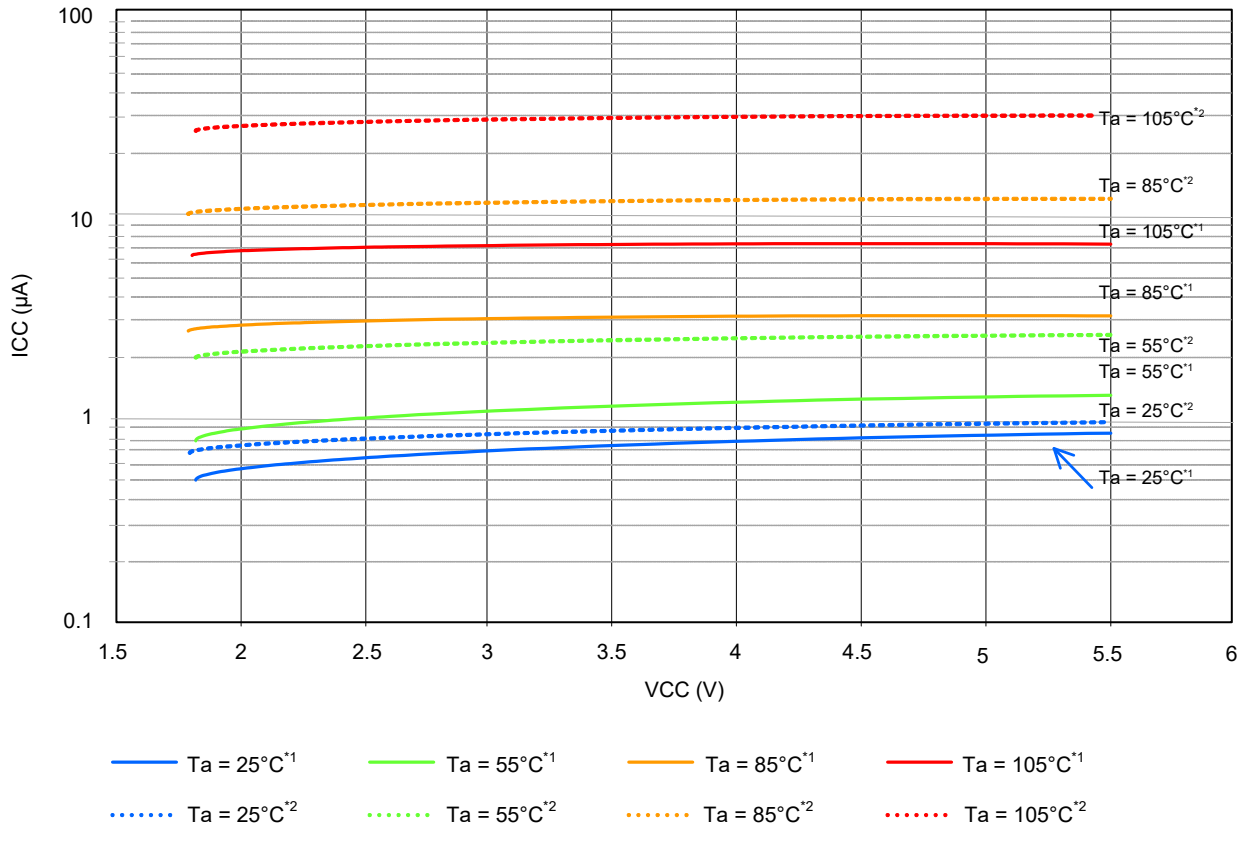
Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK <PCLK
0008 8158h	TPU4	Timer General Register A	TGRA	16	16	2 or 3 PCLKB	2 ICLK
0008 815Ah	TPU4	Timer General Register B	TGRB	16	16	2 or 3 PCLKB	2 ICLK
0008 8160h	TPU5	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8161h	TPU5	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB	2 ICLK
0008 8162h	TPU5	Timer I/O Control Register	TIOR	8	8	2 or 3 PCLKB	2 ICLK
0008 8164h	TPU5	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB	2 ICLK
0008 8165h	TPU5	Timer Status Register	TSR	8	8	2 or 3 PCLKB	2 ICLK
0008 8166h	TPU5	Timer Counter	TCNT	16	16	2 or 3 PCLKB	2 ICLK
0008 8168h	TPU5	Timer General Register A	TGRA	16	16	2 or 3 PCLKB	2 ICLK
0008 816Ah	TPU5	Timer General Register B	TGRB	16	16	2 or 3 PCLKB	2 ICLK
0008 8200h	TMR0	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8201h	TMR1	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8202h	TMR0	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB	2 ICLK
0008 8203h	TMR1	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB	2 ICLK
0008 8204h	TMR0	Time Constant Register A	TCORA	8	8	2 or 3 PCLKB	2 ICLK
0008 8205h	TMR1	Time Constant Register A	TCORA	8	8*1	2 or 3 PCLKB	2 ICLK
0008 8206h	TMR0	Time Constant Register B	TCORB	8	8	2 or 3 PCLKB	2 ICLK
0008 8207h	TMR1	Time Constant Register B	TCORB	8	8*1	2 or 3 PCLKB	2 ICLK
0008 8208h	TMR0	Timer Counter	TCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 8209h	TMR1	Timer Counter	TCNT	8	8*1	2 or 3 PCLKB	2 ICLK
0008 820Ah	TMR0	Timer Counter Control Register	TCCR	8	8	2 or 3 PCLKB	2 ICLK
0008 820Bh	TMR1	Timer Counter Control Register	TCCR	8	8*1	2 or 3 PCLKB	2 ICLK
0008 820Ch	TMR0	Timer Count Start Register	TCSTR	8	8	2 or 3 PCLKB	2 ICLK
0008 8210h	TMR2	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8211h	TMR3	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8212h	TMR2	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB	2 ICLK
0008 8213h	TMR3	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB	2 ICLK
0008 8214h	TMR2	Time Constant Register A	TCORA	8	8	2 or 3 PCLKB	2 ICLK
0008 8215h	TMR3	Time Constant Register A	TCORA	8	8*1	2 or 3 PCLKB	2 ICLK
0008 8216h	TMR2	Time Constant Register B	TCORB	8	8	2 or 3 PCLKB	2 ICLK
0008 8217h	TMR3	Time Constant Register B	TCORB	8	8*1	2 or 3 PCLKB	2 ICLK
0008 8218h	TMR2	Timer Counter	TCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 8219h	TMR3	Timer Counter	TCNT	8	8*1	2 or 3 PCLKB	2 ICLK
0008 821Ah	TMR2	Timer Counter Control Register	TCCR	8	8	2 or 3 PCLKB	2 ICLK
0008 821Bh	TMR3	Timer Counter Control Register	TCCR	8	8*1	2 or 3 PCLKB	2 ICLK
0008 821Ch	TMR2	Timer Count Start Register	TCSTR	8	8	2 or 3 PCLKB	2 ICLK
0008 8280h	CRC	CRC Control Register	CRCCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8281h	CRC	CRC Data Input Register	CRCDIR	8	8	2 or 3 PCLKB	2 ICLK
0008 8282h	CRC	CRC Data Output Register	CRCDOR	16	16	2 or 3 PCLKB	2 ICLK
0008 8300h	RIIC0	I^2C-Bus Control Register 1	ICCR1	8	8	2 or 3 PCLKB	2 ICLK
0008 8301h	RIIC0	I^2C-Bus Control Register 2	ICCR2	8	8	2 or 3 PCLKB	2 ICLK
0008 8302h	RIIC0	I^2C-Bus Mode Register 1	ICMR1	8	8	2 or 3 PCLKB	2 ICLK
0008 8303h	RIIC0	I^2C-Bus Mode Register 2	ICMR2	8	8	2 or 3 PCLKB	2 ICLK
0008 8304h	RIIC0	I^2C-Bus Mode Register 3	ICMR3	8	8	2 or 3 PCLKB	2 ICLK
0008 8305h	RIIC0	I^2C-Bus Function Enable Register	ICFER	8	8	2 or 3 PCLKB	2 ICLK
0008 8306h	RIIC0	I^2C-Bus Status Enable Register	ICSER	8	8	2 or 3 PCLKB	2 ICLK
0008 8307h	RIIC0	I^2C-Bus Interrupt Enable Register	ICIER	8	8	2 or 3 PCLKB	2 ICLK
0008 8308h	RIIC0	I^2C-Bus Status Register 1	ICSR1	8	8	2 or 3 PCLKB	2 ICLK
0008 8309h	RIIC0	I^2C-Bus Status Register 2	ICSR2	8	8	2 or 3 PCLKB	2 ICLK
0008 830Ah	RIIC0	Slave Address Register L0	SARL0	8	8	2 or 3 PCLKB	2 ICLK
0008 830Bh	RIIC0	Slave Address Register U0	SARU0	8	8	2 or 3 PCLKB	2 ICLK
0008 830Ch	RIIC0	Slave Address Register L1	SARL1	8	8	2 or 3 PCLKB	2 ICLK

Table 5.8 DC Characteristics (6)

Conditions: 1.8 V ≤ VCC= VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item			Symbol	Typ.*3	Max.	Unit	Test Conditions
Supply current*1	Software standby mode*2	T_a = 25°C	I_{CC}	0.8	3.7	μA	
		T_a = 55°C		1.2	4.3		
		T_a = 85°C		3.5	18.6		
		T_a = 105°C		7.9	45.2		
	Increment for IWDT operation			0.4	—		
	Increment for LPT operation			0.4	—		Use IWDT-Dedicated On-Chip Oscillator for clock source
	Increment for RTC operation*4			0.4	—		RCR3.RTCDV[2:0] set to low drive capacity
				1.2	—		RCR3.RTCDV[2:0] set to normal drive capacity

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. The IWDT, LVD, and CMPB are stopped.
Note 3. When VCC is 3.3 V.
Note 4. This increment includes the oscillation circuit.



Note 1. Indicates the average of the typical samples through actual measurement during product evaluation.
Note 2. Indicates the average of the upper-limit samples through actual measurement during product evaluation.

Figure 5.4 Voltage Dependency in Software Standby Mode (Reference Data)

5.2.3 Normal I/O Pin Output Characteristics (3)

Figure 5.18 to Figure 5.21 show the characteristics of the RIIC output pin.

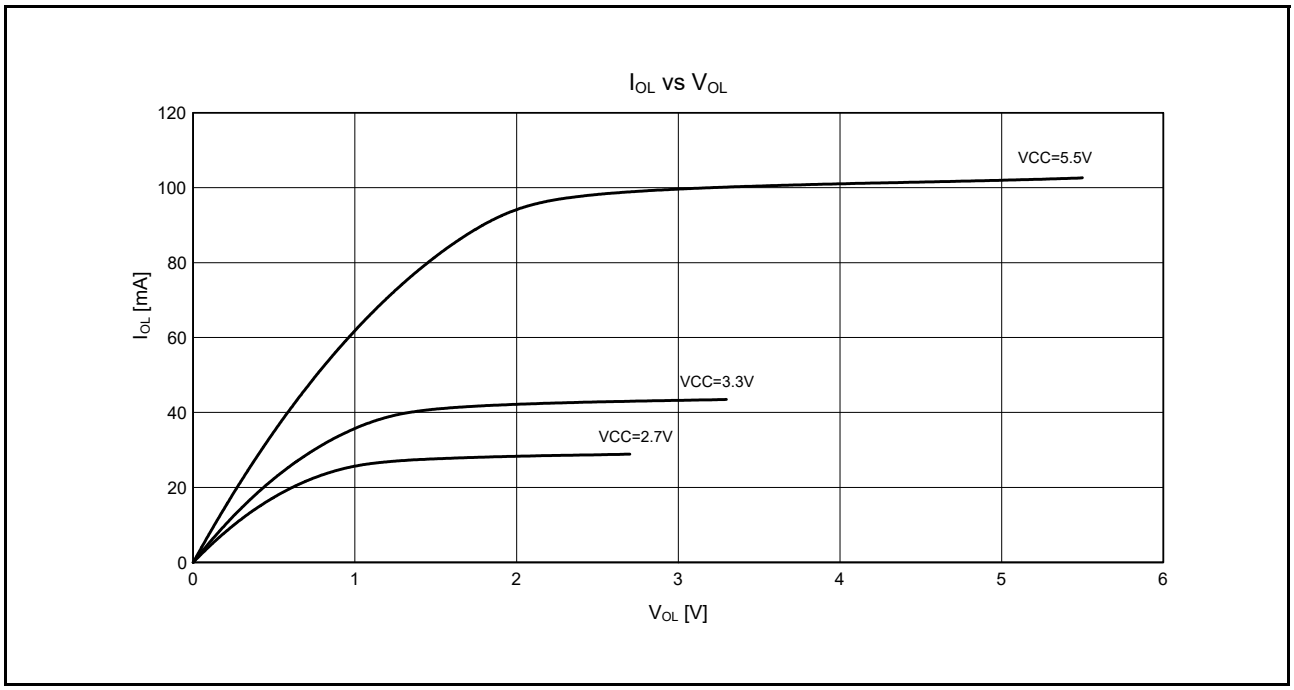


Figure 5.18 V_{OL} and I_{OL} Voltage Characteristics of RIIC Output Pin at T_a = 25°C (Reference Data)

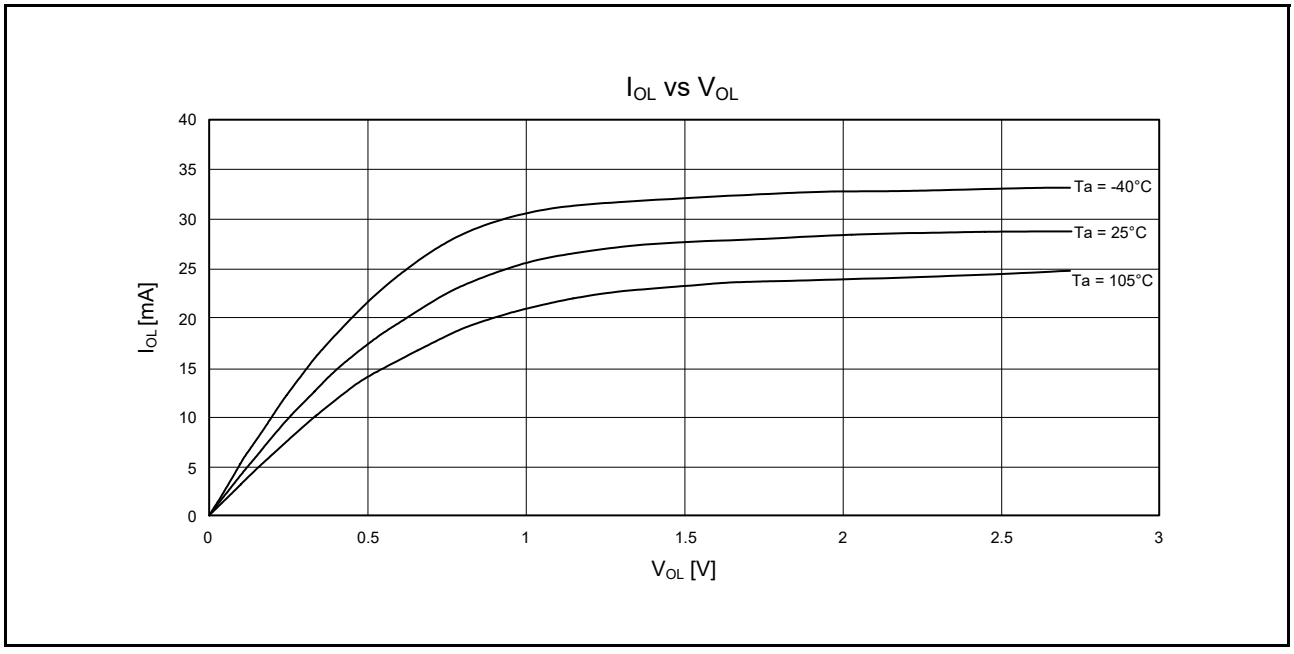


Figure 5.19 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at VCC = 2.7 V (Reference Data)

Table 5.23 Operating Frequency Value (Low-Speed Operating Mode)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VREFL0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC			Unit
			1.8 V ≤ VCC < 2.4 V	2.4 V ≤ VCC < 2.7 V	2.7 V ≤ VCC ≤ 5.5 V	
Maximum operating frequency*3	System clock (ICLK)	f_{max}	32.768			kHz
	FlashIF clock (FCLK)*1		32.768			
	Peripheral module clock (PCLKA)		32.768			
	Peripheral module clock (PCLKB)		32.768			
	Peripheral module clock (PCLKD)*2		32.768			
	External bus clock (BCLK)		32.768			
	BCLK pin output		32.768			

Note 1. Programming and erasing the flash memory is impossible.
Note 2. The A/D converter cannot be used.
Note 3. The maximum operating frequency listed above does not include errors of the external oscillator. For details on the range for the guaranteed operation, see Table 5.26, Clock Timing.

Table 5.24 BCLK Clock Timing (1)

Conditions: 2.7 V ≤ VCC= VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VREFL0 = VSS_USB = 0 V,
fBCLK ≤ 32 MHz (BCLK pin output frequency ≤ 16 MHz), T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BCLK pin output cycle time	t_{Bcyc}	62.5	—	—	ns	Figure 5.22
BCLK pin output high pulse width	t_{CH}	15	—	—	ns	
BCLK pin output low pulse width	t_{CL}	15	—	—	ns	
BCLK pin output rise time	t_{Cr}	—	—	12	ns	
BCLK pin output fall time	t_{Cf}	—	—	12	ns	

Table 5.25 BCLK Clock Timing (2)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 < 2.7 V, VSS = AVSS0 = VREFL0 = VSS_USB = 0 V,
fBCLK ≤ 16 MHz (BCLK pin output frequency ≤ 8 MHz), T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BCLK pin output cycle time	t_{Bcyc}	125	—	—	ns	Figure 5.22
BCLK pin output high pulse width	t_{CH}	30	—	—	ns	
BCLK pin output low pulse width	t_{CL}	30	—	—	ns	
BCLK pin output rise time	t_{Cr}	—	—	25	ns	
BCLK pin output fall time	t_{Cf}	—	—	25	ns	

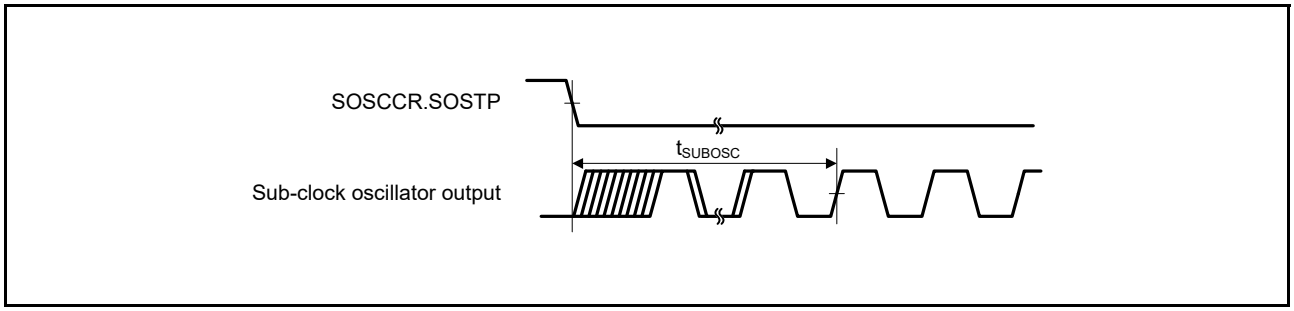


Figure 5.30 Sub-Clock Oscillation Start Timing

Table 5.30 Timing of Recovery from Low Power Consumption Modes (3)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VREFL0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from software standby mode*1	Low-speed mode	Sub-clock oscillator operating	t_{SBYSC}	—	600	750	µs	Figure 5.34

Note 1. The sub-clock continues oscillating in software standby mode during low-speed mode.

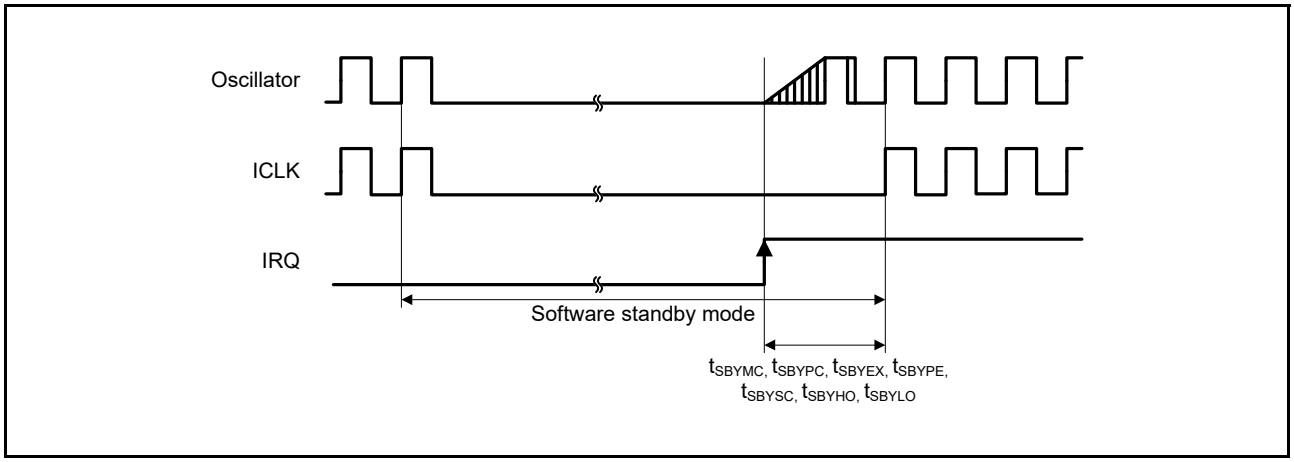


Figure 5.34 Software Standby Mode Recovery Timing

Table 5.31 Timing of Recovery from Low Power Consumption Modes (4)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VREFL0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from deep sleep mode*1	High-speed mode*2	t_{DSLP}	—	2	3.5	µs	Figure 5.35
	Middle-speed mode*3	t_{DSLP}	—	3	4	µs	
	Low-speed mode*4	t_{DSLP}	—	400	500	µs	

Note 1. Oscillators continue oscillating in deep sleep mode.
Note 2. When the frequency of the system clock is 32 MHz.
Note 3. When the frequency of the system clock is 12 MHz.
Note 4. When the frequency of the system clock is 32 kHz.

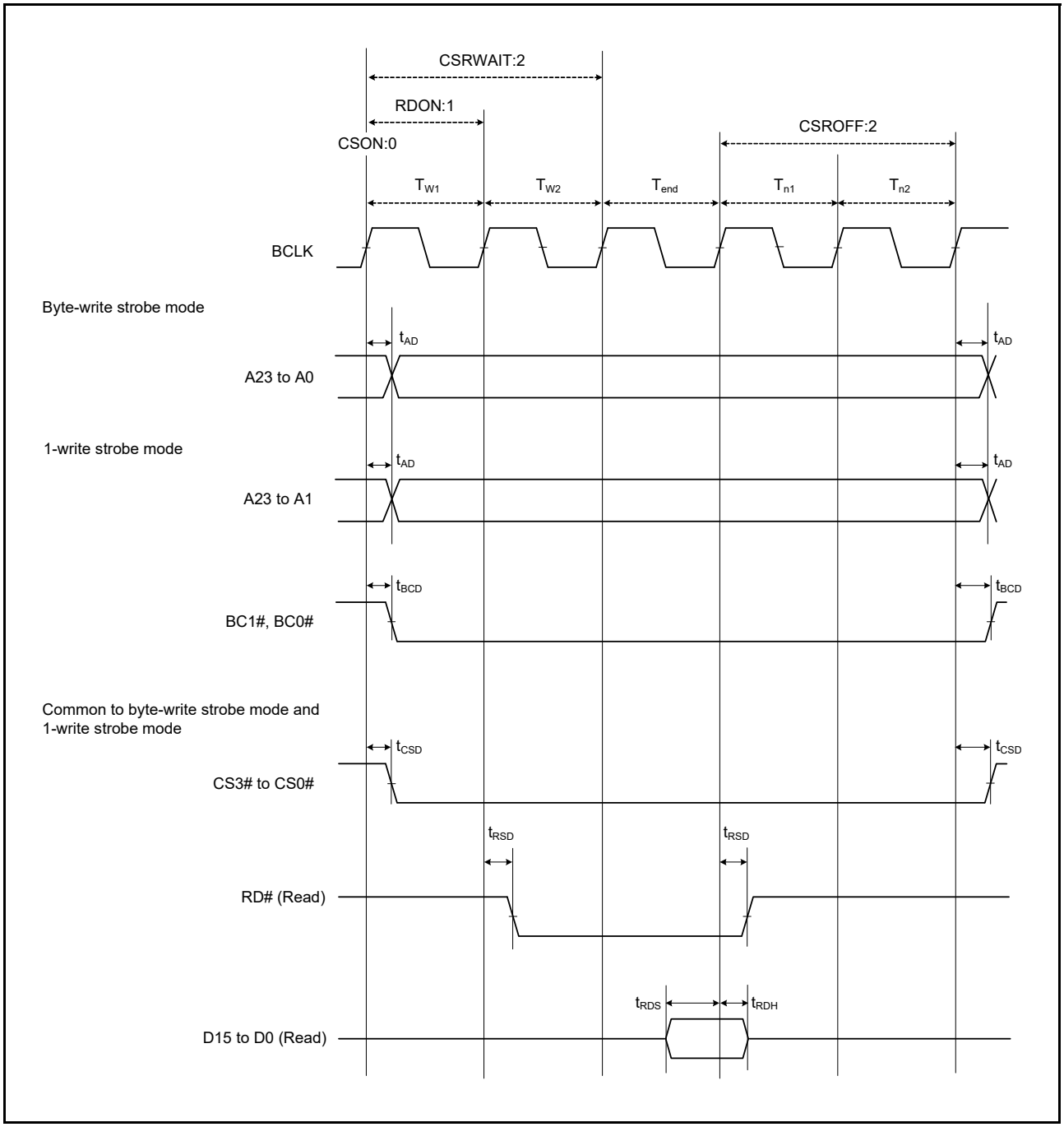
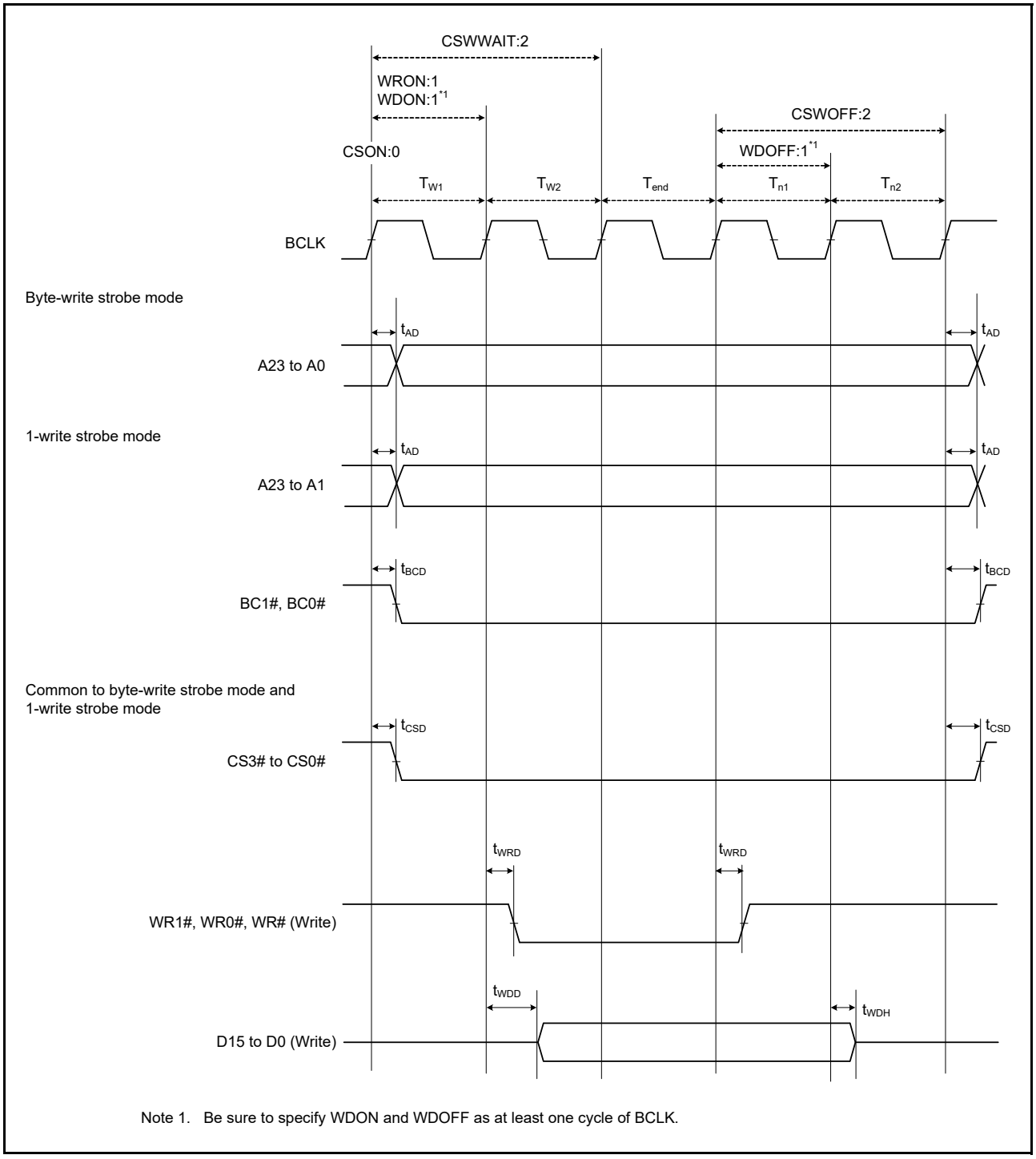


Figure 5.38 External Bus Timing/Normal Read Cycle (Bus Clock Synchronization)



Note 1. Be sure to specify WDON and WDOFF as at least one cycle of BCLK.

Figure 5.39 External Bus Timing/Normal Write Cycle (Bus Clock Synchronization)

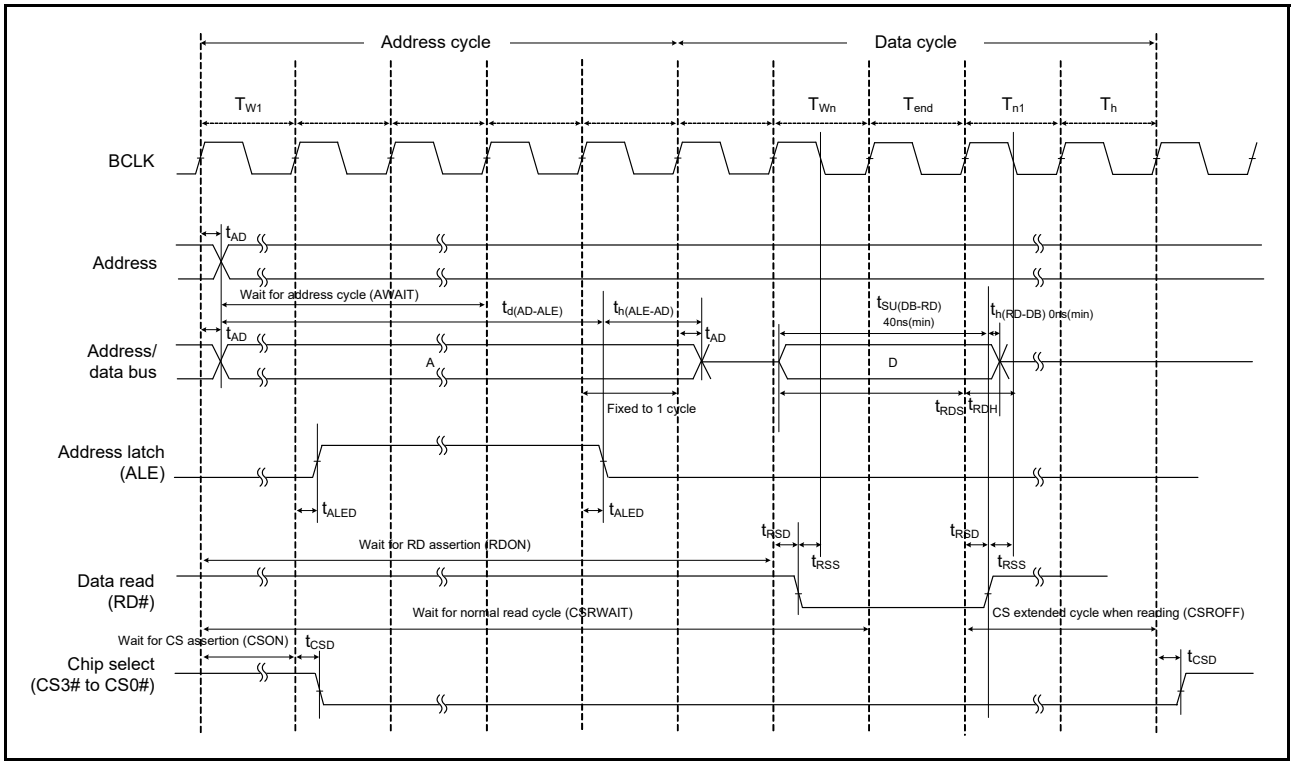


Figure 5.43 External Bus Timing/Read Access Operation Example (Multiplex)

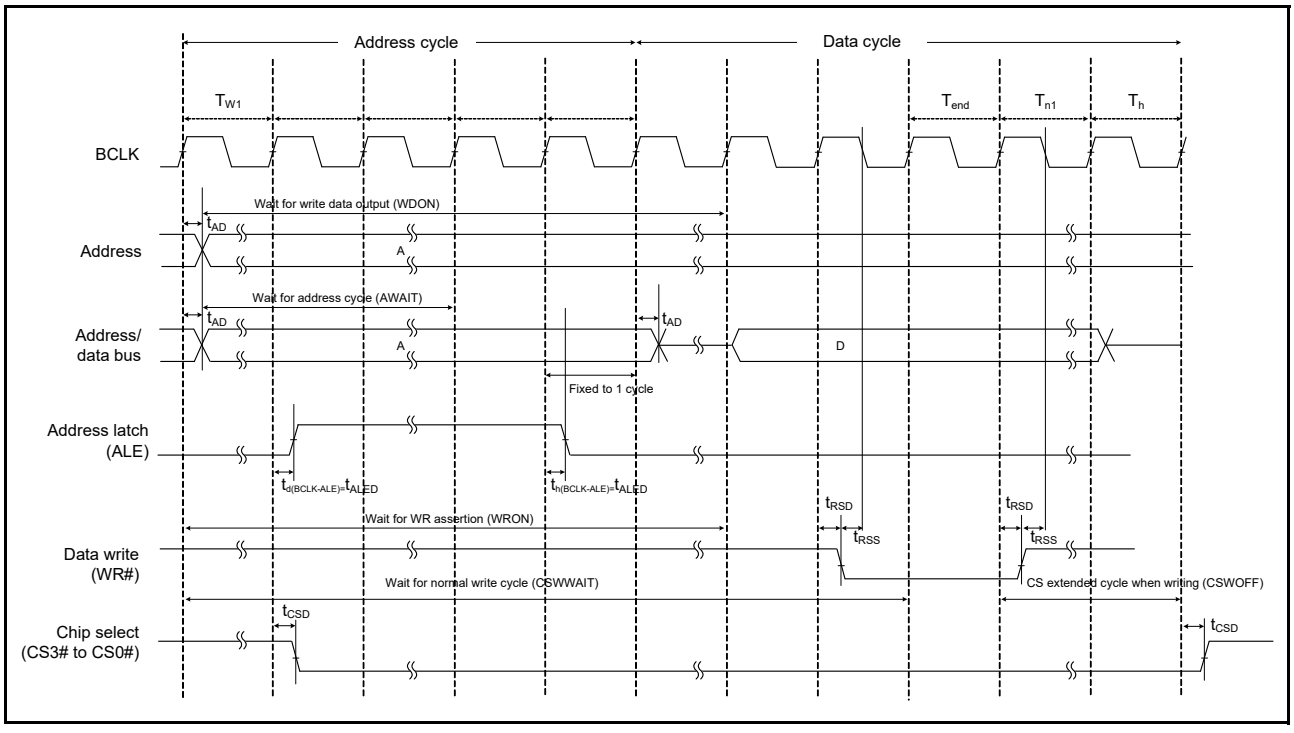


Figure 5.44 External Bus Timing/Write Access Operation Example (Multiplex)

Differential non-linearity error (DNL)

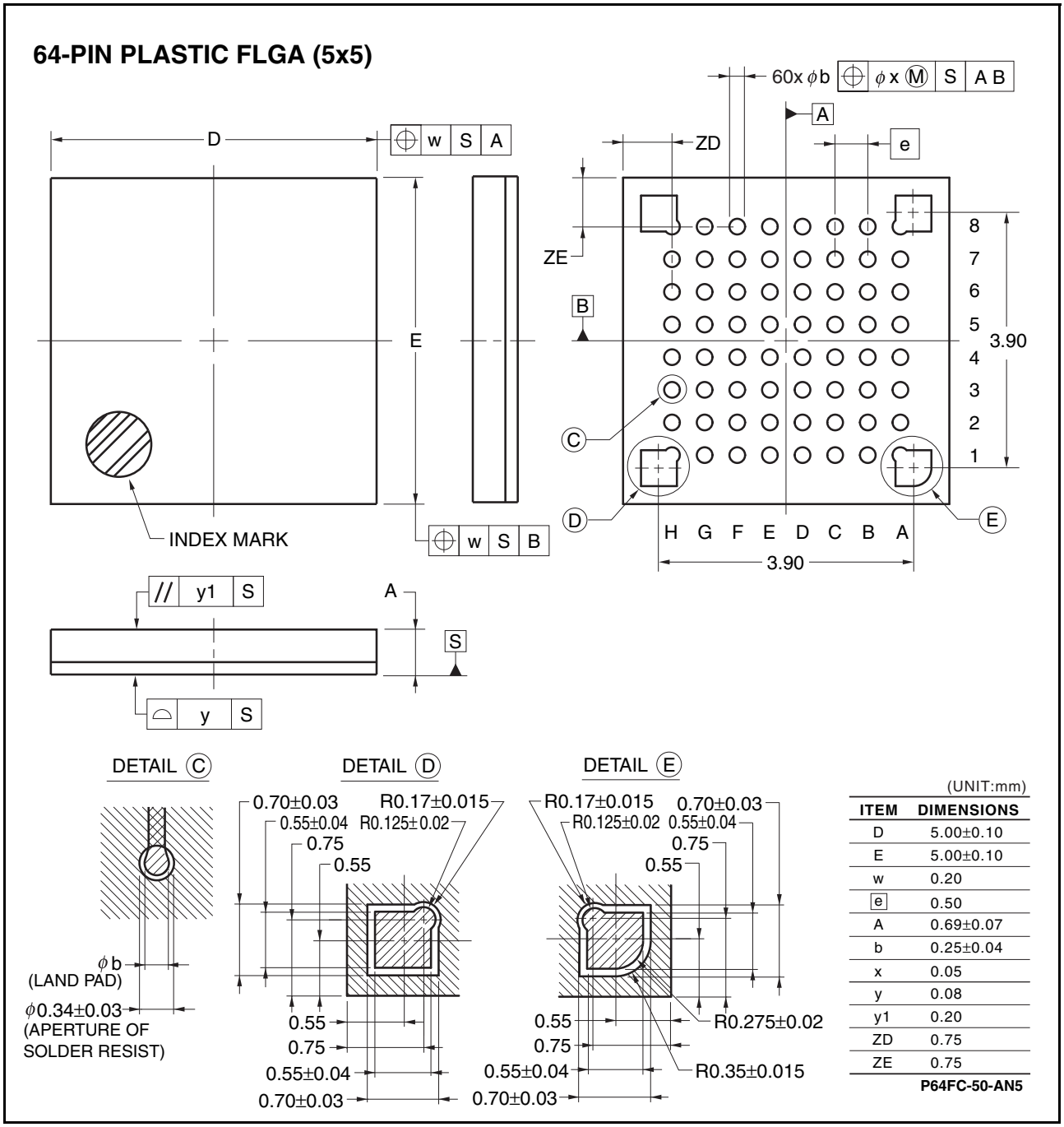
The differential non-linearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

Offset error

An offset error is the difference between a transition point of the ideal first output code and the actual first output code.

Full-scale error

A full-scale error is the difference between a transition point of the ideal last output code and the actual last output code.



(UNIT:mm)

ITEM	DIMENSIONS
D	5.00±0.10
E	5.00±0.10
w	0.20
e	0.50
A	0.69±0.07
b	0.25±0.04
x	0.05
y	0.08
y1	0.20
ZD	0.75
ZE	0.75

P64FC-50-AN5

Figure C 64 -Pin WFLGA (PWLG0064KA-A)

Rev.	Date	Description		Classification
		Page	Summary	
1.10	Oct 30, 2015	142	Table 5.45 A/D Conversion Characteristics (1): Conditions and Voltage Range of Analog Input (Max.), changed	
		143	Table 5.46 A/D Conversion Characteristics (2): Conditions changed	
		144	Table 5.47 A/D Conversion Characteristics (3): Conditions changed	
		145	Table 5.48 A/D Conversion Characteristics (4): Conditions changed	
		146	Table 5.49 A/D Conversion Characteristics (5): Conditions changed and Absolute accuracy (Test Conditions) deleted	
		153	Table 5.57 Characteristics of Power-On Reset Circuit and Voltage Detection Circuit (1), changed	TN-RX*-A137A/E
		154	Table 5.58 Characteristics of Power-On Reset Circuit and Voltage Detection Circuit (2), changed	
		155	Figure 5.73 Power-On Reset Timing and Figure 5.74 Voltage Detection Circuit Timing (Vdet0), changed	
		159	Table 5.62 ROM (Flash Memory for Code Storage) Characteristics (2) High-Speed Operating Mode: Note changed	
		160	Table 5.63 ROM (Flash Memory for Code Storage) Characteristics (3) Middle-Speed Operating Mode: Note changed	
		161	Table 5.65 E2 DataFlash Characteristics (2): high-speed operating mode, Note changed	
		161	Table 5.66 E2 DataFlash Characteristics (3): middle-speed operating mode, Conditions and Note changed	
		163	Figure 5.79 Connecting Capacitors (100 Pins), changed	
		164	Figure 5.80 Connecting Capacitors (64 Pins), changed	
		165	Figure 5.81 Connecting Capacitors (48 Pins), changed	
		Appendix 1. Package Dimensions		
		167	Figure B 100 -Pin LQFP (PLQP0100KB-B), changed	TN-RX*-A137A/E
		170	Figure E 64 -Pin LQFP (PLQP0064KB-C), changed	TN-RX*-A137A/E
		172	Figure G 48 -Pin LQFP (PLQP0048KB-B), changed	TN-RX*-A137A/E
1.20	Sep 28, 2018	Features		
		1	SD host interface (optional: one channel) SD memory/ SDIO 1-bit or 4-bit SD bus supported, Note deleted	TN-RX*-A145A/E
		1. Overview		
		6	Table 1.2 Comparison of Functions for Different Packages, changed (deletion of IRQ2 on 64-pin package)	
		6	Table 1.2 Comparison of Functions for Different Packages, Note 1 added	TN-RX*-A145A/E
		7	Table 1.3 List of Products: D Version (Ta = –40 to +85°C) (1/2), changed	TN-RX*-A145A/E
		9	Table 1.4 List of Products: G Version (Ta = –40 to +105°C) (1/2), changed	TN-RX*-A145A/E
		11	Figure 1.1 How to Read the Product Part Number, changed	TN-RX*-A145A/E
		16	Table 1.5 Pin Functions (4/4), changed (changes in description for VCC_USB)	TN-RX*-A201A/E
		24	Table 1.6 List of Pins and Pin Functions (100-Pin TFLGA) (2/3), changed (UPSEL was added to the column of P35)	
		24	Table 1.6 List of Pins and Pin Functions (100-Pin TFLGA) (2/3), changed (USB0_VBUS was added to the column of PB5)	
		26	Table 1.7 List of Pins and Pin Functions (100-Pin LFQFP) (1/3), changed (UPSEL was added to the column of P35)	
		29	Table 1.8 List of Pins and Pin Functions (64-Pin WFLGA) (1/2), changed (UPSEL was added to the column of P35)	
		30	Table 1.8 List of Pins and Pin Functions (64-Pin WFLGA) (2/2), changed (USB0_VBUS was added to the column of PB5)	
		31	Table 1.9 List of Pins and Pin Functions (64-Pin LFQFP/HWQFN) (1/2), changed (UPSEL was added to the column of P35)	
		31	Table 1.9 List of Pins and Pin Functions (64-Pin LQFP/HWQFN) (1/2), changed (USB0_VBUS was added to the column of PB5)	
		33	Table 1.10 List of Pins and Pin Functions (48-Pin LFQFP/HWQFN) (1/2), changed (UPSEL was added to the column of P35)	
		33	Table 1.10 List of Pins and Pin Functions (48-Pin LFQFP/HWQFN) (1/2), changed	TN-RX*-A145A/E
		5. Electrical Characteristics		
		92	Table 5.18 Output Values of Voltage (1), changed	TN-RX*-A201A/E
		92	Table 5.19 Output Values of Voltage (2), changed	TN-RX*-A201A/E

Rev.	Date	Description		Classification
		Page	Summary	
1.20	Sep 28, 2018	95	Figure 5.12 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 5.5 V When Normal Output is Selected (Reference Data), changed	TN-RX*-A201A/E
		124	Table 5.44 Timing of On-Chip Peripheral Modules (7), added	TN-RX*-A197A/E
		131	Figure 5.64 SD Host Interface Input/Output Signal Timing, added	TN-RX*-A197A/E
		132	Table 5.45 USB Characteristics (USB0_DP and USB0_DM Pin Characteristics) conditions, changed	

NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   ¾ The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   ¾ The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   ¾ The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   ¾ When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   ¾ The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.