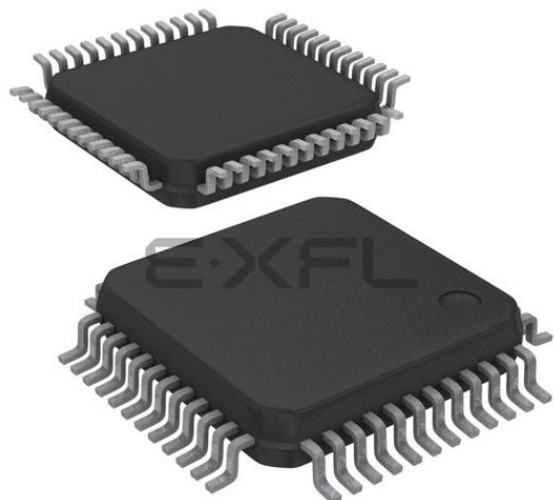




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Details

Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	54MHz
Connectivity	CANbus, I ² C, IrDA, SCI, SD/SDIO, SPI, SSI, USB OTG
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	30
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LFQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f52317adfl-30

Table 1.3 List of Products: D Version (T_a = –40 to +85°C) (2/2)

Group	Part No.	Order Part No.	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency	Security Function	SDHI	CAN	Operating Temperature
RX231	R5F52316ADFL	R5F52316ADFL#30	PLQP0048KB-B	256 Kbytes	32 Kbytes	8 Kbytes	54 MHz	Not available	Not available	Available	–40 to +85°C
	R5F52316CDFL	R5F52316CDFL#30						Not available	Not available	Not available	
	R5F52315ADLA	R5F52315ADLA#20	PTLG0100KA-A	128 Kbytes	32 Kbytes	8 Kbytes	54 MHz	Not available	Not available	Available	–40 to +85°C
	R5F52315CDLA	R5F52315CDLA#20						Not available	Not available	Not available	
	R5F52315ADFP	R5F52315ADFP#30	PLQP0100KB-B					Not available	Not available	Available	
	R5F52315CDFP	R5F52315CDFP#30						Not available	Not available	Not available	
	R5F52315CDLF	R5F52315CDLF#20	PWLG0064KA-A					Not available	Not available	Not available	
	R5F52315ADND	R5F52315ADND#U0	PWQN0064KC-A					Not available	Not available	Available	
	R5F52315CDND	R5F52315CDND#U0						Not available	Not available	Not available	
	R5F52315ADFM	R5F52315ADFM#30	PLQP0064KB-C					Not available	Not available	Available	
	R5F52315CDFM	R5F52315CDFM#30						Not available	Not available	Not available	
	R5F52315ADNE	R5F52315ADNE#U0	PWQN0048KB-A					Not available	Not available	Available	
	R5F52315CDNE	R5F52315CDNE#U0						Not available	Not available	Not available	
	R5F52315ADFL	R5F52315ADFL#30	PLQP0048KB-B					Not available	Not available	Available	
	R5F52315CDFL	R5F52315CDFL#30						Not available	Not available	Not available	
RX230	R5F52306ADLA	R5F52306ADLA#20	PTLG0100KA-A	256 Kbytes	32 Kbytes	8 Kbytes	54 MHz	Not available	Not available	Not available	–40 to +85°C
	R5F52306ADFP	R5F52306ADFP#30	PLQP0100KB-B					Not available	Not available	Not available	
	R5F52306ADLF	R5F52306ADLF#20	PWLG0064KA-A					Not available	Not available	Not available	
	R5F52306ADND	R5F52306ADND#U0	PWQN0064KC-A					Not available	Not available	Not available	
	R5F52306ADFM	R5F52306ADFM#30	PLQP0064KB-C					Not available	Not available	Not available	
	R5F52306ADNE	R5F52306ADNE#U0	PWQN0048KB-A					Not available	Not available	Not available	
	R5F52306ADFL	R5F52306ADFL#30	PLQP0048KB-B					Not available	Not available	Not available	
	R5F52305ADLA	R5F52305ADLA#20	PTLG0100KA-A	128 Kbytes				Not available	Not available	Not available	
	R5F52305ADFP	R5F52305ADFP#30	PLQP0100KB-B					Not available	Not available	Not available	
	R5F52305ADLF	R5F52305ADLF#20	PWLG0064KA-A					Not available	Not available	Not available	
	R5F52305ADND	R5F52305ADND#U0	PWQN0064KC-A					Not available	Not available	Not available	
	R5F52305ADFM	R5F52305ADFM#30	PLQP0064KB-C					Not available	Not available	Not available	
	R5F52305ADNE	R5F52305ADNE#U0	PWQN0048KB-A					Not available	Not available	Not available	
	R5F52305ADFL	R5F52305ADFL#30	PLQP0048KB-B					Not available	Not available	Not available	

Table 1.5 Pin Functions (4/4)

Classifications	Pin Name	I/O	Description
SD host interface	SDHI_D3 to SD_D0	I/O	SD data bus pins
	SDHI_CD	Input	SD card detection pin
	SDHI_WP	Input	SD write-protect signal
USB 2.0 host/ function module	VCC_USB	Input	Power supply pin for USB. Connect this pin to VCC or connect this pin to VSS via a 0.33 μ F smoothing capacitor for stabilizing the internal power supply.
	VSS_USB	Input	Ground pin for USB. Connect this pin to VSS.
	USB0_DP	I/O	D+ I/O pin of the USB on-chip transceiver.
	USB0_DM	I/O	D- I/O pin of the USB on-chip transceiver.
	USB0_VBUS	Input	USB cable connection monitor pin.
	USB0_EXICEN	Output	Low-power control signal for the OTG chip.
	USB0_VBUSEN	Output	VBUS (5 V) supply enable signal for the OTG chip.
	USB0_OVRCURA, USB0_OVRCURB	Input	External overcurrent detection pins.
	USB0_ID	Input	Mini-AB connector ID input pin during operation in OTG mode.
12-bit A/D converter	AN000 to AN007, AN016 to AN031	Input	Input pins for the analog signals to be processed by the A/D converter.
	ADTRG0#	Input	Input pin for the external trigger signal that start the A/D conversion.
12-bit D/A converter	DA0, DA1	Output	Analog output pins of the D/A converter.
Comparator B	CMPB0 to CMPB3	Input	Input pin for the analog signal to be processed by comparator B.
	CVREFB0 to CVREFB3	Input	Analog reference voltage supply pin for comparator B.
	CMPOB0 to CMPOB3	Output	Output pin for comparator B.
CTSU	TS0 to TS9, TS12, TS13, TS15 to TS20, TS22, TS23, TS27, TS30, TS33, TS35	Output	Electrostatic capacitance measurement pins (touch pins).
	TSCAP	Output	LPF connection pin.
Analog power supply	AVCC0	Input	Analog voltage supply pin for the 12-bit A/D converter and D/A converter. Connect this pin to VCC when not using the 12-bit A/D converter and D/A converter.
	AVSS0	Input	Analog ground pin for the 12-bit A/D converter and D/A converter. Connect this pin to VSS when not using the 12-bit A/D converter and D/A converter.
	VREFH0	Input	Analog reference voltage supply pin for the 12-bit A/D converter.
	VREFL0	Input	Analog reference ground pin for the 12-bit A/D converter.
	VREFH	Input	Analog reference voltage supply pin for the 12-bit D/A converter.
	VREFL	Input	Analog reference ground pin for the 12-bit D/A converter.
I/O ports	P03, P05, P07	I/O	3-bit input/output pins.
	P12 to P17	I/O	6-bit input/output pins.
	P20 to P27	I/O	8-bit input/output pins.
	P30 to P37	I/O	8-bit input/output pins (P35 input pin).
	P40 to P47	I/O	8-bit input/output pins.
	P50 to P55	I/O	6-bit input/output pins.
	PA0 to PA7	I/O	8-bit input/output pins.
	PB0 to PB7	I/O	8-bit input/output pins.
	PC0 to PC7	I/O	8-bit input/output pins.
	PD0 to PD7	I/O	8-bit input/output pins.
	PE0 to PE7	I/O	8-bit input/output pins.
	PH0 to PH3	I/O	4-bit input/output pins.
	PJ3	I/O	1-bit input/output pin.

Table 1.7 List of Pins and Pin Functions (100-Pin LQFP) (3/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCI, RSPI, RIIIC, RSCAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
79		PD7	D7[A7/D7]	MTIC5U/POE0#				IRQ7/AN031
80		PD6	D6[A6/D6]	MTIC5V/POE1#				IRQ6/AN030
81		PD5	D5[A5/D5]	MTIC5W/POE2#				IRQ5/AN029
82		PD4	D4[A4/D4]	POE3#				IRQ4/AN028
83		PD3	D3[A3/D3]	POE8#				IRQ3/AN027
84		PD2	D2[A2/D2]	MTIOC4D				IRQ2/AN026
85		PD1	D1[A1/D1]	MTIOC4B				IRQ1/AN025
86		PD0	D0[A0/D0]					IRQ0/AN024
87		P47						AN007
88		P46						AN006
89		P45						AN005
90		P44						AN004
91		P43						AN003
92		P42						AN002
93		P41						AN001
94	VREFL0							
95		P40						AN000
96	VREFH0							
97	AVCC0							
98		P07						ADTRG0#
99	AVSS0							
100		P05						DA1

Note 1. RX230: PH0/CACREF, PH1/IRQ0/TMO0, PH2/IRQ1/TMRI0, PH3/TMCI0
 RX231: VSS_USB, USB0_DP, USB0_DM, VCC_USB

Table 4.1 List of I/O Registers (Address Order) (8/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
0008 901Eh	S12AD	A/D Self-Diagnosis Data Register	ADDRD	16	16	2 or 3 PCLKB	2 ICLK
0008 9020h	S12AD	A/D Data Register 0	ADDR0	16	16	2 or 3 PCLKB	2 ICLK
0008 9022h	S12AD	A/D Data Register 1	ADDR1	16	16	2 or 3 PCLKB	2 ICLK
0008 9024h	S12AD	A/D Data Register 2	ADDR2	16	16	2 or 3 PCLKB	2 ICLK
0008 9026h	S12AD	A/D Data Register 3	ADDR3	16	16	2 or 3 PCLKB	2 ICLK
0008 9028h	S12AD	A/D Data Register 4	ADDR4	16	16	2 or 3 PCLKB	2 ICLK
0008 902Ah	S12AD	A/D Data Register 5	ADDR5	16	16	2 or 3 PCLKB	2 ICLK
0008 902Ch	S12AD	A/D Data Register 6	ADDR6	16	16	2 or 3 PCLKB	2 ICLK
0008 902Eh	S12AD	A/D Data Register 7	ADDR7	16	16	2 or 3 PCLKB	2 ICLK
0008 9040h	S12AD	A/D Data Register 16	ADDR16	16	16	2 or 3 PCLKB	2 ICLK
0008 9042h	S12AD	A/D Data Register 17	ADDR17	16	16	2 or 3 PCLKB	2 ICLK
0008 9044h	S12AD	A/D Data Register 18	ADDR18	16	16	2 or 3 PCLKB	2 ICLK
0008 9046h	S12AD	A/D Data Register 19	ADDR19	16	16	2 or 3 PCLKB	2 ICLK
0008 9048h	S12AD	A/D Data Register 20	ADDR20	16	16	2 or 3 PCLKB	2 ICLK
0008 904Ah	S12AD	A/D Data Register 21	ADDR21	16	16	2 or 3 PCLKB	2 ICLK
0008 904Ch	S12AD	A/D Data Register 22	ADDR22	16	16	2 or 3 PCLKB	2 ICLK
0008 904Eh	S12AD	A/D Data Register 23	ADDR23	16	16	2 or 3 PCLKB	2 ICLK
0008 9050h	S12AD	A/D Data Register 24	ADDR24	16	16	2 or 3 PCLKB	2 ICLK
0008 9052h	S12AD	A/D Data Register 25	ADDR25	16	16	2 or 3 PCLKB	2 ICLK
0008 9055h	S12AD	A/D Data Register 26	ADDR26	16	16	2 or 3 PCLKB	2 ICLK
0008 9056h	S12AD	A/D Data Register 27	ADDR27	16	16	2 or 3 PCLKB	2 ICLK
0008 9058h	S12AD	A/D Data Register 28	ADDR28	16	16	2 or 3 PCLKB	2 ICLK
0008 905Ah	S12AD	A/D Data Register 29	ADDR29	16	16	2 or 3 PCLKB	2 ICLK
0008 905Ch	S12AD	A/D Data Register 30	ADDR30	16	16	2 or 3 PCLKB	2 ICLK
0008 905Eh	S12AD	A/D Data Register 31	ADDR31	16	16	2 or 3 PCLKB	2 ICLK
0008 907Ah	S12AD	A/D Disconnection Detection Control Register	ADDISCR	8	8	2 or 3 PCLKB	2 ICLK
0008 907Dh	S12AD	A/D Event Link Control Register	ADELCCR	8	8	2 or 3 PCLKB	2 ICLK
0008 9080h	S12AD	A/D Group Scan Priority Control Register	ADGSPCR	16	16	2 or 3 PCLKB	2 ICLK
0008 908Ah	S12AD	A/D High-Side/Low-Side Reference Voltage Control Register	ADHVREFCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 908Ch	S12AD	A/D Compare Function Window A/B Status Monitor Register	ADWINMON	8	8	2 or 3 PCLKB	2 ICLK
0008 9090h	S12AD	A/D Compare Function Control Register	ADCMPCR	16	16	2 or 3 PCLKB	2 ICLK
0008 9092h	S12AD	A/D Compare Function Window A Extended Input Select Register	ADCMPSER	8	8	2 or 3 PCLKB	2 ICLK
0008 9093h	S12AD	A/D Compare Function Window A Extended Input Comparison Condition Setting Register	ADCMPLER	8	8	2 or 3 PCLKB	2 ICLK
0008 9094h	S12AD	A/D Compare Function Window A Channel Select Register 0	ADCMPSR0	16	16	2 or 3 PCLKB	2 ICLK
0008 9096h	S12AD	A/D Compare Function Window A Channel Select Register 1	ADCMPSR1	16	16	2 or 3 PCLKB	2 ICLK
0008 9098h	S12AD	A/D Compare Function Window A Comparison Condition Setting Register 0	ADCMPLR0	16	16	2 or 3 PCLKB	2 ICLK
0008 909Ah	S12AD	A/D Compare Function Window A Comparison Condition Setting Register 1	ADCMPLR1	16	16	2 or 3 PCLKB	2 ICLK
0008 909Ch	S12AD	A/D Compare Function Window A Lower-Side Level Setting Register	ADCMPSR0	16	16	2 or 3 PCLKB	2 ICLK
0008 909Eh	S12AD	A/D Compare Function Window A Upper-Side Level Setting Register	ADCMPSR1	16	16	2 or 3 PCLKB	2 ICLK
0008 90A0h	S12AD	A/D Compare Function Window A Channel Status Register 0	ADCMPSR0	16	16	2 or 3 PCLKB	2 ICLK
0008 90A2h	S12AD	A/D Compare Function Window A Channel Status Register 1	ADCMPSR1	16	16	2 or 3 PCLKB	2 ICLK
0008 90A4h	S12AD	A/D Compare Function Window A Extended Input Channel Status Register	ADCMPSER	16	16	2 or 3 PCLKB	2 ICLK
0008 90A6h	S12AD	A/D Compare Function Window B Channel Select Register	ADCMPSNR	8	8	2 or 3 PCLKB	2 ICLK
0008 90A8h	S12AD	A/D Compare Function Window B Lower-Side Level Setting Register	ADWINLLB	16	16	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (29/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
000A 8494h	RSCAN	Receive Buffer Register 15BL	RMTS15	16	16	2 or 3 PCLKB	2 ICLK
000A 8496h	RSCAN	Receive Buffer Register 15BH	RMPTR15	16	16	2 or 3 PCLKB	2 ICLK
000A 8498h	RSCAN	Receive Buffer Register 15CL	RMDF015	16	16	2 or 3 PCLKB	2 ICLK
000A 849Ah	RSCAN	Receive Buffer Register 15CH	RMDF115	16	16	2 or 3 PCLKB	2 ICLK
000A 849Ch	RSCAN	Receive Buffer Register 15DL	RMDF215	16	16	2 or 3 PCLKB	2 ICLK
000A 849Eh	RSCAN	Receive Buffer Register 15DH	RMDF315	16	16	2 or 3 PCLKB	2 ICLK
000A 8580h to 000A 859Fh	RSCAN	RAM Test Register 0 to RAM Test Register 15	RPGACC0 to RPGACC15	16	16	2 or 3 PCLKB	2 ICLK
000A 85A0h	RSCAN	Receive FIFO Access Register 0AL	RFIDL0	16	16	2 or 3 PCLKB	2 ICLK
000A 85A0h	RSCAN	RAM Test Register 16	RPGACC16	16	16	2 or 3 PCLKB	2 ICLK
000A 85A2h	RSCAN	Receive FIFO Access Register 0AH	RFIDH0	16	16	2 or 3 PCLKB	2 ICLK
000A 85A2h	RSCAN	RAM Test Register 17	RPGACC17	16	16	2 or 3 PCLKB	2 ICLK
000A 85A4h	RSCAN	Receive FIFO Access Register 0BL	RFTS0	16	16	2 or 3 PCLKB	2 ICLK
000A 85A4h	RSCAN	RAM Test Register 18	RPGACC18	16	16	2 or 3 PCLKB	2 ICLK
000A 85A6h	RSCAN	Receive FIFO Access Register 0BH	RFPTR0	16	16	2 or 3 PCLKB	2 ICLK
000A 85A6h	RSCAN	RAM Test Register 19	RPGACC19	16	16	2 or 3 PCLKB	2 ICLK
000A 85A8h	RSCAN	Receive FIFO Access Register 0CL	RFDF00	16	16	2 or 3 PCLKB	2 ICLK
000A 85A8h	RSCAN	RAM Test Register 20	RPGACC20	16	16	2 or 3 PCLKB	2 ICLK
000A 85AAh	RSCAN	Receive FIFO Access Register 0CH	RFDF10	16	16	2 or 3 PCLKB	2 ICLK
000A 85AAh	RSCAN	RAM Test Register 21	RPGACC21	16	16	2 or 3 PCLKB	2 ICLK
000A 85ACh	RSCAN	Receive FIFO Access Register 0DL	RFDF20	16	16	2 or 3 PCLKB	2 ICLK
000A 85ACh	RSCAN	RAM Test Register 22	RPGACC22	16	16	2 or 3 PCLKB	2 ICLK
000A 85AEh	RSCAN	Receive FIFO Access Register 0DH	RFDF30	16	16	2 or 3 PCLKB	2 ICLK
000A 85AEh	RSCAN	RAM Test Register 23	RPGACC23	16	16	2 or 3 PCLKB	2 ICLK
000A 85B0h	RSCAN	Receive FIFO Access Register 1AL	RFIDL1	16	16	2 or 3 PCLKB	2 ICLK
000A 85B0h	RSCAN	RAM Test Register 24	RPGACC24	16	16	2 or 3 PCLKB	2 ICLK
000A 85B2h	RSCAN	Receive FIFO Access Register 1AH	RFIDH1	16	16	2 or 3 PCLKB	2 ICLK
000A 85B2h	RSCAN	RAM Test Register 25	RPGACC25	16	16	2 or 3 PCLKB	2 ICLK
000A 85B4h	RSCAN	Receive FIFO Access Register 1BL	RFTS1	16	16	2 or 3 PCLKB	2 ICLK
000A 85B4h	RSCAN	RAM Test Register 26	RPGACC26	16	16	2 or 3 PCLKB	2 ICLK
000A 85B6h	RSCAN	Receive FIFO Access Register 1BH	RFPTR1	16	16	2 or 3 PCLKB	2 ICLK
000A 85B6h	RSCAN	RAM Test Register 27	RPGACC27	16	16	2 or 3 PCLKB	2 ICLK
000A 85B8h	RSCAN	Receive FIFO Access Register 1CL	RFDF01	16	16	2 or 3 PCLKB	2 ICLK
000A 85B8h	RSCAN	RAM Test Register 28	RPGACC28	16	16	2 or 3 PCLKB	2 ICLK
000A 85BAh	RSCAN	Receive FIFO Access Register 1CH	RFDF11	16	16	2 or 3 PCLKB	2 ICLK
000A 85BAh	RSCAN	RAM Test Register 29	RPGACC29	16	16	2 or 3 PCLKB	2 ICLK
000A 85BCh	RSCAN	Receive FIFO Access Register 1DL	RFDF21	16	16	2 or 3 PCLKB	2 ICLK
000A 85BCh	RSCAN	RAM Test Register 30	RPGACC30	16	16	2 or 3 PCLKB	2 ICLK
000A 85BEh	RSCAN	Receive FIFO Access Register 1DH	RFDF31	16	16	2 or 3 PCLKB	2 ICLK
000A 85BEh	RSCAN	RAM Test Register 31	RPGACC31	16	16	2 or 3 PCLKB	2 ICLK
000A 85C0h to 000A 85DEh	RSCAN	RAM Test Register 32 to RAM Test Register 47	RPGACC32 to RPGACC47	16	16	2 or 3 PCLKB	2 ICLK
000A 85E0h	RSCAN0	Transmit/Receive FIFO Access Register 0AL	CFIDL0	16	16	2 or 3 PCLKB	2 ICLK
000A 85E0h	RSCAN	RAM Test Register 48	RPGACC48	16	16	2 or 3 PCLKB	2 ICLK
000A 85E2h	RSCAN0	Transmit/Receive FIFO Access Register 0AH	CFIDH0	16	16	2 or 3 PCLKB	2 ICLK
000A 85E2h	RSCAN	RAM Test Register 49	RPGACC49	16	16	2 or 3 PCLKB	2 ICLK
000A 85E4h	RSCAN0	Transmit/Receive FIFO Access Register 0BL	CFTS0	16	16	2 or 3 PCLKB	2 ICLK
000A 85E4h	RSCAN	RAM Test Register 50	RPGACC50	16	16	2 or 3 PCLKB	2 ICLK
000A 85E6h	RSCAN0	Transmit/Receive FIFO Access Register 0BH	CFPTR0	16	16	2 or 3 PCLKB	2 ICLK
000A 85E6h	RSCAN	RAM Test Register 51	RPGACC51	16	16	2 or 3 PCLKB	2 ICLK
000A 85E8h	RSCAN0	Transmit/Receive FIFO Access Register 0CL	CFDF00	16	16	2 or 3 PCLKB	2 ICLK
000A 85E8h	RSCAN	RAM Test Register 52	RPGACC52	16	16	2 or 3 PCLKB	2 ICLK

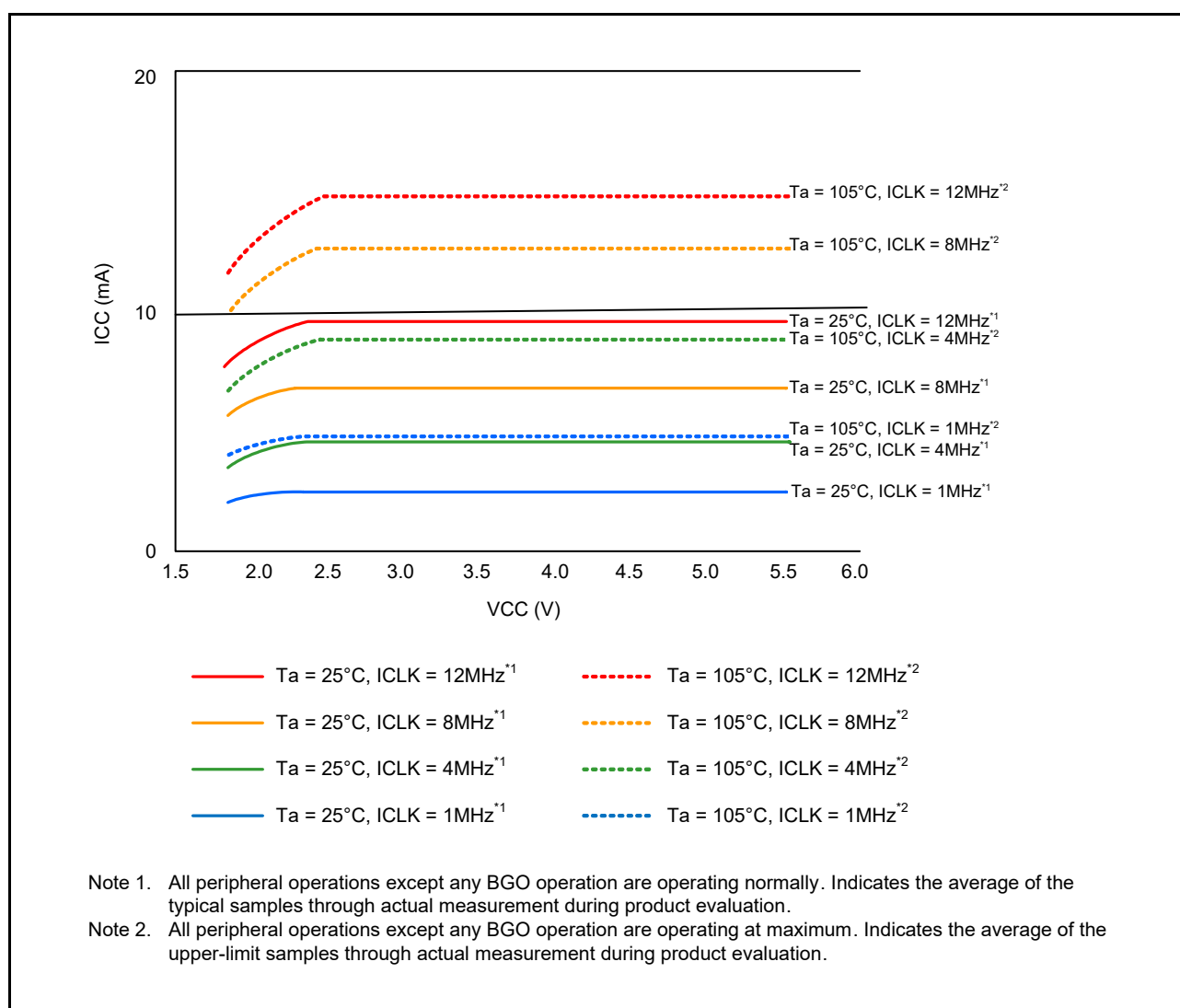


Figure 5.2 Voltage Dependency in Middle-Speed Operating Mode (Reference Data)

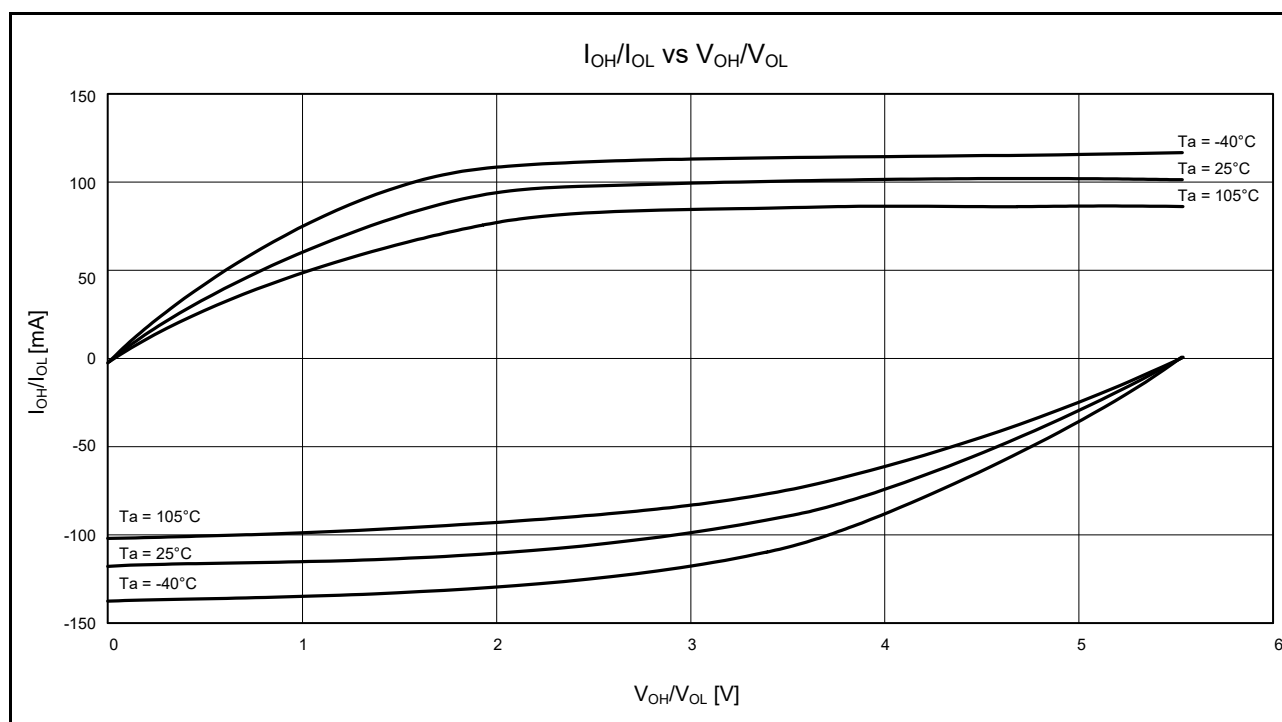


Figure 5.17 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at $V_{CC} = 5.5$ V When High-Drive Output is Selected (Reference Data)

5.3 AC Characteristics

5.3.1 Clock Timing

Table 5.21 Operating Frequency Value (High-Speed Operating Mode)

Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} = \text{AVCC0} \leq 5.5\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VREFL0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Symbol	VCC				Unit
			$1.8\text{ V} \leq \text{VCC} < 2.4\text{ V}$	$2.4\text{ V} \leq \text{VCC} < 2.7\text{ V}$	$2.7\text{ V} \leq \text{VCC} \leq 5.5\text{ V}$	When USB is in Use*3	
Maximum operating frequency*4	System clock (ICLK)	f_{max}	8	16	54	54	MHz
	FlashIF clock (FCLK)*1, *2		8	16	32	32	
	Peripheral module clock (PCLKA)		8	16	54	54	
	Peripheral module clock (PCLKB)		8	16	32	32	
	Peripheral module clock (PCLKD)		8	32	54	54	
	External bus clock (BCLK)		8	16	32	32	
	BCLK pin output		8	8	16	16	
	USB clock (UCLK)	f_{usb}	—	—	—	48	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When FCLK is in use at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note 2. The frequency accuracy of FCLK must be within $\pm 3.5\%$.

Note 3. The VCC_USB range is 3.0 to 5.5 V when the USB clock is in use.

Note 4. The maximum operating frequency listed above does not include errors of the external oscillator and internal oscillator. For details on the range for the guaranteed operation, see Table 5.26, Clock Timing.

Table 5.22 Operating Frequency Value (Middle-Speed Operating Mode)

Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} = \text{AVCC0} \leq 5.5\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VREFL0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Symbol	VCC				Unit
			$1.8\text{ V} \leq \text{VCC} < 2.4\text{ V}$	$2.4\text{ V} \leq \text{VCC} < 2.7\text{ V}$	$2.7\text{ V} \leq \text{VCC} \leq 5.5\text{ V}$	When USB is in Use*3	
Maximum operating frequency*4	System clock (ICLK)	f_{max}	8	12	12	12	MHz
	FlashIF clock (FCLK)*1, *2		8	12	12	12	
	Peripheral module clock (PCLKA)		8	12	12	12	
	Peripheral module clock (PCLKB)		8	12	12	12	
	Peripheral module clock (PCLKD)		8	12	12	12	
	External bus clock (BCLK)		8	12	12	12	
	BCLK pin output		8	8	12	12	
	USB clock (UCLK)	f_{usb}	—	—	—	48	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note 2. The frequency accuracy of FCLK must be within $\pm 3.5\%$.

Note 3. The VCC_USB range is 3.0 to 5.5 V when the USB clock is in use.

Note 4. The maximum operating frequency listed above does not include errors of the external oscillator and internal oscillator. For details on the range for the guaranteed operation, see Table 5.26, Clock Timing.

Table 5.26 Clock TimingConditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} = \text{AVCC0} \leq 5.5\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VREFL0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
EXTAL external clock input cycle time		t _{Xcyc}	50	—	—	ns	Figure 5.23
EXTAL external clock input high pulse width		t _{XH}	20	—	—	ns	
EXTAL external clock input low pulse width		t _{XL}	20	—	—	ns	
EXTAL external clock rise time		t _{Xr}	—	—	5	ns	
EXTAL external clock fall time		t _{Xf}	—	—	5	ns	
EXTAL external clock input wait time*1		t _{XWT}	0.5	—	—	μs	
Main clock oscillator oscillation frequency*2	2.4 ≤ VCC ≤ 5.5	f _{MAIN}	1	—	20	MHz	
	1.8 ≤ VCC < 2.4		1	—	8		
Main clock oscillation stabilization time (crystal)*2		t _{MAINOSC}	—	3	—	ms	Figure 5.24
Main clock oscillation stabilization time (ceramic resonator)*2		t _{MAINOSC}	—	50	—	μs	
LOCO clock oscillation frequency		f _{LOCO}	3.44	4.0	4.56	MHz	
LOCO clock oscillation stabilization time		t _{LOCO}	—	—	0.5	μs	Figure 5.25
IWDT-dedicated clock oscillation frequency		f _{ILOCO}	12.75	15	17.25	kHz	
IWDT-dedicated clock oscillation stabilization time		t _{ILOCO}	—	—	50	μs	Figure 5.26
HOCO clock oscillation frequency		f _{HOCO} (32 MHz)	31.52	32	32.48	MHz	T _a = −40 to + 85°C
			31.68	32	32.32		T _a = 0 to + 55°C
			31.36	32	32.64		T _a = −40 to +105°C
		f _{HOCO} (54 MHz)	53.19	54	54.81	MHz	T _a = −40 to + 85°C
			53.46	54	54.54		T _a = 0 to + 55°C
			52.92	54	55.08		T _a = −40 to +105°C
HOCO clock oscillation stabilization time		t _{HOCO}	—	—	30	μs	Figure 5.28
PLL input frequency*3		f _{PLLIN}	4	—	12.5	MHz	
PLL circuit oscillation frequency*3		f _{PLL}	24	—	54	MHz	
PLL clock oscillation stabilization time		t _{PLL}	—	—	50	μs	Figure 5.29
PLL free-running oscillation frequency		f _{PLLFR}	—	8	—	MHz	
USBPLL input frequency*5		f _{PLLIN}	—	6, 8*6	—	MHz	
USBPLL circuit oscillation frequency*5		f _{PLL}	—	48*6	—	MHz	
USBPLL clock oscillation stabilization time		t _{PLL}	—	—	50	μs	Figure 5.29
Sub-clock oscillator oscillation frequency*7		f _{SUB}	—	32.768	—	kHz	
Sub-clock oscillation stabilization time*4		t _{SUBOSC}	—	0.5	—	s	Figure 5.30

Note 1. Time until the clock can be used after the main clock oscillator stop bit (MOSCCR.MOSTP) is set to 0 (operating).

Note 2. Reference values when an 8-MHz resonator is used.

When specifying the main clock oscillator stabilization time, set the MOSCWTCR register with a stabilization time value that is equal to or greater than the resonator-manufacturer-recommended value.

After the MOSCCR.MOSTP bit is changed to enable the main clock oscillator, confirm that the OSCOVFSR.MOOVF flag has become 1, and then start using the main clock.

Note 3. The VCC range should be 2.4 to 5.5 V when the PLL is used.

Note 4. Reference values when a 32.768-kHz resonator is used.

After the setting of the SOSCCR.SOSTP bit or RCR3.RTCEN bit is changed to operate the sub-clock oscillator, only start using the sub-clock after the sub-clock oscillation stabilization wait time that is equal to or greater than the oscillator-manufacturer-recommended value has elapsed.

Note 5. The VCC range should be 3.0 to 5.5 V when the USBPLL is used.

Note 6. The input frequency can be set to 6 or 8 MHz and the oscillation frequency can be set to 48 MHz only.

Note 7. Only 32.768 kHz can be used.

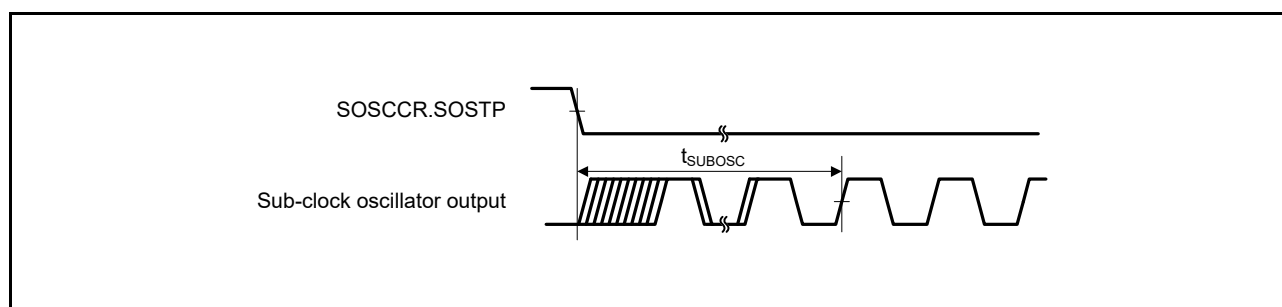


Figure 5.30 Sub-Clock Oscillation Start Timing

Table 5.40 Timing of On-Chip Peripheral Modules (3)Conditions: $1.8\text{ V} \leq VCC = VCC_USB = AVCC0 \leq 5.5\text{ V}$, $VSS = AVSS0 = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)		t_{SPcyc}	4	65536	t_{Pcyc}	Figure 5.54
	SCK clock cycle input (slave)			6	65536	t_{Pcyc}	
	SCK clock high pulse width		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time		t_{SPCKr} , t_{SPCKf}	—	20	ns	
	Data input setup time (master)	2.7 V or above	t_{SU}	65	—	ns	Figure 5.55, Figure 5.56
		1.8 V or above		95	—		
	Data input setup time (slave)			40	—		
	Data input hold time		t_H	40	—	ns	
	SSL input setup time		t_{LEAD}	3	—	t_{SPcyc}	
	SSL input hold time		t_{LAG}	3	—	t_{SPcyc}	
	Data output delay time (master)		t_{OD}	—	40	ns	
	Data output delay time (slave)	2.7 V or above		—	65		
		1.8 V or above		—	100		
	Data output hold time (master)	2.7 V or above	t_{OH}	−10	—	ns	
		1.8 V or above		−20	—		
	Data output hold time (slave)			−10	—		
	Data rise/fall time		t_{Dr} , t_{Df}	—	20	ns	
	SSL input rise/fall time		t_{SSLr} , t_{SSLf}	—	20	ns	
	Slave access time		t_{SA}	—	6	t_{Pcyc}	Figure 5.57, Figure 5.58
	Slave output release time		t_{REL}	—	6	t_{Pcyc}	

Note 1. t_{Pcyc} : PCLK cycle

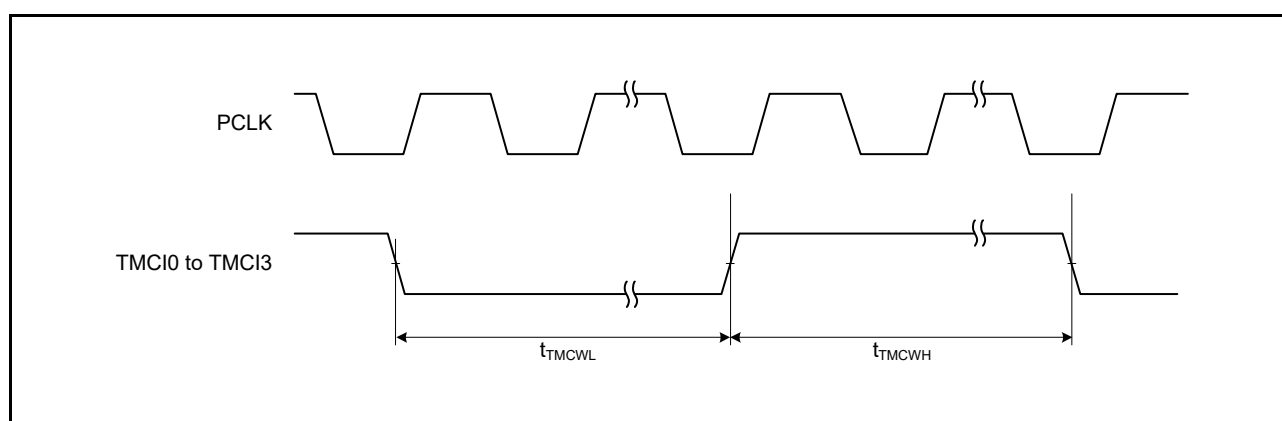


Figure 5.49 TMR Clock Input Timing

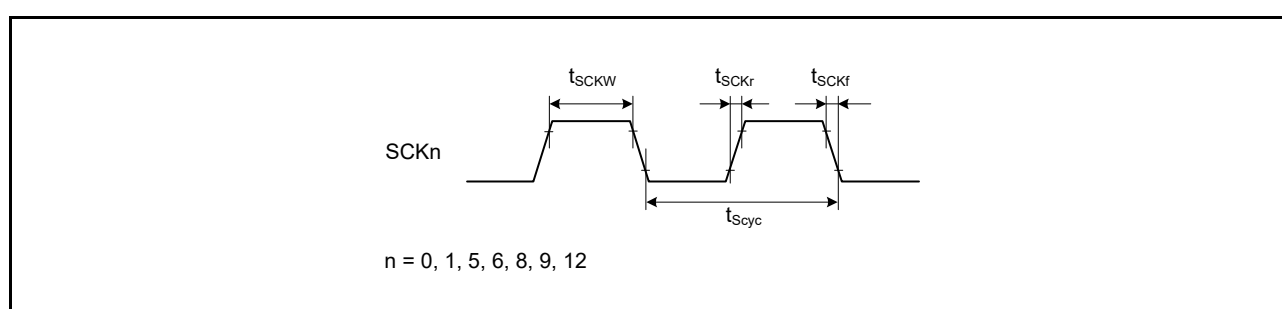


Figure 5.50 SCK Clock Input Timing

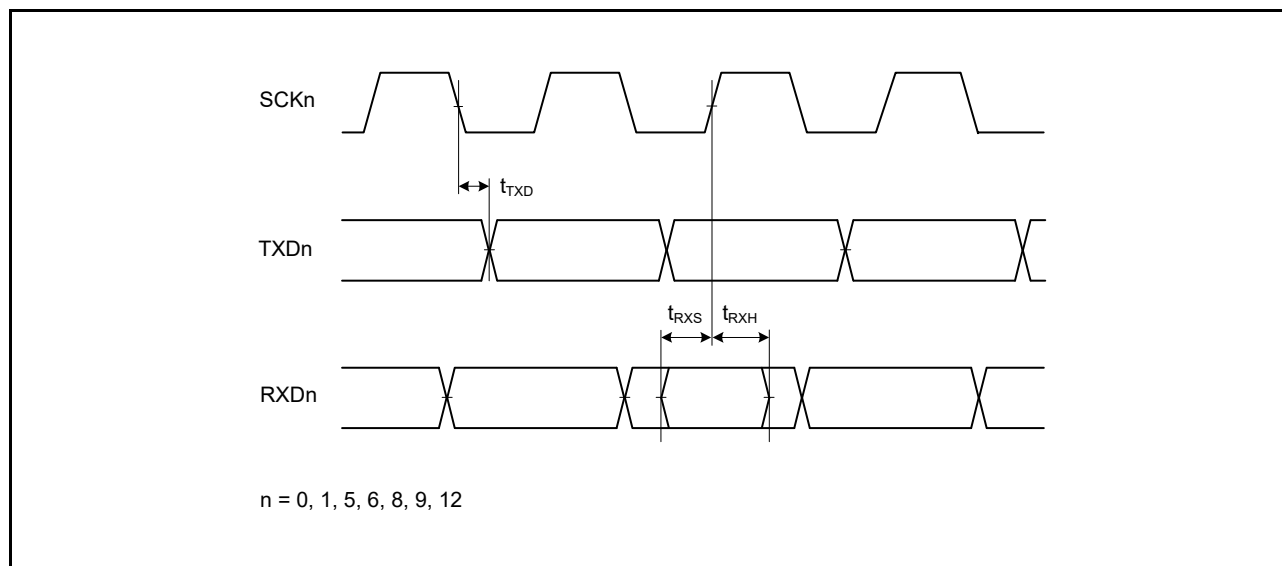


Figure 5.51 SCI Input/Output Timing: Clock Synchronous Mode

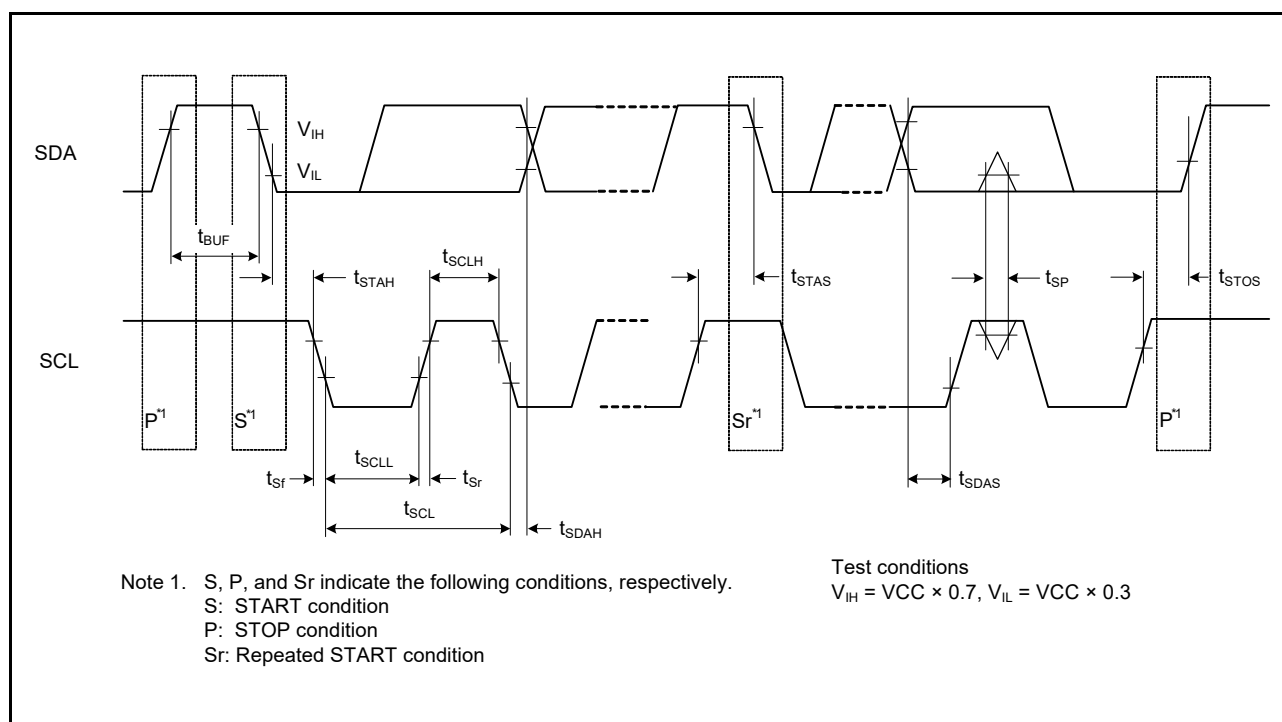
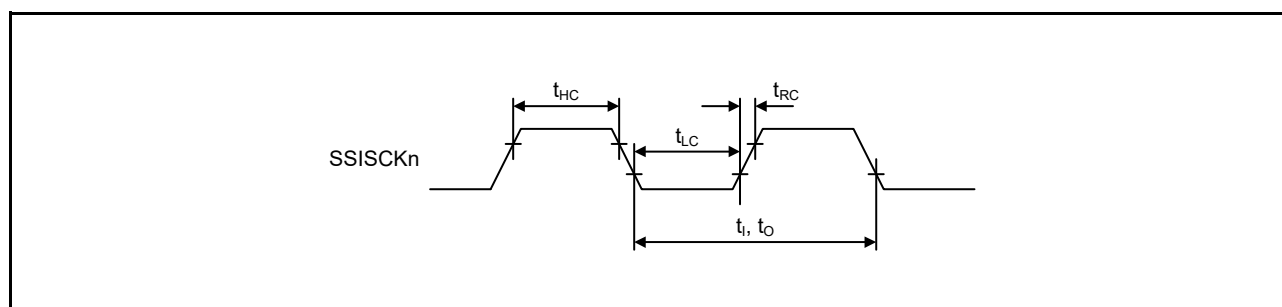
Figure 5.59 RIIC Bus Interface Input/Output Timing and Simple I²C Bus Interface Input/Output Timing

Figure 5.60 SSI Clock Input/Output Timing

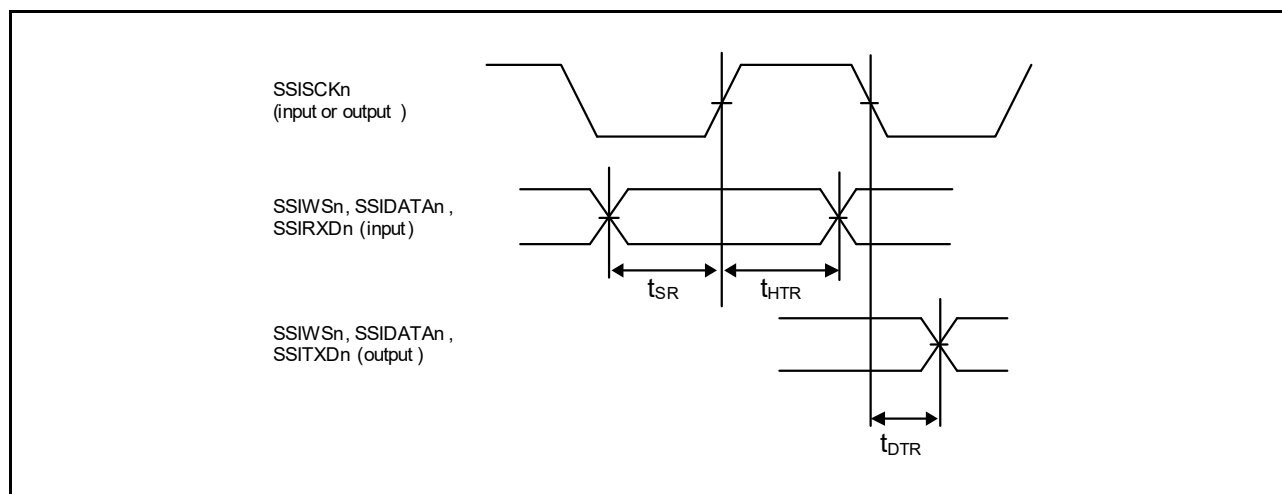


Figure 5.61 SSI Transmission/Reception Timing (SSICR.SCKP=0)

5.9 CTSU Characteristics

Table 5.57 CTSU Characteristics

Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} = AV_{CC0} \leq 5.5\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
External capacitance connected to TSCAP pin	C_{tscap}	9	10	11	nF	
TS pin capacitive load	C_{base}	—	—	50	pF	
Permissible output high current	ΣI_{OH}	—	—	−24	mA	When the mutual capacitance method is applied

5.10 Characteristics of Power-On Reset Circuit and Voltage Detection Circuit

Table 5.58 Characteristics of Power-On Reset Circuit and Voltage Detection Circuit (1)

Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} = AV_{CC0} \leq 5.5\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

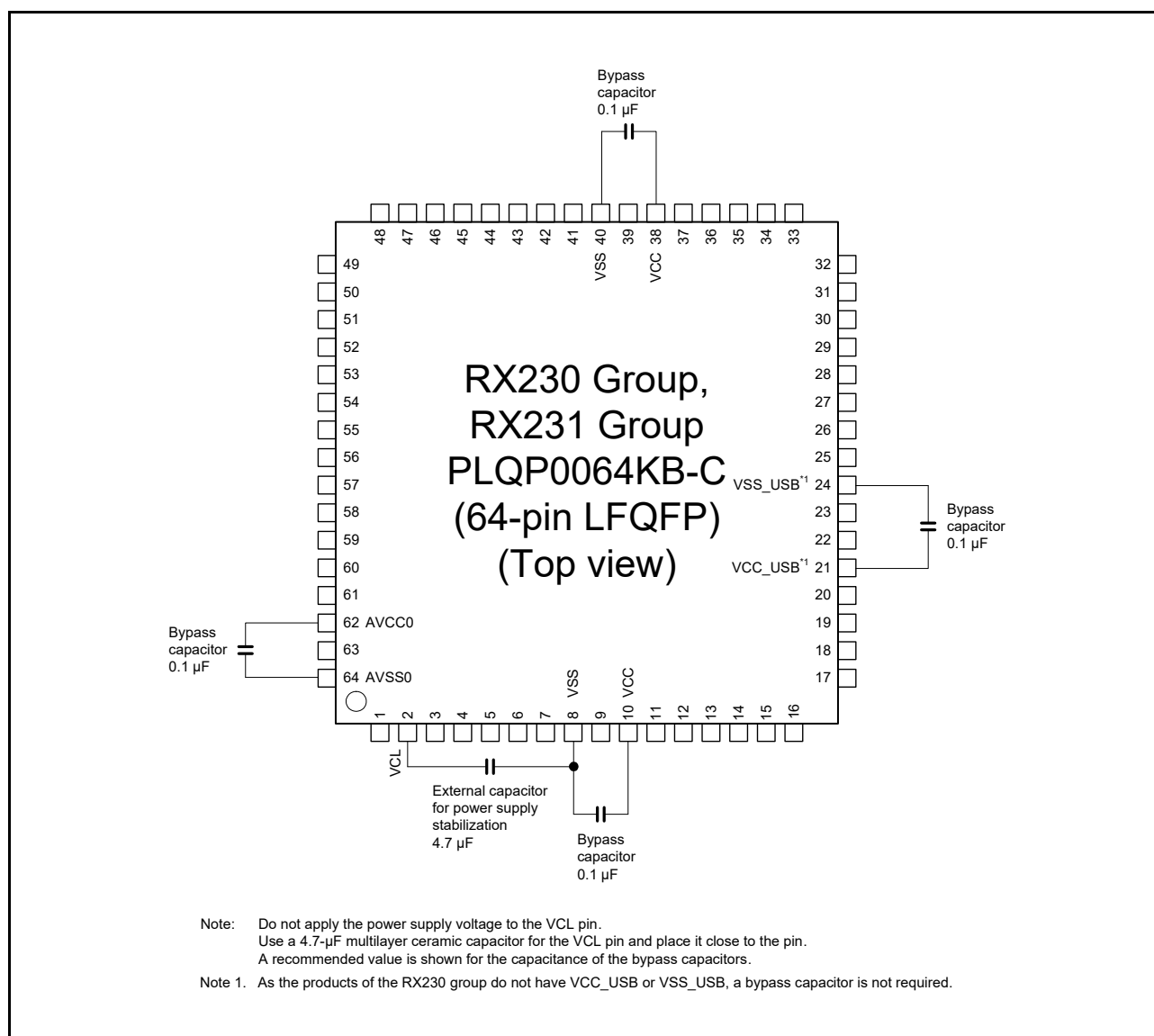
Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V _{POR}	1.35	1.50	1.65	V	Figure 5.73, Figure 5.74
	Voltage detection circuit (LVD0)* ¹	V _{det0_0}	3.67	3.84	3.97	V	Figure 5.75 At falling edge VCC
		V _{det0_1}	2.70	2.82	3.00		
		V _{det0_2}	2.37	2.51	2.67		
		V _{det0_3}	1.80	1.90	1.99		
	Voltage detection circuit (LVD1)* ²	V _{det1_0}	4.12	4.29	4.42	V	Figure 5.76 At falling edge VCC
		V _{det1_1}	3.98	4.14	4.28		
		V _{det1_2}	3.86	4.02	4.16		
		V _{det1_3}	3.68	3.84	3.98		
		V _{det1_4}	2.99	3.10	3.29		
		V _{det1_5}	2.89	3.00	3.19		
		V _{det1_6}	2.79	2.90	3.09		
		V _{det1_7}	2.68	2.79	2.98		
		V _{det1_8}	2.57	2.68	2.87		
		V _{det1_9}	2.47	2.58	2.67		
		V _{det1_A}	2.37	2.48	2.57		
		V _{det1_B}	2.10	2.20	2.30		
		V _{det1_C}	1.86	1.96	2.06		
		V _{det1_D}	1.80	1.86	1.96		
	Voltage detection circuit (LVD2)* ³	V _{det2_0}	4.08	4.29	4.48	V	Figure 5.77 At falling edge VCC
		V _{det2_1}	3.95	4.14	4.35		
		V _{det2_2}	3.82	4.02	4.22		
		V _{det2_3}	3.62	3.84	4.02		

Note: These characteristics apply when noise is not superimposed on the power supply. When a setting is made so that the voltage detection level overlaps with that of the voltage detection circuit (LVD2), it cannot be specified which of LVD1 and LVD2 is used for voltage detection.

Note 1. n in the symbol V_{det0_n} denotes the value of the OFS1.VDSEL[1:0] bits.

Note 2. n in the symbol V_{det1_n} denotes the value of the LVDLVLRLVD1LVL[3:0] bits.

Note 3. n in the symbol V_{det2_n} denotes the value of the LVDLVLRLVD2LVL[1:0] bits.

**Figure 5.81 Connecting Capacitors (64 Pins)**

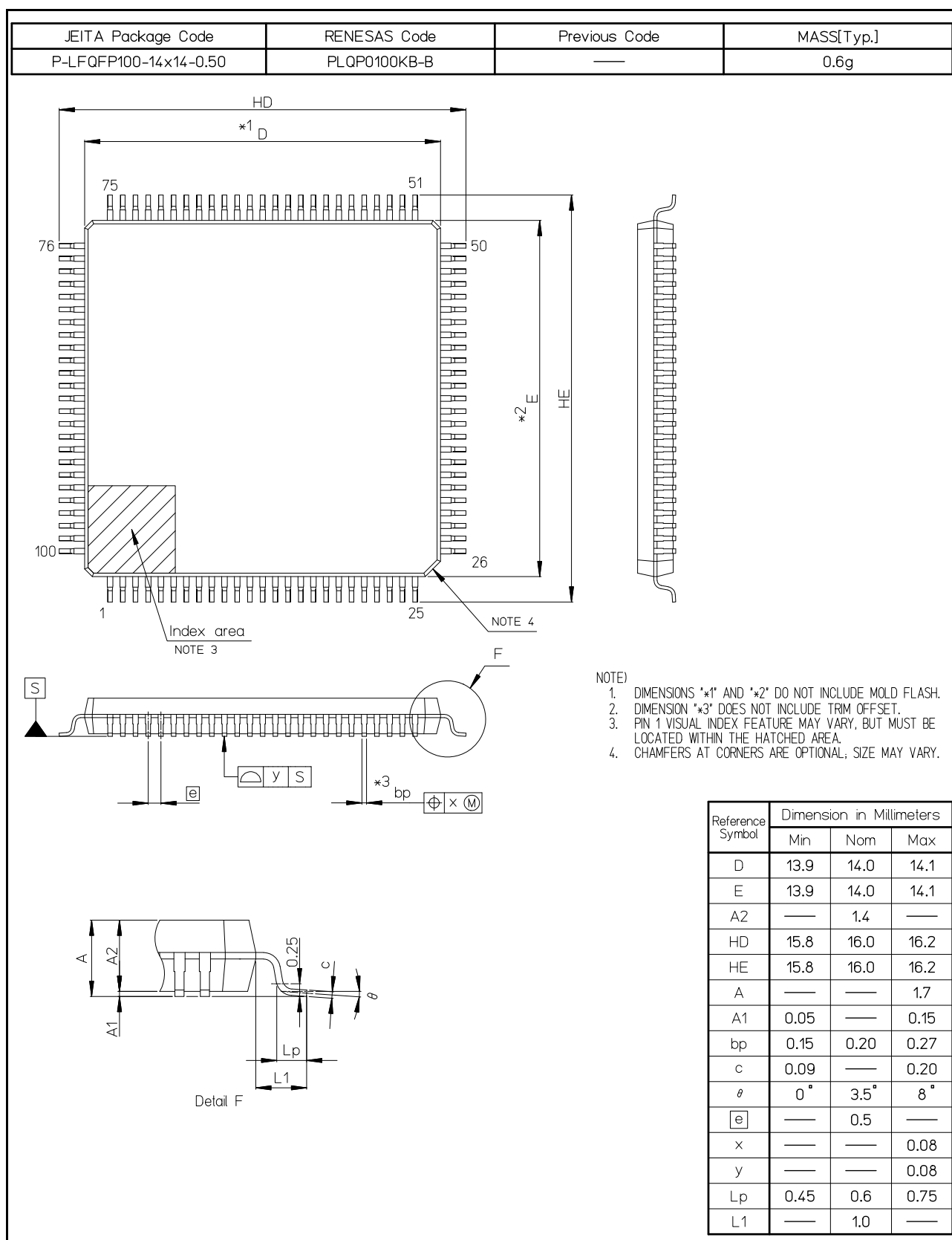


Figure B 100-Pin LFQFP (PLQP0100KB-B)

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HWQFN64-9x9-0.50	PWQN0064KC-A	P64K8-50-6B4-5	0.21

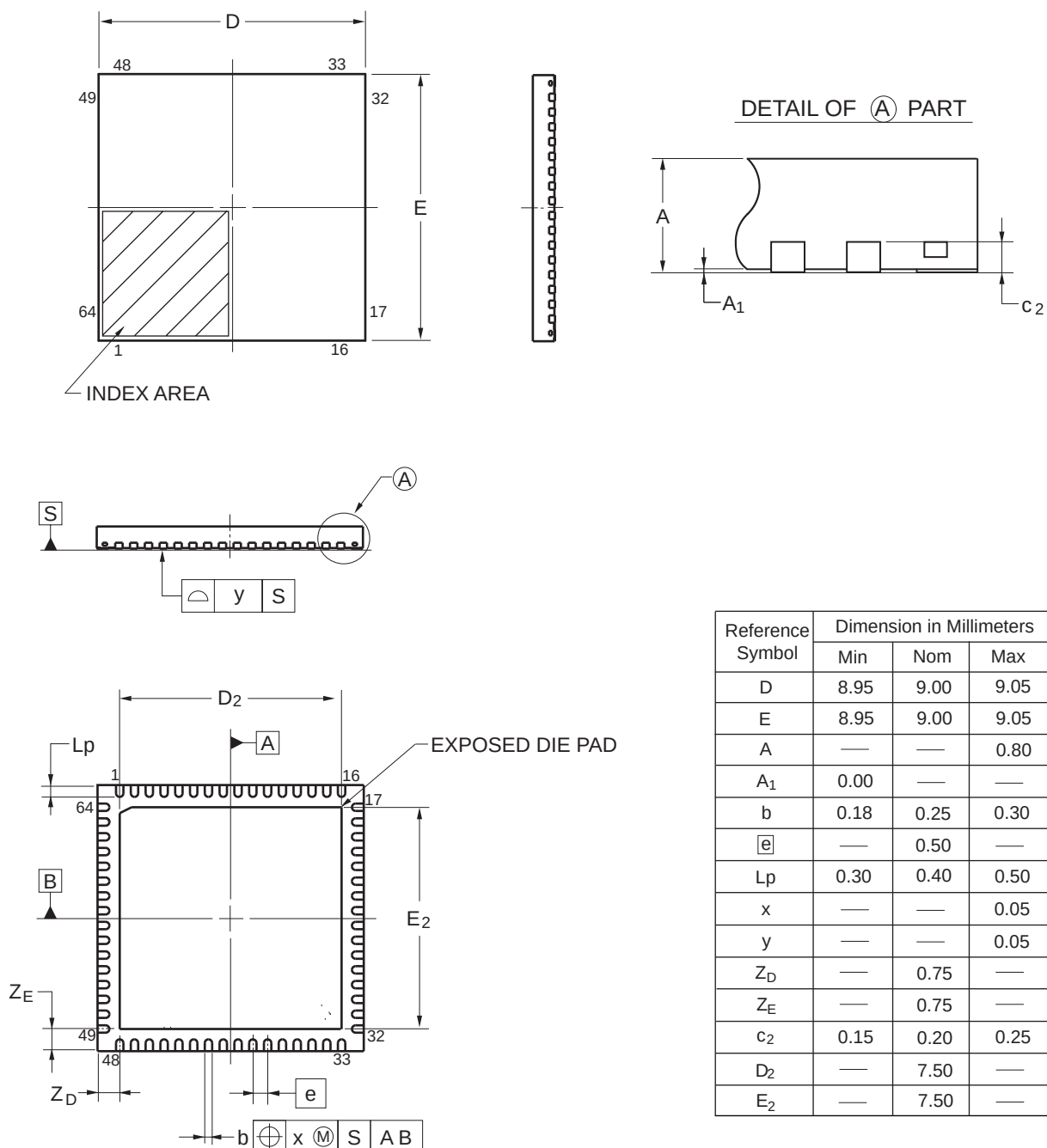


Figure D 64-Pin HWQFN (PWQN0064KC-A)

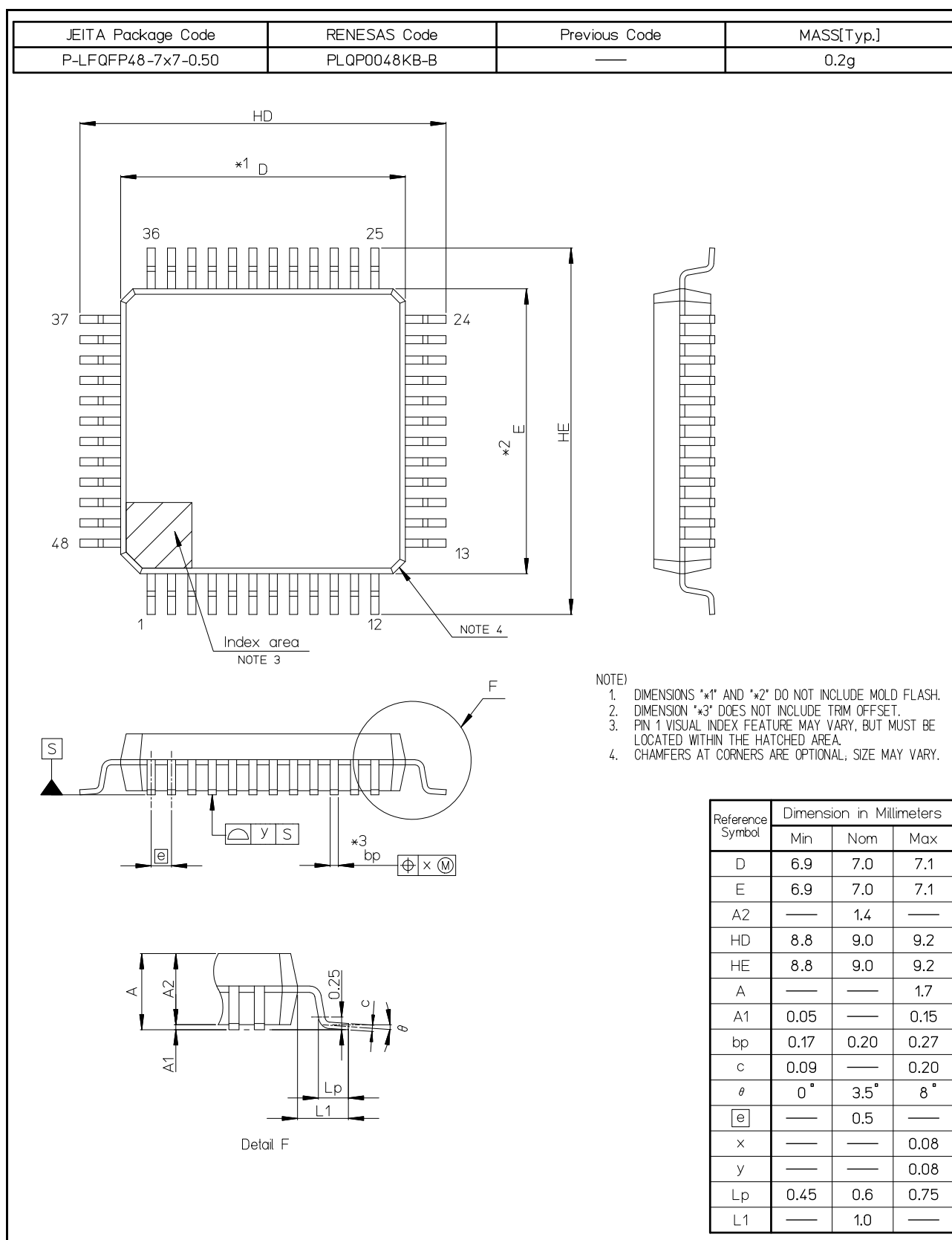


Figure G 48-Pin LFQFP (PLQP0048KB-B)

REVISION HISTORY	RX230 Group, RX231 Group Datasheet
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Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
1.00	Jun 24, 2015	—	First edition, issued	
1.10	Oct 30, 2015	1. Overview		
		3	Table 1.1 Outline of Specifications (2/4), changed	
		5	Table 1.1 Outline of Specifications (4/4): SD Host Interface (SDH1a) added	
		6	Table 1.2 Comparison of Functions for Different Packages: RX230 Group added	
		3. Address Space		
		39	Figure 3.1 Memory Map in Each Operating Mode, changed	
		4. I/O Registers		
		67	Table 4.1 List of I/O Registers (Address Order) (25 / 42), changed	TN-RX*-A139A/E
		83	Table 4.1 List of I/O Registers (Address Order) (41 / 42), changed	
		5. Electrical Characteristics		
		85	Table 5.1 Absolute Maximum Ratings, changed	TN-RX*-A137A/E
		86	Table 5.2 Recommended Operating Voltage Conditions, changed	
		87	Table 5.3 DC Characteristics (1), changed	TN-RX*-A137A/E
		88	Table 5.4 DC Characteristics (2), changed	
		88	Table 5.5 DC Characteristics (3), changed	
		89	Table 5.7 DC Characteristics (5), changed	
		91	Figure 5.1 Voltage Dependency in High-Speed Operating Mode (Reference Data), changed	
		92	Figure 5.2 Voltage Dependency in Middle-Speed Operating Mode (Reference Data), changed	
		93	Figure 5.3 Voltage Dependency in Low-Speed Operating Mode (Reference Data), changed	TN-RX*-A137A/E
		94	Table 5.8 DC Characteristics (6), changed Figure 5.4 Voltage Dependency in Software Standby Mode (Reference Data), changed	
		95	Figure 5.5 Temperature Dependency in Software Standby Mode (Reference Data), changed	
		96	Figure 5.6 Temperature Dependency of RTC Operation with VCC Off (Reference Data), changed Table 5.10 DC Characteristics (8): Conditions changed	
		97	Table 5.11 DC Characteristics (9), changed	TN-RX*-A137A/E
		99	Table 5.16 Permissible Output Currents (1), changed	TN-RX*-A137A/E
		100	Table 5.17 Permissible Output Currents (2), changed	
		101	Table 5.18 Output Values of Voltage (1), changed	
		101	Table 5.19 Output Values of Voltage (2), changed	TN-RX*-A137A/E
		101	Table 5.20 Output Values of Voltage (3), changed	TN-RX*-A137A/E
		105	Figure 5.13 VOH/VOL and IOH/IOL Voltage Characteristics at Ta = 25°C When High-Drive Output is Selected (Reference Data), changed	TN-RX*-A137A/E
		108	Figure 5.18 VOL and IOL Voltage Characteristics of RIIC Output Pin at Ta = 25°C (Reference Data)	TN-RX*-A137A/E
		110	Table 5.21 Operating Frequency Value (High-Speed Operating Mode) and Table 5.22 Operating Frequency Value (Middle-Speed Operating Mode), changed	TN-RX*-A137A/E
		112	Table 5.26 Clock Timing, changed	TN-RX*-A137A/E
		116	Table 5.27 Reset Timing, changed	
		131	Table 5.41 Timing of On-Chip Peripheral Modules (4): Note changed	
		132	Table 5.43 Timing of On-Chip Peripheral Modules (6), changed	
		138	Figure 5.61 SSI Transmission/Reception Timing (SSICP.SCKP=0), changed	TN-RX*-A137A/E
		139	Figure 5.62 SSI Transmission/Reception Timing (SSICP.SCKP=1), changed	TN-RX*-A137A/E
		142	Figure 5.66 VREFH0 Voltage Range vs. AVCC0, changed	

Rev.	Date	Description		Classification
		Page	Summary	
1.20	Sep 28, 2018	95	Figure 5.12 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 5.5 V When Normal Output is Selected (Reference Data), changed	TN-RX*-A201A/E
		124	Table 5.44 Timing of On-Chip Peripheral Modules (7), added	TN-RX*-A197A/E
		131	Figure 5.64 SD Host Interface Input/Output Signal Timing, added	TN-RX*-A197A/E
		132	Table 5.45 USB Characteristics (USB0_DP and USB0_DM Pin Characteristics) conditions, changed	

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