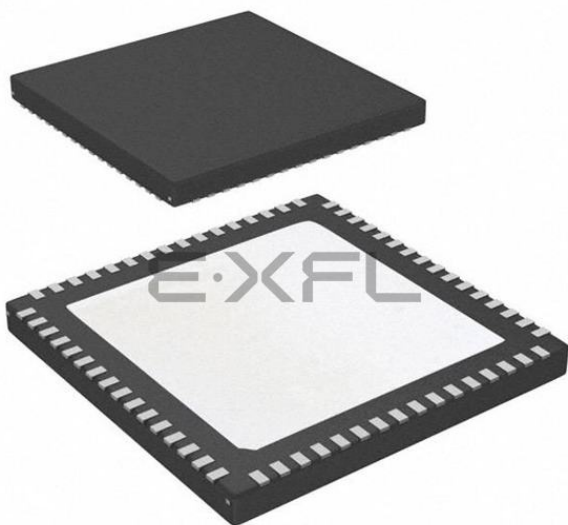




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Not For New Designs
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	54MHz
Connectivity	CANbus, I ² C, IrDA, SCI, SD/SDIO, SPI, SSI, USB OTG
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	43
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-WFQFN Exposed Pad
Supplier Device Package	64-HWQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f52317adnd-u0

Table 1.4 List of Products: G Version ($T_a = -40$ to $+105^\circ\text{C}$) (2/2)

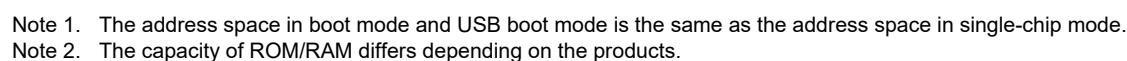
Group	Part No.	Order Part No.	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency	Security Function	SDHI	CAN	Operating Temperature
RX231	R5F52315AGFL	R5F52315AGFL#30	PLQP0048KB-B	128 Kbytes	32 Kbytes	8 Kbytes	54 MHz	Not available	Not available	Available	-40 to +105°C
	R5F52315CGFL	R5F52315CGFL#30						Not available	Not available	Not available	
RX230	R5F52306AGFP	R5F52306AGFP#30	PLQP0100KB-B	256 Kbytes	32 Kbytes	8 Kbytes	54 MHz	Not available	Not available	Not available	-40 to +105°C
	R5F52306AGND	R5F52306AGND#U0	PWQN0064KC-A					Not available	Not available	Not available	
	R5F52306AGFM	R5F52306AGFM#30	PLQP0064KB-C					Not available	Not available	Not available	
	R5F52306AGNE	R5F52306AGNE#U0	PWQN0048KB-A					Not available	Not available	Not available	
	R5F52306AGFL	R5F52306AGFL#30	PLQP0048KB-B					Not available	Not available	Not available	
	R5F52305AGFP	R5F52305AGFP#30	PLQP0100KB-B	128 Kbytes				Not available	Not available	Not available	
	R5F52305AGND	R5F52305AGND#U0	PWQN0064KC-A					Not available	Not available	Not available	
	R5F52305AGFM	R5F52305AGFM#30	PLQP0064KB-C					Not available	Not available	Not available	
	R5F52305AGNE	R5F52305AGNE#U0	PWQN0048KB-A					Not available	Not available	Not available	
	R5F52305AGFL	R5F52305AGFL#30	PLQP0048KB-B					Not available	Not available	Not available	

Table 1.5 Pin Functions (2/4)

Classifications	Pin Name	I/O	Description
16-bit timer pulse unit	TIOCA0, TIOCB0 TIOCC0, TIOCD0	I/O	The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins.
	TIOCA1, TIOCB1	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins.
	TIOCA2, TIOCB2	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins.
	TIOCA3, TIOCB3 TIOCC3, TIOCD3	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins.
	TIOCA4, TIOCB4	I/O	The TGRA4 and TGRB4 input capture input/output compare output/PWM output pins.
	TIOCA5, TIOCB5	I/O	The TGRA5 and TGRB5 input capture input/output compare output/PWM output pins.
	TCLKA, TCLKB TCLKC, TCLKD	Input	Input pins for external clock signals.
Multi-function timer pulse unit 2	MTIOC0A, MTIOC0B MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins.
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins.
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins.
	MTIOC3A, MTIOC3B MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins.
	MTIOC4A, MTIOC4B MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/PWM output pins.
	MTIC5U, MTIC5V, MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/external pulse input pins.
	MTCLKA, MTCLKB, MTCLKC, MTCLKD	Input	Input pins for the external clock.
Port output enable 2	POE0# to POE3#, POE8#	Input	Input pins for request signals to place the MTU pins in the high impedance state.
Realtime clock	RTCOUT	Output	Output pin for the 1-Hz/64-Hz clock.
	RTCIC0 to RTCIC2	Input	Time capture event input pins.
8-bit timer	TMO0 to TMO3	Output	Compare match output pins.
	TMCi0 to TMCi3	Input	Input pins for the external clock to be input to the counter.
	TMRI0 to TMRI3	Input	Counter reset input pins.
Serial communications interface (SCIg)	• Asynchronous mode/clock synchronous mode		
	SCK0, SCK1, SCK5, SCK6, SCK8, SCK9	I/O	Input/output pins for the clock.
	RXD0, RXD1, RXD5, RXD6, RXD8, RXD9	Input	Input pins for received data.
	TXD0, TXD1, TXD5, TXD6, TXD8, TXD9	Output	Output pins for transmitted data.
	CTS0#, CTS1#, CTS5#, CTS6#, CTS8#, CTS9#	Input	Input pins for controlling the start of transmission and reception.
	RTS0#, RTS1#, RTS5#, RTS6#, RTS8#, RTS9#	Output	Output pins for controlling the start of transmission and reception.
	• Simple I ² C mode		
	SSCL0, SSCL1, SSCL5, SSCL6, SSCL8, SSCL9	I/O	Input/output pins for the I ² C clock.
	SSDA0, SSDA1, SSDA5, SSDA6, SSDA8, SSDA9	I/O	Input/output pins for the I ² C data.

Table 1.8 List of Pins and Pin Functions (64-Pin WFLGA) (1/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCI, RSPI, RIIC, RSCAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
A1		P05					DA1
A2	AVCC0						
A3	VREFH0						
A4	VREFL0						
A5	VREFH						
A6	VREFL						
A7		PE2	MTIOC4A	RXD12/RXD12/SMISO12/SSCL12			IRQ7/AN018/ CVREFB0
A8		PE3	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#/AUDIO_MCLK			AN019/CLKOUT
B1	VCL						
B2	AVSS0						
B3		P40					AN000
B4		P42					AN002
B5		P44					AN004
B6		P46					AN006
B7		PE1	MTIOC4C	TXD12/TXD12/SIOX12/SMOSI12/SSDA12			AN017/CMPB0
B8		PE4	MTIOC4D/MTIOC1A				AN020/CMPA2/ CLKOUT
C1	XCIN						
C2	MD						FINED
C3		P03					DA0
C4		P41					AN001
C5		P43					AN003
C6		PE0		SCK12			AN016
C7		PE5	MTIOC4C/MTIOC2B				IRQ5/AN021/ CMPOB0
C8		PA0	MTIOC4A/TIOCA0	SSLA1			CACREF
D1	XCOUT						
D2	RES#						
D3		P27	MTIOC2B/TMC13	SCK1/ SSIWS0		TS2	CVREFB3
D4		P14	MTIOC3A/MTCLKA/TMRI2/ TIOCB5/TCLKA	CTS1#/RTS1#/SS1#/CTXD0/ USB0_OVRCURA		TS13	IRQ4/CVREFB2
D5		PA6	MTIC5V/MTCLKB/TMC13/POE2#/ TIOCA2	CTS5#/RTS5#/SS5#/MOSIA/ SSIWS0			
D6		PA4	MTIC5U/MTCLKA/TMRI0/TIOCA1	TXD5/SMOSI5/SSDA5/SSLA0/ SSITXD0/IRTXD5			IRQ5 /CVREFB1
D7		PA1	MTIOC0B/MTCLKC/TIOCB0	SCK5/SSLA2/SSISCK0			
D8		PA3	MTIOC0D/MTCLKD/TIOCD0/ TCLKB	RXD5/SMISO5/SSCL5/SSIRXD0/ IRRXD5			IRQ6 /CMPB1
E1	VSS						
E2	VBATT						
E3		P30	MTIOC4B/TMRI3/POE8#/RTIC0	RXD1/SMISO1/SSCL1/ AUDIO_MCLK			IRQ0/CMPOB3
E4		P16	MTIOC3C/MTIOC3D/TMO2/ TIOCB1/TCLKC/RTCOUT	TXD1/SMOSI1/SSDA1/MOSIA/ SCL/USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB			IRQ6/ADTRG0#
E5		PC4	MTIOC3D/MTCLKC/TMC11/ POE0#	SCK5/CTS8#/RTS8#/SS8#/ SSLA0	SDHI_D1	TSCAP	
E6	VCC						
E7	VSS						
E8		PB0	MTIC5W/TIOCA3	RXD6/SMISO6/SSCL6/RSPCKA	SDHI_C MD		
F1	VCC						
F2	UPSEL	P35					NMI
F3		P31	MTIOC4D/TMC12/RTIC1	CTS1#/RTS1#/SS1#/SSISCK0			IRQ1



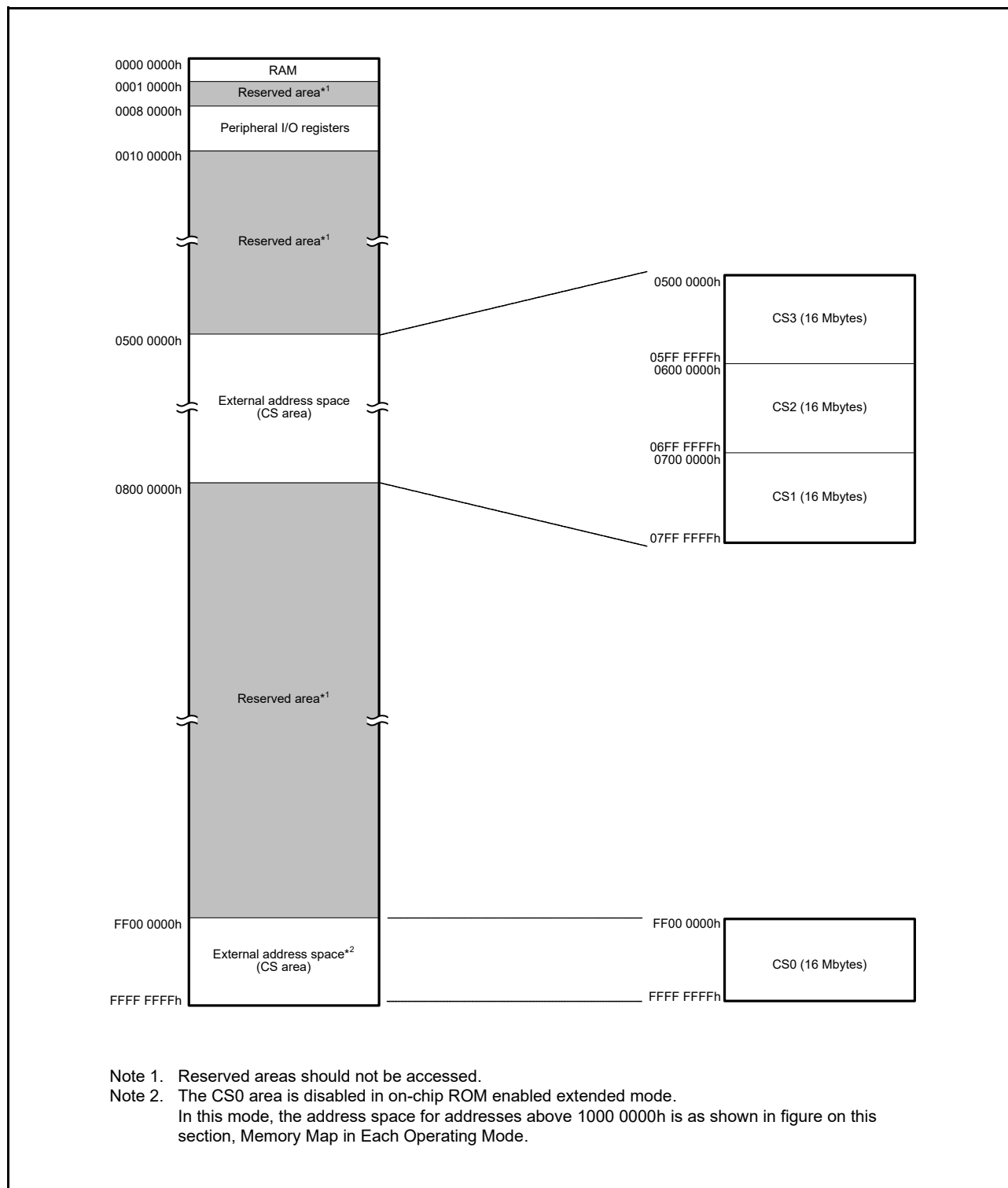
ROM (bytes)		RAM (bytes)	
Capacity	Address	Capacity	Address
512 Kbytes	FFF8 0000h to FFFF FFFFh	64 Kbytes	0000 0000h to 0000 FFFFh
384 Kbytes	FFFA 0000h to FFFF FFFFh		
256 Kbytes	FFFC 0000h to FFFF FFFFh	32 Kbytes	0000 0000h to 0000 7FFFh
128 Kbytes	FFFE 0000h to FFFF FFFFh		

Note 3. Reserved areas should not be accessed.

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Sep 28, 2018

3.2 External Address Space

The external address space is divided into up to four CS areas (CS0 to CS3), each corresponding to the CSn# signal output from a CSn# (n = 0 to 3) pin. Figure 3.2 shows the address ranges corresponding to the individual CS areas (CS0 to CS3) in on-chip ROM disabled extended mode.



**Figure 3.2 Correspondence between External Address Spaces and CS Areas
(In On-Chip ROM Disabled Extended Mode)**

Table 4.1 List of I/O Registers (Address Order) (11/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
0008 A0C9h	SCI6	I ² C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB	2 ICLK
0008 A0CAh	SCI6	I ² C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB	2 ICLK
0008 A0CBh	SCI6	I ² C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB	2 ICLK
0008 A0CCh	SCI6	I ² C Status Register	SISR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0CDh	SCI6	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0CEh	SCI6	Transmit Data Register HL	TDRHL	16	16	4 or 5 PCLKB	2 ICLK
0008 A0CEh	SCI6	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB	2 ICLK
0008 A0CFh	SCI6	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB	2 ICLK
0008 A0D0h	SCI6	Receive Data Register HL	RDRHL	16	16	4 or 5 PCLKB	2 ICLK
0008 A0D0h	SCI6	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB	2 ICLK
0008 A0D1h	SCI6	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB	2 ICLK
0008 A0D2h	SCI6	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A100h	SCI8	Serial Mode Register	SMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A101h	SCI8	Bit Rate Register	BRR	8	8	2 or 3 PCLKB	2 ICLK
0008 A102h	SCI8	Serial Control Register	SCR	8	8	2 or 3 PCLKB	2 ICLK
0008 A103h	SCI8	Transmit Data Register	TDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A104h	SCI8	Serial Status Register	SSR	8	8	2 or 3 PCLKB	2 ICLK
0008 A105h	SCI8	Receive Data Register	RDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A106h	SCI8	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A107h	SCI8	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A108h	SCI8	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB	2 ICLK
0008 A109h	SCI8	I ² C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB	2 ICLK
0008 A10Ah	SCI8	I ² C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB	2 ICLK
0008 A10Bh	SCI8	I ² C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB	2 ICLK
0008 A10Ch	SCI8	I ² C Status Register	SISR	8	8	2 or 3 PCLKB	2 ICLK
0008 A10Dh	SCI8	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A10Eh	SCI8	Transmit Data Register HL	TDRHL	16	16	4 or 5 PCLKB	2 ICLK
0008 A10Eh	SCI8	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB	2 ICLK
0008 A10Fh	SCI8	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB	2 ICLK
0008 A110h	SCI8	Receive Data Register HL	RDRHL	16	16	4 or 5 PCLKB	2 ICLK
0008 A110h	SCI8	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB	2 ICLK
0008 A111h	SCI8	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB	2 ICLK
0008 A112h	SCI8	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A120h	SCI9	Serial Mode Register	SMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A121h	SCI9	Bit Rate Register	BRR	8	8	2 or 3 PCLKB	2 ICLK
0008 A122h	SCI9	Serial Control Register	SCR	8	8	2 or 3 PCLKB	2 ICLK
0008 A123h	SCI9	Transmit Data Register	TDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A124h	SCI9	Serial Status Register	SSR	8	8	2 or 3 PCLKB	2 ICLK
0008 A125h	SCI9	Receive Data Register	RDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A126h	SCI9	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A127h	SCI9	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A128h	SCI9	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB	2 ICLK
0008 A129h	SCI9	I ² C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB	2 ICLK
0008 A12Ah	SCI9	I ² C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB	2 ICLK
0008 A12Bh	SCI9	I ² C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB	2 ICLK
0008 A12Ch	SCI9	I ² C Status Register	SISR	8	8	2 or 3 PCLKB	2 ICLK
0008 A12Dh	SCI9	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A12Eh	SCI9	Transmit Data Register HL	TDRHL	16	16	4 or 5 PCLKB	2 ICLK
0008 A12Eh	SCI9	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB	2 ICLK
0008 A12Fh	SCI9	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB	2 ICLK
0008 A130h	SCI9	Receive Data Register HL	RDRHL	16	16	4 or 5 PCLKB	2 ICLK
0008 A130h	SCI9	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (16/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK $\geq$ PCLK	ICLK < PCLK
0008 C023h	PORT3	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	2 ICLK
0008 C024h	PORT4	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	2 ICLK
0008 C025h	PORT5	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	2 ICLK
0008 C02Ah	PORTA	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	2 ICLK
0008 C02Bh	PORTB	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	2 ICLK
0008 C02Ch	PORTC	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	2 ICLK
0008 C02Dh	PORTD	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	2 ICLK
0008 C02Eh	PORTE	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	2 ICLK
0008 C031h	PORTH	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	2 ICLK
0008 C032h	PORTJ	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	2 ICLK
0008 C040h	PORT0	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB	3 ICLK
0008 C041h	PORT1	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB	3 ICLK
0008 C042h	PORT2	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB	3 ICLK
0008 C043h	PORT3	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB	3 ICLK
0008 C044h	PORT4	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB	3 ICLK
0008 C045h	PORT5	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB	3 ICLK
0008 C04Ah	PORTA	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB	3 ICLK
0008 C04Bh	PORTB	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB	3 ICLK
0008 C04Ch	PORTC	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB	3 ICLK
0008 C04Dh	PORTD	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB	3 ICLK
0008 C04Eh	PORTE	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB	3 ICLK
0008 C051h	PORTH	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB	3 ICLK
0008 C052h	PORTJ	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB	3 ICLK
0008 C060h	PORT0	Port Mode Register	PMR	8	8	2 or 3 PCLKB	2 ICLK
0008 C061h	PORT1	Port Mode Register	PMR	8	8	2 or 3 PCLKB	2 ICLK
0008 C062h	PORT2	Port Mode Register	PMR	8	8	2 or 3 PCLKB	2 ICLK
0008 C063h	PORT3	Port Mode Register	PMR	8	8	2 or 3 PCLKB	2 ICLK
0008 C064h	PORT4	Port Mode Register	PMR	8	8	2 or 3 PCLKB	2 ICLK
0008 C065h	PORT5	Port Mode Register	PMR	8	8	2 or 3 PCLKB	2 ICLK
0008 C06Ah	PORTA	Port Mode Register	PMR	8	8	2 or 3 PCLKB	2 ICLK
0008 C06Bh	PORTB	Port Mode Register	PMR	8	8	2 or 3 PCLKB	2 ICLK
0008 C06Ch	PORTC	Port Mode Register	PMR	8	8	2 or 3 PCLKB	2 ICLK
0008 C06Dh	PORTD	Port Mode Register	PMR	8	8	2 or 3 PCLKB	2 ICLK
0008 C06Eh	PORTE	Port Mode Register	PMR	8	8	2 or 3 PCLKB	2 ICLK
0008 C071h	PORTH	Port Mode Register	PMR	8	8	2 or 3 PCLKB	2 ICLK
0008 C072h	PORTJ	Port Mode Register	PMR	8	8	2 or 3 PCLKB	2 ICLK
0008 C082h	PORT1	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C083h	PORT1	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C084h	PORT2	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C085h	PORT2	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C086h	PORT3	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C087h	PORT3	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C08Ah	PORT5	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C08Bh	PORT5	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C094h	PORTA	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C095h	PORTA	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C096h	PORTB	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C097h	PORTB	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C098h	PORTC	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C099h	PORTC	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C09Ch	PORTE	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	2 ICLK
0008 C09Dh	PORTE	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (22/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
000A 0060h	USB0	DCP Control Register	DCPCTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 0064h	USB0	Pipe Window Select Register	PIPESEL	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 0068h	USB0	Pipe Configuration Register	PIPECFG	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 006Ch	USB0	Pipe Maximum Packet Size Register	PIPEMAXP	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 006Eh	USB0	Pipe Cycle Control Register	PIPEPERI	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 0070h	USB0	PIPE1 Control Register	PIPE1CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 0072h	USB0	PIPE2 Control Register	PIPE2CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 0074h	USB0	PIPE3 Control Register	PIPE3CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 0076h	USB0	PIPE4 Control Register	PIPE4CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 0078h	USB0	PIPE5 Control Register	PIPE5CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 007Ah	USB0	PIPE6 Control Register	PIPE6CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 007Ch	USB0	PIPE7 Control Register	PIPE7CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 007Eh	USB0	PIPE8 Control Register	PIPE8CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 0080h	USB0	PIPE9 Control Register	PIPE9CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 0090h	USB0	PIPE1 Transaction Counter Enable Register	PIPE1TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 0092h	USB0	PIPE1 Transaction Counter Register	PIPE1TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 0094h	USB0	PIPE2 Transaction Counter Enable Register	PIPE2TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 0096h	USB0	PIPE2 Transaction Counter Register	PIPE2TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 0098h	USB0	PIPE3 Transaction Counter Enable Register	PIPE3TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 009Ah	USB0	PIPE3 Transaction Counter Register	PIPE3TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 009Ch	USB0	PIPE4 Transaction Counter Enable Register	PIPE4TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 009Eh	USB0	PIPE4 Transaction Counter Register	PIPE4TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 00A0h	USB0	PIPE5 Transaction Counter Enable Register	PIPE5TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}
000A 00A2h	USB0	PIPE5 Transaction Counter Register	PIPE5TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*2}

Table 4.1 List of I/O Registers (Address Order) (23/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
000A 00B0h	USB0	BC Control Register 0	USBBCCTRL0	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ²
000A 00CCh	USB0	USB Module Control Register	USBMC	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ²
000A 00D0h	USB0	Device Address 0 Configuration Register	DEVADD0	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ²
000A 00D2h	USB0	Device Address 1 Configuration Register	DEVADD1	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ²
000A 00D4h	USB0	Device Address 2 Configuration Register	DEVADD2	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ²
000A 00D6h	USB0	Device Address 3 Configuration Register	DEVADD3	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ²
000A 00D8h	USB0	Device Address 4 Configuration Register	DEVADD4	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ²
000A 00DAh	USB0	Device Address 5 Configuration Register	DEVADD5	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ²
000A 0900h	CTSU	CTSU Control Register 0	CTSUCR0	8	8	2 or 3 PCLKB	2 ICLK
000A 0901h	CTSU	CTSU Control Register 1	CTSUCR1	8	8	2 or 3 PCLKB	2 ICLK
000A 0902h	CTSU	CTSU Synchronous Noise Reduction Setting Register	CTSUSDPRS	8	8	2 or 3 PCLKB	2 ICLK
000A 0903h	CTSU	CTSU Sensor Stabilization Wait Control Register	CTSUSST	8	8	2 or 3 PCLKB	2 ICLK
000A 0904h	CTSU	CTSU Measurement Channel Register 0	CTSUMCH0	8	8	2 or 3 PCLKB	2 ICLK
000A 0905h	CTSU	CTSU Measurement Channel Register 1	CTSUMCH1	8	8	2 or 3 PCLKB	2 ICLK
000A 0906h	CTSU	CTSU Channel Enable Control Register 0	CTSUCHAC0	8	8	2 or 3 PCLKB	2 ICLK
000A 0907h	CTSU	CTSU Channel Enable Control Register 1	CTSUCHAC1	8	8	2 or 3 PCLKB	2 ICLK
000A 0908h	CTSU	CTSU Channel Enable Control Register 2	CTSUCHAC2	8	8	2 or 3 PCLKB	2 ICLK
000A 0909h	CTSU	CTSU Channel Enable Control Register 3	CTSUCHAC3	8	8	2 or 3 PCLKB	2 ICLK
000A 090Ah	CTSU	CTSU Channel Enable Control Register 4	CTSUCHAC4	8	8	2 or 3 PCLKB	2 ICLK
000A 090Bh	CTSU	CTSU Channel Transmit/Receive Control Register 0	CTSUCHTRC0	8	8	2 or 3 PCLKB	2 ICLK
000A 090Ch	CTSU	CTSU Channel Transmit/Receive Control Register 1	CTSUCHTRC1	8	8	2 or 3 PCLKB	2 ICLK
000A 090Dh	CTSU	CTSU Channel Transmit/Receive Control Register 2	CTSUCHTRC2	8	8	2 or 3 PCLKB	2 ICLK
000A 090Eh	CTSU	CTSU Channel Transmit/Receive Control Register 3	CTSUCHTRC3	8	8	2 or 3 PCLKB	2 ICLK
000A 090Fh	CTSU	CTSU Channel Transmit/Receive Control Register 4	CTSUCHTRC4	8	8	2 or 3 PCLKB	2 ICLK
000A 0910h	CTSU	CTSU High-Pass Noise Reduction Control Register	CTSUDCLKC	8	8	2 or 3 PCLKB	2 ICLK
000A 0911h	CTSU	CTSU Status Register	CTSUST	8	8	2 or 3 PCLKB	2 ICLK
000A 0912h	CTSU	CTSU High-Pass Noise Reduction Spectrum Diffusion Control Register	CTSUSSC	16	16	2 or 3 PCLKB	2 ICLK
000A 0914h	CTSU	CTSU Sensor Offset Register 0	CTSUSO0	16	16	2 or 3 PCLKB	2 ICLK
000A 0916h	CTSU	CTSU Sensor Offset Register 1	CTSUSO1	16	16	2 or 3 PCLKB	2 ICLK
000A 0918h	CTSU	CTSU Sensor Counter	CTSUSC	16	16	2 or 3 PCLKB	2 ICLK
000A 091Ah	CTSU	CTSU Reference Counter	CTSURC	16	16	2 or 3 PCLKB	2 ICLK
000A 091Ch	CTSU	CTSU Error Status Register	CTSUERRS	16	16	2 or 3 PCLKB	2 ICLK
000A 8300h	RSCAN0	Bit Configuration Register L	CFGL	16	16	2 or 3 PCLKB	2 ICLK
000A 8302h	RSCAN0	Bit Configuration Register H	CFGH	16	16	2 or 3 PCLKB	2 ICLK
000A 8304h	RSCAN0	Control Register L	CTRL	16	16	2 or 3 PCLKB	2 ICLK
000A 8306h	RSCAN0	Control Register H	CTRH	16	16	2 or 3 PCLKB	2 ICLK
000A 8308h	RSCAN0	Status Register L	STSL	16	16	2 or 3 PCLKB	2 ICLK
000A 830Ah	RSCAN0	Status Register H	STSH	16	16	2 or 3 PCLKB	2 ICLK
000A 830Ch	RSCAN0	Error Flag Register L	ERFLL	16	16	2 or 3 PCLKB	2 ICLK
000A 830Eh	RSCAN0	Error Flag Register H	ERFLH	16	16	2 or 3 PCLKB	2 ICLK
000A 8322h	RSCAN	Global Configuration Register L	GCFGFL	16	16	2 or 3 PCLKB	2 ICLK
000A 8324h	RSCAN	Global Configuration Register H	GCFGH	16	16	2 or 3 PCLKB	2 ICLK

Table 5.7 DC Characteristics (5)Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} = AV_{CC0} \leq 5.5\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item					Symbol	Typ. *4	Max.	Unit	Test Conditions	
Supply current *1	High-speed operating mode	Normal operating mode	No peripheral operation*2	ICLK = 54 MHz	I _{CC}	6.5	—	mA		
				ICLK = 32 MHz		4.1	—			
				ICLK = 16 MHz		2.9	—			
				ICLK = 8 MHz		2.2	—			
				ICLK = 4 MHz		1.9	—			
			All peripheral operation: Normal	ICLK = 54 MHz*11		26.5	—			
				ICLK = 32 MHz*3		21.0	—			
				ICLK = 16 MHz*3		11.8	—			
				ICLK = 8 MHz*3		6.6	—			
				ICLK = 4 MHz*3		4.2	—			
			All peripheral operation: Max.	ICLK = 54 MHz*11		—	53.3			
				ICLK = 32 MHz*3		—	40.8			
			Increase due to operation of the Trusted Secure IP	PCLKB = 32 MHz		—	2			
			Sleep mode	No peripheral operation*2		ICLK = 54 MHz	3.5			—
						ICLK = 32 MHz	2.4			—
						ICLK = 16 MHz	1.9			—
						ICLK = 8 MHz	1.6			—
						ICLK = 4 MHz	1.5			—
		All peripheral operation: Normal		ICLK = 54 MHz*11		13.4	—			
				ICLK = 32 MHz*3		12.5	—			
				ICLK = 16 MHz*3		7.3	—			
				ICLK = 8 MHz*3		4.6	—			
				ICLK = 4 MHz*3		3.3	—			
		Deep sleep mode	No peripheral operation*2	ICLK = 54 MHz		2.3	—			
				ICLK = 32 MHz		1.5	—			
				ICLK = 16 MHz		1.3	—			
				ICLK = 8 MHz		1.2	—			
				ICLK = 4 MHz		1.1	—			
			All peripheral operation: Normal	ICLK = 54 MHz*11		10.6	—			
				ICLK = 32 MHz*3		9.9	—			
	ICLK = 16 MHz*3			5.9	—					
	ICLK = 8 MHz*3			3.8	—					
	ICLK = 4 MHz*3			2.7	—					
	Increase during BGO operation*5						2.5	—		
	Middle-speed operating mode	Normal operating mode	No peripheral operation*6	ICLK = 12 MHz	I _{CC}	2.7	—	mA		
				ICLK = 8 MHz		1.8	—			
				ICLK = 4 MHz		1.4	—			
				ICLK = 1 MHz		1.1	—			
			All peripheral operation: Normal*7	ICLK = 12 MHz		9.6	—			
				ICLK = 8 MHz		6.2	—			
				ICLK = 4 MHz		3.8	—			
				ICLK = 1 MHz		2.3	—			

Table 5.13 DC Characteristics (11)Conditions: $0\text{ V} \leq \text{VCC} = \text{VCC_USB} = \text{AVCC0} \leq 5.5\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Power-on VCC rising gradient	At normal startup*1	SrVCC	0.02	—	20	ms/V
	During fast startup time*2		0.02	—	2	
	Voltage monitoring 0 reset enabled at startup*3, *4		0.02	—	—	

Note 1. When OFS1.(FASTSTUP, LVDAS) bits are 11b.

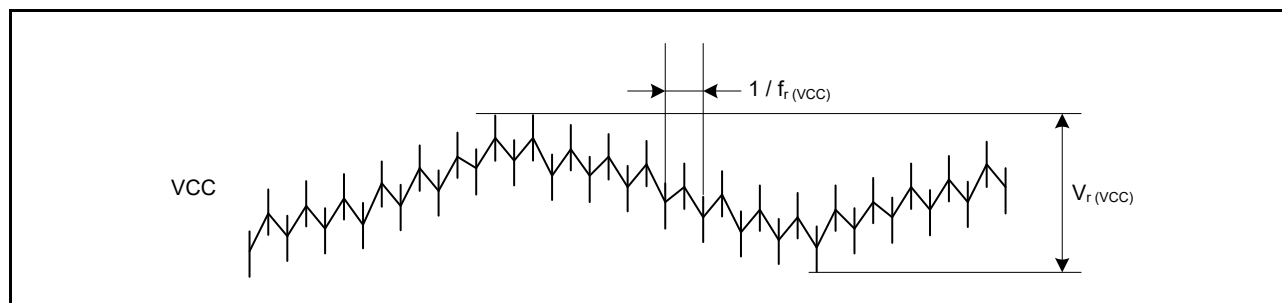
Note 2. When OFS1.(FASTSTUP, LVDAS) bits are 01b.

Note 3. When OFS1.LVDAS bit is 0.

Note 4. Turn on the power supply voltage according to the normal startup rising gradient because the settings in the OFS1 register are not read in boot mode.

Table 5.14 DC Characteristics (12)Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} = \text{AVCC0} \leq 5.5\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$ The ripple voltage must meet the allowable ripple frequency $f_r(\text{VCC})$ within the range between the VCC upper limit and lower limit. When VCC change exceeds $\text{VCC} \pm 10\%$, the allowable voltage change rising/falling gradient $dt/d\text{VCC}$ must be met.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Allowable ripple frequency	$f_r(\text{VCC})$	—	—	10	kHz	Figure 5.7 $V_r(\text{VCC}) \leq \text{VCC} \times 0.2$
		—	—	1	MHz	Figure 5.7 $V_r(\text{VCC}) \leq \text{VCC} \times 0.08$
		—	—	10	MHz	Figure 5.7 $V_r(\text{VCC}) \leq \text{VCC} \times 0.06$
Allowable voltage change rising/falling gradient	$dt/d\text{VCC}$	1.0	—	—	ms/V	When VCC change exceeds $\text{VCC} \pm 10\%$

**Figure 5.7 Ripple Waveform****Table 5.15 DC Characteristics (13)**Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} = \text{AVCC0} \leq 5.5\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Permissible error of VCL pin external capacitance	C_{VCL}	1.4	4.7	7.0	μF	

Note: The recommended capacitance is $4.7\text{ }\mu\text{F}$. Variations in connected capacitors should be within the above range.

Table 5.18 Output Values of Voltage (1)Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} = AV_{CC0} < 2.7\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40$ to $+105^\circ\text{C}$

Item				Symbol	Min.	Max.	Unit	Test Conditions
Output low	All output ports	Normal output mode		V _{OL}	—	0.3	V	I _{OL} = 0.5 mA
		High-drive output mode			—	0.3		I _{OL} = 1.0 mA
Output high	All output ports	Normal output mode	Ports 03, 05, 07, Ports 40 to 47	V _{OH}	AVCC0 – 0.3	—	V	I _{OH} = –0.5 mA
			Ports other than above		VCC – 0.3	—		
		High-drive output mode				VCC – 0.3		—

Table 5.19 Output Values of Voltage (2)Conditions: $2.7\text{ V} \leq V_{CC} = V_{CC_USB} = AV_{CC0} < 4.0\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40$ to $+105^\circ\text{C}$

Item				Symbol	Min.	Max.	Unit	Test Conditions
Output low	All output ports (except for RIIC)	Normal output mode		V_{OL}	—	0.5	V	$I_{OL} = 1.0\text{ mA}$
		High-drive output mode			—	0.5		$I_{OL} = 2.0\text{ mA}$
	RIIC pins	Standard mode (Normal output mode)			—	0.4		$I_{OL} = 3.0\text{ mA}$
		Fast mode (High-drive output mode)			—	0.6		$I_{OL} = 6.0\text{ mA}$
Output high	All output ports	Normal output mode	Ports 03, 05, 07, Ports 40 to 47	V_{OH}	$AVCC0 - 0.5$	—	V	$I_{OH} = -1.0\text{ mA}$
			Ports other than above		$VCC - 0.5$			
		High-drive output mode			$VCC - 0.5$	—		$I_{OH} = -2.0\text{ mA}$

Table 5.20 Output Values of Voltage (3)Conditions: $4.0\text{ V} \leq V_{CC} = V_{CC_USB} = AV_{CC0} \leq 5.5\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40$ to $+105^\circ\text{C}$

Item				Symbol	Min.	Max.	Unit	Test Conditions
Output low	All output ports (except for RIIC)	Normal output mode		V_{OL}	—	0.8	V	$I_{OL} = 2.0\text{ mA}$
		High-drive output mode			—	0.8		$I_{OL} = 4.0\text{ mA}$
	RIIC pins	Standard mode(Normal output mode)			—	0.4		$I_{OL} = 3.0\text{ mA}$
		Fast mode (High-drive output mode)			—	0.6		$I_{OL} = 6.0\text{ mA}$
Output high	All output ports	Normal output mode	Ports 03, 05, 07, Ports 40 to 47	V_{OH}	$AVCC0 - 0.8$	—	V	$I_{OH} = -2.0\text{ mA}$
			Ports other than above		$VCC - 0.8$	—		
		High-drive output mode			$VCC - 0.8$	—		$I_{OH} = -4.0\text{ mA}$

5.3 AC Characteristics

5.3.1 Clock Timing

Table 5.21 Operating Frequency Value (High-Speed Operating Mode)

Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} = \text{AVCC0} \leq 5.5\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VREFL0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Symbol	VCC				Unit
			$1.8\text{ V} \leq \text{VCC} < 2.4\text{ V}$	$2.4\text{ V} \leq \text{VCC} < 2.7\text{ V}$	$2.7\text{ V} \leq \text{VCC} \leq 5.5\text{ V}$	When USB is in Use*3	
Maximum operating frequency*4	System clock (ICLK)	f_{max}	8	16	54	54	MHz
	FlashIF clock (FCLK)*1, *2		8	16	32	32	
	Peripheral module clock (PCLKA)		8	16	54	54	
	Peripheral module clock (PCLKB)		8	16	32	32	
	Peripheral module clock (PCLKD)		8	32	54	54	
	External bus clock (BCLK)		8	16	32	32	
	BCLK pin output		8	8	16	16	
	USB clock (UCLK)	f_{usb}	—	—	—	48	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When FCLK is in use at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note 2. The frequency accuracy of FCLK must be within $\pm 3.5\%$.

Note 3. The VCC_USB range is 3.0 to 5.5 V when the USB clock is in use.

Note 4. The maximum operating frequency listed above does not include errors of the external oscillator and internal oscillator. For details on the range for the guaranteed operation, see Table 5.26, Clock Timing.

Table 5.22 Operating Frequency Value (Middle-Speed Operating Mode)

Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} = \text{AVCC0} \leq 5.5\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VREFL0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Symbol	VCC				Unit
			$1.8\text{ V} \leq \text{VCC} < 2.4\text{ V}$	$2.4\text{ V} \leq \text{VCC} < 2.7\text{ V}$	$2.7\text{ V} \leq \text{VCC} \leq 5.5\text{ V}$	When USB is in Use*3	
Maximum operating frequency*4	System clock (ICLK)	f_{max}	8	12	12	12	MHz
	FlashIF clock (FCLK)*1, *2		8	12	12	12	
	Peripheral module clock (PCLKA)		8	12	12	12	
	Peripheral module clock (PCLKB)		8	12	12	12	
	Peripheral module clock (PCLKD)		8	12	12	12	
	External bus clock (BCLK)		8	12	12	12	
	BCLK pin output		8	8	12	12	
	USB clock (UCLK)	f_{usb}	—	—	—	48	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note 2. The frequency accuracy of FCLK must be within $\pm 3.5\%$.

Note 3. The VCC_USB range is 3.0 to 5.5 V when the USB clock is in use.

Note 4. The maximum operating frequency listed above does not include errors of the external oscillator and internal oscillator. For details on the range for the guaranteed operation, see Table 5.26, Clock Timing.

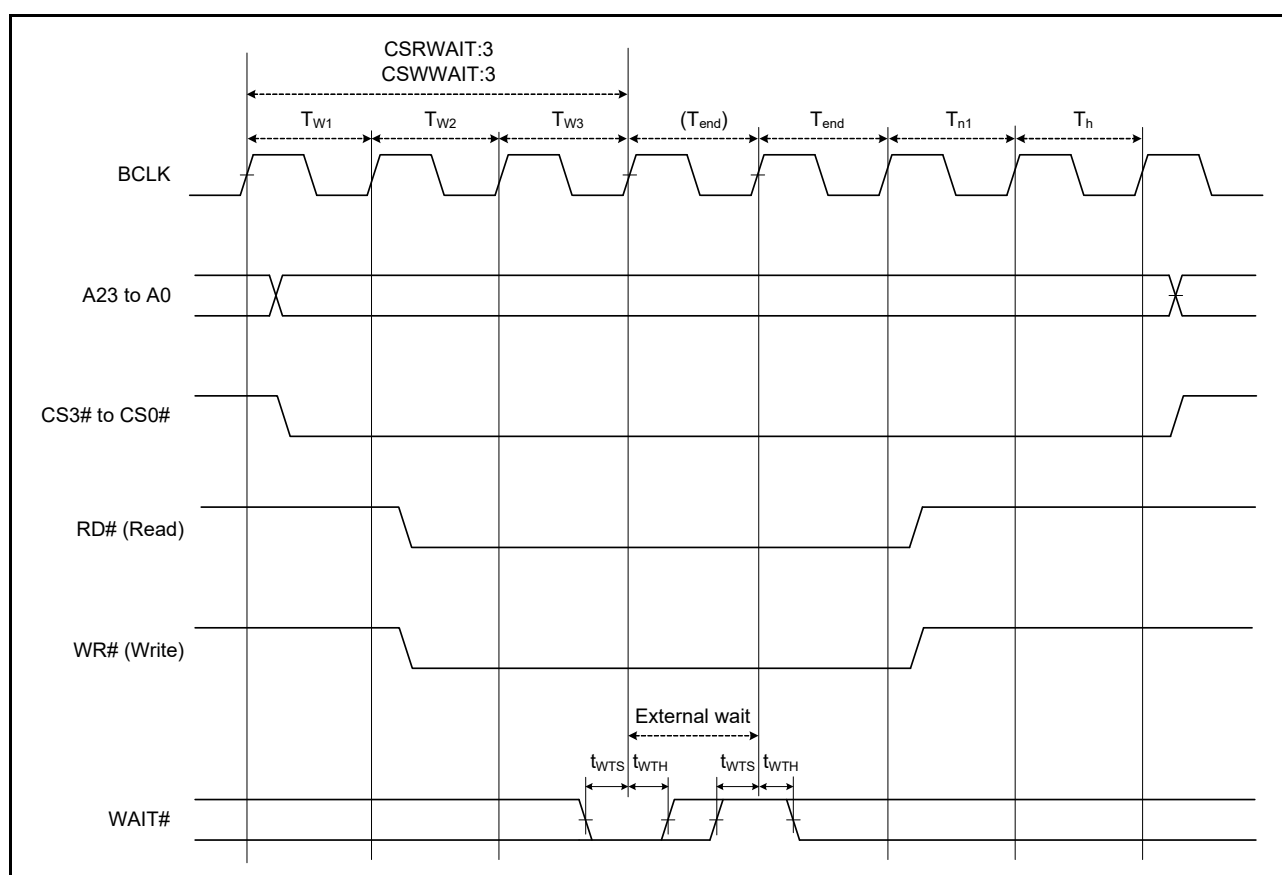


Figure 5.42 External Bus Timing/External Wait Control

Table 5.36 Bus Timing (Multiplex bus) (1)

Conditions: $2.7\text{ V} \leq V_{CC} = V_{CC_USB} = AV_{CC0} \leq 5.5\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$,
 $f_{BCLK} \leq 32\text{ MHz}$ (BCLK pin output frequency $\leq 16\text{ MHz}$), $T_a = -40\text{ to }+105^\circ\text{C}$, $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$,
 $I_{OH} = -1.0\text{ mA}$, $I_{OL} = 1.0\text{ mA}$, $C_L = 30\text{ pF}$, when normal output is selected by the drive capacity control register

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	55	ns	Figure 5.43, Figure 5.44
Byte control delay time	t_{BCD}	—	55	ns	
CS# delay time	t_{CSD}	—	55	ns	
RD# delay time	t_{RSD}	—	55	ns	
ALE delay time	t_{ALED}	—	55	ns	
Read data setup time	t_{RDS}	40	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	55	ns	
Write data delay time	t_{WDD}	—	55	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	40	—	ns	Figure 5.42
WAIT# hold time	t_{WTH}	0	—	ns	

Table 5.37 Bus Timing (Multiplex bus) (2)

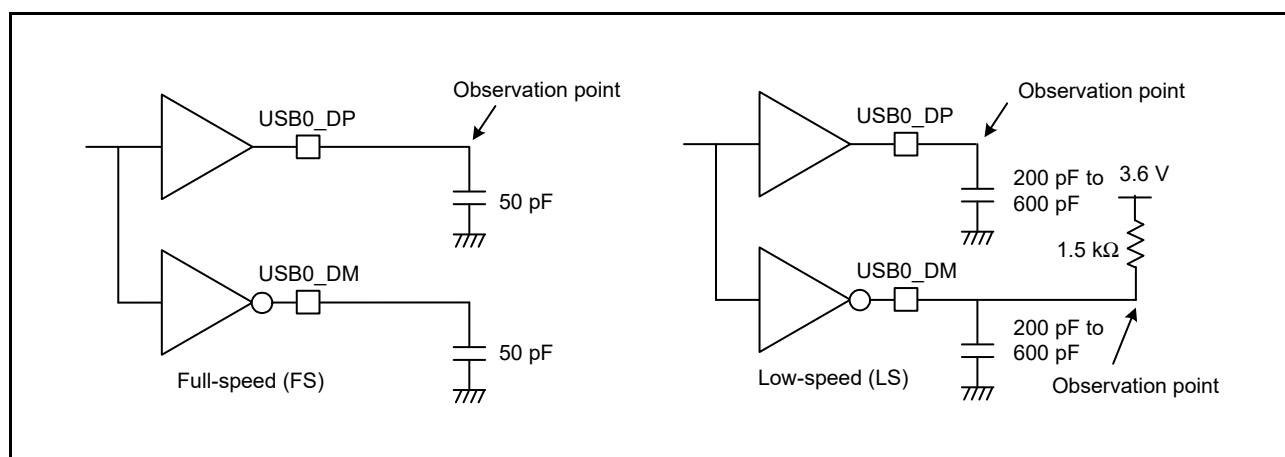
Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} = AV_{CC0} < 5.5\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$,
 $f_{BCLK} \leq 16\text{ MHz}$ (BCLK pin output frequency $\leq 8\text{ MHz}$), $T_a = -40\text{ to }+105^\circ\text{C}$, $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$,
 $I_{OH} = -1.0\text{ mA}$, $I_{OL} = 1.0\text{ mA}$, $C_L = 30\text{ pF}$, when normal output is selected by the drive capacity control register

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	90	ns	Figure 5.43, Figure 5.44
Byte control delay time	t_{BCD}	—	90	ns	
CS# delay time	t_{CSD}	—	90	ns	
RD# delay time	t_{RSD}	—	90	ns	
ALE delay time	t_{ALED}	—	90	ns	
Read data setup time	t_{RDS}	60	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	90	ns	
Write data delay time	t_{WDD}	—	90	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	60	—	ns	Figure 5.42
WAIT# hold time	t_{WTH}	0	—	ns	

Table 5.40 Timing of On-Chip Peripheral Modules (3)Conditions: $1.8\text{ V} \leq VCC = VCC_USB = AVCC0 \leq 5.5\text{ V}$, $VSS = AVSS0 = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)		t_{SPcyc}	4	65536	t_{Pcyc}	Figure 5.54
	SCK clock cycle input (slave)			6	65536	t_{Pcyc}	
	SCK clock high pulse width		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time		t_{SPCKr} , t_{SPCKf}	—	20	ns	
	Data input setup time (master)	2.7 V or above	t_{SU}	65	—	ns	Figure 5.55, Figure 5.56
		1.8 V or above		95	—		
	Data input setup time (slave)			40	—		
	Data input hold time		t_H	40	—	ns	
	SSL input setup time		t_{LEAD}	3	—	t_{SPcyc}	
	SSL input hold time		t_{LAG}	3	—	t_{SPcyc}	
	Data output delay time (master)		t_{OD}	—	40	ns	
	Data output delay time (slave)	2.7 V or above		—	65		
		1.8 V or above		—	100		
	Data output hold time (master)	2.7 V or above	t_{OH}	−10	—	ns	
		1.8 V or above		−20	—		
	Data output hold time (slave)			−10	—		
	Data rise/fall time		t_{Dr} , t_{Df}	—	20	ns	
	SSL input rise/fall time		t_{SSLr} , t_{SSLf}	—	20	ns	
	Slave access time		t_{SA}	—	6	t_{Pcyc}	Figure 5.57, Figure 5.58
	Slave output release time		t_{REL}	—	6	t_{Pcyc}	

Note 1. t_{Pcyc} : PCLK cycle

**Figure 5.66** Test Circuit

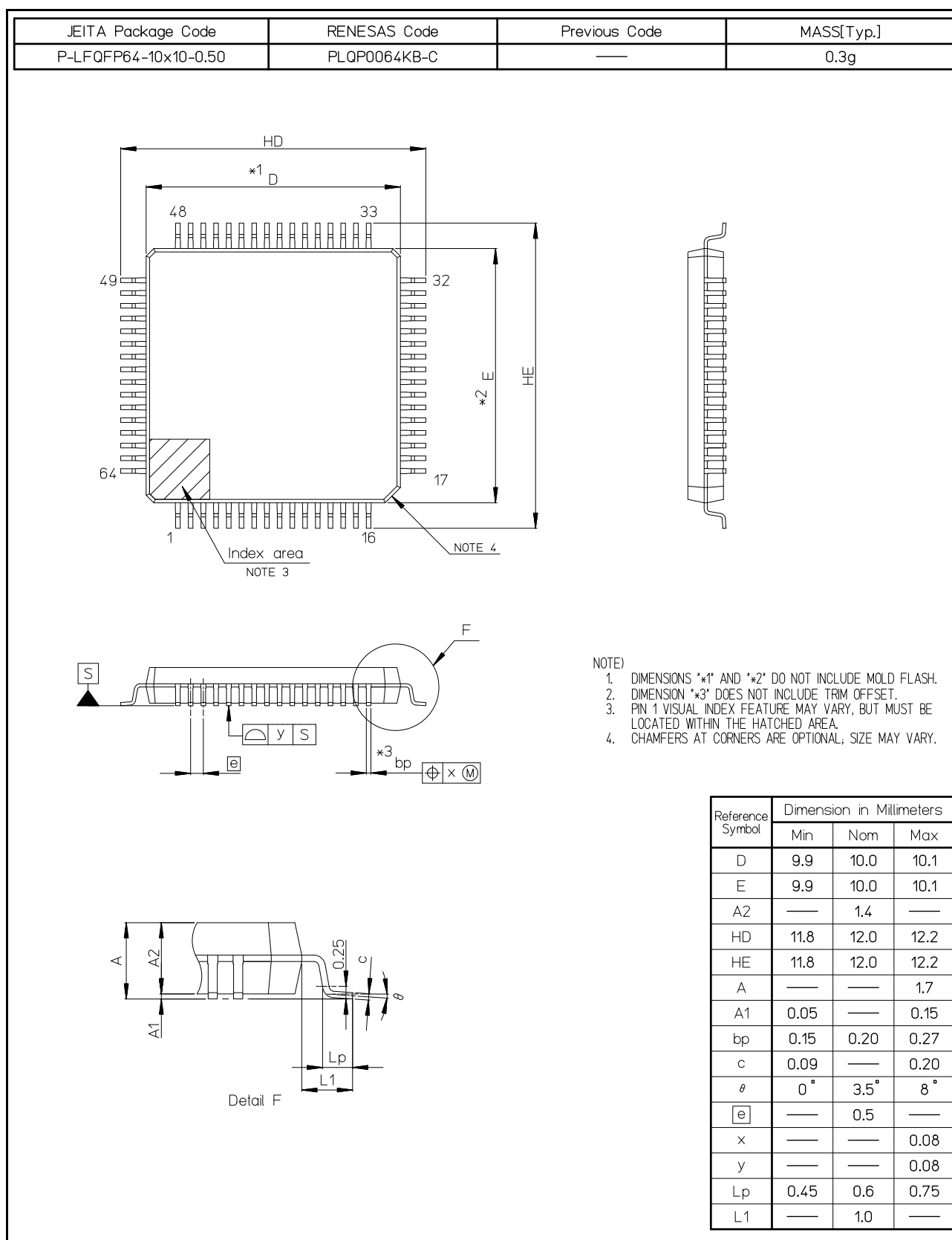


Figure E 64-Pin LFQFP (PLQP0064KB-C)

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

¾ The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

¾ The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

¾ The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

¾ When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

¾ The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.4.0-1 November 2017)



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