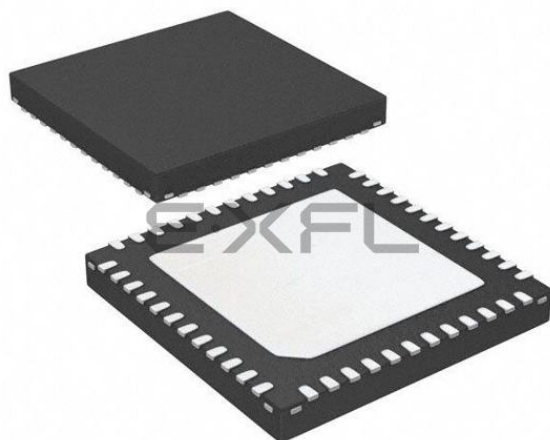




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Details

Product Status	Not For New Designs
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	54MHz
Connectivity	CANbus, I ² C, IrDA, SCI, SD/SDIO, SPI, SSI, USB OTG
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	30
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-WFQFN Exposed Pad
Supplier Device Package	48-HWQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f52317adne-u0

1.4 Pin Functions

Table 1.5 lists the pin functions.

Table 1.5 Pin Functions (1/4)

Classifications	Pin Name	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply.
	VCL	—	Connect this pin to the VSS pin via a 4.7 μ F smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
	VBATT	Input	Backup power pin
Clock	XTAL	Output	Pins for connecting a crystal. An external clock can be input through the EXTAL pin.
	EXTAL	Input	
	BCLK	Output	Outputs the external bus clock for external devices.
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal between XCIN and XCOU.
	XCOU	Output	
	CLKOUT	Output	Clock output pin.
Operating mode control	MD	Input	Pin for setting the operating mode. The signal levels on this pin must not be changed during operation.
	UB	Input	Pin used for boot mode (USB interface).
	UPSEL	Input	Pin used for boot mode (USB interface).
System control	RES#	Input	Reset pin. This MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Input pin for the clock frequency accuracy measurement circuit.
On-chip emulator	FINED	I/O	FINE interface pin.
Address bus	A0 to A23	Output	Output pins for the address.
Data bus	D0 to D15	I/O	Input and output pins for the bidirectional data bus.
Multiplexed bus	A0/D0 to A15/D15	I/O	Address/data multiplexed bus
Bus control	RD#	Output	Strobe signal which indicates that reading from the external bus interface space is in progress.
	WR#	Output	Strobe signal which indicates that writing to the external bus interface space is in progress, in single-write strobe mode.
	WR0#, WR1#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0, and D15 to D8) is valid in writing to the external bus interface space, in byte strobe mode.
	BC0#, BC1#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0 and D15 to D8) is valid in access to the external bus interface space, in single-write strobe mode.
	CS0# to CS3#	Output	Select signals for areas 0 to 3.
	WAIT#	Input	Input pin for wait request signals in access to the external space.
	ALE	Output	Address latch signal when address/data multiplexed bus is selected.
LVD	CMPA2	Input	Detection target voltage pin for voltage detection 2.
Interrupts	NMI	Input	Non-maskable interrupt request pin.
	IRQ0 to IRQ7	Input	Interrupt request pins.

1.5 Pin Assignments

Figure 1.3 to Figure 1.9 show the pin assignments. Table 1.6 to Table 1.10 show the lists of pins and pin functions.

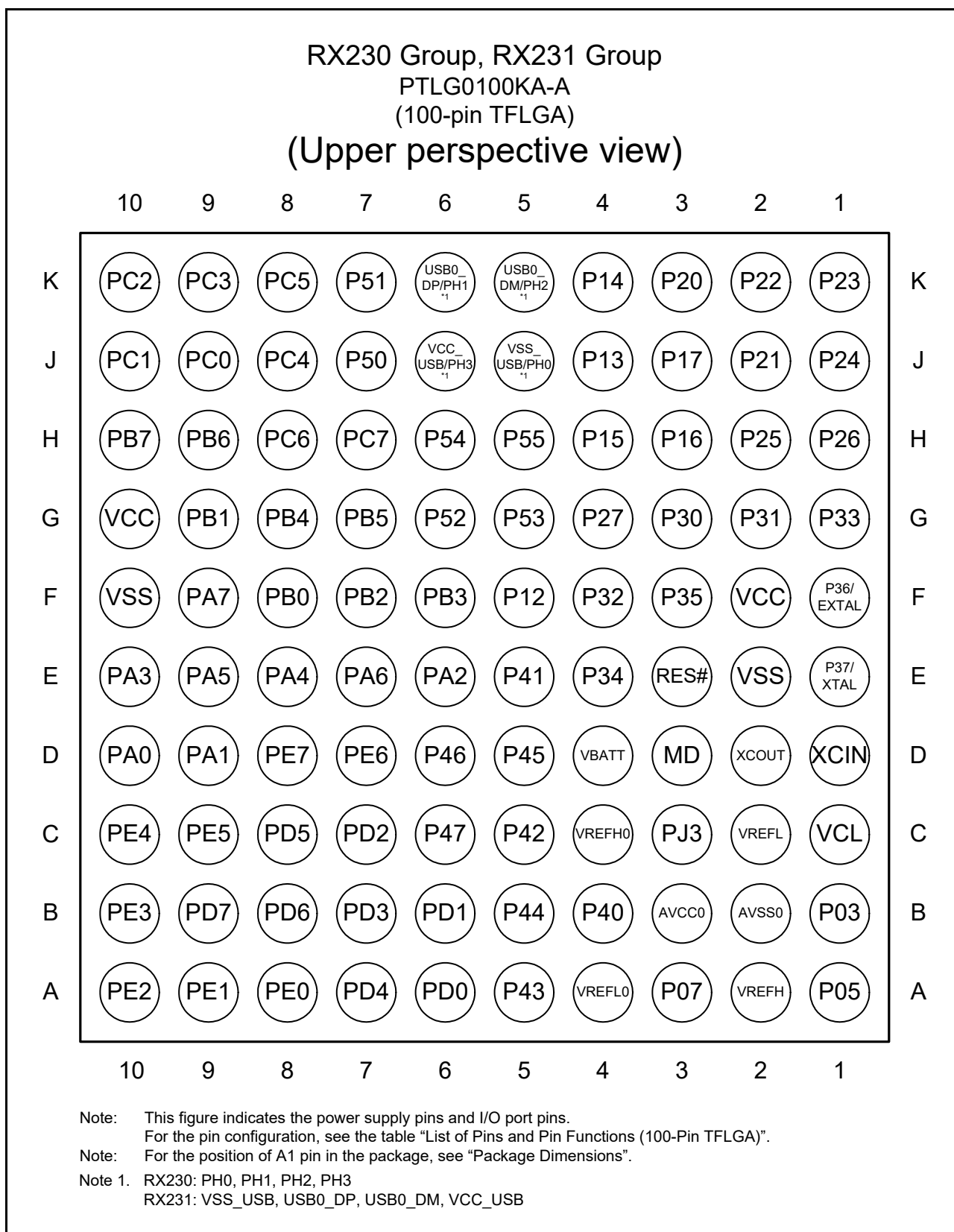


Figure 1.3 Pin Assignments of the 100-Pin TFLGA (Upper Perspective View)

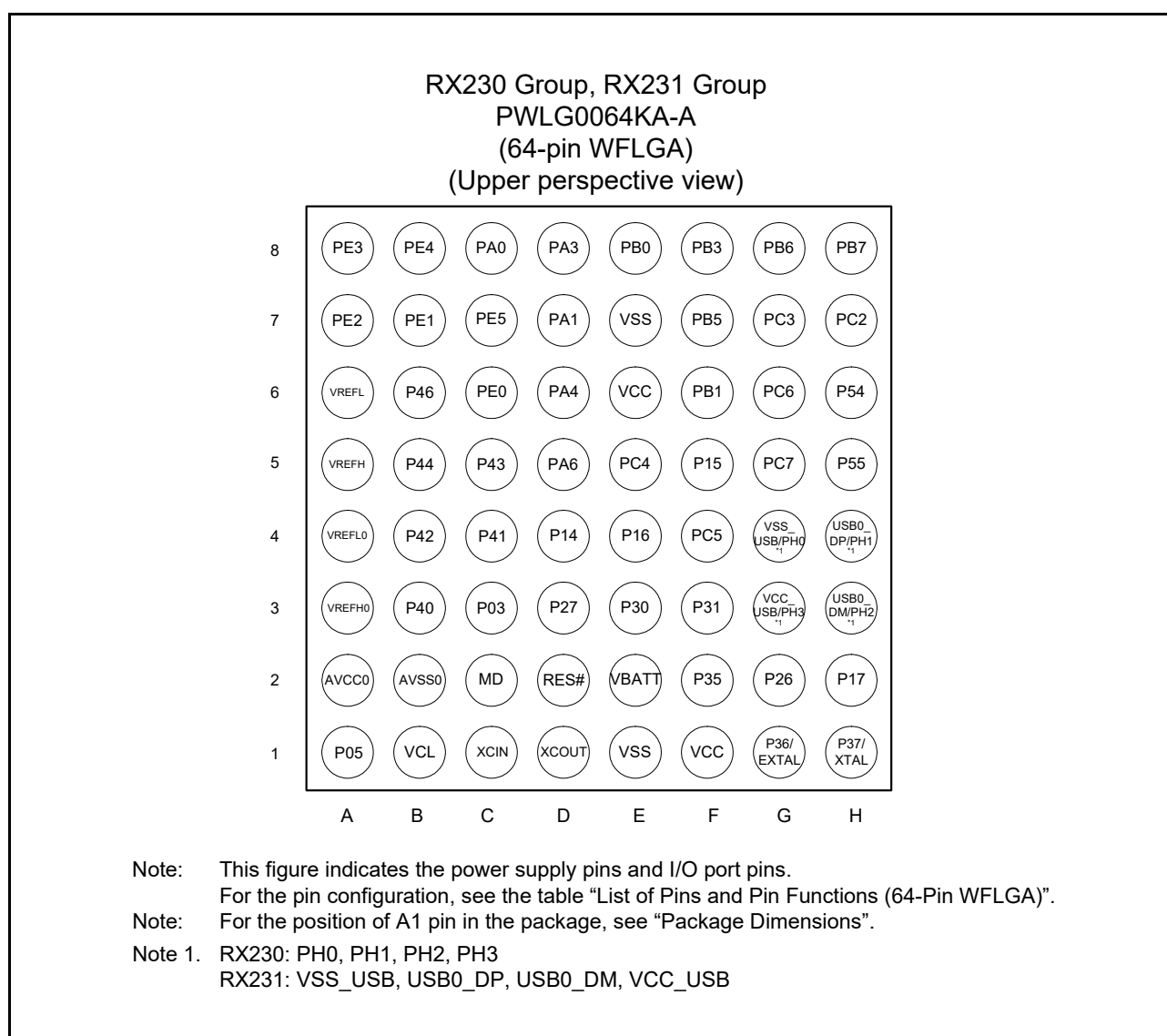
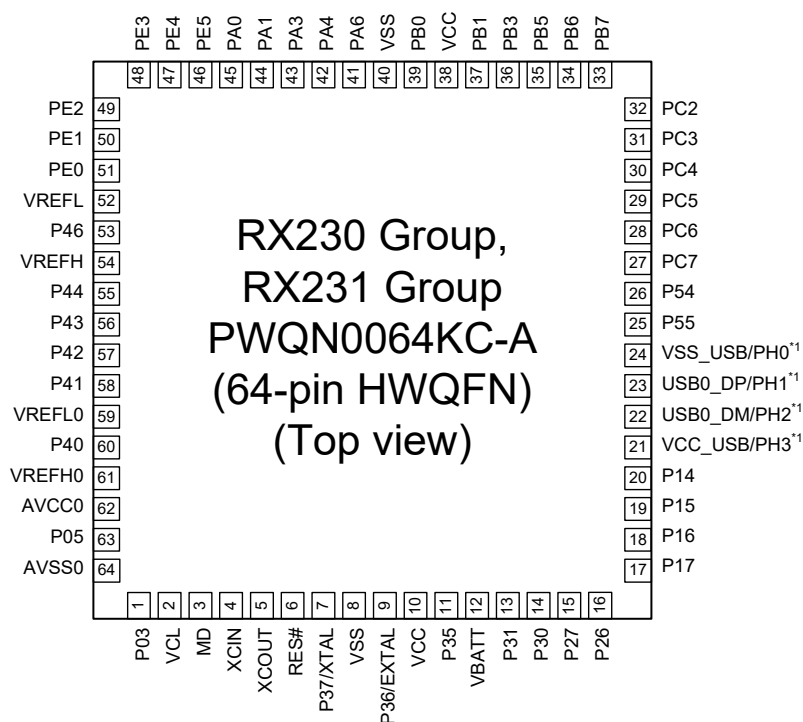


Figure 1.5 Pin Assignments of the 64-Pin WFLGA



- Note: This figure indicates the power supply pins and I/O port pins.
For the pin configuration, see the table "List of Pins and Pin Functions (64-Pin LQFP/HWQFN)".
- Note: It is recommended to connect an exposed die pad to VSS.
- Note 1. RX230: PH0, PH1, PH2, PH3
RX231: VSS_USB, USB0_DP, USB0_DM, VCC_USB

Figure 1.6 Pin Assignments of the 64-Pin HWQFN

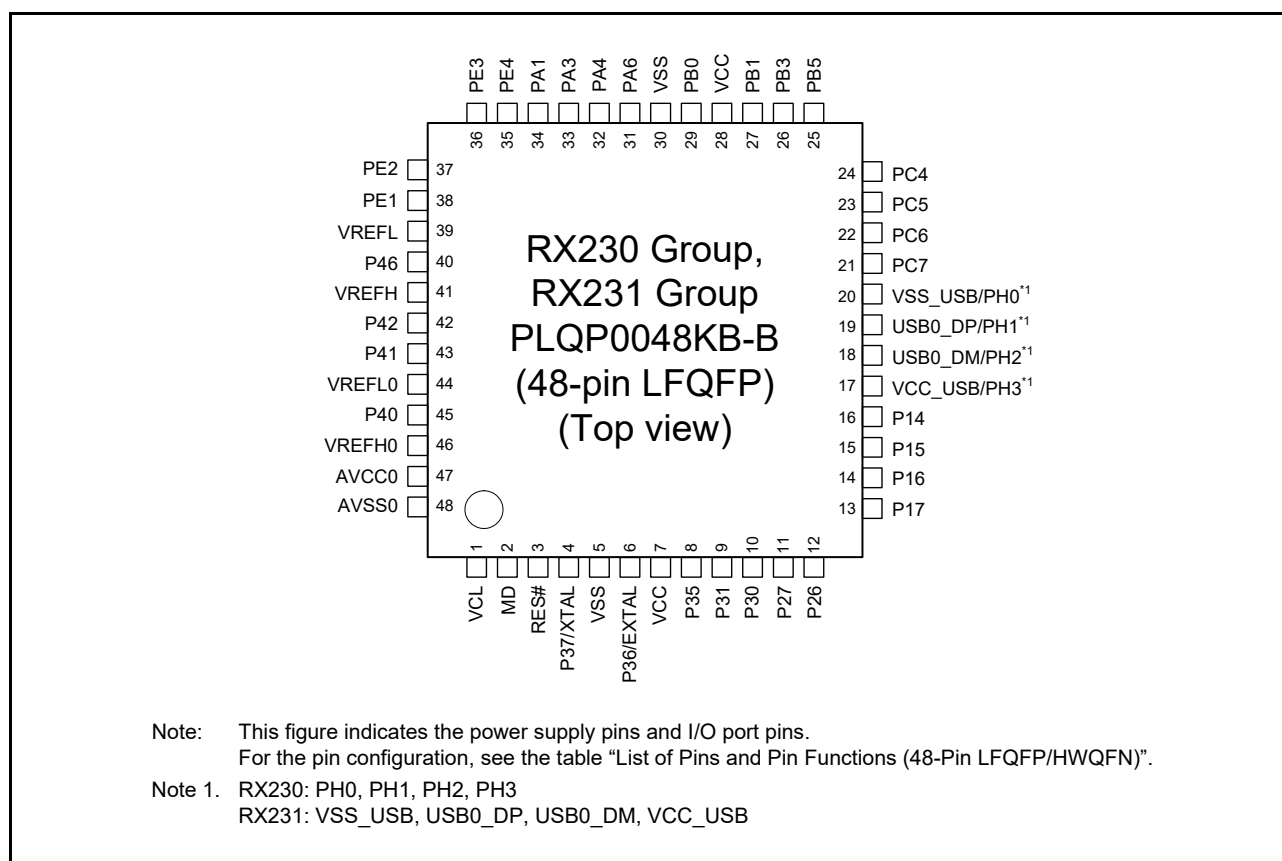


Figure 1.8 Pin Assignments of the 48-Pin LQFP

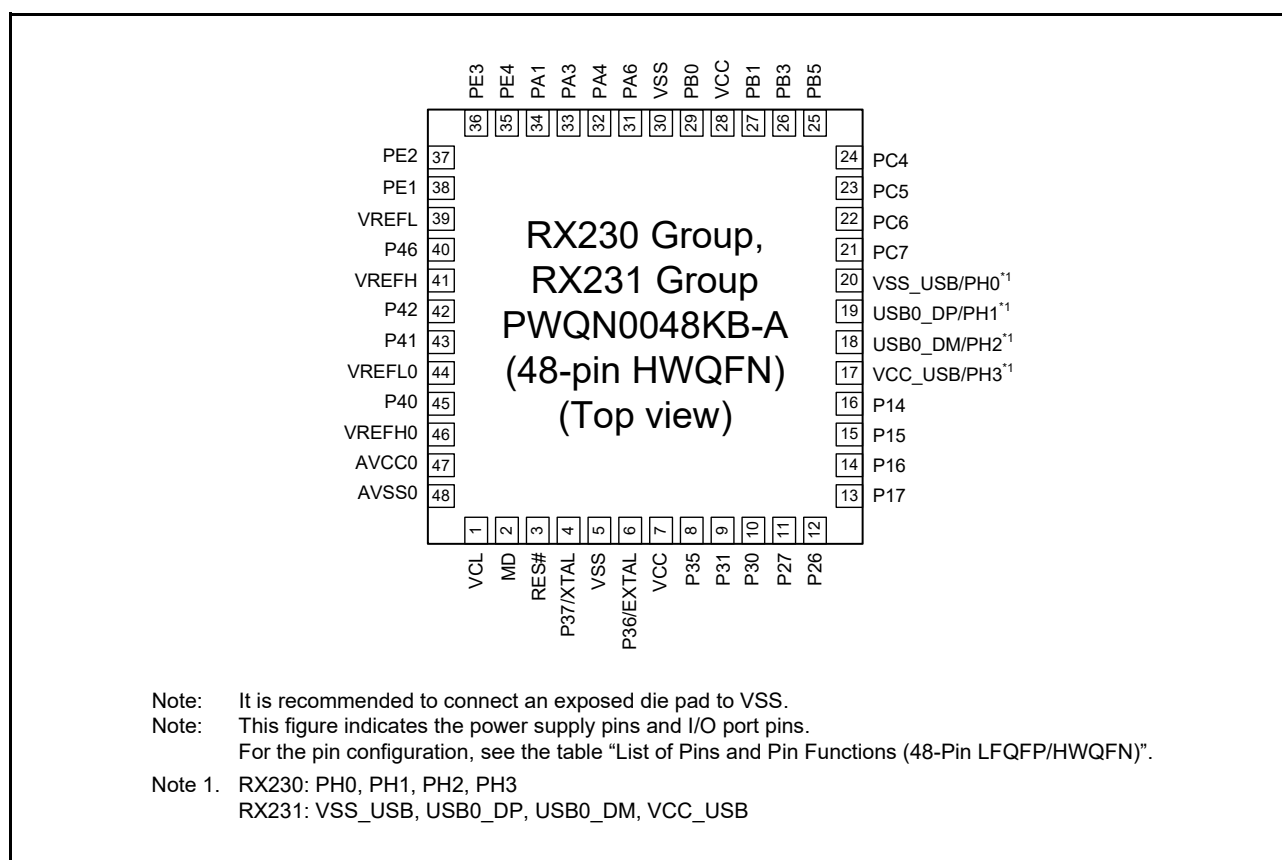


Figure 1.9 Pin Assignments of the 48-Pin HWQFN

Table 1.7 List of Pins and Pin Functions (100-Pin LQFP) (1/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCI, RSPI, RIIC, RSCAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
1	VREFH							
2		P03						DA0
3	VREFL							
4		PJ3		MTIOC3C	CTS6#/RTS6#/SS6#			
5	VCL							
6	VBATT							
7	MD							FINED
8	XCIN							
9	XCOUT							
10	RES#							
11	XTAL	P37						
12	VSS							
13	EXTAL	P36						
14	VCC							
15	UPSEL	P35						NMI
16		P34		MTIOC0A/TMC13/POE2#	SCK6		TS0	IRQ4
17		P33		MTIOC0D/TMRI3/POE3#/TIOC0D	RXD6/SMISO6/SSCL6		TS1	IRQ3
18		P32		MTIOC0C/TMO3/TIOCC0/RTCOUT/RTCIC2	TXD6/SMOSI6/SSDA6/USB0_VBUSEN			IRQ2
19		P31		MTIOC4D/TMC12/RTCIC1	CTS1#/RTS1#/SS1#/SSISCK0			IRQ1
20		P30		MTIOC4B/TMRI3/POE8#/RTCIC0	RXD1/SMISO1/SSCL1/AUDIO_MCLK			IRQ0/CMPOB3
21		P27	CS3#	MTIOC2B/TMC13	SCK1/SSIWS0		TS2	CVREFB3
22		P26	CS2#	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1/SSIRXD0		TS3	CMPB3
23		P25	CS1#	MTIOC4C/MTCLKB/TIOCA4			TS4	ADTRG0#
24		P24	CS0#	MTIOC4A/MTCLKA/TMRI1/TIOCB4	USB0_VBUSEN		TS5	
25		P23		MTIOC3D/MTCLKD/TIOC0D3	CTS0#/RTS0#/SS0#/SSISCK0		TS6	
26		P22		MTIOC3B/MTCLKC/TMO0/TIOCC3	SCK0/USB0_OVRCURB/AUDIO_MCLK		TS7	
27		P21		MTIOC1B/TMC10/TIOCA3	RXD0/SMISO0/SSCL0/USB0_EXICEN/SSIWS0		TS8	
28		P20		MTIOC1A/TMRI0/TIOCB3	TXD0/SMOSI0/SSDA0/USB0_ID/SSIRXD0		TS9	
29		P17		MTIOC3A/MTIOC3B/TMO1/POE8#/TIOCB0/TCLKD	SCK1/MISOA/SDA/SSITXD0			IRQ7/CMPOB2
30		P16		MTIOC3C/MTIOC3D/TMO2/TIOCB1/TCLKC/RTCOUT	TXD1/SMOSI1/SSDA1/MOSIA/SCL/USB0_VBUS/USB0_VBUSEN/USB0_OVRCURB			IRQ6/ADTRG0#
31		P15		MTIOC0B/MTCLKB/TMC12/TIOCB2/TCLKB	RXD1/SMISO1/SSCL1/CRXD0		TS12	IRQ5/CMPB2
32		P14		MTIOC3A/MTCLKA/TMRI2/TIOCB5/TCLKA	CTS1#/RTS1#/SS1#/CTXD0/USB0_OVRCURA		TS13	IRQ4/CVREFB2
33		P13		MTIOC0B/TMO3/TIOCA5	SDA			IRQ3
34		P12		TMC11	SCL			IRQ2
35	VCC_USB*1	PH3*1		TMC10*1				
36		PH2*1		TMRI0*1	USB0_DM*1			IRQ1*1
37		PH1*1		TMO0*1	USB0_DP*1			IRQ0*1
38	VSS_USB*1	PH0*1						CACREF*1
39		P55	WAIT#	MTIOC4D/TMO3	CRXD0		TS15	
40		P54	ALE	MTIOC4B/TMC11	CTXD0		TS16	
41	BCLK	P53					TS17	

Table 1.7 List of Pins and Pin Functions (100-Pin LFQFP) (2/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCI, RSPI, IIC, RSCAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
42		P52	RD#				TS18	
43		P51	WR1#/BC1#/WAIT#				TS19	
44		P50	WR0#/WR#				TS20	
45	UB	PC7	A23/CS0#	MTIOC3A/MTCLKB/TMO2	TXD8/SMOSI8/SSDA8/MISOA			CACREF
46		PC6	A22/CS1#	MTIOC3C/MTCLKA/TMC12	RXD8/SMISO8/SSCL8/MOSIA		TS22	
47		PC5	A21/CS2#/WAIT#	MTIOC3B/MTCLKD/TMRI2	SCK8/RSPCKA		TS23	
48		PC4	A20/CS3#	MTIOC3D/MTCLKC/TMC11/POE0#	SCK5/CTS8#/RTS8#/SS8#/SSLA0	SDHI_D1	TSCAP	
49		PC3	A19	MTIOC4D/TCLKB	TXD5/SMOSI5/SSDA5/IRTXD5	SDHI_D0	TS27	
50		PC2	A18	MTIOC4B/TCLKA	RXD5/SMISO5/SSCL5/SSLA3/IRRXD5	SDHI_D3	TS30	
51		PC1	A17	MTIOC3A/TCLKD	SCK5/SSLA2		TS33	
52		PC0	A16	MTIOC3C/TCLKC	CTS5#/RTS5#/SS5#/SSLA1		TS35	
53		PB7	A15	MTIOC3B/TIOCB5	TXD9/SMOSI9/SSDA9	SDHI_D2		
54		PB6	A14	MTIOC3D/TIOCA5	RXD9/SMISO9/SSCL9	SDHI_D1		
55		PB5	A13	MTIOC2A/MTIOC1B/TMRI1/POE1#/TIOCB4	SCK9/USB0_VBUS	SDHI_CD		
56		PB4	A12	TIOCA4	CTS9#/RTS9#/SS9#			
57		PB3	A11	MTIOC0A/MTIOC4A/TMO0/POE3#/TIOC3D/TCLKD	SCK6	SDHI_W P		
58		PB2	A10	TIOCC3/TCLKC	CTS6#/RTS6#/SS6#			
59		PB1	A9	MTIOC0C/MTIOC4C/TMC10/TIOCB3	TXD6/SMOSI6/SSDA6	SDHI_CLK		IRQ4/CMPOB1
60	VCC							
61		PB0	A8	MTIC5W/TIOCA3	RXD6/SMISO6/SSCL6/RSPCKA	SDHI_C MD		
62	VSS							
63		PA7	A7	TIOCB2	MISOA			
64		PA6	A6	MTIC5V/MTCLKB/TMC13/POE2#/TIOCA2	CTS5#/RTS5#/SS5#/MOSIA/SSIWS0			
65		PA5	A5	TIOCB1	RSPCKA			
66		PA4	A4	MTIC5U/MTCLKA/TMRI0/TIOCA1	TXD5/SMOSI5/SSDA5/SSLA0/SSITXD0/IRTXD5			IRQ5 / CVREFB1
67		PA3	A3	MTIOC0D/MTCLKD/TIOC0D/TCLKB	RXD5/SMISO5/SSCL5/SSIRXD0/IRRXD5			IRQ6 /CMPB1
68		PA2	A2		RXD5/SMISO5/SSCL5/SSLA3/IRRXD5			
69		PA1	A1	MTIOC0B/MTCLKC/TIOCB0	SCK5/SSLA2/SSISCK0			
70		PA0	A0/BC0#	MTIOC4A/TIOCA0	SSLA1			CACREF
71		PE7	D15[A15/D15]					IRQ7/AN023
72		PE6	D14[A14/D14]					IRQ6/AN022
73		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B				IRQ5/AN021/CMPOB0
74		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A				AN020/ CMPA2/ CLKOUT
75		PE3	D11[A11/D11]	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#/AUDIO_MCLK			AN019/ CLKOUT
76		PE2	D10[A10/D10]	MTIOC4A	RXD12/RXDX12/SMISO12/SSCL12			IRQ7/AN018/ CVREFB0
77		PE1	D9[A9/D9]	MTIOC4C	TXD12/TXDX12/SIOX12/SMOSI12/SSDA12			AN017/ CMPB0
78		PE0	D8[A8/D8]		SCK12			AN016

Table 4.1 List of I/O Registers (Address Order) (3/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
0008 240Ch	DTC	DTC Module Start Register	DTCST	8	8		2 ICLK
0008 240Eh	DTC	DTC Status Register	DTCSTS	16	16		2 ICLK
0008 3002h	BSC	CS0 Mode Register	CS0MOD	16	16		1 or 2 BCLK
0008 3004h	BSC	CS0 Wait Control Register 1	CS0WCR1	32	32		1 or 2 BCLK
0008 3008h	BSC	CS0 Wait Control Register 2	CS0WCR2	32	32		1 or 2 BCLK
0008 3012h	BSC	CS1 Mode Register	CS1MOD	16	16		1 or 2 BCLK
0008 3014h	BSC	CS1 Wait Control Register 1	CS1WCR1	32	32		1 or 2 BCLK
0008 3018h	BSC	CS1 Wait Control Register 2	CS1WCR2	32	32		1 or 2 BCLK
0008 3022h	BSC	CS2 Mode Register	CS2MOD	16	16		1 or 2 BCLK
0008 3024h	BSC	CS2 Wait Control Register 1	CS2WCR1	32	32		1 or 2 BCLK
0008 3028h	BSC	CS2 Wait Control Register 2	CS2WCR2	32	32		1 or 2 BCLK
0008 3032h	BSC	CS3 Mode Register	CS3MOD	16	16		1 or 2 BCLK
0008 3034h	BSC	CS3 Wait Control Register 1	CS3WCR1	32	32		1 or 2 BCLK
0008 3038h	BSC	CS3 Wait Control Register 2	CS3WCR2	32	32		1 or 2 BCLK
0008 3802h	BSC	CS0 Control Register	CS0CR	16	16		1 or 2 BCLK
0008 380Ah	BSC	CS0 Recovery Cycle Register	CS0REC	16	16		1 or 2 BCLK
0008 3812h	BSC	CS1 Control Register	CS1CR	16	16		1 or 2 BCLK
0008 381Ah	BSC	CS1 Recovery Cycle Register	CS1REC	16	16		1 or 2 BCLK
0008 3822h	BSC	CS2 Control Register	CS2CR	16	16		1 or 2 BCLK
0008 382Ah	BSC	CS2 Recovery Cycle Register	CS2REC	16	16		1 or 2 BCLK
0008 3832h	BSC	CS3 Control Register	CS3CR	16	16		1 or 2 BCLK
0008 383Ah	BSC	CS3 Recovery Cycle Register	CS3REC	16	16		1 or 2 BCLK
0008 3880h	BSC	CS Recovery Cycle Insertion Enable Register	CSRECEN	16	16		1 or 2 BCLK
0008 6400h	MPU	Region-0 Start Page Number Register	RSPAGE0	32	32		1 ICLK
0008 6404h	MPU	Region-0 End Page Number Register	REPAGE0	32	32		1 ICLK
0008 6408h	MPU	Region-1 Start Page Number Register	RSPAGE1	32	32		1 ICLK
0008 640Ch	MPU	Region-1 End Page Number Register	REPAGE1	32	32		1 ICLK
0008 6410h	MPU	Region-2 Start Page Number Register	RSPAGE2	32	32		1 ICLK
0008 6414h	MPU	Region-2 End Page Number Register	REPAGE2	32	32		1 ICLK
0008 6418h	MPU	Region-3 Start Page Number Register	RSPAGE3	32	32		1 ICLK
0008 641Ch	MPU	Region-3 End Page Number Register	REPAGE3	32	32		1 ICLK
0008 6420h	MPU	Region-4 Start Page Number Register	RSPAGE4	32	32		1 ICLK
0008 6424h	MPU	Region-4 End Page Number Register	REPAGE4	32	32		1 ICLK
0008 6428h	MPU	Region-5 Start Page Number Register	RSPAGE5	32	32		1 ICLK
0008 642Ch	MPU	Region-5 End Page Number Register	REPAGE5	32	32		1 ICLK
0008 6430h	MPU	Region-6 Start Page Number Register	RSPAGE6	32	32		1 ICLK
0008 6434h	MPU	Region-6 End Page Number Register	REPAGE6	32	32		1 ICLK
0008 6438h	MPU	Region-7 Start Page Number Register	RSPAGE7	32	32		1 ICLK
0008 643Ch	MPU	Region-7 End Page Number Register	REPAGE7	32	32		1 ICLK
0008 6500h	MPU	Memory-Protection Enable Register	MPEN	32	32		1 ICLK
0008 6504h	MPU	Background Access Control Register	MPBAC	32	32		1 ICLK
0008 6508h	MPU	Memory-Protection Error Status-Clearing Register	MPECLR	32	32		1 ICLK
0008 650Ch	MPU	Memory-Protection Error Status Register	MPESTS	32	32		1 ICLK
0008 6514h	MPU	Data Memory-Protection Error Address Register	MPDEA	32	32		1 ICLK
0008 6520h	MPU	Region Search Address Register	MPSA	32	32		1 ICLK
0008 6524h	MPU	Region Search Operation Register	MPOPS	16	16		1 ICLK
0008 6526h	MPU	Region Invalidation Operation Register	MPOPI	16	16		1 ICLK
0008 6528h	MPU	Instruction-Hit Region Register	MHITI	32	32		1 ICLK
0008 652Ch	MPU	Data-Hit Region Register	MHITD	32	32		1 ICLK
0008 7010h to 0008 70FFh	ICU	Interrupt Request Register 016 to Interrupt Request Register 255	IR016 to IR255	8	8		2 ICLK

Table 4.1 List of I/O Registers (Address Order) (21/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK $\geq$ PCLK	ICLK < PCLK
000A 0008h	USB0	Device State Control Register 0	DVSTCTR0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^2$
000A 0014h	USB0	CFIFO Port Register	CFIFO	16	16	3, 4 PCLKB	2 ICLK
000A 0018h	USB0	D0FIFO Port Register	D0FIFO	16	16	3, 4 PCLKB	2 ICLK
000A 001Ch	USB0	D1FIFO Port Register	D1FIFO	16	16	3, 4 PCLKB	2 ICLK
000A 0020h	USB0	CFIFO Port Select Register	CFIFOSEL	16	16	3, 4 PCLKB	2 ICLK
000A 0022h	USB0	CFIFO Port Control Register	CFIFOCTR	16	16	3, 4 PCLKB	2 ICLK
000A 0028h	USB0	D0FIFO Port Select Register	D0FIFOSEL	16	16	3, 4 PCLKB	2 ICLK
000A 002Ah	USB0	D0FIFO Port Control Register	D0FIFOCTR	16	16	3, 4 PCLKB	2 ICLK
000A 002Ch	USB0	D1FIFO Port Select Register	D1FIFOSEL	16	16	3, 4 PCLKB	2 ICLK
000A 002Eh	USB0	D1FIFO Port Control Register	D1FIFOCTR	16	16	3, 4 PCLKB	2 ICLK
000A 0030h	USB0	Interrupt Enable Register 0	INTENB0	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^2$
000A 0032h	USB0	Interrupt Enable Register 1	INTENB1	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^2$
000A 0036h	USB0	BRDY Interrupt Enable Register	BRDYENB	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^2$
000A 0038h	USB0	NRDY Interrupt Enable Register	NRDYENB	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^2$
000A 003Ah	USB0	BEMP Interrupt Enable Register	BEMPENB	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^2$
000A 003Ch	USB0	SOF Output Configuration Register	SOFCFG	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^2$
000A 0040h	USB0	Interrupt Status Register 0	INTSTS0	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^2$
000A 0042h	USB0	Interrupt Status Register 1	INTSTS1	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^2$
000A 0046h	USB0	BRDY Interrupt Status Register	BRDYSTS	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^2$
000A 0048h	USB0	NRDY Interrupt Status Register	NRDYSTS	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^2$
000A 004Ah	USB0	BEMP Interrupt Status Register	BEMPSTS	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^2$
000A 004Ch	USB0	Frame Number Register	FRMNUM	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^2$
000A 0054h	USB0	USB Request Type Register	USBREQ	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^2$
000A 0056h	USB0	USB Request Value Register	USBVAL	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^2$
000A 0058h	USB0	USB Request Index Register	USBINDX	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^2$
000A 005Ah	USB0	USB Request Length Register	USBLENG	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^2$
000A 005Ch	USB0	DCP Configuration Register	DCPCFG	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^2$
000A 005Eh	USB0	DCP Maximum Packet Size Register	DCPMAXP	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^2$

Table 4.1 List of I/O Registers (Address Order) (23/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
000A 00B0h	USB0	BC Control Register 0	USBBCCTRL0	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ²
000A 00CCh	USB0	USB Module Control Register	USBMC	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ²
000A 00D0h	USB0	Device Address 0 Configuration Register	DEVADD0	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ²
000A 00D2h	USB0	Device Address 1 Configuration Register	DEVADD1	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ²
000A 00D4h	USB0	Device Address 2 Configuration Register	DEVADD2	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ²
000A 00D6h	USB0	Device Address 3 Configuration Register	DEVADD3	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ²
000A 00D8h	USB0	Device Address 4 Configuration Register	DEVADD4	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ²
000A 00DAh	USB0	Device Address 5 Configuration Register	DEVADD5	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ²
000A 0900h	CTSU	CTSU Control Register 0	CTSUCR0	8	8	2 or 3 PCLKB	2 ICLK
000A 0901h	CTSU	CTSU Control Register 1	CTSUCR1	8	8	2 or 3 PCLKB	2 ICLK
000A 0902h	CTSU	CTSU Synchronous Noise Reduction Setting Register	CTSUSDPRS	8	8	2 or 3 PCLKB	2 ICLK
000A 0903h	CTSU	CTSU Sensor Stabilization Wait Control Register	CTSUSST	8	8	2 or 3 PCLKB	2 ICLK
000A 0904h	CTSU	CTSU Measurement Channel Register 0	CTSUMCH0	8	8	2 or 3 PCLKB	2 ICLK
000A 0905h	CTSU	CTSU Measurement Channel Register 1	CTSUMCH1	8	8	2 or 3 PCLKB	2 ICLK
000A 0906h	CTSU	CTSU Channel Enable Control Register 0	CTSUCHAC0	8	8	2 or 3 PCLKB	2 ICLK
000A 0907h	CTSU	CTSU Channel Enable Control Register 1	CTSUCHAC1	8	8	2 or 3 PCLKB	2 ICLK
000A 0908h	CTSU	CTSU Channel Enable Control Register 2	CTSUCHAC2	8	8	2 or 3 PCLKB	2 ICLK
000A 0909h	CTSU	CTSU Channel Enable Control Register 3	CTSUCHAC3	8	8	2 or 3 PCLKB	2 ICLK
000A 090Ah	CTSU	CTSU Channel Enable Control Register 4	CTSUCHAC4	8	8	2 or 3 PCLKB	2 ICLK
000A 090Bh	CTSU	CTSU Channel Transmit/Receive Control Register 0	CTSUCHTRC0	8	8	2 or 3 PCLKB	2 ICLK
000A 090Ch	CTSU	CTSU Channel Transmit/Receive Control Register 1	CTSUCHTRC1	8	8	2 or 3 PCLKB	2 ICLK
000A 090Dh	CTSU	CTSU Channel Transmit/Receive Control Register 2	CTSUCHTRC2	8	8	2 or 3 PCLKB	2 ICLK
000A 090Eh	CTSU	CTSU Channel Transmit/Receive Control Register 3	CTSUCHTRC3	8	8	2 or 3 PCLKB	2 ICLK
000A 090Fh	CTSU	CTSU Channel Transmit/Receive Control Register 4	CTSUCHTRC4	8	8	2 or 3 PCLKB	2 ICLK
000A 0910h	CTSU	CTSU High-Pass Noise Reduction Control Register	CTSUDCLKC	8	8	2 or 3 PCLKB	2 ICLK
000A 0911h	CTSU	CTSU Status Register	CTSUST	8	8	2 or 3 PCLKB	2 ICLK
000A 0912h	CTSU	CTSU High-Pass Noise Reduction Spectrum Diffusion Control Register	CTSUSSC	16	16	2 or 3 PCLKB	2 ICLK
000A 0914h	CTSU	CTSU Sensor Offset Register 0	CTSUSO0	16	16	2 or 3 PCLKB	2 ICLK
000A 0916h	CTSU	CTSU Sensor Offset Register 1	CTSUSO1	16	16	2 or 3 PCLKB	2 ICLK
000A 0918h	CTSU	CTSU Sensor Counter	CTSUSC	16	16	2 or 3 PCLKB	2 ICLK
000A 091Ah	CTSU	CTSU Reference Counter	CTSURC	16	16	2 or 3 PCLKB	2 ICLK
000A 091Ch	CTSU	CTSU Error Status Register	CTSUERRS	16	16	2 or 3 PCLKB	2 ICLK
000A 8300h	RSCAN0	Bit Configuration Register L	CFGL	16	16	2 or 3 PCLKB	2 ICLK
000A 8302h	RSCAN0	Bit Configuration Register H	CFGH	16	16	2 or 3 PCLKB	2 ICLK
000A 8304h	RSCAN0	Control Register L	CTRL	16	16	2 or 3 PCLKB	2 ICLK
000A 8306h	RSCAN0	Control Register H	CTRH	16	16	2 or 3 PCLKB	2 ICLK
000A 8308h	RSCAN0	Status Register L	STSL	16	16	2 or 3 PCLKB	2 ICLK
000A 830Ah	RSCAN0	Status Register H	STSH	16	16	2 or 3 PCLKB	2 ICLK
000A 830Ch	RSCAN0	Error Flag Register L	ERFLL	16	16	2 or 3 PCLKB	2 ICLK
000A 830Eh	RSCAN0	Error Flag Register H	ERFLH	16	16	2 or 3 PCLKB	2 ICLK
000A 8322h	RSCAN	Global Configuration Register L	GCFGFL	16	16	2 or 3 PCLKB	2 ICLK
000A 8324h	RSCAN	Global Configuration Register H	GCFGH	16	16	2 or 3 PCLKB	2 ICLK

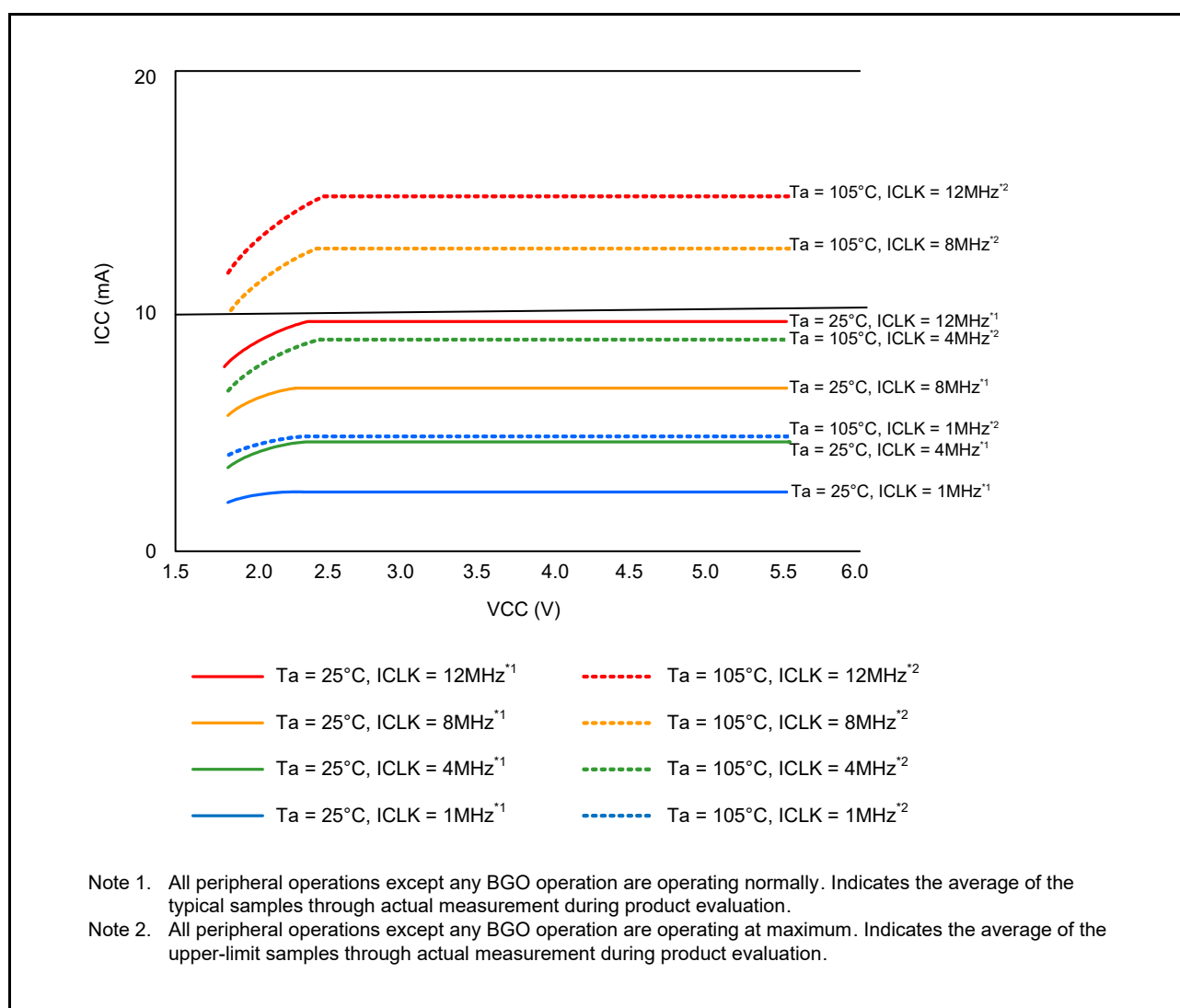


Figure 5.2 Voltage Dependency in Middle-Speed Operating Mode (Reference Data)

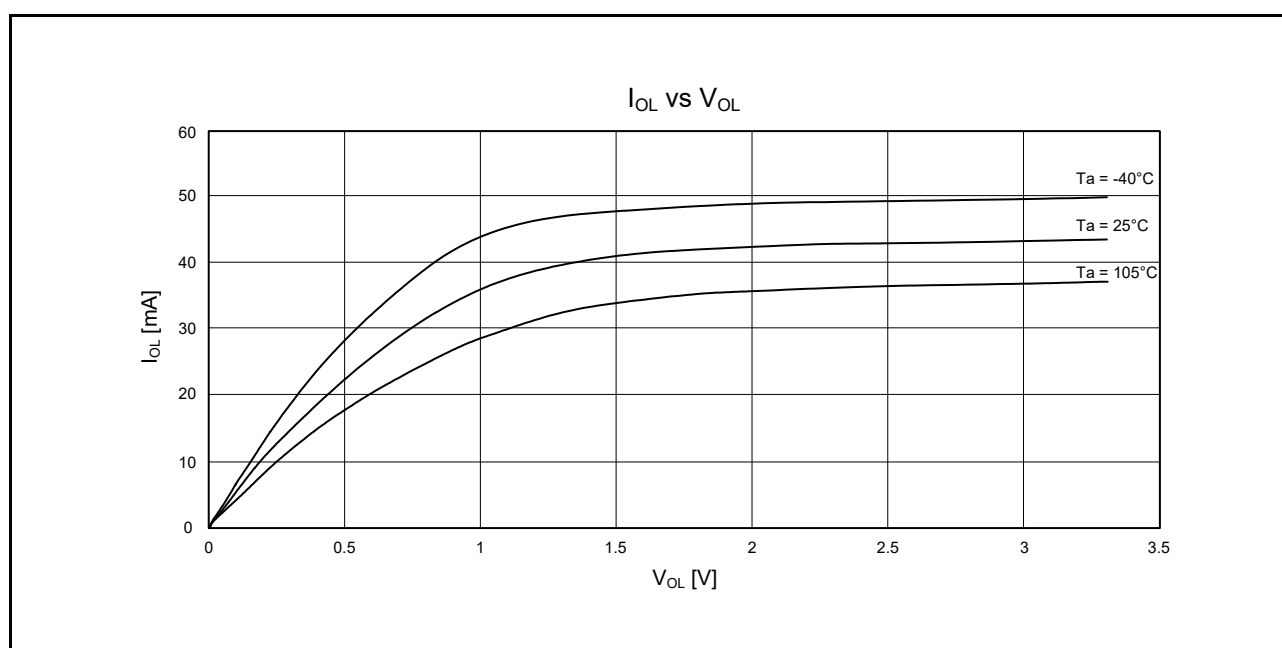


Figure 5.20 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at $V_{CC} = 3.3\text{ V}$ (Reference Data)

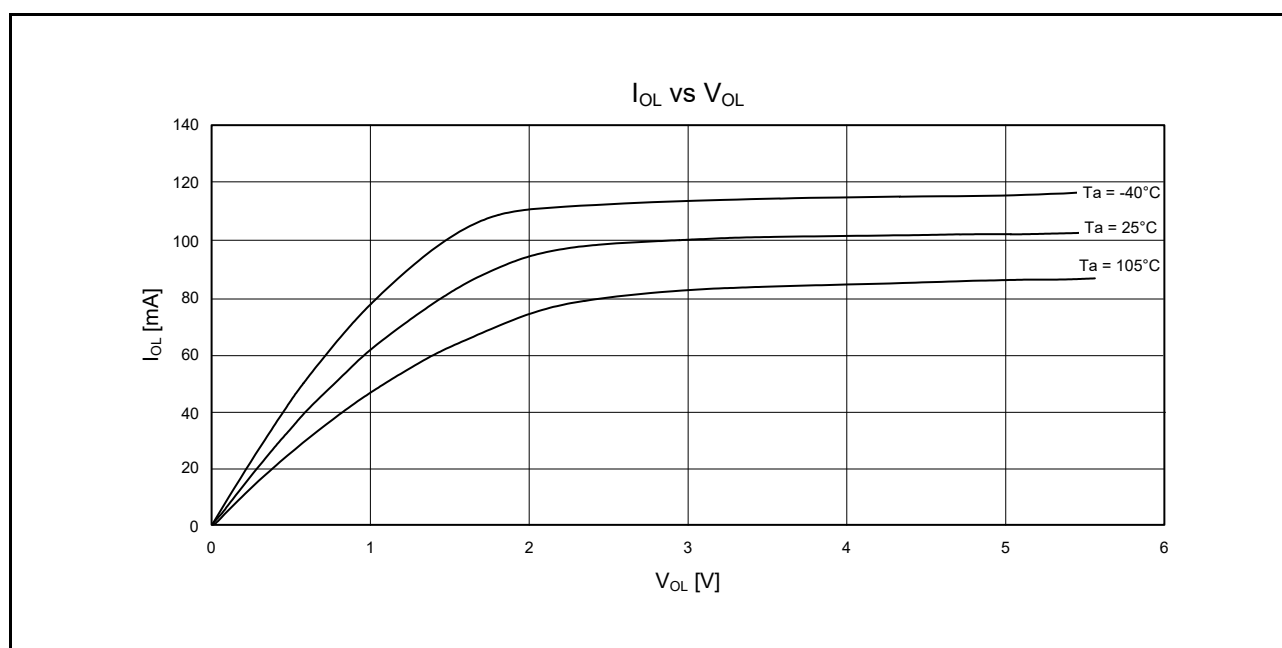


Figure 5.21 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at $V_{CC} = 5.5\text{ V}$ (Reference Data)

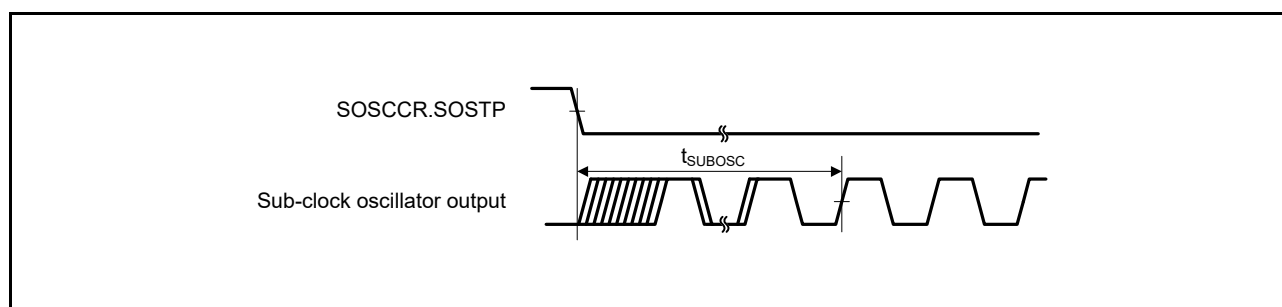


Figure 5.30 Sub-Clock Oscillation Start Timing

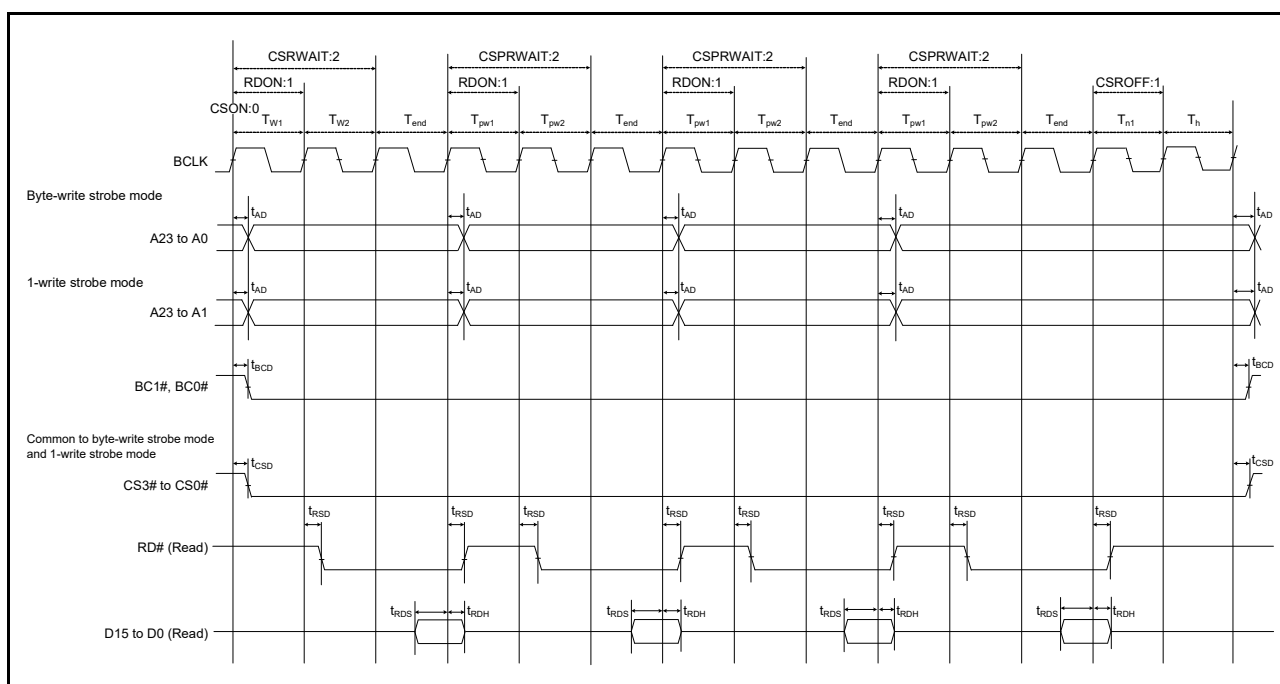


Figure 5.40 External Bus Timing/Page Read Cycle (Bus Clock Synchronization)

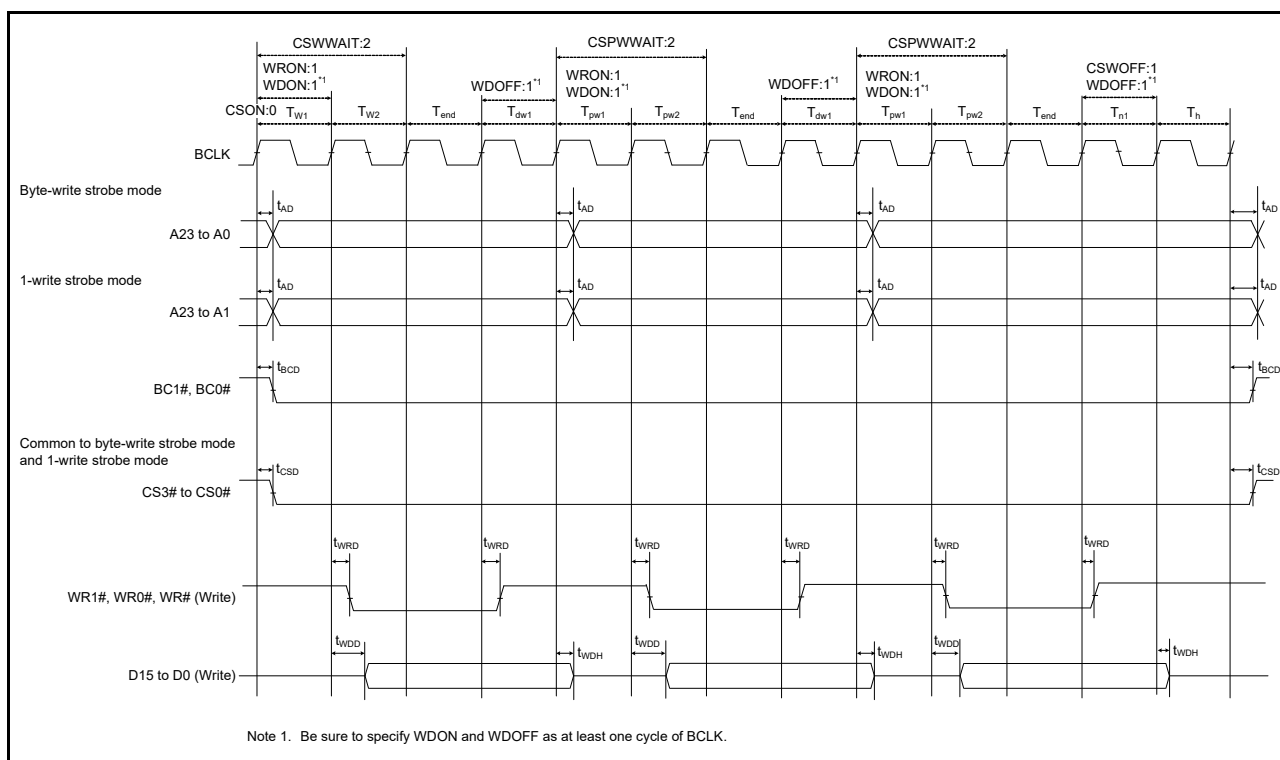


Figure 5.41 External Bus Timing/Page Write Cycle (Bus Clock Synchronization)

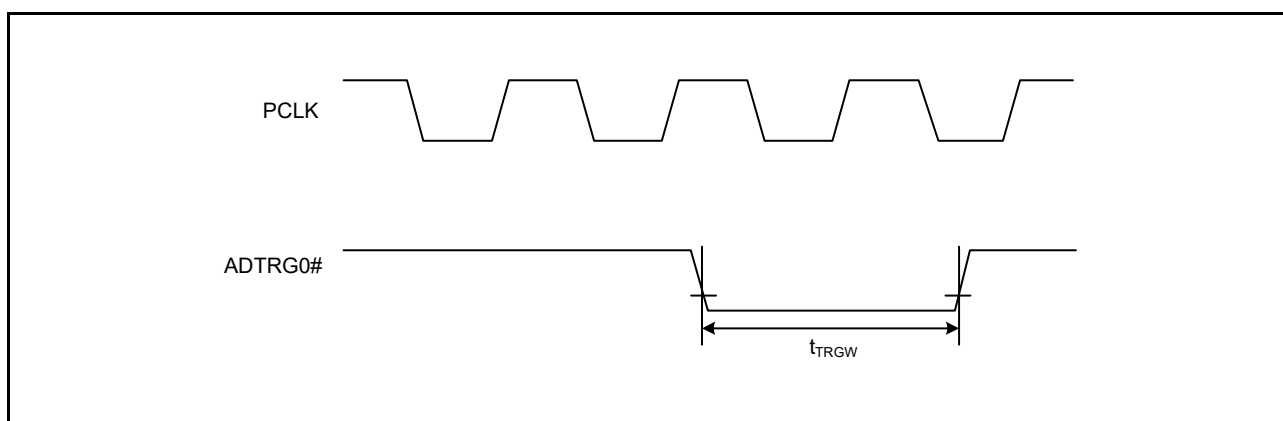


Figure 5.52 A/D Converter External Trigger Input Timing

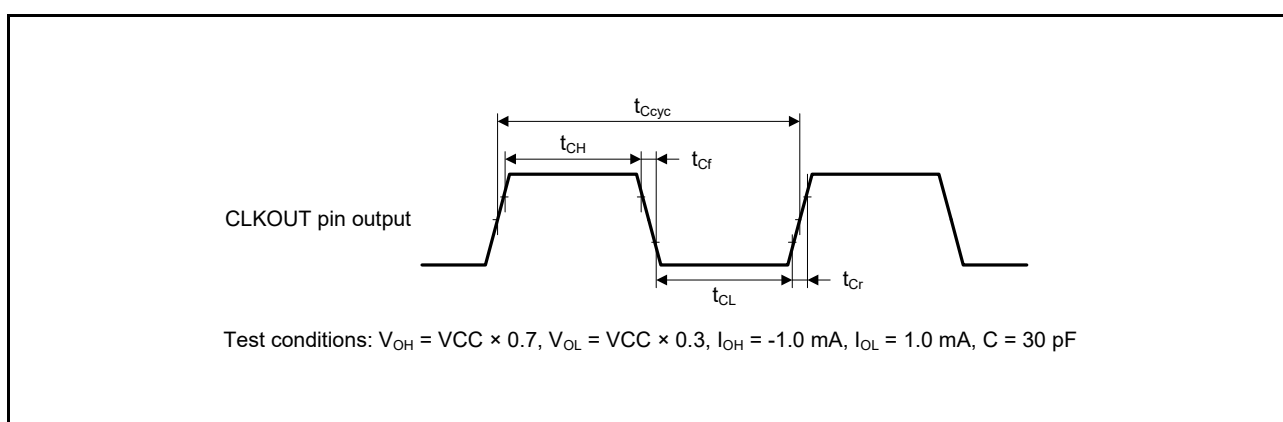


Figure 5.53 CLKOUT Output Timing

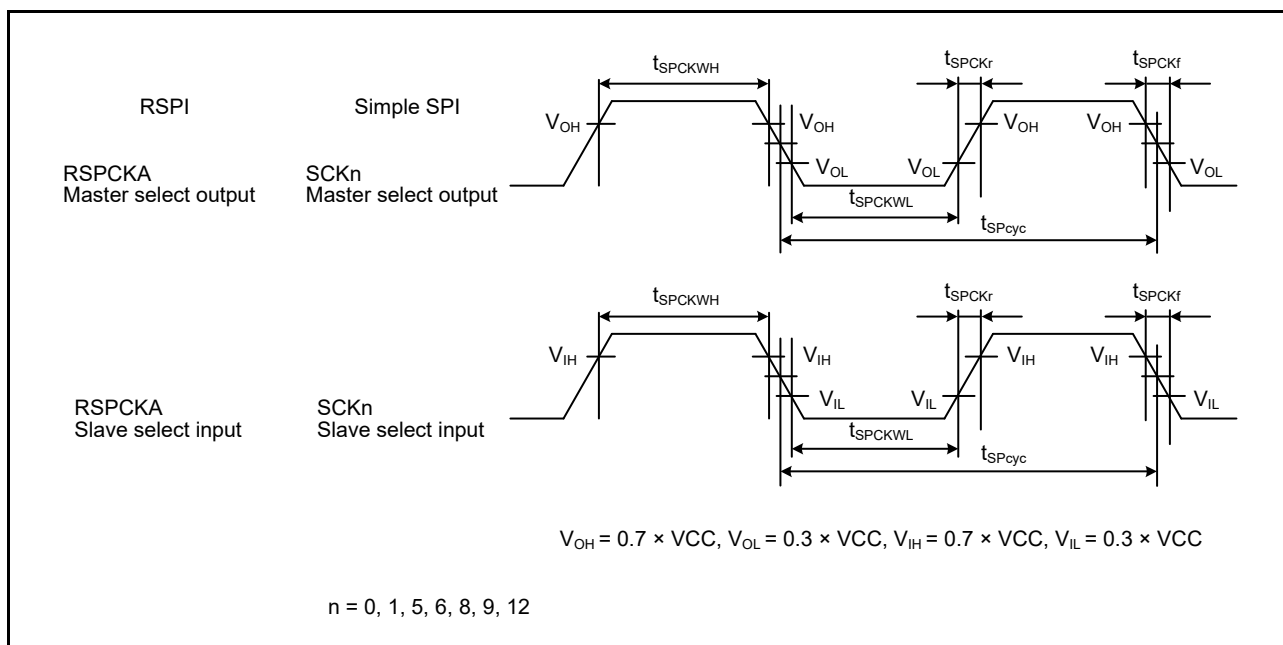


Figure 5.54 RSPI Clock Timing and Simple SPI Clock Timing

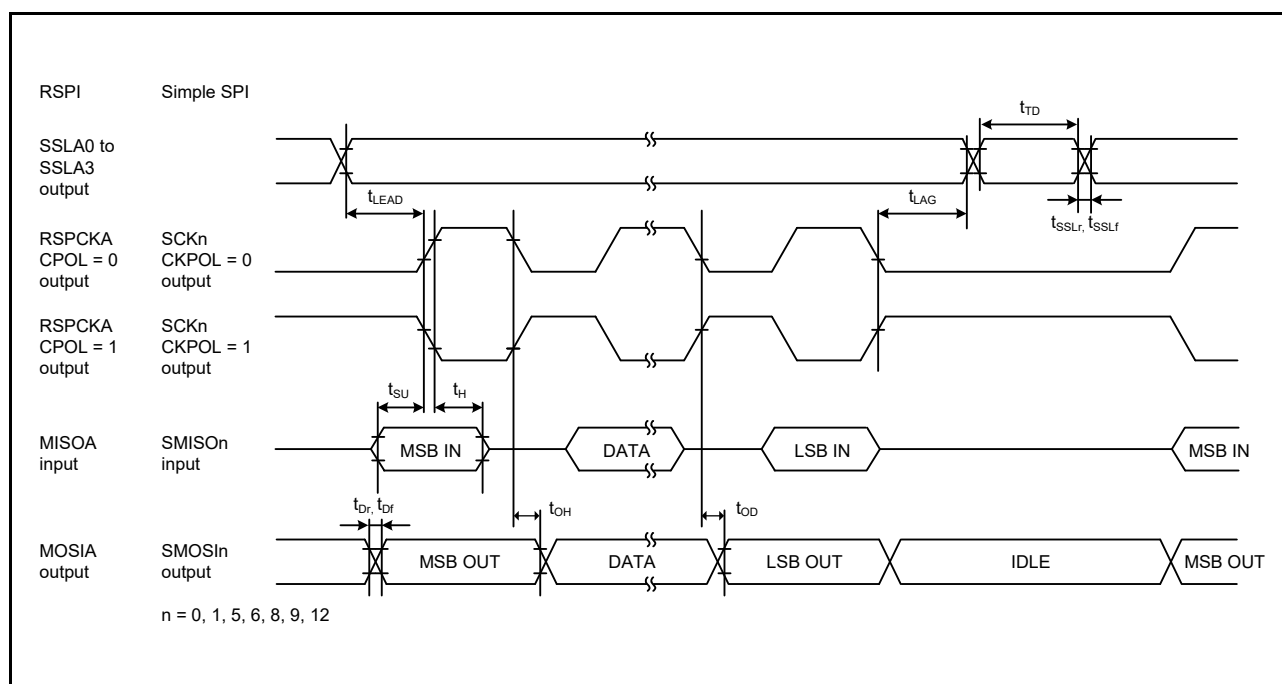


Figure 5.55 RSPI Timing (Master, CPHA = 0) and Simple SPI Clock Timing (Master, CKPH = 1)

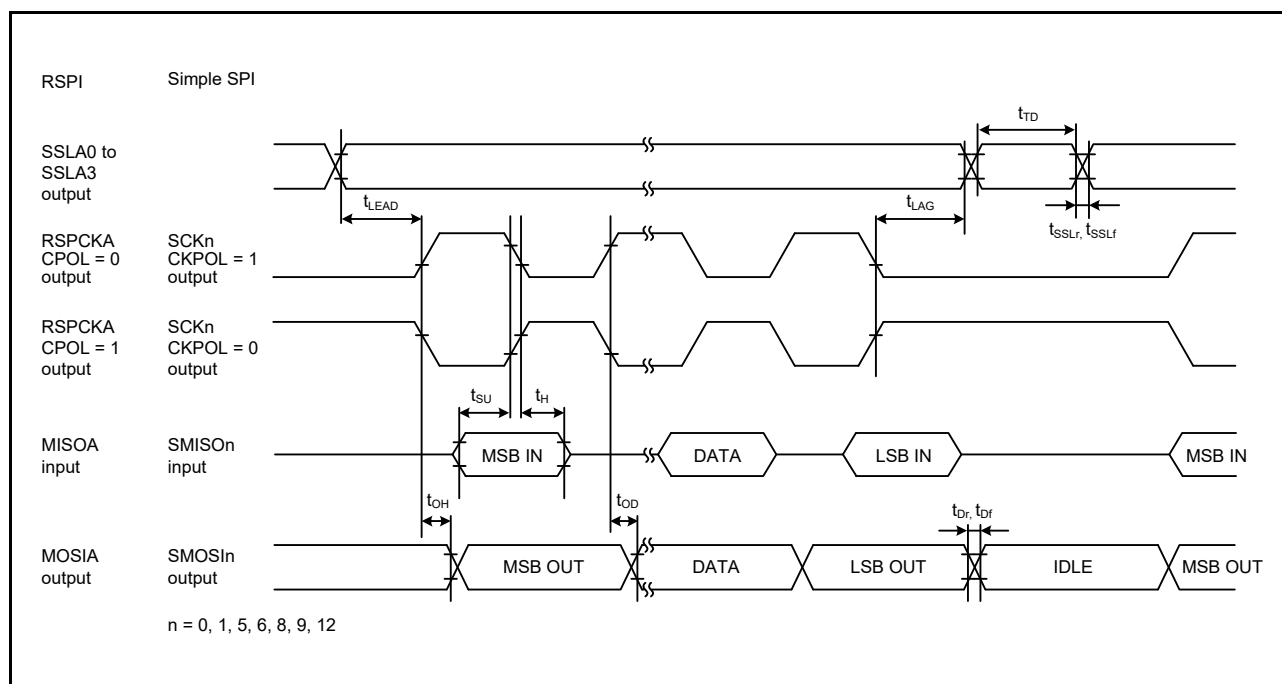


Figure 5.56 RSPI Timing (Master, CPHA = 1) and Simple SPI Clock Timing (Master, CKPH = 0)

Table 5.50 A/D Conversion Characteristics (5)

Conditions: $1.8\text{V} \leq V_{CC} = V_{CC_USB} = AVCC0 \leq 5.5\text{V}$, $1.8\text{V} \leq V_{REFH0} \leq AVCC0$, $V_{SS} = AVSS0 = V_{SS_USB} = 0\text{V}$,
reference voltage = V_{REFH0} selected, $T_a = -40$ to $+105^\circ\text{C}$

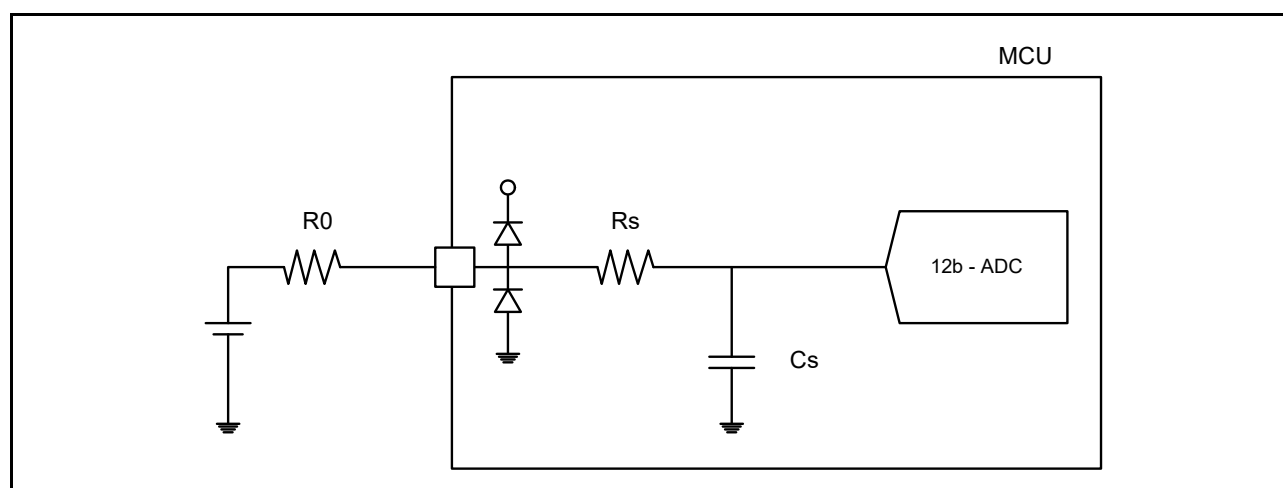
Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	8	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 8 MHz)	Permissible signal source impedance (Max.) = 5 kΩ	6.75	—	—	μs	High-precision channel The ADCSR.ADHSC bit is 1 The ADSSTRn register is 0Dh
		10.13	—	—		Normal-precision channel The ADCSR.ADHSC bit is 1 The ADSSTRn register is 28h
Analog input capacitance	Cs	—	—	15	pF	Pin capacitance included Figure 5.68
Analog input resistance	Rs	—	—	2.5	kΩ	Figure 5.68
Offset error		—	±1	±7.5	LSB	
Full-scale error		—	±1.5	±7.5	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±3.0	±8.0	LSB	
DNL differential non-linearity error		—	±1.0	—	LSB	
INL integral non-linearity error		—	±1.25	±3.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential non-linearity error, and INL integral non-linearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 5.51 A/D Converter Channel Classification

Classification	Channel	Conditions	Remarks
High-precision channel	AN000 to AN007	$AVCC0 = 1.8$ to 5.5V	Pins AN000 to AN007 cannot be used as digital outputs when the A/D converter is in use.
Normal-precision channel	AN016 to AN031		
Internal reference voltage input channel	Internal reference voltage	$AVCC0 = 2.0$ to 5.5V	
Temperature sensor input channel	Temperature sensor output	$AVCC0 = 2.0$ to 5.5V	

**Figure 5.68 Equivalent Circuit**

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HWQFN64-9x9-0.50	PWQN0064KC-A	P64K8-50-6B4-5	0.21

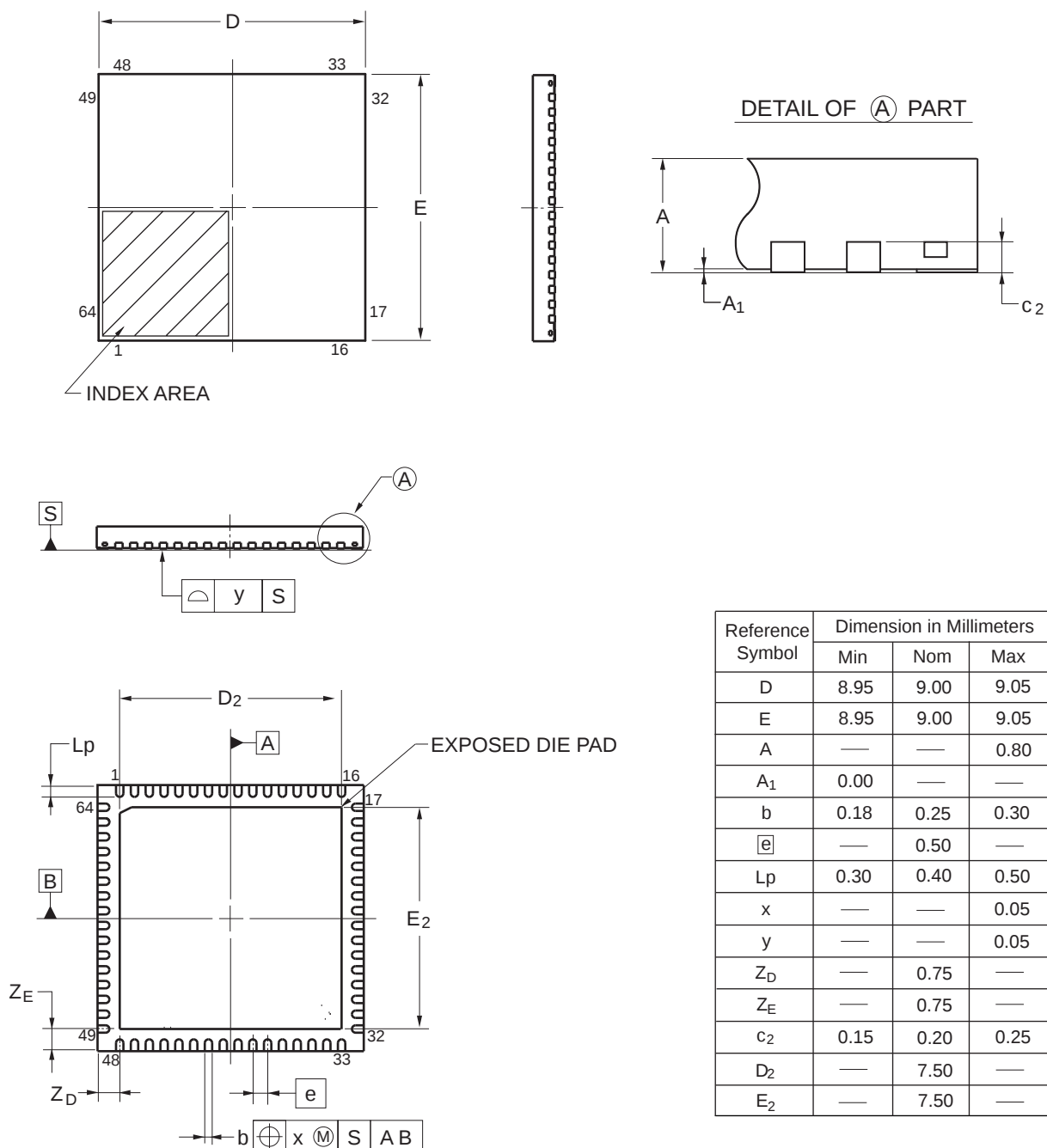


Figure D 64-Pin HWQFN (PWQN0064KC-A)

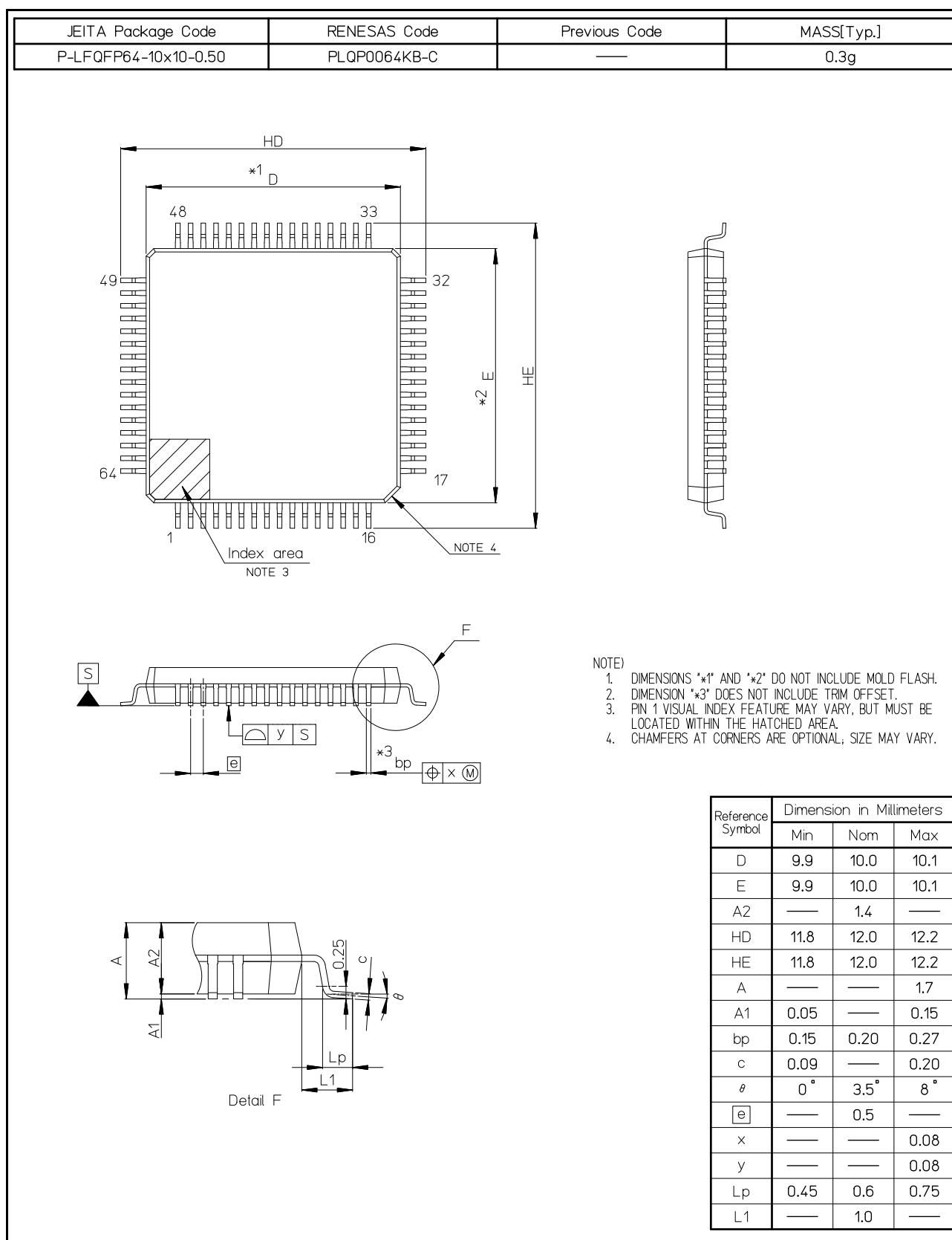


Figure E 64-Pin LFQFP (PLQP0064KB-C)

Rev.	Date	Description		Classification
		Page	Summary	
1.20	Sep 28, 2018	95	Figure 5.12 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 5.5 V When Normal Output is Selected (Reference Data), changed	TN-RX*-A201A/E
		124	Table 5.44 Timing of On-Chip Peripheral Modules (7), added	TN-RX*-A197A/E
		131	Figure 5.64 SD Host Interface Input/Output Signal Timing, added	TN-RX*-A197A/E
		132	Table 5.45 USB Characteristics (USB0_DP and USB0_DM Pin Characteristics) conditions, changed	

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