Renesas Electronics America Inc - R5F52317BDFM#30 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	54MHz
Connectivity	CANbus, I²C, IrDA, SCI, SD/SDIO, SPI, SSI, USB OTG
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	43
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f52317bdfm-30

Table 1.1 Outline of Specifications (3/4)

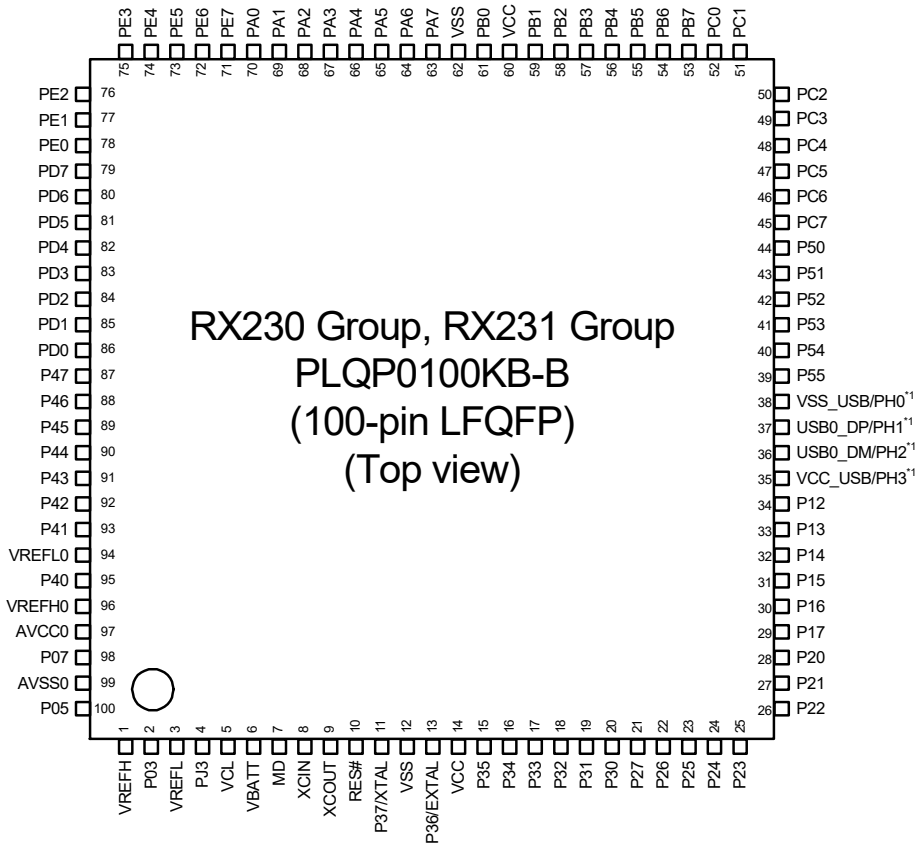
Classification	Module/Function	Description
Timers	Independent watchdog timer (IWDTa)	• 14 bits × 1 channel • Count clock: Dedicated low-speed on-chip oscillator for the IWDT Frequency divided by 1, 16, 32, 64, 128, or 256
	Realtime clock (RTCe)	• Clock source: Sub-clock • Time/calendar • Interrupts: Alarm interrupt, periodic interrupt, and carry interrupt • Time-capture facility for three values
	Low power timer (LPT)	• 16 bits × 1 channel • Clock source: Sub-clock, Dedicated low-speed on-chip oscillator for the IWDT Frequency divided by 2, 4, 8, 16, or 32
	8-bit timer (TMR)	• (8 bits × 2 channels) × 2 units • Seven internal clocks (PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, and PCLK/8192) and an external clock can be selected • Pulse output and PWM output with any duty cycle are available • Two channels can be cascaded and used as a 16-bit timer
Communication functions	Serial communications interfaces (SCIg, SCIh)	• 7 channels (channel 0, 1, 5, 6, 8, 9: SCIg, channel 12: SCIh) • SCIg Serial communications modes: Asynchronous, clock synchronous, and smart-card interface Multi-processor function On-chip baud rate generator allows selection of the desired bit rate Choice of LSB-first or MSB-first transfer Average transfer rate clock can be input from TMR timers for SCI5, SCI6, and SCI12 Start-bit detection: Level or edge detection is selectable. Simple I^2C Simple SPI 9-bit transfer mode Bit rate modulation Event linking by the ELC (only on channel 5) • SCIh (The following functions are added to SCIg) Supports the serial communications protocol, which contains the start frame and information frame Supports the LIN format
	IrDA interface (IRDA)	• 1 channel (SCI5 used) • Supports encoding/decoding of waveforms conforming to IrDA standard 1.0
	I^2C bus interface (RIICa)	• 1 channel • Communications formats: I^2C bus format/SMBus format • Master mode or slave mode selectable • Supports fast mode
	Serial peripheral interface (RSPIa)	• 1 channel • Transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPI clock) enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) • Capable of handling serial transfer as a master or slave • Data formats • Choice of LSB-first or MSB-first transfer The number of bits in each transfer can be changed to 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • Double buffers for both transmission and reception
	USB 2.0 host/function module (USBd)	• USB Device Controller (UDC) and transceiver for USB 2.0 are incorporated. • Host/function module: 1 port • Compliant with USB version 2.0 • Transfer speed: Full-speed (12 Mbps), low-speed (1.5 Mbps) • OTG (ON-The-Go) is supported. • Isochronous transfer is supported. • BC1.2 (Battery Charging Specification Revision 1.2) is supported. • Internal power supply for USB (allows operation without external power input to the VCC_USB pin when VCC = 4.0 to 5.5V)
	CAN module (RSCAN)	• 1 channel • Compliance with the ISO11898-1 specification (standard frame and extended frame) • 16 Message boxes

1.4 Pin Functions

Table 1.5 lists the pin functions.

Table 1.5 Pin Functions (1/4)

Classifications	Pin Name	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply.
	VCL	—	Connect this pin to the VSS pin via a 4.7 μF smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
	VBATT	Input	Backup power pin
Clock	XTAL	Output	Pins for connecting a crystal. An external clock can be input through the EXTAL pin.
	EXTAL	Input	
	BCLK	Output	Outputs the external bus clock for external devices.
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal between XCIN and XCOUT.
	XCOUT	Output	
	CLKOUT	Output	Clock output pin.
Operating mode control	MD	Input	Pin for setting the operating mode. The signal levels on this pin must not be changed during operation.
	UB	Input	Pin used for boot mode (USB interface).
	UPSEL	Input	Pin used for boot mode (USB interface).
System control	RES#	Input	Reset pin. This MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Input pin for the clock frequency accuracy measurement circuit.
On-chip emulator	FINED	I/O	FINE interface pin.
Address bus	A0 to A23	Output	Output pins for the address.
Data bus	D0 to D15	I/O	Input and output pins for the bidirectional data bus.
Multiplexed bus	A0/D0 to A15/D15	I/O	Address/data multiplexed bus
Bus control	RD#	Output	Strobe signal which indicates that reading from the external bus interface space is in progress.
	WR#	Output	Strobe signal which indicates that writing to the external bus interface space is in progress, in single-write strobe mode.
	WR0#, WR1#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0, and D15 to D8) is valid in writing to the external bus interface space, in byte strobe mode.
	BC0#, BC1#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0 and D15 to D8) is valid in access to the external bus interface space, in single-write strobe mode.
	CS0# to CS3#	Output	Select signals for areas 0 to 3.
	WAIT#	Input	Input pin for wait request signals in access to the external space.
	ALE	Output	Address latch signal when address/data multiplexed bus is selected.
LVD	CMPA2	Input	Detection target voltage pin for voltage detection 2.
Interrupts	NMI	Input	Non-maskable interrupt request pin.
	IRQ0 to IRQ7	Input	Interrupt request pins.



Note: This figure indicates the power supply pins and I/O port pins.
For the pin configuration, see the table “List of Pins and Pin Functions (100-Pin LFQFP)”.

Note 1. RX230: PH0, PH1, PH2, PH3
RX231: VSS_USB, USB0_DP, USB0_DM, VCC_USB

Figure 1.4 Pin Assignments of the 100-Pin LFQFP

(9) Floating-point status word (FPSW)

The floating-point status word (FPSW) indicates the results of floating-point operations.
When an exception handling enable bit (Ej) enables the exception handling (Ej = 1), the exception cause can be identified by checking the corresponding Cj flag in the exception handling routine. If the exception handling is masked (Ej = 0), the occurrence of exception can be checked by reading the Fj flag at the end of a series of processing. Once the Fj flag has been set to 1, this value is retained until it is cleared to 0 by software (j = X, U, Z, O, or V).

2.3 Accumulator

The accumulator (ACC0 or ACC1) is a 72-bit register used for DSP instructions. The accumulator is handled as a 96-bit register for reading and writing. At this time, when bits 95 to 72 of the accumulator are read, the value where the value of bit 71 is sign extended is read. Writing to bits 95 to 72 of the accumulator is ignored. ACC0 is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, FMUL, MUL, and RMPA, in which case the prior value in ACC0 is modified by execution of the instruction.
Use the MVTACGU, MVTACHI, and MVTACLO instructions for writing to the accumulator. The MVTACGU, MVTACHI, and MVTACLO instructions write data to bits 95 to 64, the higher-order 32 bits (bits 63 to 32), and the lower-order 32 bits (bits 31 to 0), respectively.
Use the MVFACGU, MVFACHI, MVFACMI, and MVFACLO instructions for reading data from the accumulator. The MVFACGU, MVFACHI, MVFACMI, and MVFACLO instructions read data from the guard bits (bits 95 to 64), higher-order 32 bits (bits 63 to 32), the middle 32 bits (bits 47 to 16), and the lower-order 32 bits (bits 31 to 0), respectively.

3. Address Space

3.1 Address Space

This LSI has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.
Figure 3.1 shows the memory maps in the respective operating modes. Accessible areas will differ according to the operating mode and states of control bits.

Table 4.1 List of I/O Registers (Address Order) (6/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK <PCLK
0008 8158h	TPU4	Timer General Register A	TGRA	16	16	2 or 3 PCLKB	2 ICLK
0008 815Ah	TPU4	Timer General Register B	TGRB	16	16	2 or 3 PCLKB	2 ICLK
0008 8160h	TPU5	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8161h	TPU5	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB	2 ICLK
0008 8162h	TPU5	Timer I/O Control Register	TIOR	8	8	2 or 3 PCLKB	2 ICLK
0008 8164h	TPU5	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB	2 ICLK
0008 8165h	TPU5	Timer Status Register	TSR	8	8	2 or 3 PCLKB	2 ICLK
0008 8166h	TPU5	Timer Counter	TCNT	16	16	2 or 3 PCLKB	2 ICLK
0008 8168h	TPU5	Timer General Register A	TGRA	16	16	2 or 3 PCLKB	2 ICLK
0008 816Ah	TPU5	Timer General Register B	TGRB	16	16	2 or 3 PCLKB	2 ICLK
0008 8200h	TMR0	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8201h	TMR1	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8202h	TMR0	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB	2 ICLK
0008 8203h	TMR1	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB	2 ICLK
0008 8204h	TMR0	Time Constant Register A	TCORA	8	8	2 or 3 PCLKB	2 ICLK
0008 8205h	TMR1	Time Constant Register A	TCORA	8	8*1	2 or 3 PCLKB	2 ICLK
0008 8206h	TMR0	Time Constant Register B	TCORB	8	8	2 or 3 PCLKB	2 ICLK
0008 8207h	TMR1	Time Constant Register B	TCORB	8	8*1	2 or 3 PCLKB	2 ICLK
0008 8208h	TMR0	Timer Counter	TCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 8209h	TMR1	Timer Counter	TCNT	8	8*1	2 or 3 PCLKB	2 ICLK
0008 820Ah	TMR0	Timer Counter Control Register	TCCR	8	8	2 or 3 PCLKB	2 ICLK
0008 820Bh	TMR1	Timer Counter Control Register	TCCR	8	8*1	2 or 3 PCLKB	2 ICLK
0008 820Ch	TMR0	Timer Count Start Register	TCSTR	8	8	2 or 3 PCLKB	2 ICLK
0008 8210h	TMR2	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8211h	TMR3	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8212h	TMR2	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB	2 ICLK
0008 8213h	TMR3	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB	2 ICLK
0008 8214h	TMR2	Time Constant Register A	TCORA	8	8	2 or 3 PCLKB	2 ICLK
0008 8215h	TMR3	Time Constant Register A	TCORA	8	8*1	2 or 3 PCLKB	2 ICLK
0008 8216h	TMR2	Time Constant Register B	TCORB	8	8	2 or 3 PCLKB	2 ICLK
0008 8217h	TMR3	Time Constant Register B	TCORB	8	8*1	2 or 3 PCLKB	2 ICLK
0008 8218h	TMR2	Timer Counter	TCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 8219h	TMR3	Timer Counter	TCNT	8	8*1	2 or 3 PCLKB	2 ICLK
0008 821Ah	TMR2	Timer Counter Control Register	TCCR	8	8	2 or 3 PCLKB	2 ICLK
0008 821Bh	TMR3	Timer Counter Control Register	TCCR	8	8*1	2 or 3 PCLKB	2 ICLK
0008 821Ch	TMR2	Timer Count Start Register	TCSTR	8	8	2 or 3 PCLKB	2 ICLK
0008 8280h	CRC	CRC Control Register	CRCCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8281h	CRC	CRC Data Input Register	CRCDIR	8	8	2 or 3 PCLKB	2 ICLK
0008 8282h	CRC	CRC Data Output Register	CRCDOR	16	16	2 or 3 PCLKB	2 ICLK
0008 8300h	RIIC0	I^2C-Bus Control Register 1	ICCR1	8	8	2 or 3 PCLKB	2 ICLK
0008 8301h	RIIC0	I^2C-Bus Control Register 2	ICCR2	8	8	2 or 3 PCLKB	2 ICLK
0008 8302h	RIIC0	I^2C-Bus Mode Register 1	ICMR1	8	8	2 or 3 PCLKB	2 ICLK
0008 8303h	RIIC0	I^2C-Bus Mode Register 2	ICMR2	8	8	2 or 3 PCLKB	2 ICLK
0008 8304h	RIIC0	I^2C-Bus Mode Register 3	ICMR3	8	8	2 or 3 PCLKB	2 ICLK
0008 8305h	RIIC0	I^2C-Bus Function Enable Register	ICFER	8	8	2 or 3 PCLKB	2 ICLK
0008 8306h	RIIC0	I^2C-Bus Status Enable Register	ICSER	8	8	2 or 3 PCLKB	2 ICLK
0008 8307h	RIIC0	I^2C-Bus Interrupt Enable Register	ICIER	8	8	2 or 3 PCLKB	2 ICLK
0008 8308h	RIIC0	I^2C-Bus Status Register 1	ICSR1	8	8	2 or 3 PCLKB	2 ICLK
0008 8309h	RIIC0	I^2C-Bus Status Register 2	ICSR2	8	8	2 or 3 PCLKB	2 ICLK
0008 830Ah	RIIC0	Slave Address Register L0	SARL0	8	8	2 or 3 PCLKB	2 ICLK
0008 830Bh	RIIC0	Slave Address Register U0	SARU0	8	8	2 or 3 PCLKB	2 ICLK
0008 830Ch	RIIC0	Slave Address Register L1	SARL1	8	8	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (7/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK <PCLK
0008 830Dh	RIIC0	Slave Address Register U1	SARU1	8	8	2 or 3 PCLKB	2 ICLK
0008 830Eh	RIIC0	Slave Address Register L2	SARL2	8	8	2 or 3 PCLKB	2 ICLK
0008 830Fh	RIIC0	Slave Address Register U2	SARU2	8	8	2 or 3 PCLKB	2 ICLK
0008 8310h	RIIC0	I²C-Bus Bit Rate Low-Level Register	ICBRL	8	8	2 or 3 PCLKB	2 ICLK
0008 8311h	RIIC0	I²C-Bus Bit Rate High-Level Register	ICBRH	8	8	2 or 3 PCLKB	2 ICLK
0008 8312h	RIIC0	I²C-Bus Transmit Data Register	ICDRT	8	8	2 or 3 PCLKB	2 ICLK
0008 8313h	RIIC0	I²C-Bus Receive Data Register	ICDRR	8	8	2 or 3 PCLKB	2 ICLK
0008 8380h	RSPI0	RSPI Control Register	SPCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8381h	RSPI0	RSPI Slave Select Polarity Register	SSLP	8	8	2 or 3 PCLKB	2 ICLK
0008 8382h	RSPI0	RSPI Pin Control Register	SPPCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8383h	RSPI0	RSPI Status Register	SPSR	8	8	2 or 3 PCLKB	2 ICLK
0008 8384h	RSPI0	RSPI Data Register	SPDR	32	16, 32	2 or 3 PCLKB	2 ICLK
0008 8388h	RSPI0	RSPI Sequence Control Register	SPSCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8389h	RSPI0	RSPI Sequence Status Register	SPSSR	8	8	2 or 3 PCLKB	2 ICLK
0008 838Ah	RSPI0	RSPI Bit Rate Register	SPBR	8	8	2 or 3 PCLKB	2 ICLK
0008 838Bh	RSPI0	RSPI Data Control Register	SPDCR	8	8	2 or 3 PCLKB	2 ICLK
0008 838Ch	RSPI0	RSPI Clock Delay Register	SPCKD	8	8	2 or 3 PCLKB	2 ICLK
0008 838Dh	RSPI0	RSPI Slave Select Negation Delay Register	SSLND	8	8	2 or 3 PCLKB	2 ICLK
0008 838Eh	RSPI0	RSPI Next-Access Delay Register	SPND	8	8	2 or 3 PCLKB	2 ICLK
0008 838Fh	RSPI0	RSPI Control Register 2	SPCR2	8	8	2 or 3 PCLKB	2 ICLK
0008 8390h	RSPI0	RSPI Command Register 0	SPCMD0	16	16	2 or 3 PCLKB	2 ICLK
0008 8392h	RSPI0	RSPI Command Register 1	SPCMD1	16	16	2 or 3 PCLKB	2 ICLK
0008 8394h	RSPI0	RSPI Command Register 2	SPCMD2	16	16	2 or 3 PCLKB	2 ICLK
0008 8396h	RSPI0	RSPI Command Register 3	SPCMD3	16	16	2 or 3 PCLKB	2 ICLK
0008 8398h	RSPI0	RSPI Command Register 4	SPCMD4	16	16	2 or 3 PCLKB	2 ICLK
0008 839Ah	RSPI0	RSPI Command Register 5	SPCMD5	16	16	2 or 3 PCLKB	2 ICLK
0008 839Ch	RSPI0	RSPI Command Register 6	SPCMD6	16	16	2 or 3 PCLKB	2 ICLK
0008 839Eh	RSPI0	RSPI Command Register 7	SPCMD7	16	16	2 or 3 PCLKB	2 ICLK
0008 8410h	IRDA	IrDA Control Register	IRCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8900h	POE	Input Level Control/Status Register 1	ICSR1	16	8, 16	2 or 3 PCLKB	2 ICLK
0008 8902h	POE	Output Level Control/Status Register 1	OCSR1	16	8, 16	2 or 3 PCLKB	2 ICLK
0008 8908h	POE	Input Level Control/Status Register 2	ICSR2	16	8, 16	2 or 3 PCLKB	2 ICLK
0008 890Ah	POE	Software Port Output Enable Register	SPOER	8	8	2 or 3 PCLKB	2 ICLK
0008 890Bh	POE	Port Output Enable Control Register 1	POECR1	8	8	2 or 3 PCLKB	2 ICLK
0008 890Ch	POE	Port Output Enable Control Register 2	POECR2	8	8	2 or 3 PCLKB	2 ICLK
0008 890Eh	POE	Input Level Control/Status Register 3	ICSR3	16	8, 16	2 or 3 PCLKB	2 ICLK
0008 9000h	S12AD	A/D Control Register	ADCSR	16	16	2 or 3 PCLKB	2 ICLK
0008 9004h	S12AD	A/D Channel Select Register A0	ADANSA0	16	16	2 or 3 PCLKB	2 ICLK
0008 9006h	S12AD	A/D Channel Select Register A1	ADANSA1	16	16	2 or 3 PCLKB	2 ICLK
0008 9008h	S12AD	A/D-Converted Value Addition/Average Function Select Register 0	ADADS0	16	16	2 or 3 PCLKB	2 ICLK
0008 900Ah	S12AD	A/D-Converted Value Addition/Average Function Select Register 1	ADADS1	16	16	2 or 3 PCLKB	2 ICLK
0008 900Ch	S12AD	A/D-Converted Value Addition/Average Count Select Register	ADADC	8	8	2 or 3 PCLKB	2 ICLK
0008 900Eh	S12AD	A/D Control Extended Register	ADCER	16	16	2 or 3 PCLKB	2 ICLK
0008 9010h	S12AD	A/D Conversion Start Trigger Select Register	ADSTRGR	16	16	2 or 3 PCLKB	2 ICLK
0008 9012h	S12AD	A/D Conversion Extended Input Control Register	ADEXICR	16	16	2 or 3 PCLKB	2 ICLK
0008 9014h	S12AD	A/D Channel Select Register B0	ADANSB0	16	16	2 or 3 PCLKB	2 ICLK
0008 9016h	S12AD	A/D Channel Select Register B1	ADANSB1	16	16	2 or 3 PCLKB	2 ICLK
0008 9018h	S12AD	A/D Data Duplication Register	ADDBLDR	16	16	2 or 3 PCLKB	2 ICLK
0008 901Ah	S12AD	A/D Temperature Sensor Data Register	ADTSDR	16	16	2 or 3 PCLKB	2 ICLK
0008 901Ch	S12AD	A/D Internal Reference Voltage Data Register	ADOCDR	16	16	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (12/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK <PCLK
0008 A131h	SCI9	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB	2 ICLK
0008 A132h	SCI9	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A500h	SSI0	Control Register	SSICR	32	32	2 or 3 PCLKB	2 ICLK
0008 A504h	SSI0	Status Register	SSISR	32	32	2 or 3 PCLKB	2 ICLK
0008 A510h	SSI0	FIFO Control Register	SSIFCR	32	32	2 or 3 PCLKB	2 ICLK
0008 A514h	SSI0	FIFO Status Register	SSIFSR	32	32	2 or 3 PCLKB	2 ICLK
0008 A518h	SSI0	Transmit FIFO Data Register	SSIFTDR	32	32	2 or 3 PCLKB	2 ICLK
0008 A51Ch	SSI0	Receive FIFO Data Register	SSIFRDR	32	32	2 or 3 PCLKB	2 ICLK
0008 A520h	SSI0	TDM Mode Register	SSITDMR	32	32	2 or 3 PCLKB	2 ICLK
0008 AC00h	SDHI	Command Register	SDCMD	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 AC08h	SDHI	Argument Register	SDARG	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 AC10h	SDHI	Data Stop Register	SDSTOP	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 AC14h	SDHI	Block Count Register	SDBLKCNT	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 AC18h	SDHI	Response Register 10	SDRSP10	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 AC20h	SDHI	Response Register 32	SDRSP32	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 AC28h	SDHI	Response Register 54	SDRSP54	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 AC30h	SDHI	Response Register 76	SDRSP76	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 AC38h	SDHI	SD Status Register 1	SDSTS1	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 AC3Ch	SDHI	SD Status Register 2	SDSTS2	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 AC40h	SDHI	SD Interrupt Mask Register 1	SDIMSK1	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing

Table 4.1 List of I/O Registers (Address Order) (19/33)

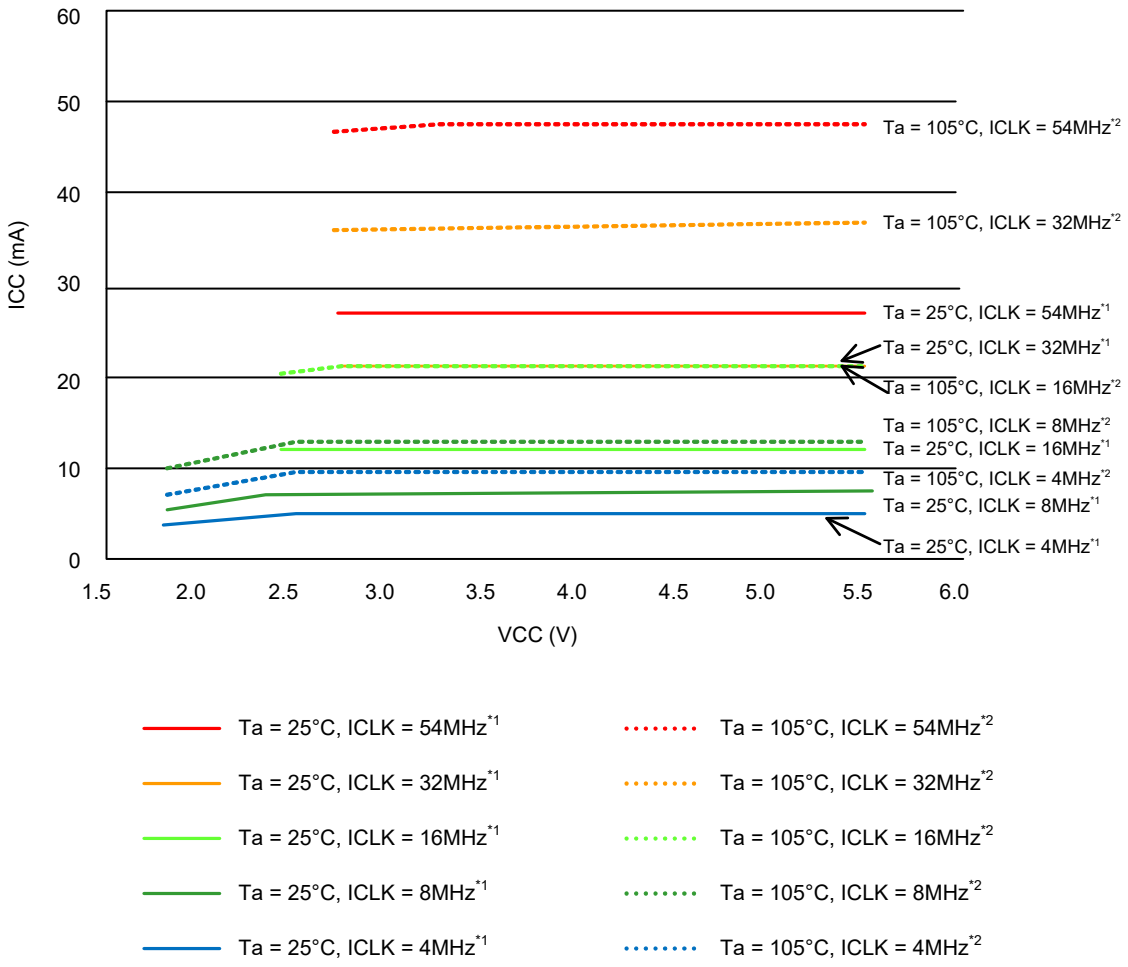
Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK <PCLK
0008 C1B3h	MPC	PE3 Pin Function Control Register	PE3PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1B4h	MPC	PE4 Pin Function Control Register	PE4PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1B5h	MPC	PE5 Pin Function Control Register	PE5PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1B6h	MPC	PE6 Pin Function Control Register	PE6PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1B7h	MPC	PE7 Pin Function Control Register	PE7PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1C8h	MPC	PH0 Pin Function Control Register	PH0PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1C9h	MPC	PH1 Pin Function Control Register	PH1PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1CAh	MPC	PH2 Pin Function Control Register	PH2PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1CBh	MPC	PH3 Pin Function Control Register	PH3PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1D3h	MPC	PJ3 Pin Function Control Register	PJ3PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C290h	SYSTEM	Reset Status Register 0	RSTSR0	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C291h	SYSTEM	Reset Status Register 1	RSTSR1	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C293h	SYSTEM	Main Clock Oscillator Forced Oscillation Control Register	MOFCR	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C297h	SYSTEM	Voltage Monitoring Circuit Control Register	LVCMPCR	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C298h	SYSTEM	Voltage Detection Level Select Register	LVDLVLR	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C29Ah	SYSTEM	Voltage Monitoring 1 Circuit Control Register 0	LVD1CR0	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C29Bh	SYSTEM	Voltage Monitoring 2 Circuit Control Register 0	LVD2CR0	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C29Dh	SYSTEM	VBATT Control Register	VBATTCR	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C29Eh	SYSTEM	VBATT Status Register	VBATTSR	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C29Fh	SYSTEM	VBATT Pin Voltage Drop Detection Interrupt Control Register	VBTLVDICR	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C400h	RTC	64-Hz Counter	R64CNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C402h	RTC	Second Counter	RSECCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C402h	RTC	Binary Counter 0	BCNT0	8	8	2 or 3 PCLKB	2 ICLK
0008 C404h	RTC	Minute Counter	RMINCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C404h	RTC	Binary Counter 1	BCNT1	8	8	2 or 3 PCLKB	2 ICLK
0008 C406h	RTC	Hour Counter	RHRCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C406h	RTC	Binary Counter 2	BCNT2	8	8	2 or 3 PCLKB	2 ICLK
0008 C408h	RTC	Day-of-Week Counter	RWKCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C408h	RTC	Binary Counter 3	BCNT3	8	8	2 or 3 PCLKB	2 ICLK
0008 C40Ah	RTC	Date Counter	RDAYCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C40Ch	RTC	Month Counter	RMONCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C40Eh	RTC	Year Counter	RYRCNT	16	16	2 or 3 PCLKB	2 ICLK
0008 C410h	RTC	Second Alarm Register	RSECAR	8	8	2 or 3 PCLKB	2 ICLK
0008 C410h	RTC	Binary Counter 0 Alarm Register	BCNT0AR	8	8	2 or 3 PCLKB	2 ICLK
0008 C412h	RTC	Minute Alarm Register	RMINAR	8	8	2 or 3 PCLKB	2 ICLK
0008 C412h	RTC	Binary Counter 1 Alarm Register	BCNT1AR	8	8	2 or 3 PCLKB	2 ICLK
0008 C414h	RTC	Hour Alarm Register	RHRAR	8	8	2 or 3 PCLKB	2 ICLK
0008 C414h	RTC	Binary Counter 2 Alarm Register	BCNT2AR	8	8	2 or 3 PCLKB	2 ICLK
0008 C416h	RTC	Day-of-Week Alarm Register	RWKAR	8	8	2 or 3 PCLKB	2 ICLK
0008 C416h	RTC	Binary Counter 3 Alarm Register	BCNT3AR	8	8	2 or 3 PCLKB	2 ICLK
0008 C418h	RTC	Date Alarm Register	RDAYAR	8	8	2 or 3 PCLKB	2 ICLK
0008 C418h	RTC	Binary Counter 0 Alarm Enable Register	BCNT0AER	8	8	2 or 3 PCLKB	2 ICLK
0008 C41Ah	RTC	Month Alarm Register	RMONAR	8	8	2 or 3 PCLKB	2 ICLK
0008 C41Ah	RTC	Binary Counter 1 Alarm Enable Register	BCNT1AER	8	8	2 or 3 PCLKB	2 ICLK
0008 C41Ch	RTC	Year Alarm Register	RYRAR	16	16	2 or 3 PCLKB	2 ICLK
0008 C41Ch	RTC	Binary Counter 2 Alarm Enable Register	BCNT2AER	16	16	2 or 3 PCLKB	2 ICLK
0008 C41Eh	RTC	Year Alarm Enable Register	RYRAREN	8	8	2 or 3 PCLKB	2 ICLK
0008 C41Eh	RTC	Binary Counter 3 Alarm Enable Register	BCNT3AER	8	8	2 or 3 PCLKB	2 ICLK
0008 C422h	RTC	RTC Control Register 1	RCR1	8	8	2 or 3 PCLKB	2 ICLK
0008 C424h	RTC	RTC Control Register 2	RCR2	8	8	2 or 3 PCLKB	2 ICLK
0008 C426h	RTC	RTC Control Register 3	RCR3	8	8	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (22/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK <PCLK
000A 0060h	USB0	DCP Control Register	DCPCTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 0064h	USB0	Pipe Window Select Register	PIPESEL	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 0068h	USB0	Pipe Configuration Register	PIPECFG	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 006Ch	USB0	Pipe Maximum Packet Size Register	PIPEMAXP	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 006Eh	USB0	Pipe Cycle Control Register	PIPEPERI	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 0070h	USB0	PIPE1 Control Register	PIPE1CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 0072h	USB0	PIPE2 Control Register	PIPE2CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 0074h	USB0	PIPE3 Control Register	PIPE3CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 0076h	USB0	PIPE4 Control Register	PIPE4CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 0078h	USB0	PIPE5 Control Register	PIPE5CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 007Ah	USB0	PIPE6 Control Register	PIPE6CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 007Ch	USB0	PIPE7 Control Register	PIPE7CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 007Eh	USB0	PIPE8 Control Register	PIPE8CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 0080h	USB0	PIPE9 Control Register	PIPE9CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 0090h	USB0	PIPE1 Transaction Counter Enable Register	PIPE1TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 0092h	USB0	PIPE1 Transaction Counter Register	PIPE1TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 0094h	USB0	PIPE2 Transaction Counter Enable Register	PIPE2TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 0096h	USB0	PIPE2 Transaction Counter Register	PIPE2TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 0098h	USB0	PIPE3 Transaction Counter Enable Register	PIPE3TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 009Ah	USB0	PIPE3 Transaction Counter Register	PIPE3TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 009Ch	USB0	PIPE4 Transaction Counter Enable Register	PIPE4TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 009Eh	USB0	PIPE4 Transaction Counter Register	PIPE4TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 00A0h	USB0	PIPE5 Transaction Counter Enable Register	PIPE5TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2
000A 00A2h	USB0	PIPE5 Transaction Counter Register	PIPE5TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*2

Table 4.1 List of I/O Registers (Address Order) (25/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK <PCLK
000A 83AAh	RSCAN	Receive Rule Entry Register 0CH	GAFLPH0	16	16	2 or 3 PCLKB	2 ICLK
000A 83AAh	RSCAN	Receive Buffer Register 0CH	RMDF10	16	16	2 or 3 PCLKB	2 ICLK
000A 83ACh	RSCAN	Receive Rule Entry Register 1AL	GAFLIDL1	16	16	2 or 3 PCLKB	2 ICLK
000A 83ACh	RSCAN	Receive Buffer Register 0DL	RMDF20	16	16	2 or 3 PCLKB	2 ICLK
000A 83AEh	RSCAN	Receive Rule Entry Register 1AH	GAFLIDH1	16	16	2 or 3 PCLKB	2 ICLK
000A 83AEh	RSCAN	Receive Buffer Register 0DH	RMDF30	16	16	2 or 3 PCLKB	2 ICLK
000A 83B0h	RSCAN	Receive Rule Entry Register 1BL	GAFLML1	16	16	2 or 3 PCLKB	2 ICLK
000A 83B0h	RSCAN	Receive Buffer Register 1AL	RMIDL1	16	16	2 or 3 PCLKB	2 ICLK
000A 83B2h	RSCAN	Receive Rule Entry Register 1BH	GAFLMH1	16	16	2 or 3 PCLKB	2 ICLK
000A 83B2h	RSCAN	Receive Buffer Register 1AH	RMIDH1	16	16	2 or 3 PCLKB	2 ICLK
000A 83B4h	RSCAN	Receive Rule Entry Register 1CL	GAFLPL1	16	16	2 or 3 PCLKB	2 ICLK
000A 83B4h	RSCAN	Receive Buffer Register 1BL	RMTS1	16	16	2 or 3 PCLKB	2 ICLK
000A 83B6h	RSCAN	Receive Rule Entry Register 1CH	GAFLPH1	16	16	2 or 3 PCLKB	2 ICLK
000A 83B6h	RSCAN	Receive Buffer Register 1BH	RMPTR1	16	16	2 or 3 PCLKB	2 ICLK
000A 83B8h	RSCAN	Receive Rule Entry Register 2AL	GAFLIDL2	16	16	2 or 3 PCLKB	2 ICLK
000A 83B8h	RSCAN	Receive Buffer Register 1CL	RMDF01	16	16	2 or 3 PCLKB	2 ICLK
000A 83BAh	RSCAN	Receive Rule Entry Register 2AH	GAFLIDH2	16	16	2 or 3 PCLKB	2 ICLK
000A 83BAh	RSCAN	Receive Buffer Register 1CH	RMDF11	16	16	2 or 3 PCLKB	2 ICLK
000A 83BCh	RSCAN	Receive Rule Entry Register 2BL	GAFLML2	16	16	2 or 3 PCLKB	2 ICLK
000A 83BCh	RSCAN	Receive Buffer Register 1DL	RMDF21	16	16	2 or 3 PCLKB	2 ICLK
000A 83BEh	RSCAN	Receive Rule Entry Register 2BH	GAFLMH2	16	16	2 or 3 PCLKB	2 ICLK
000A 83BEh	RSCAN	Receive Buffer Register 1DH	RMDF31	16	16	2 or 3 PCLKB	2 ICLK
000A 83C0h	RSCAN	Receive Rule Entry Register 2CL	GAFLPL2	16	16	2 or 3 PCLKB	2 ICLK
000A 83C0h	RSCAN	Receive Buffer Register 2AL	RMIDL2	16	16	2 or 3 PCLKB	2 ICLK
000A 83C2h	RSCAN	Receive Rule Entry Register 2CH	GAFLPH2	16	16	2 or 3 PCLKB	2 ICLK
000A 83C2h	RSCAN	Receive Buffer Register 2AH	RMIDH2	16	16	2 or 3 PCLKB	2 ICLK
000A 83C4h	RSCAN	Receive Rule Entry Register 3AL	GAFLIDL3	16	16	2 or 3 PCLKB	2 ICLK
000A 83C4h	RSCAN	Receive Buffer Register 2BL	RMTS2	16	16	2 or 3 PCLKB	2 ICLK
000A 83C6h	RSCAN	Receive Rule Entry Register 3AH	GAFLIDH3	16	16	2 or 3 PCLKB	2 ICLK
000A 83C6h	RSCAN	Receive Buffer Register 2BH	RMPTR2	16	16	2 or 3 PCLKB	2 ICLK
000A 83C8h	RSCAN	Receive Rule Entry Register 3BL	GAFLML3	16	16	2 or 3 PCLKB	2 ICLK
000A 83C8h	RSCAN	Receive Buffer Register 2CL	RMDF02	16	16	2 or 3 PCLKB	2 ICLK
000A 83CAh	RSCAN	Receive Rule Entry Register 3BH	GAFLMH3	16	16	2 or 3 PCLKB	2 ICLK
000A 83CAh	RSCAN	Receive Buffer Register 2CH	RMDF12	16	16	2 or 3 PCLKB	2 ICLK
000A 83CCh	RSCAN	Receive Rule Entry Register 3CL	GAFLPL3	16	16	2 or 3 PCLKB	2 ICLK
000A 83CCh	RSCAN	Receive Buffer Register 2DL	RMDF22	16	16	2 or 3 PCLKB	2 ICLK
000A 83CEh	RSCAN	Receive Rule Entry Register 3CH	GAFLPH3	16	16	2 or 3 PCLKB	2 ICLK
000A 83CEh	RSCAN	Receive Buffer Register 2DH	RMDF32	16	16	2 or 3 PCLKB	2 ICLK
000A 83D0h	RSCAN	Receive Rule Entry Register 4AL	GAFLIDL4	16	16	2 or 3 PCLKB	2 ICLK
000A 83D0h	RSCAN	Receive Buffer Register 3AL	RMIDL3	16	16	2 or 3 PCLKB	2 ICLK
000A 83D2h	RSCAN	Receive Rule Entry Register 4AH	GAFLIDH4	16	16	2 or 3 PCLKB	2 ICLK
000A 83D2h	RSCAN	Receive Buffer Register 3AH	RMIDH3	16	16	2 or 3 PCLKB	2 ICLK
000A 83D4h	RSCAN	Receive Rule Entry Register 4BL	GAFLML4	16	16	2 or 3 PCLKB	2 ICLK
000A 83D4h	RSCAN	Receive Buffer Register 3BL	RMTS3	16	16	2 or 3 PCLKB	2 ICLK
000A 83D6h	RSCAN	Receive Rule Entry Register 4BH	GAFLMH4	16	16	2 or 3 PCLKB	2 ICLK
000A 83D6h	RSCAN	Receive Buffer Register 3BH	RMPTR3	16	16	2 or 3 PCLKB	2 ICLK
000A 83D8h	RSCAN	Receive Rule Entry Register 4CL	GAFLPL4	16	16	2 or 3 PCLKB	2 ICLK
000A 83D8h	RSCAN	Receive Buffer Register 3CL	RMDF03	16	16	2 or 3 PCLKB	2 ICLK
000A 83DAh	RSCAN	Receive Rule Entry Register 4CH	GAFLPH4	16	16	2 or 3 PCLKB	2 ICLK
000A 83DAh	RSCAN	Receive Buffer Register 3CH	RMDF13	16	16	2 or 3 PCLKB	2 ICLK
000A 83DCh	RSCAN	Receive Rule Entry Register 5AL	GAFLIDL5	16	16	2 or 3 PCLKB	2 ICLK
000A 83DCh	RSCAN	Receive Buffer Register 3DL	RMDF23	16	16	2 or 3 PCLKB	2 ICLK



Note 1. All peripheral operations except any BGO operation are operating normally. Indicates the average of the typical samples through actual measurement during product evaluation.
Note 2. All peripheral operations except any BGO operation are operating at maximum. Indicates the average of the upper-limit samples through actual measurement during product evaluation.

Figure 5.1 Voltage Dependency in High-Speed Operating Mode (Reference Data)

5.2.3 Normal I/O Pin Output Characteristics (3)

Figure 5.18 to Figure 5.21 show the characteristics of the RIIC output pin.

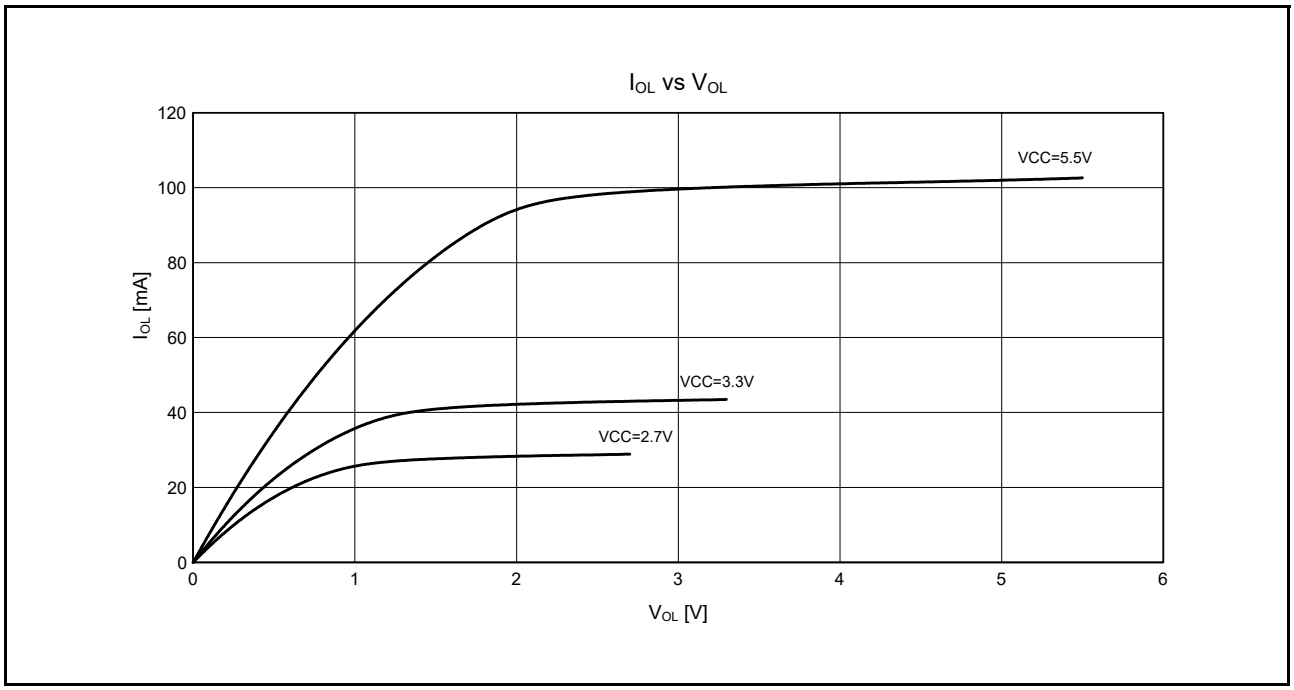


Figure 5.18 V_{OL} and I_{OL} Voltage Characteristics of RIIC Output Pin at T_a = 25°C (Reference Data)

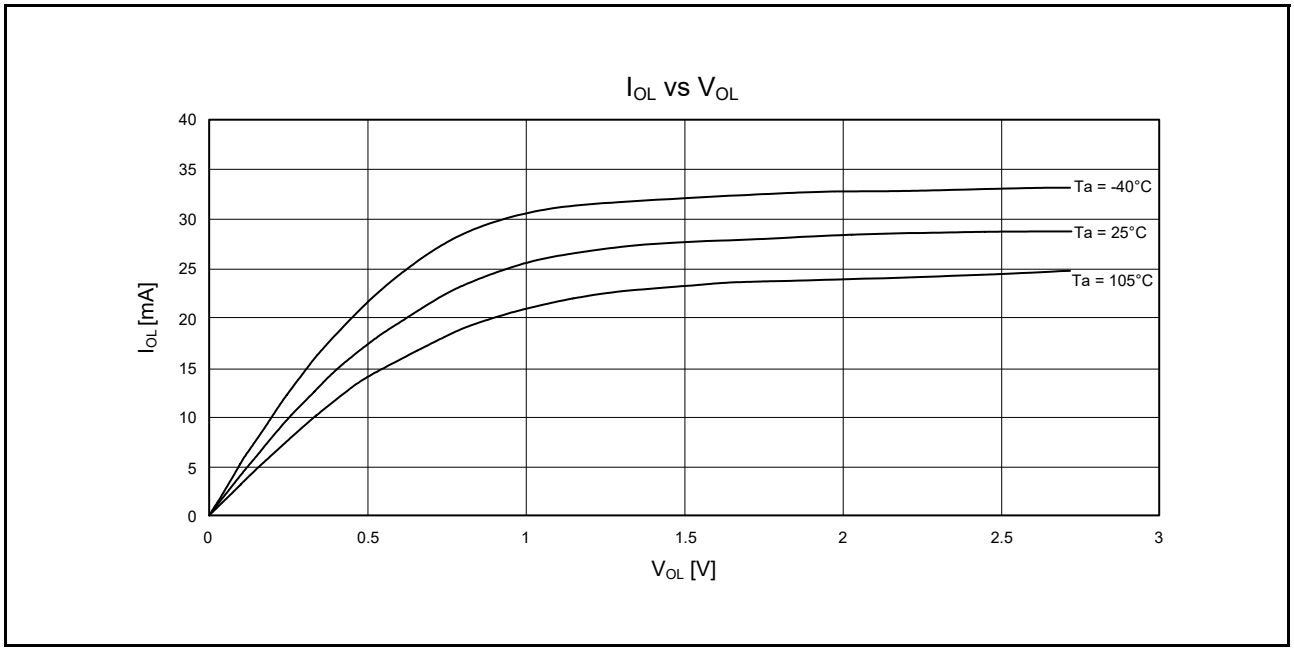


Figure 5.19 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at VCC = 2.7 V (Reference Data)

5.3 AC Characteristics

5.3.1 Clock Timing

Table 5.21 Operating Frequency Value (High-Speed Operating Mode)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VREFL0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC				Unit
			1.8 V ≤ VCC < 2.4 V	2.4 V ≤ VCC < 2.7 V	2.7 V ≤ VCC ≤ 5.5 V	When USB is in Use*3	
Maximum operating frequency*4	System clock (ICLK)	f_{max}	8	16	54	54	MHz
	FlashIF clock (FCLK)*1, *2		8	16	32	32	
	Peripheral module clock (PCLKA)		8	16	54	54	
	Peripheral module clock (PCLKB)		8	16	32	32	
	Peripheral module clock (PCLKD)		8	32	54	54	
	External bus clock (BCLK)		8	16	32	32	
	BCLK pin output		8	8	16	16	
	USB clock (UCLK)	f_{usb}	—	—	—	48	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When FCLK is in use at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK must be within ±3.5%.
Note 3. The VCC_USB range is 3.0 to 5.5 V when the USB clock is in use.
Note 4. The maximum operating frequency listed above does not include errors of the external oscillator and internal oscillator. For details on the range for the guaranteed operation, see Table 5.26, Clock Timing.

Table 5.22 Operating Frequency Value (Middle-Speed Operating Mode)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VREFL0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC				Unit
			1.8 V ≤ VCC < 2.4 V	2.4 V ≤ VCC < 2.7 V	2.7 V ≤ VCC ≤ 5.5 V	When USB is in Use*3	
Maximum operating frequency*4	System clock (ICLK)	f_{max}	8	12	12	12	MHz
	FlashIF clock (FCLK)*1, *2		8	12	12	12	
	Peripheral module clock (PCLKA)		8	12	12	12	
	Peripheral module clock (PCLKB)		8	12	12	12	
	Peripheral module clock (PCLKD)		8	12	12	12	
	External bus clock (BCLK)		8	12	12	12	
	BCLK pin output		8	8	12	12	
	USB clock (UCLK)	f_{usb}	—	—	—	48	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK must be within ±3.5%.
Note 3. The VCC_USB range is 3.0 to 5.5 V when the USB clock is in use.
Note 4. The maximum operating frequency listed above does not include errors of the external oscillator and internal oscillator. For details on the range for the guaranteed operation, see Table 5.26, Clock Timing.

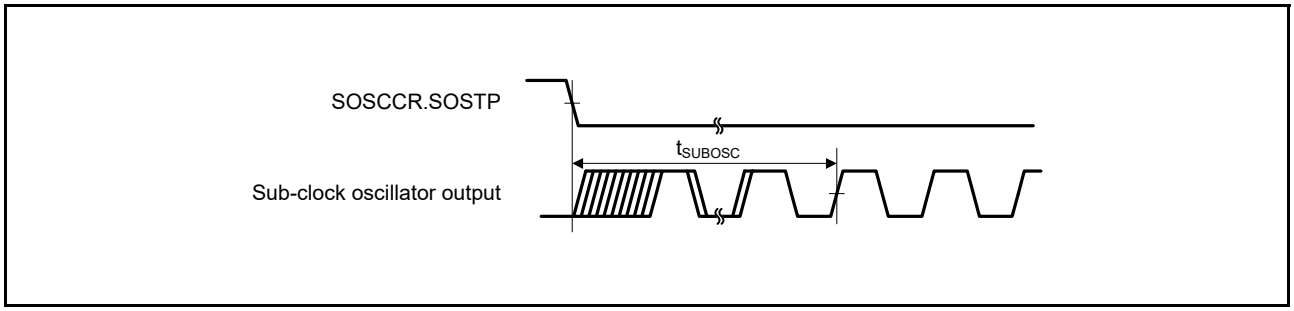


Figure 5.30 Sub-Clock Oscillation Start Timing

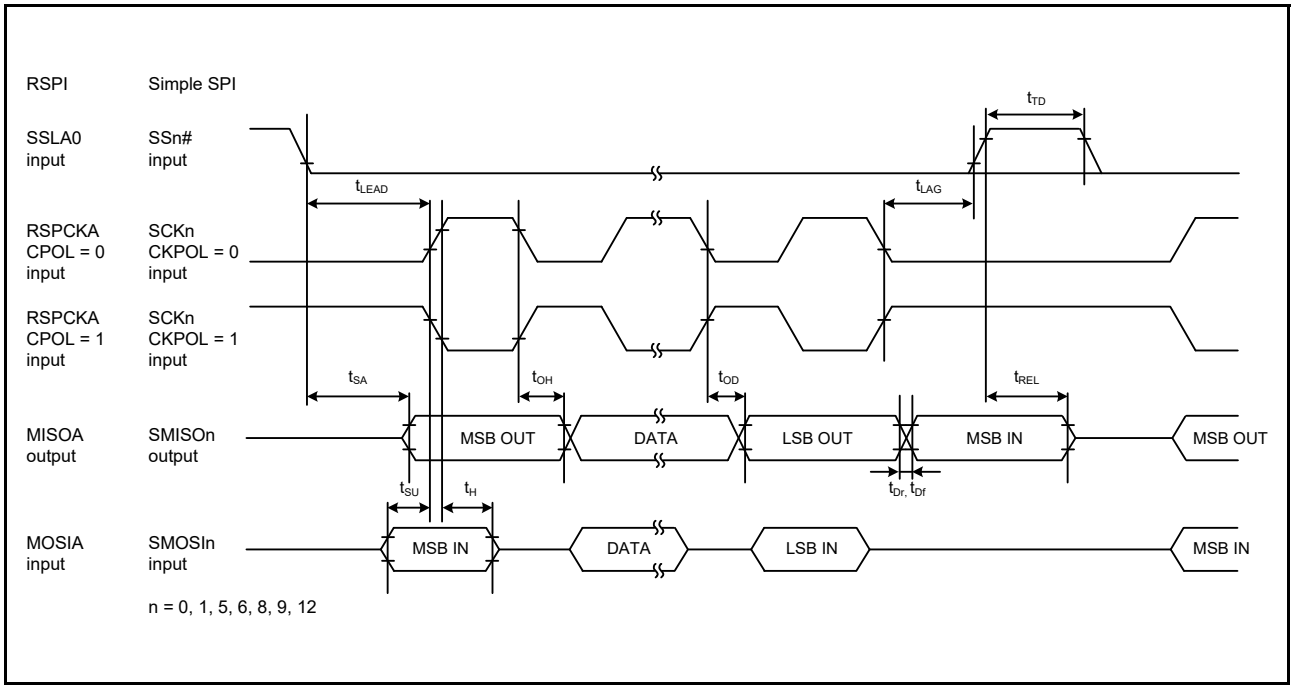


Figure 5.57 RSPI Timing (Slave, CPHA = 0) and Simple SPI Clock Timing (Slave, CKPH = 1)

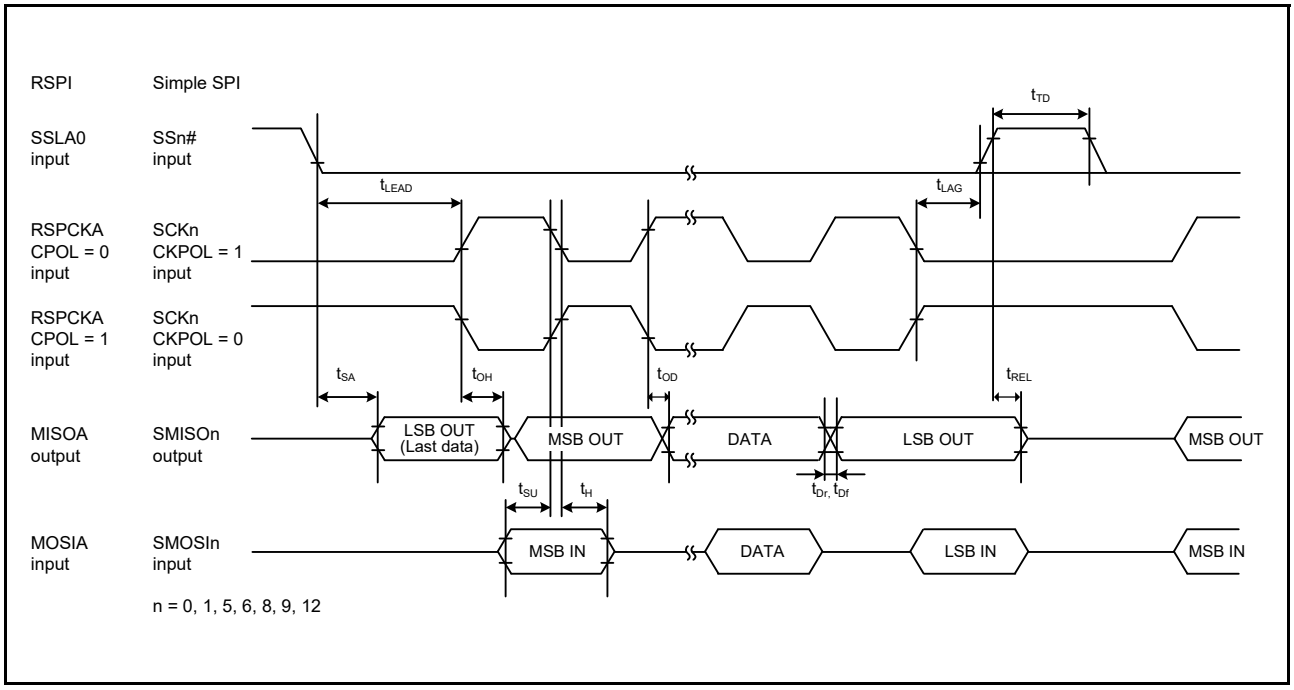


Figure 5.58 RSPI Timing (Slave, CPHA = 1) and Simple SPI Clock Timing (Slave, CKPH = 0)

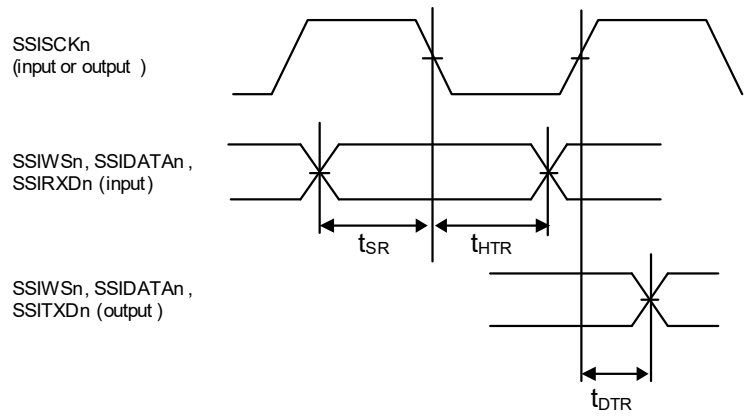
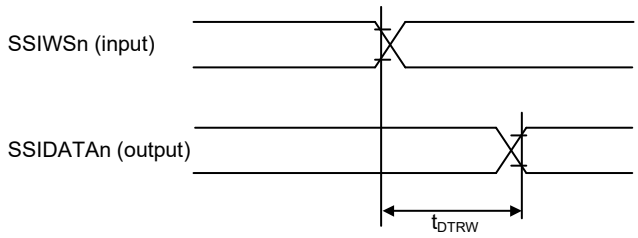


Figure 5.62 SSI Transmission/Reception Timing (SSICR.SCKP=1)



Note. Timing to output the MSB bit during slave transmission from SSIWSn
when DEL = 1 and SDTA = 0 or DEL = 1, SDTA = 1, and SWL[2:0] = DWL[2:0]

Figure 5.63 SSIDATA Output Delay After SSIWSn Changing Edge

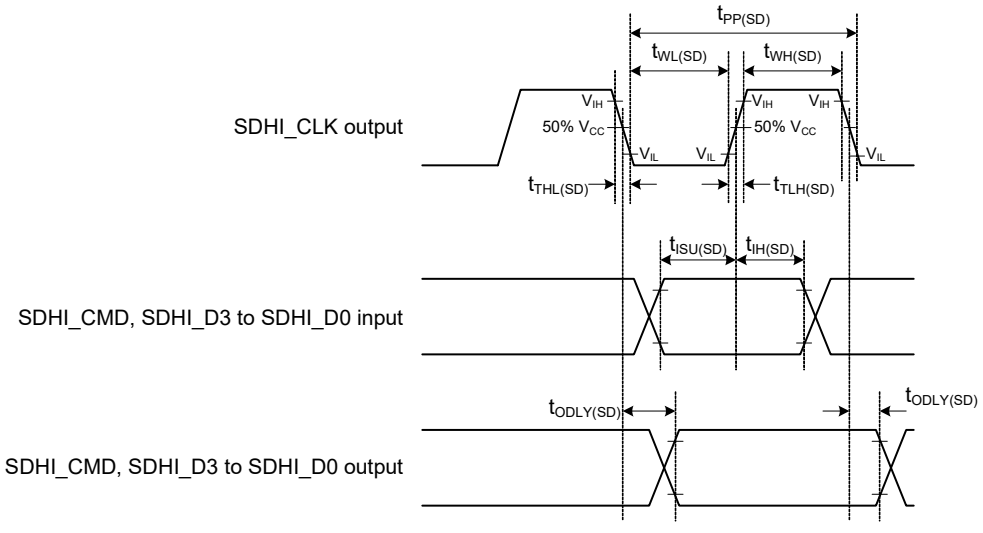


Figure 5.64 SD Host Interface Input/Output Signal Timing

5.4 USB Characteristics

Table 5.45 USB Characteristics (USB0_DP and USB0_DM Pin Characteristics)

Conditions: 3.0 V ≤ VCC = VCC_USB = AVCC < 3.6 V (when a regulator is not in use) or 4.0 V ≤ VCC = AVCC0 < 5.5 V (when a regulator is in use), VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
Input characteristics	Input high level voltage		V_{IH}	2.0	—	V	
	Input low level voltage		V_{IL}	—	0.8	V	
	Differential input sensitivity		V_{DI}	0.2	—	V	| USB0_DP – USB0_DM |
	Differential common mode range		V_{CM}	0.8	2.5	V	
Output characteristics	Output high level voltage		V_{OH}	2.8	VCC_USB	V	I_{OH} = –200 µA
	Output low level voltage		V_{OL}	0.0	0.3	V	I_{OL} = 2 mA
	Cross-over voltage		V_{CRS}	1.3	2.0	V	Figure 5.65, Figure 5.66
	Rise time	FS	t_r	4	20	ns	
		LS		75	300		
	Fall time	FS	t_f	4	20	ns	
		LS		75	300		
	Rise/fall time ratio	FS	t_r/t_f	90	111.11	%	t_r/t_f
		LS		80	125		
	Output resistance		Z_{DRV}	28	44	Ω	(Adjusting the resistance by external elements is not necessary.)
VBUS characteristics	VBUS input voltage		V_{IH}	VCC × 0.8	—	V	
			V_{IL}	—	VCC × 0.2	V	
Pull-up, pull-down	Pull-down resistor		R_{PD}	14.25	24.80	kΩ	
	Pull-up resistor		R_{PUI}	0.9	1.575	kΩ	During idle state
			R_{PUA}	1.425	3.09	kΩ	During reception
Battery Charging Specification Ver 1.2	D+ sink current		I_{DP_SINK}	25	175	µA	
	D- sink current		I_{DM_SINK}	25	175	µA	
	DCD source current		I_{DP_SRC}	7	13	µA	
	Data detection voltage		V_{DAT_REF}	0.25	0.4	V	
	D+ source current		V_{DP_SRC}	0.5	0.7	V	Output current = 250 µA
	D- source current		V_{DM_SRC}	0.5	0.7	V	Output current = 250 µA

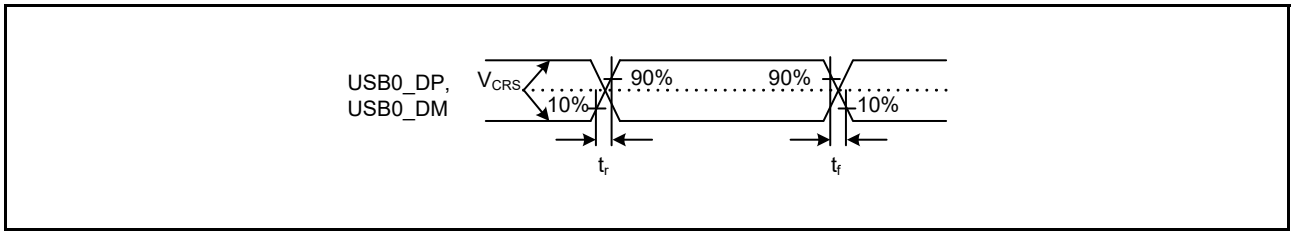


Figure 5.65 USB0_DP and USB0_DM Output Timing

Rev.	Date	Description		Classification
		Page	Summary	
1.10	Oct 30, 2015	142	Table 5.45 A/D Conversion Characteristics (1): Conditions and Voltage Range of Analog Input (Max.), changed	
		143	Table 5.46 A/D Conversion Characteristics (2): Conditions changed	
		144	Table 5.47 A/D Conversion Characteristics (3): Conditions changed	
		145	Table 5.48 A/D Conversion Characteristics (4): Conditions changed	
		146	Table 5.49 A/D Conversion Characteristics (5): Conditions changed and Absolute accuracy (Test Conditions) deleted	
		153	Table 5.57 Characteristics of Power-On Reset Circuit and Voltage Detection Circuit (1), changed	TN-RX*-A137A/E
		154	Table 5.58 Characteristics of Power-On Reset Circuit and Voltage Detection Circuit (2), changed	
		155	Figure 5.73 Power-On Reset Timing and Figure 5.74 Voltage Detection Circuit Timing (Vdet0), changed	
		159	Table 5.62 ROM (Flash Memory for Code Storage) Characteristics (2) High-Speed Operating Mode: Note changed	
		160	Table 5.63 ROM (Flash Memory for Code Storage) Characteristics (3) Middle-Speed Operating Mode: Note changed	
		161	Table 5.65 E2 DataFlash Characteristics (2): high-speed operating mode, Note changed	
		161	Table 5.66 E2 DataFlash Characteristics (3): middle-speed operating mode, Conditions and Note changed	
		163	Figure 5.79 Connecting Capacitors (100 Pins), changed	
		164	Figure 5.80 Connecting Capacitors (64 Pins), changed	
		165	Figure 5.81 Connecting Capacitors (48 Pins), changed	
		Appendix 1. Package Dimensions		
		167	Figure B 100 -Pin LQFP (PLQP0100KB-B), changed	TN-RX*-A137A/E
		170	Figure E 64 -Pin LQFP (PLQP0064KB-C), changed	TN-RX*-A137A/E
		172	Figure G 48 -Pin LQFP (PLQP0048KB-B), changed	TN-RX*-A137A/E
1.20	Sep 28, 2018	Features		
		1	SD host interface (optional: one channel) SD memory/ SDIO 1-bit or 4-bit SD bus supported, Note deleted	TN-RX*-A145A/E
		1. Overview		
		6	Table 1.2 Comparison of Functions for Different Packages, changed (deletion of IRQ2 on 64-pin package)	
		6	Table 1.2 Comparison of Functions for Different Packages, Note 1 added	TN-RX*-A145A/E
		7	Table 1.3 List of Products: D Version (Ta = –40 to +85°C) (1/2), changed	TN-RX*-A145A/E
		9	Table 1.4 List of Products: G Version (Ta = –40 to +105°C) (1/2), changed	TN-RX*-A145A/E
		11	Figure 1.1 How to Read the Product Part Number, changed	TN-RX*-A145A/E
		16	Table 1.5 Pin Functions (4/4), changed (changes in description for VCC_USB)	TN-RX*-A201A/E
		24	Table 1.6 List of Pins and Pin Functions (100-Pin TFLGA) (2/3), changed (UPSEL was added to the column of P35)	
		24	Table 1.6 List of Pins and Pin Functions (100-Pin TFLGA) (2/3), changed (USB0_VBUS was added to the column of PB5)	
		26	Table 1.7 List of Pins and Pin Functions (100-Pin LFQFP) (1/3), changed (UPSEL was added to the column of P35)	
		29	Table 1.8 List of Pins and Pin Functions (64-Pin WFLGA) (1/2), changed (UPSEL was added to the column of P35)	
		30	Table 1.8 List of Pins and Pin Functions (64-Pin WFLGA) (2/2), changed (USB0_VBUS was added to the column of PB5)	
		31	Table 1.9 List of Pins and Pin Functions (64-Pin LFQFP/HWQFN) (1/2), changed (UPSEL was added to the column of P35)	
		31	Table 1.9 List of Pins and Pin Functions (64-Pin LQFP/HWQFN) (1/2), changed (USB0_VBUS was added to the column of PB5)	
		33	Table 1.10 List of Pins and Pin Functions (48-Pin LFQFP/HWQFN) (1/2), changed (UPSEL was added to the column of P35)	
		33	Table 1.10 List of Pins and Pin Functions (48-Pin LFQFP/HWQFN) (1/2), changed	TN-RX*-A145A/E
		5. Electrical Characteristics		
		92	Table 5.18 Output Values of Voltage (1), changed	TN-RX*-A201A/E
		92	Table 5.19 Output Values of Voltage (2), changed	TN-RX*-A201A/E

NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.