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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	54MHz
Connectivity	CANbus, EBI/EMI, I ² C, IrDA, SCI, SD/SDIO, SPI, SSI, USB OTG
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	79
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f52317bdfp-30

Table 1.4 List of Products: G Version (T_a = –40 to +105°C) (1/2)

Group	Part No.	Order Part No.	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency	Security Function	SDHI	CAN	Operating Temperature
RX231	R5F52318AGFP	R5F52318AGFP#30	PLQP0100KB-B	512 Kbytes	64 Kbytes	8 Kbytes	54 MHz	Not available	Not available	Available	–40 to +105°C
	R5F52318BGFP	R5F52318BGFP#30						Available	Available	Available	
	R5F52318AGND	R5F52318AGND#U0	PWQN0064KC-A					Not available	Not available	Available	
	R5F52318BGND	R5F52318BGND#U0						Available	Available	Available	
	R5F52318AGFM	R5F52318AGFM#30	PLQP0064KB-C					Not available	Not available	Available	
	R5F52318BGFM	R5F52318BGFM#30						Available	Available	Available	
	R5F52318AGNE	R5F52318AGNE#U0	PWQN0048KB-A					Not available	Not available	Available	
	R5F52318BGNE	R5F52318BGNE#U0						Available	Not available	Available	
	R5F52318AGFL	R5F52318AGFL#30	PLQP0048KB-B					Not available	Not available	Available	
	R5F52318BGFL	R5F52318BGFL#30						Available	Not available	Available	
	R5F52317AGFP	R5F52317AGFP#30	PLQP0100KB-B	384 Kbytes				Not available	Not available	Available	
	R5F52317BGFP	R5F52317BGFP#30						Available	Available	Available	
	R5F52317AGND	R5F52317AGND#U0	PWQN0064KC-A					Not available	Not available	Available	
	R5F52317BGND	R5F52317BGND#U0						Available	Available	Available	
	R5F52317AGFM	R5F52317AGFM#30	PLQP0064KB-C					Not available	Not available	Available	
	R5F52317BGFM	R5F52317BGFM#30						Available	Available	Available	
	R5F52317AGNE	R5F52317AGNE#U0	PWQN0048KB-A					Not available	Not available	Available	
	R5F52317BGNE	R5F52317BGNE#U0						Available	Not available	Available	
	R5F52317AGFL	R5F52317AGFL#30	PLQP0048KB-B					Not available	Not available	Available	
	R5F52317BGFL	R5F52317BGFL#30						Available	Not available	Available	
	R5F52316AGFP	R5F52316AGFP#30	PLQP0100KB-B	256 Kbytes	32 Kbytes			Not available	Not available	Available	
	R5F52316CGFP	R5F52316CGFP#30						Not available	Not available	Not available	
	R5F52316AGND	R5F52316AGND#U0	PWQN0064KC-A					Not available	Not available	Available	
	R5F52316CGND	R5F52316CGND#U0						Not available	Not available	Not available	
	R5F52316AGFM	R5F52316AGFM#30	PLQP0064KB-C					Not available	Not available	Available	
	R5F52316CGFM	R5F52316CGFM#30						Not available	Not available	Not available	
	R5F52316AGNE	R5F52316AGNE#U0	PWQN0048KB-A					Not available	Not available	Available	
	R5F52316CGNE	R5F52316CGNE#U0						Not available	Not available	Not available	
	R5F52316AGFL	R5F52316AGFL#30	PLQP0048KB-B					Not available	Not available	Available	
	R5F52316CGFL	R5F52316CGFL#30						Not available	Not available	Not available	
	R5F52315AGFP	R5F52315AGFP#30	PLQP0100KB-B	128 Kbytes				Not available	Not available	Available	
	R5F52315CGFP	R5F52315CGFP#30						Not available	Not available	Not available	
	R5F52315AGND	R5F52315AGND#U0	PWQN0064KC-A					Not available	Not available	Available	
	R5F52315CGND	R5F52315CGND#U0						Not available	Not available	Not available	
	R5F52315AGFM	R5F52315AGFM#30	PLQP0064KB-C					Not available	Not available	Available	
	R5F52315CGFM	R5F52315CGFM#30						Not available	Not available	Not available	
	R5F52315AGNE	R5F52315AGNE#U0	PWQN0048KB-A					Not available	Not available	Available	
	R5F52315CGNE	R5F52315CGNE#U0						Not available	Not available	Not available	

Table 1.5 Pin Functions (4/4)

Classifications	Pin Name	I/O	Description
SD host interface	SDHI_D3 to SD_D0	I/O	SD data bus pins
	SDHI_CD	Input	SD card detection pin
	SDHI_WP	Input	SD write-protect signal
USB 2.0 host/ function module	VCC_USB	Input	Power supply pin for USB. Connect this pin to VCC or connect this pin to VSS via a 0.33 μ F smoothing capacitor for stabilizing the internal power supply.
	VSS_USB	Input	Ground pin for USB. Connect this pin to VSS.
	USB0_DP	I/O	D+ I/O pin of the USB on-chip transceiver.
	USB0_DM	I/O	D- I/O pin of the USB on-chip transceiver.
	USB0_VBUS	Input	USB cable connection monitor pin.
	USB0_EXICEN	Output	Low-power control signal for the OTG chip.
	USB0_VBUSEN	Output	VBUS (5 V) supply enable signal for the OTG chip.
	USB0_OVRCURA, USB0_OVRCURB	Input	External overcurrent detection pins.
	USB0_ID	Input	Mini-AB connector ID input pin during operation in OTG mode.
12-bit A/D converter	AN000 to AN007, AN016 to AN031	Input	Input pins for the analog signals to be processed by the A/D converter.
	ADTRG0#	Input	Input pin for the external trigger signal that start the A/D conversion.
12-bit D/A converter	DA0, DA1	Output	Analog output pins of the D/A converter.
Comparator B	CMPB0 to CMPB3	Input	Input pin for the analog signal to be processed by comparator B.
	CVREFB0 to CVREFB3	Input	Analog reference voltage supply pin for comparator B.
	CMPOB0 to CMPOB3	Output	Output pin for comparator B.
CTSU	TS0 to TS9, TS12, TS13, TS15 to TS20, TS22, TS23, TS27, TS30, TS33, TS35	Output	Electrostatic capacitance measurement pins (touch pins).
	TSCAP	Output	LPF connection pin.
Analog power supply	AVCC0	Input	Analog voltage supply pin for the 12-bit A/D converter and D/A converter. Connect this pin to VCC when not using the 12-bit A/D converter and D/A converter.
	AVSS0	Input	Analog ground pin for the 12-bit A/D converter and D/A converter. Connect this pin to VSS when not using the 12-bit A/D converter and D/A converter.
	VREFH0	Input	Analog reference voltage supply pin for the 12-bit A/D converter.
	VREFL0	Input	Analog reference ground pin for the 12-bit A/D converter.
	VREFH	Input	Analog reference voltage supply pin for the 12-bit D/A converter.
	VREFL	Input	Analog reference ground pin for the 12-bit D/A converter.
I/O ports	P03, P05, P07	I/O	3-bit input/output pins.
	P12 to P17	I/O	6-bit input/output pins.
	P20 to P27	I/O	8-bit input/output pins.
	P30 to P37	I/O	8-bit input/output pins (P35 input pin).
	P40 to P47	I/O	8-bit input/output pins.
	P50 to P55	I/O	6-bit input/output pins.
	PA0 to PA7	I/O	8-bit input/output pins.
	PB0 to PB7	I/O	8-bit input/output pins.
	PC0 to PC7	I/O	8-bit input/output pins.
	PD0 to PD7	I/O	8-bit input/output pins.
	PE0 to PE7	I/O	8-bit input/output pins.
	PH0 to PH3	I/O	4-bit input/output pins.
	PJ3	I/O	1-bit input/output pin.

1.5 Pin Assignments

Figure 1.3 to Figure 1.9 show the pin assignments. Table 1.6 to Table 1.10 show the lists of pins and pin functions.

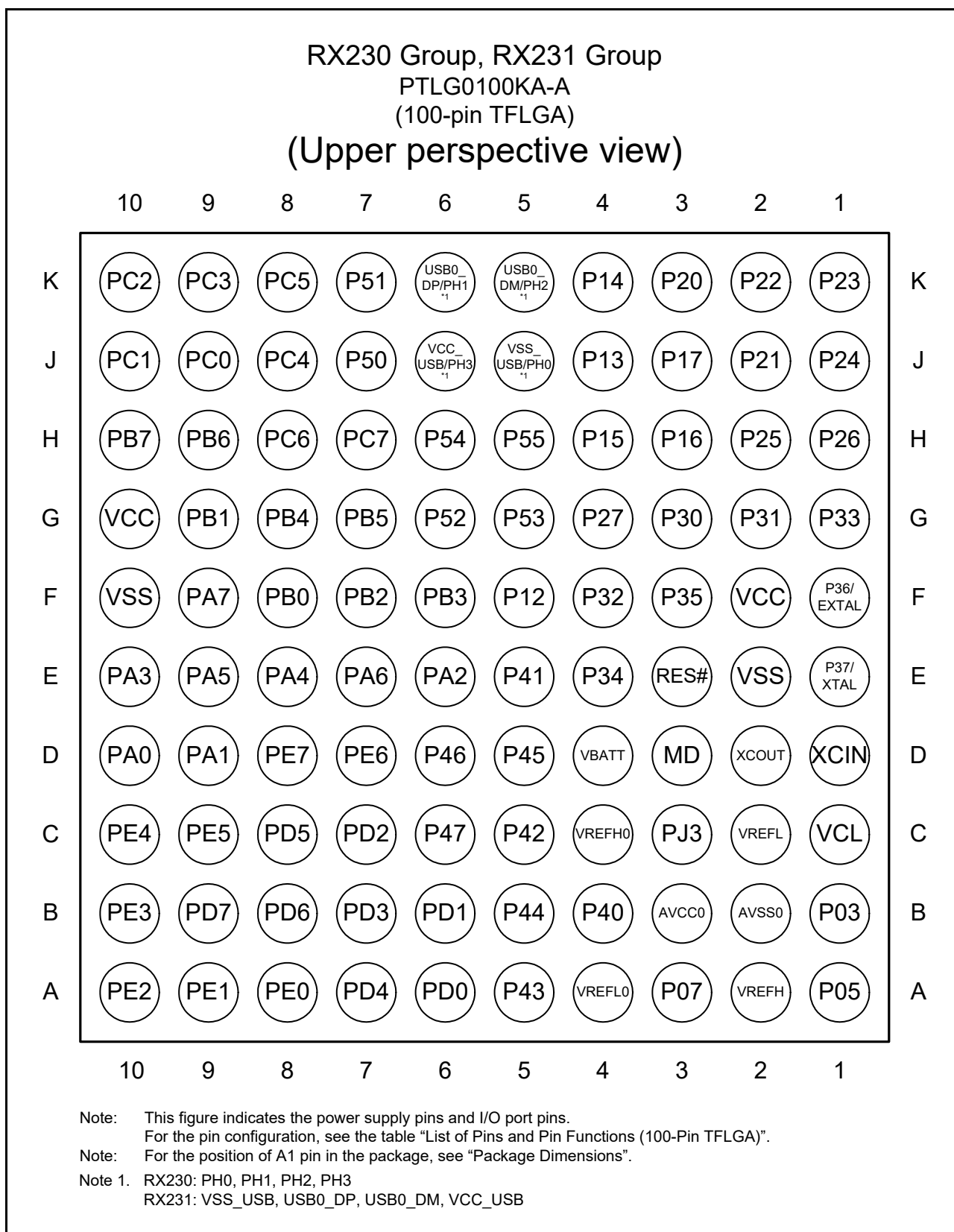


Figure 1.3 Pin Assignments of the 100-Pin TFLGA (Upper Perspective View)

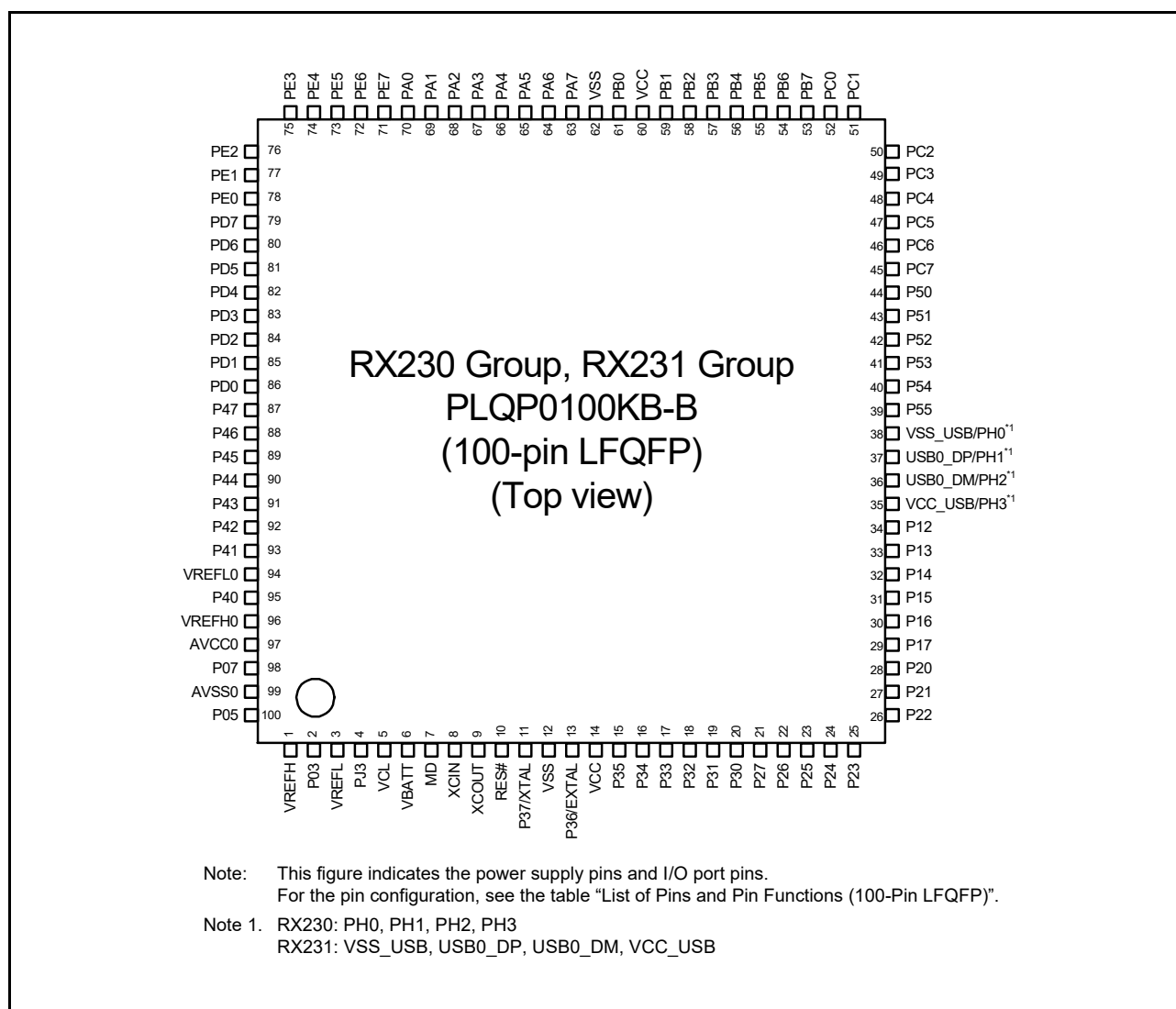
**Figure 1.4 Pin Assignments of the 100-Pin LFQFP**

Table 4.1 List of I/O Registers (Address Order) (13/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
0008 AC44h	SDHI	SD Interrupt Mask Register 2	SDIMSK2	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 AC48h	SDHI	SDHI Clock Control Register	SDCLKCR	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 AC4Ch	SDHI	Transfer Data Size Register	SDSIZE	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 AC50h	SDHI	Card Access Option Register	SDOPT	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 AC58h	SDHI	SD Error Status Register 1	SDERSTS1	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 AC5Ch	SDHI	SD Error Status Register 2	SDERSTS2	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 AC60h	SDHI	SD Buffer Register	SDBUFR	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 AC68h	SDHI	SDIO Mode Control Register	SDIOMD	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 AC6Ch	SDHI	SDIO Status Register	SDIOSTS	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 AC70h	SDHI	SDIO Interrupt Mask Register	SDIOIMSK	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 ADB0h	SDHI	DMA Transfer Enable Register	SDDMAEN	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 ADC0h	SDHI	SDHI Software Reset Register	SDRST	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 ADE0h	SDHI	Swap Control Register	SDSWAP	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 B000h	CAC	CAC Control Register 0	CACR0	8	8	2 or 3 PCLKB	2 ICLK
0008 B001h	CAC	CAC Control Register 1	CACR1	8	8	2 or 3 PCLKB	2 ICLK
0008 B002h	CAC	CAC Control Register 2	CACR2	8	8	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (19/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
0008 C1B3h	MPC	PE3 Pin Function Control Register	PE3PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1B4h	MPC	PE4 Pin Function Control Register	PE4PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1B5h	MPC	PE5 Pin Function Control Register	PE5PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1B6h	MPC	PE6 Pin Function Control Register	PE6PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1B7h	MPC	PE7 Pin Function Control Register	PE7PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1C8h	MPC	PH0 Pin Function Control Register	PH0PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1C9h	MPC	PH1 Pin Function Control Register	PH1PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1CAh	MPC	PH2 Pin Function Control Register	PH2PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1CBh	MPC	PH3 Pin Function Control Register	PH3PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1D3h	MPC	PJ3 Pin Function Control Register	PJ3PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C290h	SYSTEM	Reset Status Register 0	RSTSR0	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C291h	SYSTEM	Reset Status Register 1	RSTSR1	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C293h	SYSTEM	Main Clock Oscillator Forced Oscillation Control Register	MOFCR	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C297h	SYSTEM	Voltage Monitoring Circuit Control Register	LVCMPCR	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C298h	SYSTEM	Voltage Detection Level Select Register	LVDLVL	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C29Ah	SYSTEM	Voltage Monitoring 1 Circuit Control Register 0	LVD1CR0	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C29Bh	SYSTEM	Voltage Monitoring 2 Circuit Control Register 0	LVD2CR0	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C29Dh	SYSTEM	VBATT Control Register	VBATTCT	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C29Eh	SYSTEM	VBATT Status Register	VBATTST	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C29Fh	SYSTEM	VBATT Pin Voltage Drop Detection Interrupt Control Register	VBTLVDICR	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C400h	RTC	64-Hz Counter	R64CNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C402h	RTC	Second Counter	RSECCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C402h	RTC	Binary Counter 0	BCNT0	8	8	2 or 3 PCLKB	2 ICLK
0008 C404h	RTC	Minute Counter	RMINCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C404h	RTC	Binary Counter 1	BCNT1	8	8	2 or 3 PCLKB	2 ICLK
0008 C406h	RTC	Hour Counter	RHRCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C406h	RTC	Binary Counter 2	BCNT2	8	8	2 or 3 PCLKB	2 ICLK
0008 C408h	RTC	Day-of-Week Counter	RWKCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C408h	RTC	Binary Counter 3	BCNT3	8	8	2 or 3 PCLKB	2 ICLK
0008 C40Ah	RTC	Date Counter	RDAYCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C40Ch	RTC	Month Counter	RMONCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C40Eh	RTC	Year Counter	RYRCNT	16	16	2 or 3 PCLKB	2 ICLK
0008 C410h	RTC	Second Alarm Register	RSECAR	8	8	2 or 3 PCLKB	2 ICLK
0008 C410h	RTC	Binary Counter 0 Alarm Register	BCNT0AR	8	8	2 or 3 PCLKB	2 ICLK
0008 C412h	RTC	Minute Alarm Register	RMINAR	8	8	2 or 3 PCLKB	2 ICLK
0008 C412h	RTC	Binary Counter 1 Alarm Register	BCNT1AR	8	8	2 or 3 PCLKB	2 ICLK
0008 C414h	RTC	Hour Alarm Register	RHRAR	8	8	2 or 3 PCLKB	2 ICLK
0008 C414h	RTC	Binary Counter 2 Alarm Register	BCNT2AR	8	8	2 or 3 PCLKB	2 ICLK
0008 C416h	RTC	Day-of-Week Alarm Register	RWKAR	8	8	2 or 3 PCLKB	2 ICLK
0008 C416h	RTC	Binary Counter 3 Alarm Register	BCNT3AR	8	8	2 or 3 PCLKB	2 ICLK
0008 C418h	RTC	Date Alarm Register	RDAYAR	8	8	2 or 3 PCLKB	2 ICLK
0008 C418h	RTC	Binary Counter 0 Alarm Enable Register	BCNT0AER	8	8	2 or 3 PCLKB	2 ICLK
0008 C41Ah	RTC	Month Alarm Register	RMONAR	8	8	2 or 3 PCLKB	2 ICLK
0008 C41Ah	RTC	Binary Counter 1 Alarm Enable Register	BCNT1AER	8	8	2 or 3 PCLKB	2 ICLK
0008 C41Ch	RTC	Year Alarm Register	RYRAR	16	16	2 or 3 PCLKB	2 ICLK
0008 C41Ch	RTC	Binary Counter 2 Alarm Enable Register	BCNT2AER	16	16	2 or 3 PCLKB	2 ICLK
0008 C41Eh	RTC	Year Alarm Enable Register	RYRAREN	8	8	2 or 3 PCLKB	2 ICLK
0008 C41Eh	RTC	Binary Counter 3 Alarm Enable Register	BCNT3AER	8	8	2 or 3 PCLKB	2 ICLK
0008 C422h	RTC	RTC Control Register 1	RCR1	8	8	2 or 3 PCLKB	2 ICLK
0008 C424h	RTC	RTC Control Register 2	RCR2	8	8	2 or 3 PCLKB	2 ICLK
0008 C426h	RTC	RTC Control Register 3	RCR3	8	8	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (24/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
000A 8326h	RSCAN	Global Control Register L	GCTRL	16	16	2 or 3 PCLKB	2 ICLK
000A 8328h	RSCAN	Global Control Register H	GCTRH	16	16	2 or 3 PCLKB	2 ICLK
000A 832Ah	RSCAN	Global Status Register	GSTS	16	16	2 or 3 PCLKB	2 ICLK
000A 832Ch	RSCAN	Global Error Flag Register	GERFLL	8	8	2 or 3 PCLKB	2 ICLK
000A 832Eh	RSCAN	Timestamp Register	GTSC	16	16	2 or 3 PCLKB	2 ICLK
000A 8330h	RSCAN	Receive Rule Number Configuration Register	GAFLCFG	16	16	2 or 3 PCLKB	2 ICLK
000A 8332h	RSCAN	Receive Buffer Number Configuration Register	RMNB	16	16	2 or 3 PCLKB	2 ICLK
000A 8334h	RSCAN	Receive Buffer Receive Complete Flag Register	RMND0	16	16	2 or 3 PCLKB	2 ICLK
000A 8338h	RSCAN	Receive FIFO Control Register 0	RFCC0	16	16	2 or 3 PCLKB	2 ICLK
000A 833Ah	RSCAN	Receive FIFO Control Register 1	RFCC1	16	16	2 or 3 PCLKB	2 ICLK
000A 8340h	RSCAN	Receive FIFO Status Register 0	RFSTS0	16	16	2 or 3 PCLKB	2 ICLK
000A 8342h	RSCAN	Receive FIFO Status Register 1	RFSTS1	16	16	2 or 3 PCLKB	2 ICLK
000A 8348h	RSCAN	Receive FIFO Pointer Control Register 0	RFPCTR0	16	16	2 or 3 PCLKB	2 ICLK
000A 834Ah	RSCAN	Receive FIFO Pointer Control Register 1	RFPCTR1	16	16	2 or 3 PCLKB	2 ICLK
000A 8350h	RSCAN0	Transmit/Receive FIFO Control Register 0L	CFCCLO	16	16	2 or 3 PCLKB	2 ICLK
000A 8352h	RSCAN0	Transmit/Receive FIFO Control Register 0H	CFCH0	16	16	2 or 3 PCLKB	2 ICLK
000A 8358h	RSCAN0	Transmit/Receive FIFO Status Register 0	CFSTS0	16	16	2 or 3 PCLKB	2 ICLK
000A 835Ch	RSCAN0	Transmit/Receive FIFO Pointer Control Register 0	CFPCTR0	16	16	2 or 3 PCLKB	2 ICLK
000A 8360h	RSCAN	Receive FIFO Message Lost Status Register	RFMSTS	8	8	2 or 3 PCLKB	2 ICLK
000A 8361h	RSCAN0	Transmit/Receive FIFO Message Lost Status Register	CFMSTS	8	8	2 or 3 PCLKB	2 ICLK
000A 8362h	RSCAN	Receive FIFO Interrupt Status Register	RFISTS	8	8	2 or 3 PCLKB	2 ICLK
000A 8363h	RSCAN	Transmit/Receive FIFO Receive Interrupt Status Register	CFISTS	8	8	2 or 3 PCLKB	2 ICLK
000A 8364h	RSCAN0	Transmit Buffer Control Register 0	TMC0	8	8	2 or 3 PCLKB	2 ICLK
000A 8365h	RSCAN0	Transmit Buffer Control Register 1	TMC1	8	8	2 or 3 PCLKB	2 ICLK
000A 8366h	RSCAN0	Transmit Buffer Control Register 2	TMC2	8	8	2 or 3 PCLKB	2 ICLK
000A 8367h	RSCAN0	Transmit Buffer Control Register 3	TMC3	8	8	2 or 3 PCLKB	2 ICLK
000A 836Ch	RSCAN0	Transmit Buffer Status Register 0	TMSTS0	8	8	2 or 3 PCLKB	2 ICLK
000A 836Dh	RSCAN0	Transmit Buffer Status Register 1	TMSTS1	8	8	2 or 3 PCLKB	2 ICLK
000A 836Eh	RSCAN0	Transmit Buffer Status Register 2	TMSTS2	8	8	2 or 3 PCLKB	2 ICLK
000A 836Fh	RSCAN0	Transmit Buffer Status Register 3	TMSTS3	8	8	2 or 3 PCLKB	2 ICLK
000A 8374h	RSCAN0	Transmit Buffer Transmit Request Status Register	TMTRSTS	16	16	2 or 3 PCLKB	2 ICLK
000A 8376h	RSCAN0	Transmit Buffer Transmit Complete Status Register	TMTCTS	16	16	2 or 3 PCLKB	2 ICLK
000A 8378h	RSCAN0	Transmit Buffer Transmit Abort Status Register	TMTASTS	16	16	2 or 3 PCLKB	2 ICLK
000A 837Ah	RSCAN0	Transmit Buffer Interrupt Enable Register	TMIEC	16	16	2 or 3 PCLKB	2 ICLK
000A 837Ch	RSCAN0	Transmit History Buffer Control Register	THLCC0	16	16	2 or 3 PCLKB	2 ICLK
000A 8380h	RSCAN0	Transmit History Buffer Status Register	THLSTS0	16	16	2 or 3 PCLKB	2 ICLK
000A 8384h	RSCAN0	Transmit History Buffer Pointer Control Register	THLPCTR0	16	16	2 or 3 PCLKB	2 ICLK
000A 8388h	RSCAN	Global Transmit Interrupt Status Register	GTINTSTS	16	16	2 or 3 PCLKB	2 ICLK
000A 838Ah	RSCAN	Global RAM Window Control Register	GRWCR	16	16	2 or 3 PCLKB	2 ICLK
000A 838Ch	RSCAN	Global Test Configuration Register	GTSTCFG	16	16	2 or 3 PCLKB	2 ICLK
000A 838Eh	RSCAN	Global Test Control Register	GTSTCTRL	16	16	2 or 3 PCLKB	2 ICLK
000A 8394h	RSCAN	Global Test Protection Unlock Register	GLOCKK	16	16	2 or 3 PCLKB	2 ICLK
000A 83A0h	RSCAN	Receive Rule Entry Register 0AL	GAFLIDL0	16	16	2 or 3 PCLKB	2 ICLK
000A 83A0h	RSCAN	Receive Buffer Register 0AL	RMIDL0	16	16	2 or 3 PCLKB	2 ICLK
000A 83A2h	RSCAN	Receive Rule Entry Register 0AH	GAFLIDH0	16	16	2 or 3 PCLKB	2 ICLK
000A 83A2h	RSCAN	Receive Buffer Register 0AH	RMIDH0	16	16	2 or 3 PCLKB	2 ICLK
000A 83A4h	RSCAN	Receive Rule Entry Register 0BL	GAFLML0	16	16	2 or 3 PCLKB	2 ICLK
000A 83A4h	RSCAN	Receive Buffer Register 0BL	RMTS0	16	16	2 or 3 PCLKB	2 ICLK
000A 83A6h	RSCAN	Receive Rule Entry Register 0BH	GAFLMH0	16	16	2 or 3 PCLKB	2 ICLK
000A 83A6h	RSCAN	Receive Buffer Register 0BH	RMPTR0	16	16	2 or 3 PCLKB	2 ICLK
000A 83A8h	RSCAN	Receive Rule Entry Register 0CL	GAFLPL0	16	16	2 or 3 PCLKB	2 ICLK
000A 83A8h	RSCAN	Receive Buffer Register 0CL	RMDFO0	16	16	2 or 3 PCLKB	2 ICLK

Table 5.2 Recommended Operating Voltage Conditions

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltages	VCC*1, *2	When USB is not used	1.8	—	5.5	V
		When USB is used When USB regulator is not used	3.0	—	3.6	
		When USB is used When USB regulator is used	4.0	—	5.5	
	VSS		—	0	—	
USB power supply voltages	VCC_USB	When USB regulator is not used	—	VCC	—	V
	VSS_USB		—	0	—	
VBATT power supply voltage	VBATT		1.8	—	5.5	V
Analog power supply voltages	AVCC0*1, *2		1.8	—	5.5	V
	AVSS0		—	0	—	
	VREFH0		1.8	—	AVCC0	
	VREFL0		—	0	—	
	VREFH		1.8	—	AVCC0	
	VREFL		—	0	—	

Note 1. Use AVCC0 and VCC under the following conditions:

AVCC0 and VCC can be set individually within the operating range when VCC ≥ 2.0 V

AVCC0 = VCC when VCC < 2.0 V

Note 2. When powering on the VCC and AVCC0 pins, power them on at the same time or the VCC pin first and then the AVCC0 pin.

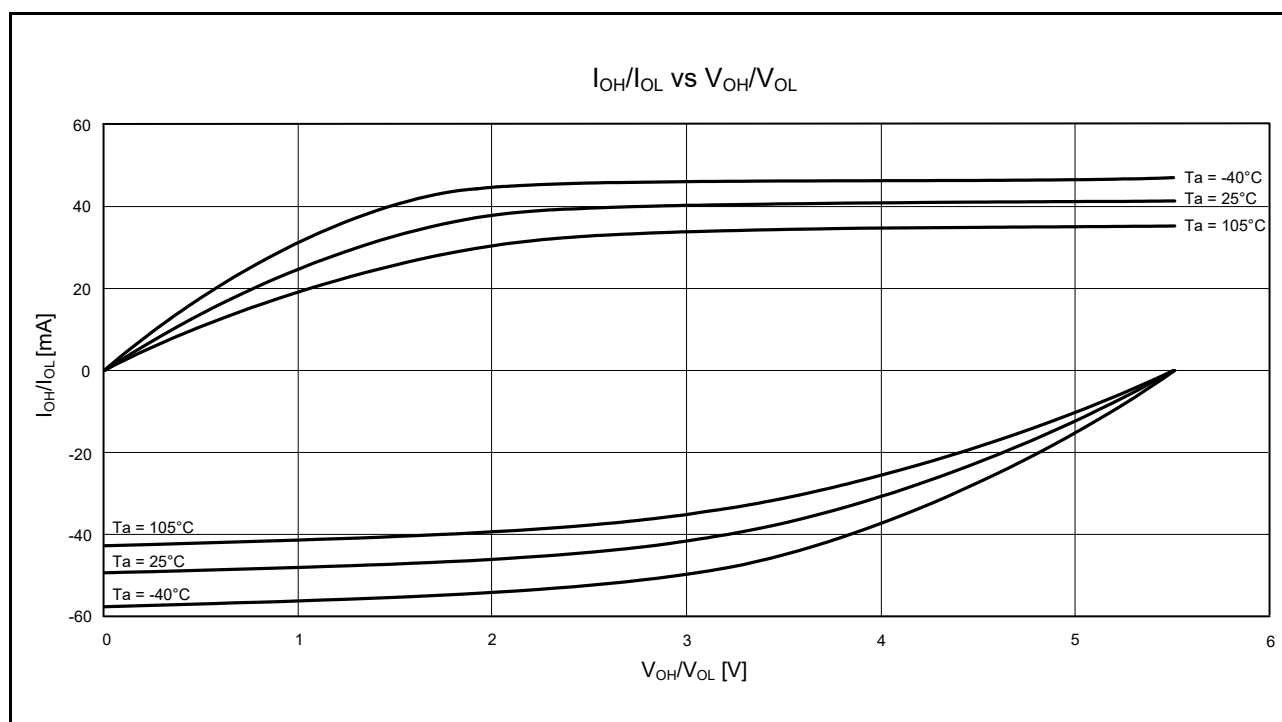


Figure 5.12 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at $V_{CC} = 5.5$ V When Normal Output is Selected (Reference Data)

5.3.5 Bus Timing

Table 5.34 Bus Timing (1)

Conditions: $2.7\text{ V} \leq V_{CC} = V_{CC_USB} = AV_{CC0} \leq 5.5\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$,
 $f_{BCLK} \leq 32\text{ MHz}$ (BCLK pin output frequency $\leq 16\text{ MHz}$), $T_a = -40\text{ to }+105^\circ\text{C}$, $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$,
 $I_{OH} = -1.0\text{ mA}$, $I_{OL} = 1.0\text{ mA}$, $C_L = 30\text{ pF}$, when normal output is selected by the drive capacity control register

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	55	ns	Figure 5.38 to Figure 5.41
Byte control delay time	t_{BCD}	—	55	ns	
CS# delay time	t_{CSD}	—	55	ns	
RD# delay time	t_{RSD}	—	55	ns	
Read data setup time	t_{RDS}	40	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	55	ns	
Write data delay time	t_{WDD}	—	55	ns	
Write data hold time	t_{WDH}	0	—	ns	Figure 5.42
WAIT# setup time	t_{WTS}	40	—	ns	
WAIT# hold time	t_{WTH}	0	—	ns	

Table 5.35 Bus Timing (2)

Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} = AV_{CC0} < 2.7\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$,
 $f_{BCLK} \leq 16\text{ MHz}$ (BCLK pin output frequency $\leq 8\text{ MHz}$), $T_a = -40\text{ to }+105^\circ\text{C}$, $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$,
 $I_{OH} = -1.0\text{ mA}$, $I_{OL} = 1.0\text{ mA}$, $C_L = 30\text{ pF}$, when normal output is selected by the drive capacity control register

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	90	ns	Figure 5.38 to Figure 5.41
Byte control delay time	t_{BCD}	—	90	ns	
CS# delay time	t_{CSD}	—	90	ns	
RD# delay time	t_{RSD}	—	90	ns	
Read data setup time	t_{RDS}	60	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	90	ns	
Write data delay time	t_{WDD}	—	90	ns	
Write data hold time	t_{WDH}	0	—	ns	Figure 5.42
WAIT# setup time	t_{WTS}	60	—	ns	
WAIT# hold time	t_{WTH}	0	—	ns	

Table 5.39 Timing of On-Chip Peripheral Modules (2)

Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} = AV_{CC0} \leq 5.5\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$, $C = 30\text{ pF}$,
when high-drive output is selected by the drive capacity control register

Item				Symbol	Min.	Max.	Unit	Test Conditions
RSPI	RSPCK clock cycle	Master		t_{SPCyc}	2	4096	t_{Pcyc}^{*1}	Figure 5.54
		Slave			8	4096		
	RSPCK clock high pulse width	Master		t_{SPCKWH}	$(t_{SPCyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
		Slave			$(t_{SPCyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock low pulse width	Master		t_{SPCKWL}	$(t_{SPCyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
		Slave			$(t_{SPCyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock rise/fall time	Output	2.7 V or above	t_{SPCKr} t_{SPCKf}	—	10	ns	
			1.8 V or above		—	15		
		Input			—	1	μs	
	Data input setup time	Master	2.7 V or above	t_{SU}	10	—	ns	Figure 5.55 to Figure 5.58
			1.8 V or above		30	—		
		Slave			$25 - t_{Pcyc}$	—		
	Data input hold time	Master	RSPCK set to a division ratio other than PCLKB divided by 2	t_H	t_{Pcyc}	—	ns	
			RSPCK set to PCLKB divided by 2	t_{HF}	0	—		
		Slave		t_H	$20 + 2 \times t_{Pcyc}$	—		
	SSL setup time	Master		t_{LEAD}	$-30 + N^2 \times t_{SPcyc}$	—	ns	
		Slave			2	—	t_{Pcyc}	
	SSL hold time	Master		t_{LAG}	$-30 + N^3 \times t_{SPcyc}$	—	ns	
		Slave			2	—	t_{Pcyc}	
Data output delay time	Master	2.7 V or above	t_{OD}	—	14	ns		
		1.8 V or above		—	30			
	Slave	2.7 V or above		—	$3 \times t_{Pcyc} + 65$			
		1.8 V or above		—	$3 \times t_{Pcyc} + 105$			
Data output hold time	Master		t_{OH}	0	—	ns		
	Slave			0	—			
Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns		
	Slave			$4 \times t_{Pcyc}$	—			
MOSI and MISO rise/fall time	Output	2.7 V or above	t_{Dr} , t_{Df}	—	10	ns		
		1.8 V or above		—	15			
	Input			—	1	μs		
SSL rise/fall time	Output	2.7 V or above	t_{SSLr} , t_{SSLf}	—	10	ns		
		1.8 V or above		—	15	ns		
	Input			—	1	μs		
Slave access time		2.7 V or above	t_{SA}	—	6	t_{Pcyc}	Figure 5.57, Figure 5.58	
		1.8 V or above		—	7			
Slave output release time		2.7 V or above	t_{REL}	—	5	t_{Pcyc}		
		1.8 V or above		—	6			

Note 1. t_{Pcyc} : PCLK cycle

Note 2. N: An integer from 1 to 8 that can be set by the RSPI clock delay register (SPCKD)

Note 3. N: An integer from 1 to 8 that can be set by the RSPI slave select negation delay register (SSLND)

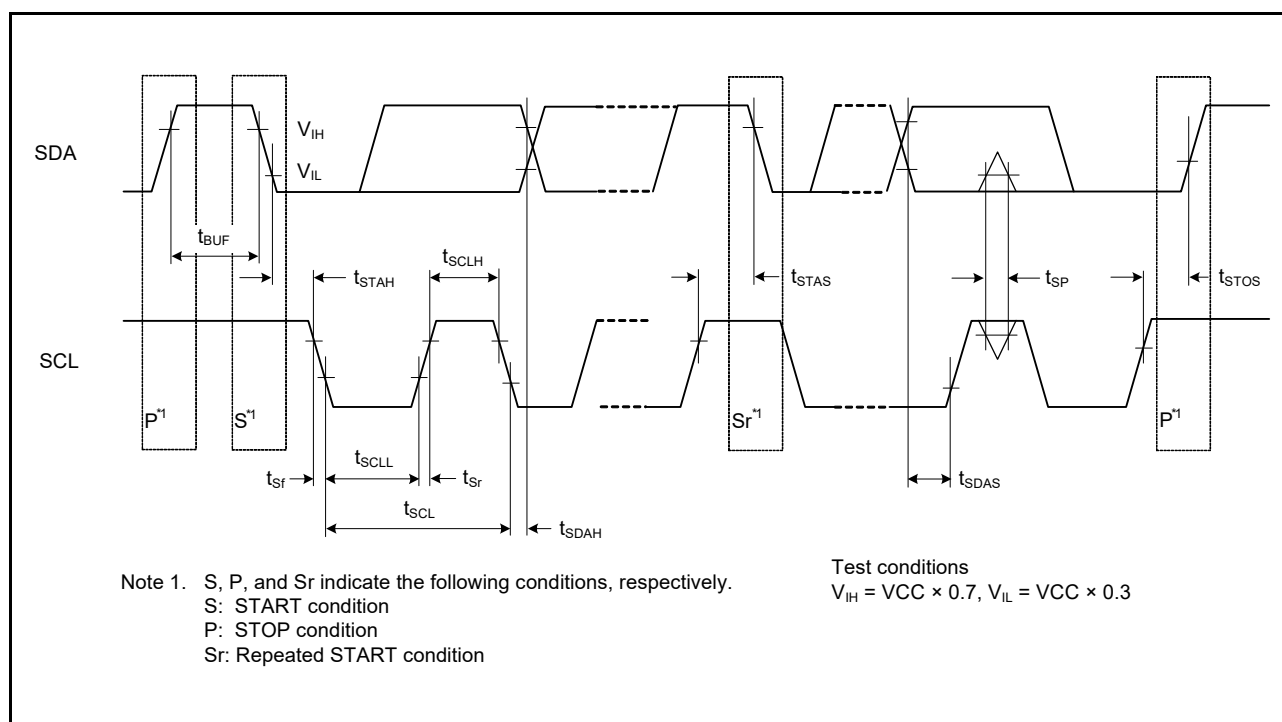
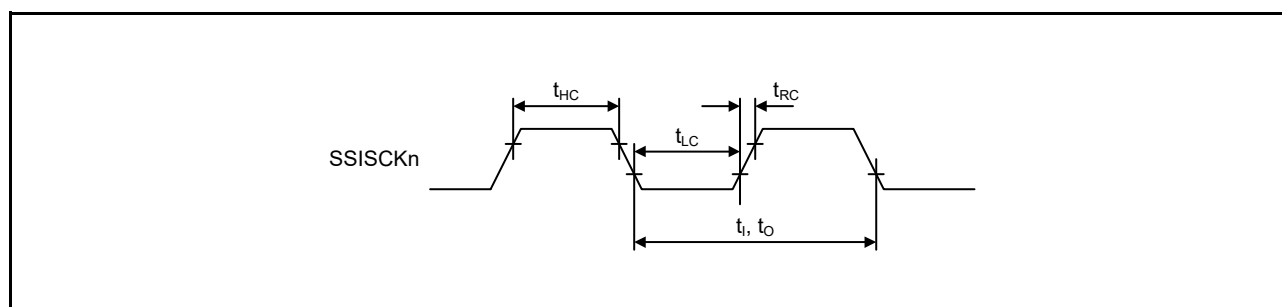
Figure 5.59 RIIC Bus Interface Input/Output Timing and Simple I²C Bus Interface Input/Output Timing

Figure 5.60 SSI Clock Input/Output Timing

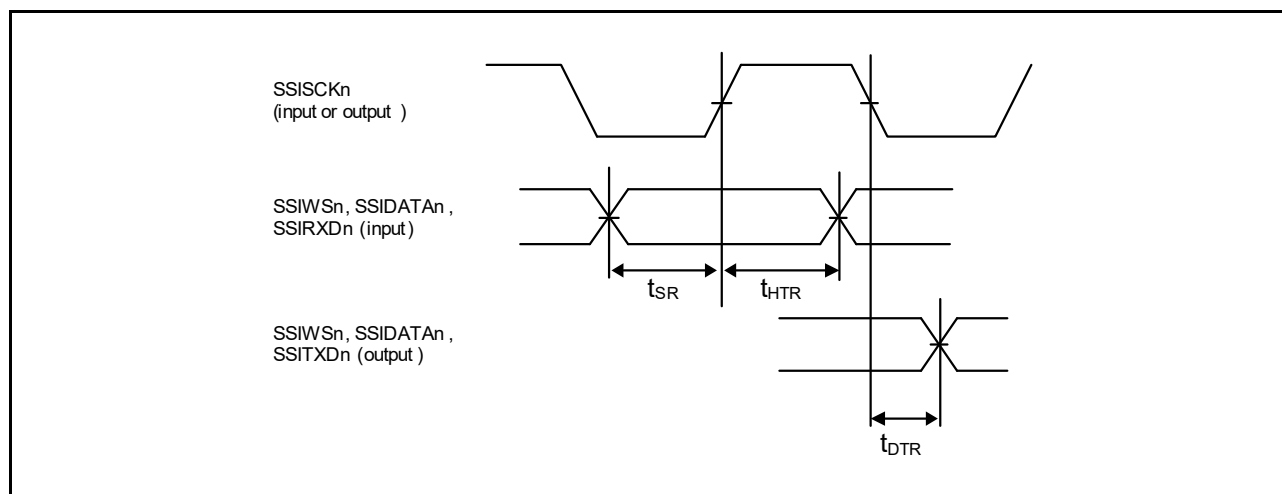


Figure 5.61 SSI Transmission/Reception Timing (SSICR.SCKP=0)

5.4 USB Characteristics

Table 5.45 USB Characteristics (USB0_DP and USB0_DM Pin Characteristics)

Conditions: $3.0\text{ V} \leq VCC = VCC_USB = AVCC < 3.6\text{ V}$ (when a regulator is not in use) or $4.0\text{ V} \leq VCC = AVCC < 5.5\text{ V}$ (when a regulator is in use), $VSS = AVSS0 = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item			Symbol	Min.	Max.	Unit	Test Conditions	
Input characteristics	Input high level voltage		V _{IH}	2.0	—	V		
	Input low level voltage		V _{IL}	—	0.8	V		
	Differential input sensitivity		V _{DI}	0.2	—	V	USB0_DP – USB0_DM	
	Differential common mode range		V _{CM}	0.8	2.5	V		
Output characteristics	Output high level voltage		V _{OH}	2.8	VCC_USB	V	I _{OH} = –200 μA	
	Output low level voltage		V _{OL}	0.0	0.3	V	I _{OL} = 2 mA	
	Cross-over voltage		V _{CRS}	1.3	2.0	V		Figure 5.65, Figure 5.66
	Rise time	FS	t _r	4	20	ns		
		LS		75	300			
	Fall time	FS	t _f	4	20	ns		
		LS		75	300			
	Rise/fall time ratio	FS	t _r /t _f	90	111.11	%	t _r /t _f	
		LS		80	125			
	Output resistance		Z _{DRV}	28	44	Ω	(Adjusting the resistance by external elements is not necessary.)	
VBUS characteristics	VBUS input voltage		V _{IH}	VCC × 0.8	—	V		
			V _{IL}	—	VCC × 0.2	V		
Pull-up, pull-down	Pull-down resistor		R _{PD}	14.25	24.80	kΩ		
	Pull-up resistor		R _{PUI}	0.9	1.575	kΩ	During idle state	
			R _{PUA}	1.425	3.09	kΩ	During reception	
Battery Charging Specification Ver 1.2	D+ sink current		I _{DP_SINK}	25	175	μA		
	D- sink current		I _{DM_SINK}	25	175	μA		
	DCD source current		I _{DP_SRC}	7	13	μA		
	Data detection voltage		V _{DAT_REF}	0.25	0.4	V		
	D+ source current		V _{DP_SRC}	0.5	0.7	V	Output current = 250 μA	
	D- source current		V _{DM_SRC}	0.5	0.7	V	Output current = 250 μA	

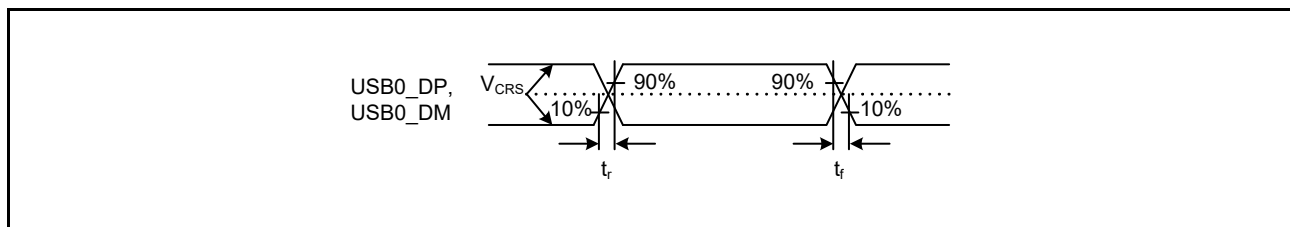
**Figure 5.65 USB0_DP and USB0_DM Output Timing**

Table 5.50 A/D Conversion Characteristics (5)

Conditions: $1.8\text{V} \leq V_{CC} = V_{CC_USB} = AVCC0 \leq 5.5\text{V}$, $1.8\text{V} \leq V_{REFH0} \leq AVCC0$, $V_{SS} = AVSS0 = V_{SS_USB} = 0\text{V}$,
reference voltage = V_{REFH0} selected, $T_a = -40$ to $+105^\circ\text{C}$

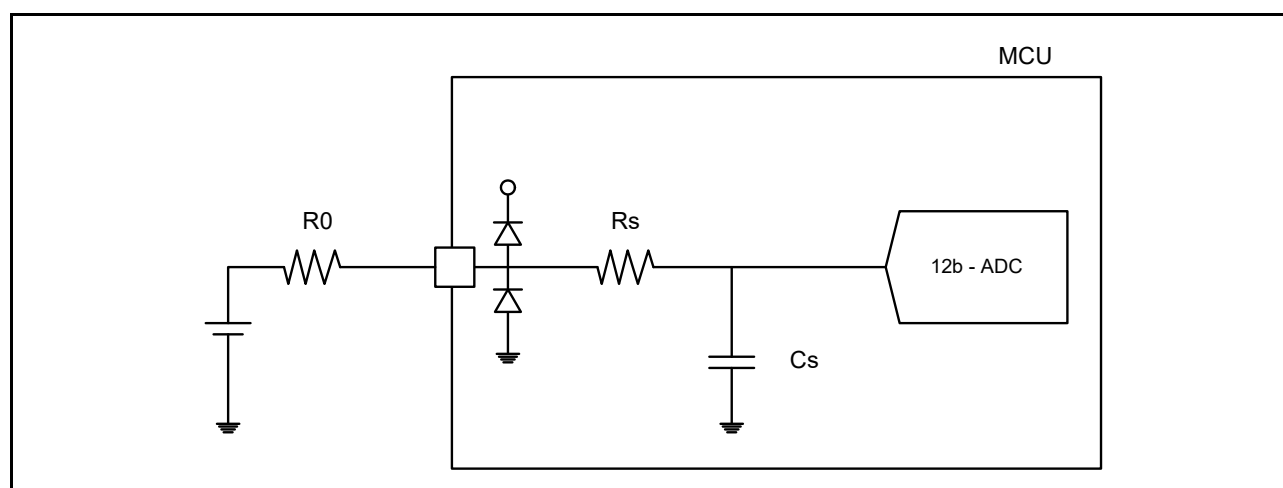
Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	8	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 8 MHz)	Permissible signal source impedance (Max.) = 5 k Ω	6.75	—	—	μs	High-precision channel The ADCSR.ADHSC bit is 1 The ADSSTRn register is 0Dh
		10.13	—	—		Normal-precision channel The ADCSR.ADHSC bit is 1 The ADSSTRn register is 28h
Analog input capacitance	Cs	—	—	15	pF	Pin capacitance included Figure 5.68
Analog input resistance	Rs	—	—	2.5	k Ω	Figure 5.68
Offset error		—	± 1	± 7.5	LSB	
Full-scale error		—	± 1.5	± 7.5	LSB	
Quantization error		—	± 0.5	—	LSB	
Absolute accuracy		—	± 3.0	± 8.0	LSB	
DNL differential non-linearity error		—	± 1.0	—	LSB	
INL integral non-linearity error		—	± 1.25	± 3.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential non-linearity error, and INL integral non-linearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 5.51 A/D Converter Channel Classification

Classification	Channel	Conditions	Remarks
High-precision channel	AN000 to AN007	$AVCC0 = 1.8$ to 5.5V	Pins AN000 to AN007 cannot be used as digital outputs when the A/D converter is in use.
Normal-precision channel	AN016 to AN031		
Internal reference voltage input channel	Internal reference voltage	$AVCC0 = 2.0$ to 5.5V	
Temperature sensor input channel	Temperature sensor output	$AVCC0 = 2.0$ to 5.5V	

**Figure 5.68 Equivalent Circuit**

5.7 Temperature Sensor Characteristics

Table 5.55 Temperature Sensor Characteristics

Conditions: $2.0\text{ V} \leq \text{VCC} = \text{VCC_USB} = \text{AVCC0} \leq 5.5\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Relative accuracy	—	—	± 1.5	—	$^\circ\text{C}$	2.4 V or above
		—	± 2.0	—		Below 2.4 V
Temperature slope	—	—	-3.65	—	mV/ $^\circ\text{C}$	
Output voltage (25 $^\circ\text{C}$)	—	—	1.05	—	V	VCC = 3.3 V
Temperature sensor start time	t_{START}	—	—	5	μs	
Sampling time	—	5	—	—	μs	

5.8 Comparator Characteristics

Table 5.56 Comparator Characteristics

Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} = \text{AVCC0} \leq 5.5\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
CVREFB0 to CVREFB3 input reference voltage		VREF	0	—	VCC - 1.4	V	
CMPB0 to CMPB3 input voltage		VI	-0.3	—	VCC + 0.3	V	
Offset	Comparator high-speed mode	—	—	—	50	mV	
	Comparator high-speed mode Window function enabled	—	—	—	60	mV	
	Comparator low-speed mode	—	—	—	40	mV	
Comparator output delay time	Comparator high-speed mode	Td	—	—	1.2	μs	VCC = 3 V, input slew rate $\geq 50\text{ mV}/\mu\text{s}$
	Comparator high-speed mode Window function enabled	Tdw	—	—	2.0	μs	
	Comparator low-speed mode	Td	—	—	5.0	μs	
High-side reference voltage (comparator high-speed mode, window function enabled)		VRFH	—	0.76 VCC	—	V	
Low-side reference voltage (comparator high-speed mode, window function enabled)		VRFL	—	0.24 VCC	—	V	
Operation stabilization wait time		Tcmp	100	—	—	μs	

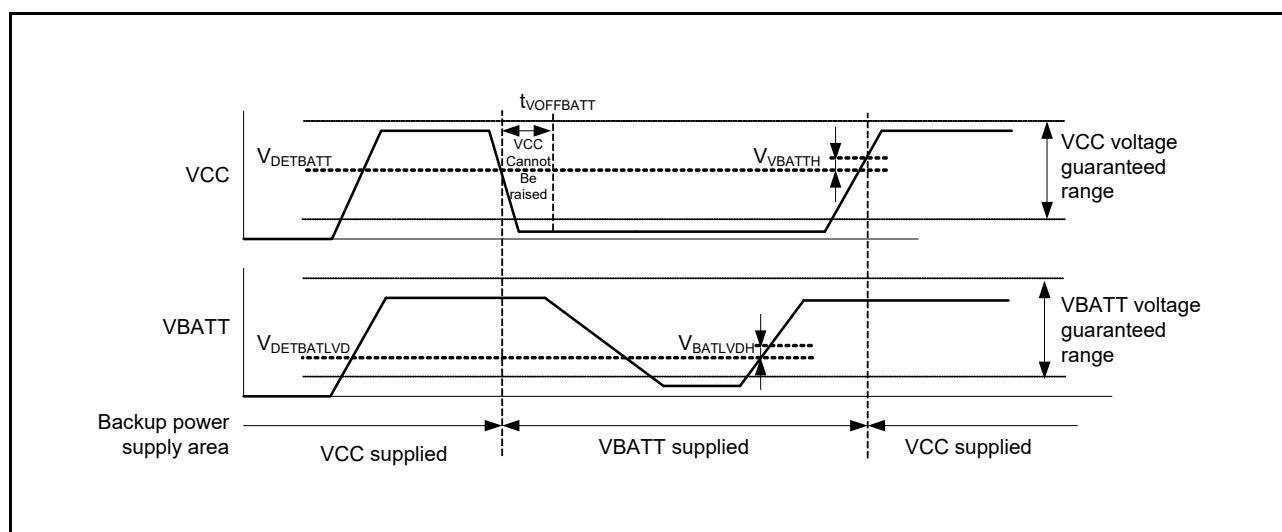
5.12 Battery Backup Function Characteristics

Table 5.61 Battery Backup Function Characteristics

Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} = \text{AVCC0} \leq 5.5\text{ V}$, $1.8\text{ V} \leq \text{VBATT} \leq 5.5\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VREFL0} = \text{VSS_USB} = 0\text{ V}$,
 $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage level for switching to battery backup (falling)		V _{DETBATT}	1.99	2.09	2.19	V	Figure 5.79
Hysteresis width		V _{VBATTH}	—	100	—	mV	
VCC-off period for starting power supply switching		t _{VOFFBATT}	—	—	350	μs	
Allowable voltage change rising/falling gradient		dt/dVCC	1.0	—	—	ms/V	Figure 5.7
Level for detection of voltage drop on the VBATT pin (falling)	VBTLVDLVL[1:0] = 10b	V _{DETBATLVD}	2.11	2.20	2.29	V	Figure 5.79
	VBTLVDLVL[1:0] = 11b		1.87	2.00	2.13	V	
Hysteresis width for detection of voltage drop on the VBATT pin		V _{BATLVDH}	—	50	—	mV	

Note: The VCC-off period for starting power supply switching indicates the period in which VCC is below the minimum value of the voltage level for switching to battery backup (V_{DETBATT}).

**Figure 5.79 Battery Backup Function Characteristics**

5.15 Usage Notes

5.15.1 Connecting VCL Capacitor and Bypass Capacitors

This MCU integrates an internal voltage-down circuit, which is used for lowering the power supply voltage in the internal MCU automatically to the optimum level. A 4.7- μ F capacitor needs to be connected between this internal voltage-down power supply (VCL pin) and the VSS pin. Figure 5.80 to Figure 5.82 shows how to connect external capacitors. Place an external capacitor close to the pins. Do not apply the power supply voltage to the VCL pin.

Insert a multilayer ceramic capacitor as a bypass capacitor between each pair of the power supply pins. Implement a bypass capacitor as closer to the MCU power supply pins as possible. Use a recommended value of 0.1 μ F as the capacitance of the capacitors. For the capacitors related to crystal oscillation, see section 9, Clock Generation Circuit in the User's Manual: Hardware. For the capacitors related to analog modules, also see section 43, 12-Bit A/D Converter (S12ADE) in the User's Manual: Hardware.

For notes on designing the printed circuit board, see the descriptions of the application note, the Hardware Design Guide (R01AN1411EJ). The latest version can be downloaded from the Renesas Electronics website.

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
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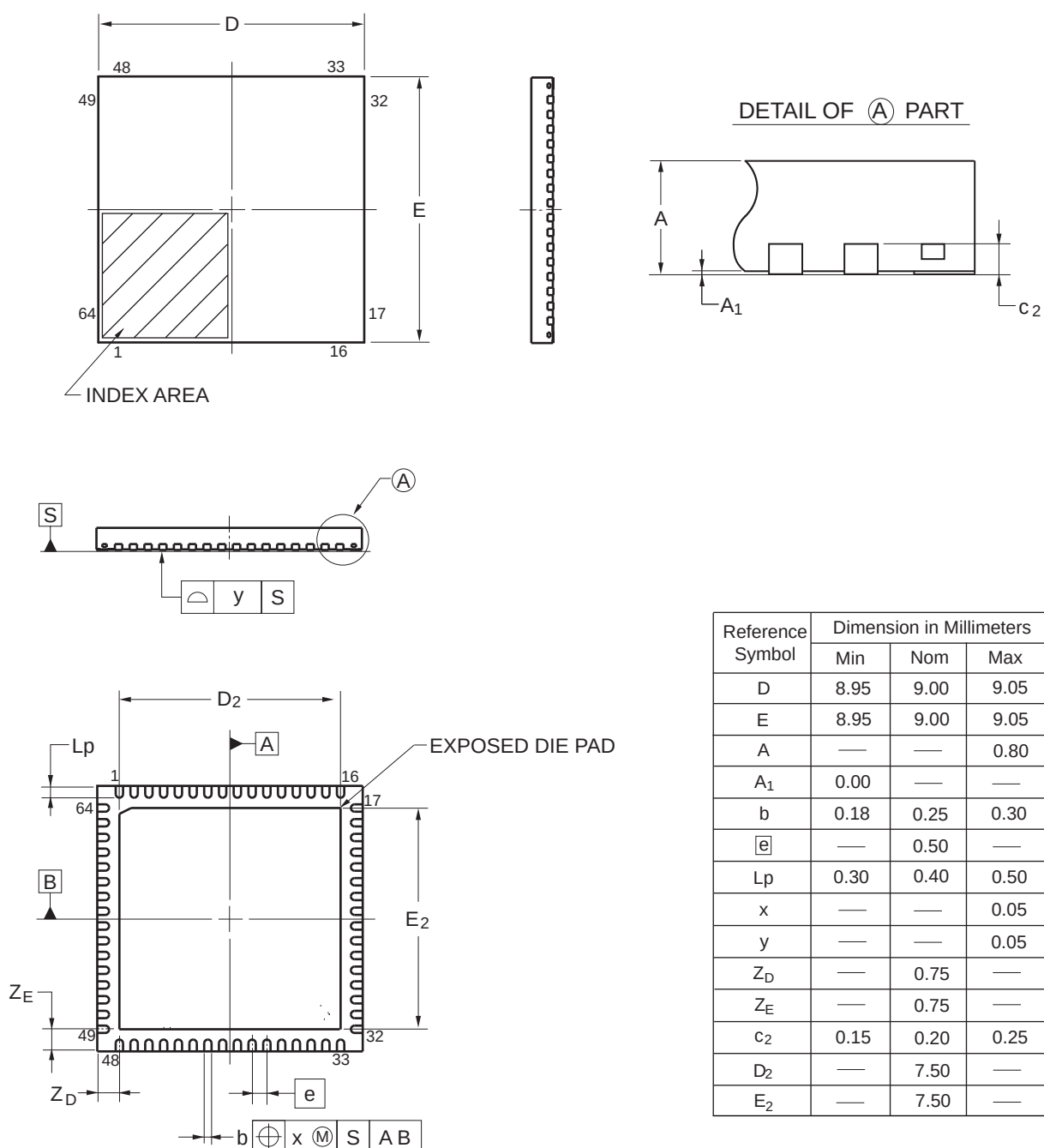


Figure D 64-Pin HWQFN (PWQN0064KC-A)

NOTES FOR CMOS DEVICES

- (1) **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN:** Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).
- (2) **HANDLING OF UNUSED INPUT PINS:** Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
- (3) **PRECAUTION AGAINST ESD:** A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.
- (4) **STATUS BEFORE INITIALIZATION:** Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.
- (5) **POWER ON/OFF SEQUENCE:** In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.
- (6) **INPUT OF SIGNAL DURING POWER OFF STATE :** Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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