Renesas Electronics America Inc - R5F52318ADFM#30 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	54MHz
Connectivity	CANbus, I²C, IrDA, SCI, SD/SDIO, SPI, SSI, USB OTG
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	43
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f52318adfm-30

1.2 List of Products

Table 1.3 and Table 1.4 are a list of products, and Figure 1.1 shows how to read the product part no., memory capacity, and package type.

Table 1.3 List of Products: D Version (T_a = –40 to +85°C) (1/2)

Group	Part No.	Order Part No.	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency	Security Function	SDHI	CAN	Operating Temperature
RX231	R5F52318ADLA	R5F52318ADLA#20	PTLG0100KA-A	512 Kbytes	64 Kbytes	8 Kbytes	54 MHz	Not available	Not available	Available	–40 to +85°C
	R5F52318BDLA	R5F52318BDLA#20						Available	Available	Available	
	R5F52318ADFP	R5F52318ADFP#30	PLQP0100KB-B					Not available	Not available	Available	
	R5F52318BDFP	R5F52318BDFP#30						Available	Available	Available	
	R5F52318ADND	R5F52318ADND#U0	PWQN0064KC-A					Not available	Not available	Available	
	R5F52318BDND	R5F52318BDND#U0						Available	Available	Available	
	R5F52318ADFM	R5F52318ADFM#30	PLQP0064KB-C					Not available	Not available	Available	
	R5F52318BDFM	R5F52318BDFM#30						Available	Available	Available	
	R5F52318ADNE	R5F52318ADNE#U0	PWQN0048KB-A					Not available	Not available	Available	
	R5F52318BDNE	R5F52318BDNE#U0						Available	Not available	Available	
	R5F52318ADFL	R5F52318ADFL#30	PLQP0048KB-B					Not available	Not available	Available	
	R5F52318BDFL	R5F52318BDFL#30						Available	Not available	Available	
	R5F52317ADLA	R5F52317ADLA#20	PTLG0100KA-A	384 Kbytes				Not available	Not available	Available	
	R5F52317BDLA	R5F52317BDLA#20						Available	Available	Available	
	R5F52317ADFP	R5F52317ADFP#30	PLQP0100KB-B					Not available	Not available	Available	
	R5F52317BDFP	R5F52317BDFP#30						Available	Available	Available	
	R5F52317ADND	R5F52317ADND#U0	PWQN0064KC-A					Not available	Not available	Available	
	R5F52317BDND	R5F52317BDND#U0						Available	Available	Available	
	R5F52317ADFM	R5F52317ADFM#30	PLQP0064KB-C					Not available	Not available	Available	
	R5F52317BDFM	R5F52317BDFM#30						Available	Available	Available	
	R5F52317ADNE	R5F52317ADNE#U0	PWQN0048KB-A					Not available	Not available	Available	
	R5F52317BDNE	R5F52317BDNE#U0						Available	Not available	Available	
	R5F52317ADFL	R5F52317ADFL#30	PLQP0048KB-B					Not available	Not available	Available	
	R5F52317BDFL	R5F52317BDFL#30						Available	Not available	Available	
	R5F52316ADLA	R5F52316ADLA#20	PTLG0100KA-A	256 Kbytes	32 Kbytes			Not available	Not available	Available	
	R5F52316CDLA	R5F52316CDLA#20						Not available	Not available	Not available	
	R5F52316ADFP	R5F52316ADFP#30	PLQP0100KB-B					Not available	Not available	Available	
	R5F52316CDFP	R5F52316CDFP#30						Not available	Not available	Not available	
	R5F52316CDLF	R5F52316CDLF#U0	PWLG0064KA-A					Not available	Not available	Not available	
	R5F52316ADND	R5F52316ADND#U0	PWQN0064KC-A					Not available	Not available	Available	
	R5F52316CDND	R5F52316CDND#U0						Not available	Not available	Not available	
	R5F52316ADFM	R5F52316ADFM#30	PLQP0064KB-C					Not available	Not available	Available	
	R5F52316CDFM	R5F52316CDFM#30						Not available	Not available	Not available	
	R5F52316ADNE	R5F52316ADNE#U0	PWQN0048KB-A					Not available	Not available	Available	
	R5F52316CDNE	R5F52316CDNE#U0						Not available	Not available	Not available	

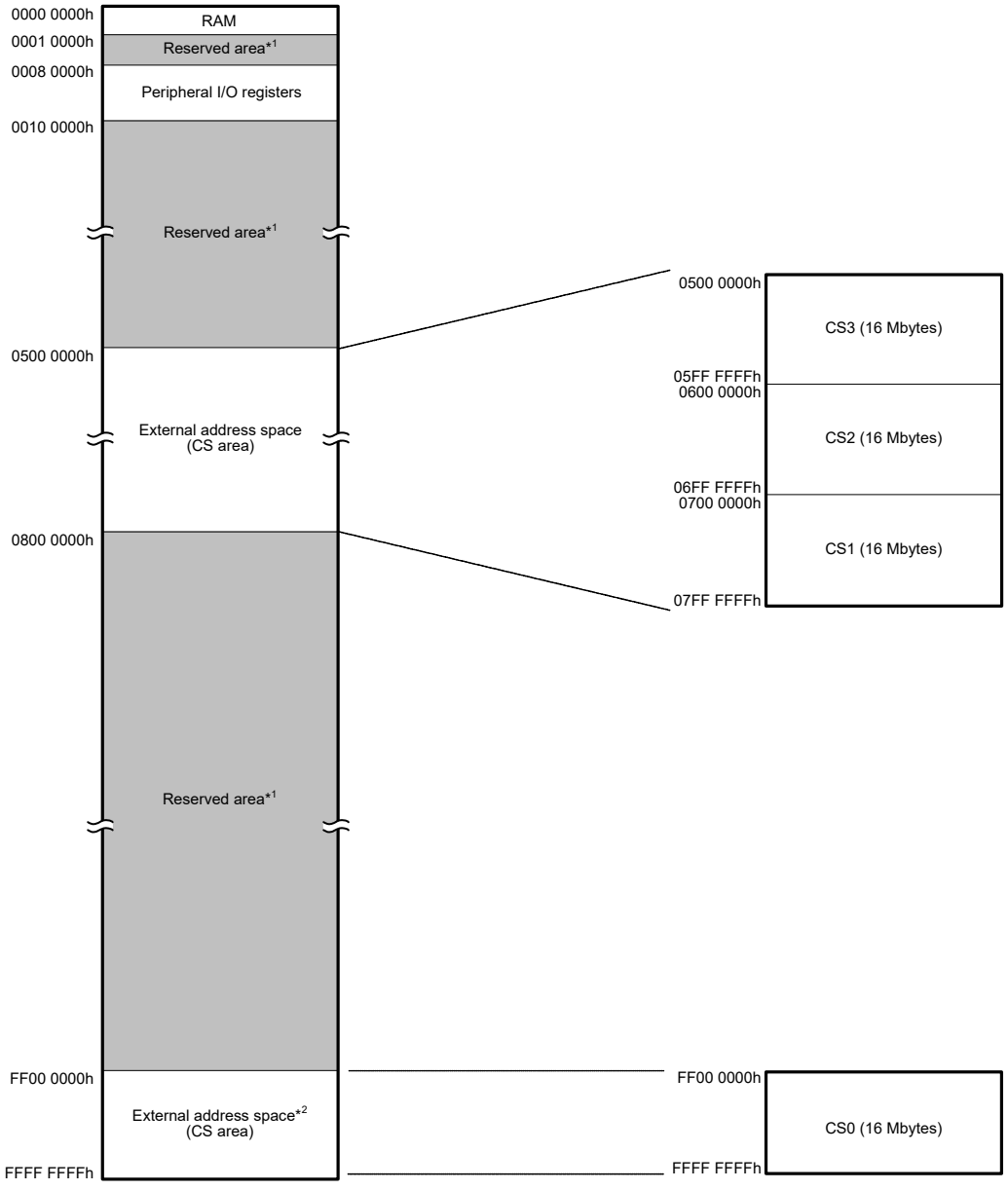
Table 1.10 List of Pins and Pin Functions (48-Pin LFQFP/HWQFN) (2/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCI, RSPI, RIIC, RSCAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
42		P42					AN002
43		P41					AN001
44	VREFL0						
45		P40					AN000
46	VREFH0						
47	AVCC0						
48	AVSS0						

Note 1. RX230: PH0/CACREF, PH1/IRQ0/TMO0, PH2/IRQ1/TMRI0, PH3/TMCI0
RX231: VSS_USB, USB0_DP, USB0_DM, VCC_USB

3.2 External Address Space

The external address space is divided into up to four CS areas (CS0 to CS3), each corresponding to the CSn# signal output from a CSn# (n = 0 to 3) pin. Figure 3.2 shows the address ranges corresponding to the individual CS areas (CS0 to CS3) in on-chip ROM disabled extended mode.



Note 1. Reserved areas should not be accessed.
Note 2. The CS0 area is disabled in on-chip ROM enabled extended mode.
In this mode, the address space for addresses above 1000 0000h is as shown in figure on this section, Memory Map in Each Operating Mode.

Figure 3.2 Correspondence between External Address Spaces and CS Areas (In On-Chip ROM Disabled Extended Mode)

Table 4.1 List of I/O Registers (Address Order) (10/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK <PCLK
0008 A012h	SCI0	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A020h	SCI1	Serial Mode Register	SMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A021h	SCI1	Bit Rate Register	BRR	8	8	2 or 3 PCLKB	2 ICLK
0008 A022h	SCI1	Serial Control Register	SCR	8	8	2 or 3 PCLKB	2 ICLK
0008 A023h	SCI1	Transmit Data Register	TDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A024h	SCI1	Serial Status Register	SSR	8	8	2 or 3 PCLKB	2 ICLK
0008 A025h	SCI1	Receive Data Register	RDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A026h	SCI1	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A027h	SCI1	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A028h	SCI1	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB	2 ICLK
0008 A029h	SCI1	I^2C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB	2 ICLK
0008 A02Ah	SCI1	I^2C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB	2 ICLK
0008 A02Bh	SCI1	I^2C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB	2 ICLK
0008 A02Ch	SCI1	I^2C Status Register	SISR	8	8	2 or 3 PCLKB	2 ICLK
0008 A02Dh	SCI1	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A02Eh	SCI1	Transmit Data Register HL	TDRHL	16	16	4 or 5 PCLKB	2 ICLK
0008 A02Eh	SCI1	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB	2 ICLK
0008 A02Fh	SCI1	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB	2 ICLK
0008 A030h	SCI1	Receive Data Register HL	RDRHL	16	16	4 or 5 PCLKB	2 ICLK
0008 A030h	SCI1	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB	2 ICLK
0008 A031h	SCI1	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB	2 ICLK
0008 A032h	SCI1	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0A0h	SCI5	Serial Mode Register	SMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0A1h	SCI5	Bit Rate Register	BRR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0A2h	SCI5	Serial Control Register	SCR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0A3h	SCI5	Transmit Data Register	TDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0A4h	SCI5	Serial Status Register	SSR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0A5h	SCI5	Receive Data Register	RDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0A6h	SCI5	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0A7h	SCI5	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0A8h	SCI5	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0A9h	SCI5	I^2C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB	2 ICLK
0008 A0AAh	SCI5	I^2C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB	2 ICLK
0008 A0ABh	SCI5	I^2C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB	2 ICLK
0008 A0ACh	SCI5	I^2C Status Register	SISR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0ADh	SCI5	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0AEh	SCI5	Transmit Data Register HL	TDRHL	16	16	4 or 5 PCLKB	2 ICLK
0008 A0AEh	SCI5	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB	2 ICLK
0008 A0AFh	SCI5	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB	2 ICLK
0008 A0B0h	SCI5	Receive Data Register HL	RDRHL	16	16	4 or 5 PCLKB	2 ICLK
0008 A0B0h	SCI5	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB	2 ICLK
0008 A0B1h	SCI5	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB	2 ICLK
0008 A0B2h	SCI5	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0C0h	SCI6	Serial Mode Register	SMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0C1h	SCI6	Bit Rate Register	BRR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0C2h	SCI6	Serial Control Register	SCR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0C3h	SCI6	Transmit Data Register	TDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0C4h	SCI6	Serial Status Register	SSR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0C5h	SCI6	Receive Data Register	RDR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0C6h	SCI6	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0C7h	SCI6	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB	2 ICLK
0008 A0C8h	SCI6	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (32/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK <PCLK
000D 0A34h	MTU	Timer Dead Time Enable Register	TDER	8	8	2 or 3 PCLKA	2 ICLK
000D 0A36h	MTU	Timer Output Level Buffer Register	TOLBR	8	8	2 or 3 PCLKA	2 ICLK
000D 0A38h	MTU3	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	2 or 3 PCLKA	2 ICLK
000D 0A39h	MTU4	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	2 or 3 PCLKA	2 ICLK
000D 0A40h	MTU4	Timer A/D Converter Start Request Control Register	TADCR	16	16	2 or 3 PCLKA	2 ICLK
000D 0A44h	MTU4	Timer A/D Converter Start Request Cycle Set Register A	TADCORA	16	16	2 or 3 PCLKA	2 ICLK
000D 0A46h	MTU4	Timer A/D Converter Start Request Cycle Set Register B	TADCORB	16	16	2 or 3 PCLKA	2 ICLK
000D 0A48h	MTU4	Timer A/D Converter Start Request Cycle Set Buffer Register A	TADCOBRA	16	16	2 or 3 PCLKA	2 ICLK
000D 0A4Ah	MTU4	Timer A/D Converter Start Request Cycle Set Buffer Register B	TADCOBRB	16	16	2 or 3 PCLKA	2 ICLK
000D 0A60h	MTU	Timer Waveform Control Register	TWCR	8	8, 16	2 or 3 PCLKA	2 ICLK
000D 0A80h	MTU	Timer Start Register	TSTR	8	8, 16	2 or 3 PCLKA	2 ICLK
000D 0A81h	MTU	Timer Synchronous Register	TSYR	8	8, 16	2 or 3 PCLKA	2 ICLK
000D 0A84h	MTU	Timer Read/Write Enable Register	TRWER	8	8, 16	2 or 3 PCLKA	2 ICLK
000D 0A90h	MTU0	Noise Filter Control Register	NFCR	8	8, 16	2 or 3 PCLKA	2 ICLK
000D 0A91h	MTU1	Noise Filter Control Register	NFCR	8	8, 16	2 or 3 PCLKA	2 ICLK
000D 0A92h	MTU2	Noise Filter Control Register	NFCR	8	8, 16	2 or 3 PCLKA	2 ICLK
000D 0A93h	MTU3	Noise Filter Control Register	NFCR	8	8, 16	2 or 3 PCLKA	2 ICLK
000D 0A94h	MTU4	Noise Filter Control Register	NFCR	8	8, 16	2 or 3 PCLKA	2 ICLK
000D 0A95h	MTU5	Noise Filter Control Register	NFCR	8	8, 16	2 or 3 PCLKA	2 ICLK
000D 0B00h	MTU0	Timer Control Register	TCR	8	8	2 or 3 PCLKA	2 ICLK
000D 0B01h	MTU0	Timer Mode Register	TMDR	8	8	2 or 3 PCLKA	2 ICLK
000D 0B02h	MTU0	Timer I/O Control Register H	TIORH	8	8	2 or 3 PCLKA	2 ICLK
000D 0B03h	MTU0	Timer I/O Control Register L	TIORL	8	8	2 or 3 PCLKA	2 ICLK
000D 0B04h	MTU0	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKA	2 ICLK
000D 0B05h	MTU0	Timer Status Register	TSR	8	8	2 or 3 PCLKA	2 ICLK
000D 0B06h	MTU0	Timer Counter	TCNT	16	16	2 or 3 PCLKA	2 ICLK
000D 0B08h	MTU0	Timer General Register A	TGRA	16	16	2 or 3 PCLKA	2 ICLK
000D 0B0Ah	MTU0	Timer General Register B	TGRB	16	16	2 or 3 PCLKA	2 ICLK
000D 0B0Ch	MTU0	Timer General Register C	TGRC	16	16	2 or 3 PCLKA	2 ICLK
000D 0B0Eh	MTU0	Timer General Register D	TGRD	16	16	2 or 3 PCLKA	2 ICLK
000D 0B20h	MTU0	Timer General Register E	TGRE	16	16	2 or 3 PCLKA	2 ICLK
000D 0B22h	MTU0	Timer General Register F	TGRF	16	16	2 or 3 PCLKA	2 ICLK
000D 0B24h	MTU0	Timer Interrupt Enable Register 2	TIER2	8	8	2 or 3 PCLKA	2 ICLK
000D 0B26h	MTU0	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	2 or 3 PCLKA	2 ICLK
000D 0B80h	MTU1	Timer Control Register	TCR	8	8	2 or 3 PCLKA	2 ICLK
000D 0B81h	MTU1	Timer Mode Register	TMDR	8	8	2 or 3 PCLKA	2 ICLK
000D 0B82h	MTU1	Timer I/O Control Register	TIOR	8	8	2 or 3 PCLKA	2 ICLK
000D 0B84h	MTU1	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKA	2 ICLK
000D 0B85h	MTU1	Timer Status Register	TSR	8	8	2 or 3 PCLKA	2 ICLK
000D 0B86h	MTU1	Timer Counter	TCNT	16	16	2 or 3 PCLKA	2 ICLK
000D 0B88h	MTU1	Timer General Register A	TGRA	16	16	2 or 3 PCLKA	2 ICLK
000D 0B8Ah	MTU1	Timer General Register B	TGRB	16	16	2 or 3 PCLKA	2 ICLK
000D 0B90h	MTU1	Timer Input Capture Control Register	TICCR	8	8	2 or 3 PCLKA	2 ICLK
000D 0C00h	MTU2	Timer Control Register	TCR	8	8	2 or 3 PCLKA	2 ICLK
000D 0C01h	MTU2	Timer Mode Register	TMDR	8	8	2 or 3 PCLKA	2 ICLK
000D 0C02h	MTU2	Timer I/O Control Register	TIOR	8	8	2 or 3 PCLKA	2 ICLK
000D 0C04h	MTU2	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKA	2 ICLK
000D 0C05h	MTU2	Timer Status Register	TSR	8	8	2 or 3 PCLKA	2 ICLK
000D 0C06h	MTU2	Timer Counter	TCNT	16	16	2 or 3 PCLKA	2 ICLK
000D 0C08h	MTU2	Timer General Register A	TGRA	16	16	2 or 3 PCLKA	2 ICLK
000D 0C0Ah	MTU2	Timer General Register B	TGRB	16	16	2 or 3 PCLKA	2 ICLK

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Conditions: VSS = AVSS0 = VREFL0 = VREFL= VSS_USB = 0 V

Item		Symbol	Value	Unit
Power supply voltage		VCC, VCC_USB	–0.3 to +6.5	V
VBATT power supply voltage		Vbatt	–0.3 to +6.5	V
Input voltage	Ports for 5 V tolerant*1	V_{in}	–0.3 to +6.5	V
	P03, P05, P07, P40 to P47		–0.3 to AVCC0 +0.3	
	Ports other than above		–0.3 to VCC +0.3	
Reference power supply voltage		VREFH0	–0.3 to AVCC0 +0.3	V
		VREFH		
Analog power supply voltage		AVCC0	–0.3 to +6.5	V
Analog input voltage	When AN000 to AN007 are used	V_{AN}	–0.3 to AVCC0 +0.3	V
	When AN016 to AN031 are used		–0.3 to VCC +0.3	
Operating temperature*2		T_{opr}	–40 to +85 –40 to +105	°C
Storage temperature		T_{stg}	–55 to +125	°C

Caution: Permanent damage to the MCU may be caused if absolute maximum ratings are exceeded.

To preclude any malfunctions due to noise interference, insert capacitors with high frequency characteristics between the VCC and VSS pins, between the AVCC0 and AVSS0 pins, between the VCC_USB and VSS_USB pins, between the VREFH0 and VREFL0 pins, and between the VREFH and VREFL pins. Place capacitors of about 0.1 µF as close as possible to every power supply pin and use the shortest and heaviest possible traces.

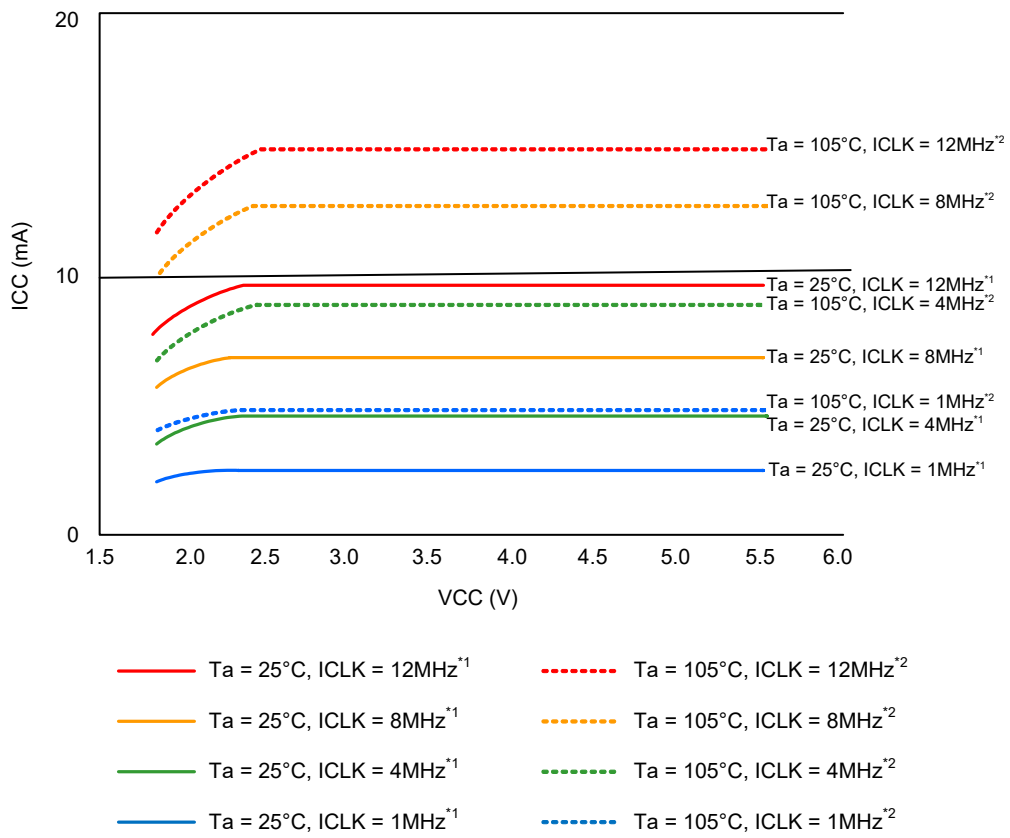
Connect the VCL pin to a VSS pin via a 4.7 µF capacitor. The capacitor must be placed close to the pin. For details, refer to section 5.15.1, Connecting VCL Capacitor and Bypass Capacitors.

Do not input signals or an I/O pull-up power supply to ports other than 5-V tolerant ports while the device is not powered.

The current injection that results from input of such a signal or I/O pull-up may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Even if –0.3 to +6.5 V is input to 5-V tolerant ports, it will not cause problems such as damage to the MCU.

Note 1. Ports 12, 13, 16, 17, 30, 31, 32, and B5 are 5 V tolerant.

Note 2. The upper limit of operating temperature is 85°C or 105°C, depending on the product. For details, refer to section 1.2, List of Products.



Note 1. All peripheral operations except any BGO operation are operating normally. Indicates the average of the typical samples through actual measurement during product evaluation.
Note 2. All peripheral operations except any BGO operation are operating at maximum. Indicates the average of the upper-limit samples through actual measurement during product evaluation.

Figure 5.2 Voltage Dependency in Middle-Speed Operating Mode (Reference Data)

Table 5.16 Permissible Output Currents (1)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +85°C

Item			Symbol	Max.	Unit
Permissible output low current (average value per pin)	Ports 40 to 47, ports 03, 05, 07, port 36, 37		I_{OL}	4.0	mA
	Ports other than above	Normal output mode		4.0	
		High-drive output mode		8.0	
Permissible output low current (maximum value per pin)	Ports 40 to 47, ports 03, 05, 07, ports 36, 37			4.0	
	Ports other than above	Normal output mode		4.0	
		High-drive output mode		8.0	
Permissible output low current	Total of ports 40 to 47, ports 03, 05, 07		ΣI_{OL}	40	
	Total of ports 12 to 17, ports 20 to 27, ports 30 to 37, port PJ3			40	
	Total of ports 50 to 55, ports C0 to C7, ports B0 to B7			40	
	Total of ports E0 to E7, ports A0 to A7, ports D0 to D4			40	
	Total of all output pins			80	
Permissible output high current (average value per pin)	Ports 40 to 47, ports 03, 05, 07, ports 36, 37		I_{OH}	–4.0	
	Ports other than above	Normal output mode		–4.0	
		High-drive output mode		–8.0	
Permissible output high current (maximum value per pin)	Ports 40 to 47, ports 03, 05, 07, ports 36, 37			–4.0	
	Ports other than above	Normal output mode		–4.0	
		High-drive output mode		–8.0	
Permissible output high current	Total of ports 40 to 47, ports 03, 05, 07		ΣI_{OH}	–40	
	Total of ports 12 to 17, ports 20 to 27, ports 30 to 37, port PJ3			–40	
	Total of ports 50 to 55, ports C0 to C7, ports B0 to B7			–40	
	Total of ports E0 to E7, ports A0 to A7, ports D0 to D4			–40	
	Total of all output pins			–80	

Note: Do not exceed the permissible total supply current.

5.2.1 Normal I/O Pin Output Characteristics (1)

Figure 5.8 to Figure 5.12 show the characteristics when normal output is selected by the drive capacity control register.

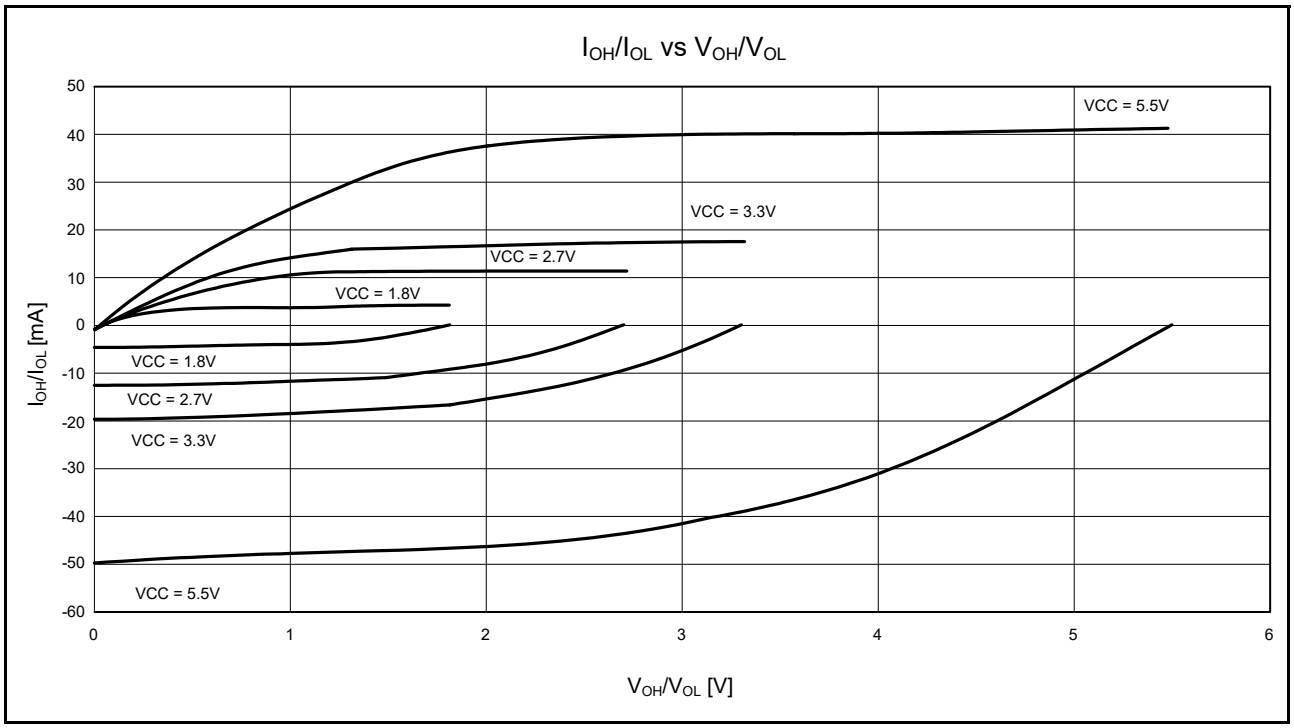


Figure 5.8 V_{OH}/V_{OL} and I_{OH}/I_{OL} Voltage Characteristics at T_a = 25°C When Normal Output is Selected (Reference Data)

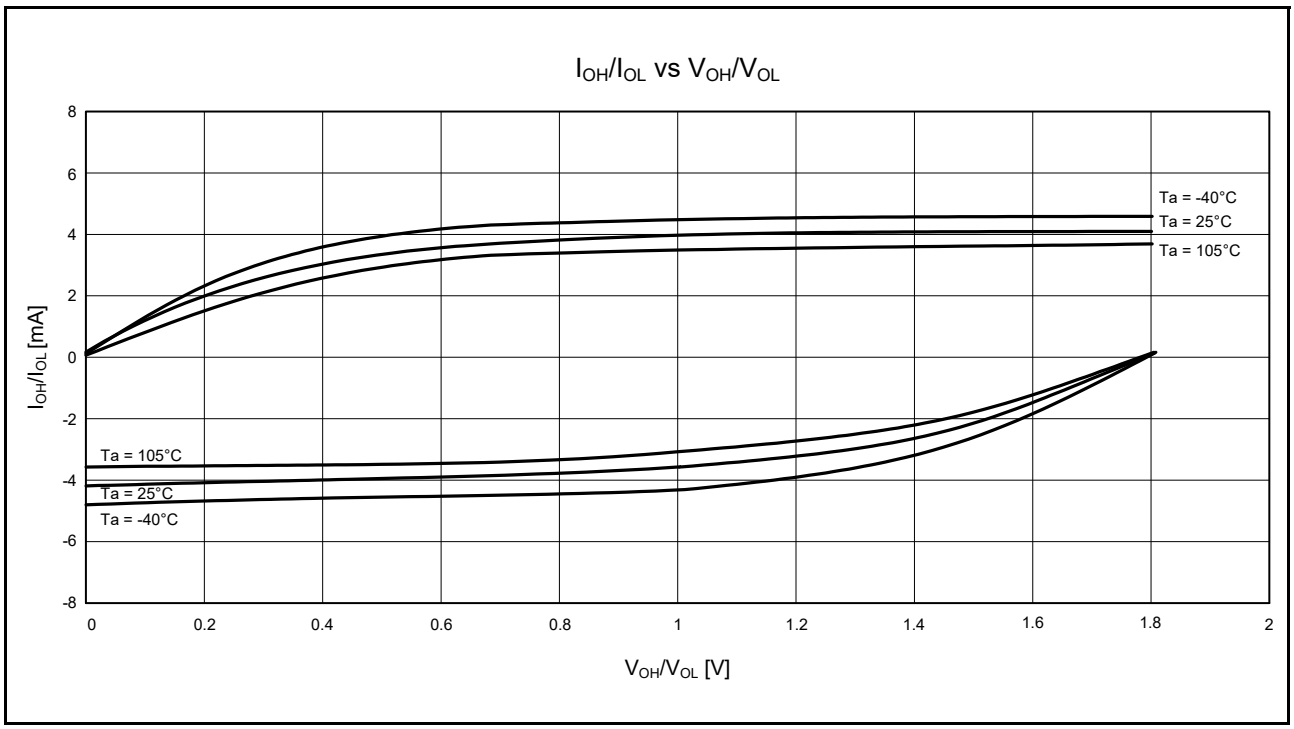


Figure 5.9 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 1.8 V When Normal Output is Selected (Reference Data)

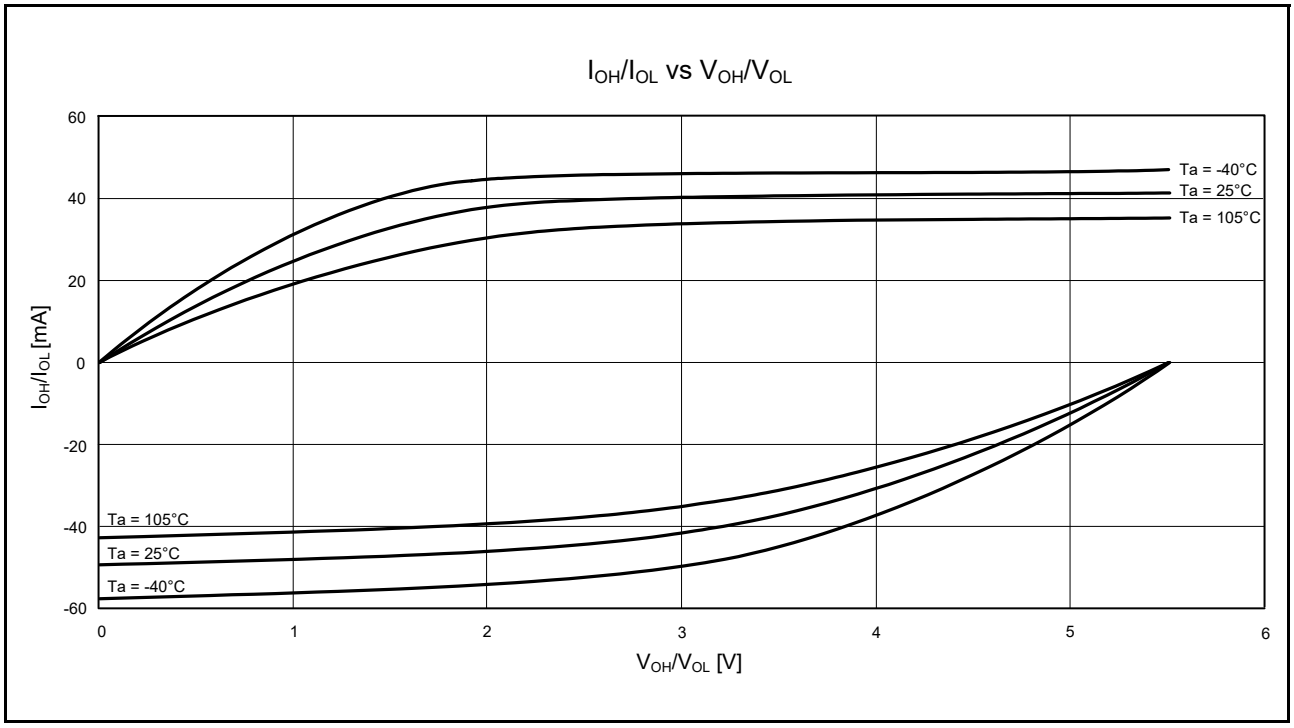


Figure 5.12 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 5.5 V When Normal Output is Selected (Reference Data)

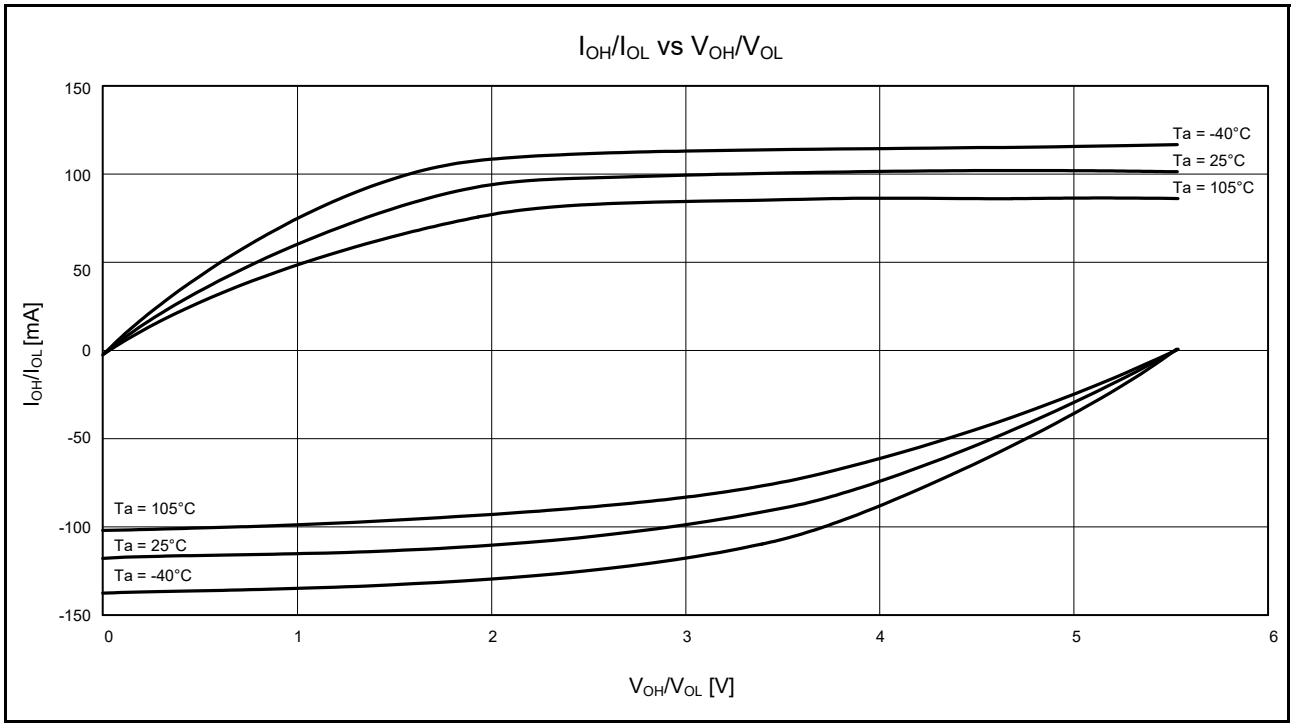


Figure 5.17 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 5.5 V When High-Drive Output is Selected (Reference Data)

5.3.3 Timing of Recovery from Low Power Consumption Modes

Table 5.28 Timing of Recovery from Low Power Consumption Modes (1)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VREFL0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from software standby mode*1	High-speed mode	Crystal connected to main clock oscillator	Main clock oscillator operating*2	t_{SBYMC}	—	2	3	ms	Figure 5.34
		External clock input to main clock oscillator	Main clock oscillator operating*3	t_{SBYEX}	—	35	50	µs	
		Sub-clock oscillator operating		t_{SBYSC}	—	650	800	µs	
		HOCO clock oscillator operating		t_{SBYHO}	—	40	55	µs	
		LOCO clock oscillator operating		t_{SBYLO}	—	40	55	µs	

Note 1. The recovery time varies depending on the state of each oscillator when the WAIT instruction is executed. When multiple oscillators are operating, the recovery time varies depending on the operating state of the oscillators that are not selected as the system clock source. The above table applies when only the corresponding clock is operating.
Note 2. When the frequency of the crystal is 20 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.
Note 3. When the frequency of the external clock is 20 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 00h.

Table 5.29 Timing of Recovery from Low Power Consumption Modes (2)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VREFL0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from software standby mode*1	Middle-speed mode	Crystal connected to main clock oscillator	Main clock oscillator operating*2	t_{SBYMC}	—	2	3	ms	Figure 5.34
			Main clock oscillator and PLL circuit operating*3	t_{SBYPC}	—	2	3	ms	
		External clock input to main clock oscillator	Main clock oscillator operating*4	t_{SBYEX}	—	3	4	µs	
			Main clock oscillator and PLL circuit operating*5	t_{SBYPE}	—	65	85	µs	
		Sub-clock oscillator operating		t_{SBYSC}	—	600	750	µs	
		HOCO clock oscillator operating*6		t_{SBYHO}	—	40	50	µs	
		LOCO clock oscillator operating		t_{SBYLO}	—	5	7	µs	

Note 1. The recovery time varies depending on the state of each oscillator when the WAIT instruction is executed. When multiple oscillators are operating, the recovery time varies depending on the operating state of the oscillators that are not selected as the system clock source. The above table applies when only the corresponding clock is operating.
Note 2. When the frequency of the crystal is 12 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.
Note 3. When the frequency of PLL is 12 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.
Note 4. When the frequency of the external clock is 12 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 00h.
Note 5. When the frequency of PLL is 12 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 00h.
Note 6. This is the case when HOCO is selected as the system clock and its frequency division is set to be 8 MHz.

Table 5.40 Timing of On-Chip Peripheral Modules (3)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)		t_{SPcyc}	4	65536	t_{Pcyc}	Figure 5.54
	SCK clock cycle input (slave)			6	65536	t_{Pcyc}	
	SCK clock high pulse width		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time		t_{SPCKr}, t_{SPCKf}	—	20	ns	
	Data input setup time (master)	2.7 V or above	t_{SU}	65	—	ns	Figure 5.55, Figure 5.56
		1.8 V or above		95	—		
	Data input setup time (slave)			40	—		
	Data input hold time		t_H	40	—	ns	
	SSL input setup time		t_{LEAD}	3	—	t_{SPcyc}	
	SSL input hold time		t_{LAG}	3	—	t_{SPcyc}	
	Data output delay time (master)		t_{OD}	—	40	ns	
	Data output delay time (slave)	2.7 V or above		—	65		
		1.8 V or above		—	100		
	Data output hold time (master)	2.7 V or above	t_{OH}	–10	—	ns	
		1.8 V or above		–20	—		
	Data output hold time (slave)			–10	—		
	Data rise/fall time		t_{Dr}, t_{Df}	—	20	ns	
	SSL input rise/fall time		t_{SSLr}, t_{SSLf}	—	20	ns	
	Slave access time		t_{SA}	—	6	t_{Pcyc}	Figure 5.57, Figure 5.58
	Slave output release time		t_{REL}	—	6	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLK cycle

Table 5.44 Timing of On-Chip Peripheral Modules (7)

Conditions: 2.7 V ≤ VCC = VCC_USB = AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, fPCLKB ≤ 32 MHz,
T_a = –40 to +105°C,
when high-drive output is selected by the drive capacity control register

Item		Symbol	Min.	Max.	Unit	Test Conditions
SDHI	SDHI_CLK pin output cycle time	$t_{PP(SD)}$	62.5	—	ns	Figure 5.64
	SDHI_CLK pin output high pulse width	$t_{WH(SD)}$	18.25	—	ns	
	SDHI_CLK pin output low pulse width	$t_{WL(SD)}$	18.25	—	ns	
	SDHI_CLK pin output rise time	$t_{TLH(SD)}$	—	10	ns	
	SDHI_CLK pin output fall time	$t_{THL(SD)}$	—	10	ns	
	Output data delay time (data transfer mode) for SDHI_CMD and SDHI_D0 to SDHI_D3 pins	$t_{ODLY(SD)}$	–18.25	18.25	ns	
	Input data setup time for SDHI_CMD and SDHI_D0 to SDHI_D3 pins	$t_{ISU(SD)}$	9.25	—	ns	
	Input data hold time for SDHI_CMD and SDHI_D0 to SDHI_D3 pins	$t_{IH(SD)}$	8.3	—	ns	

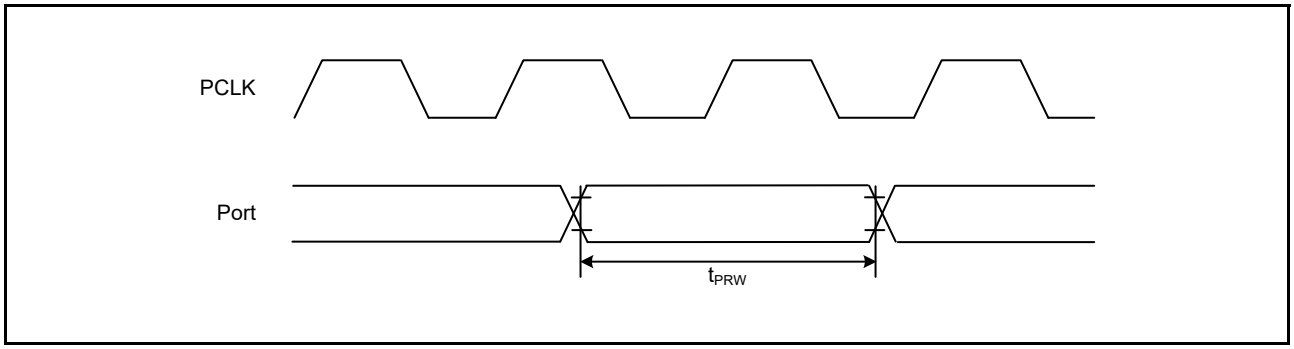


Figure 5.45 I/O Port Input Timing

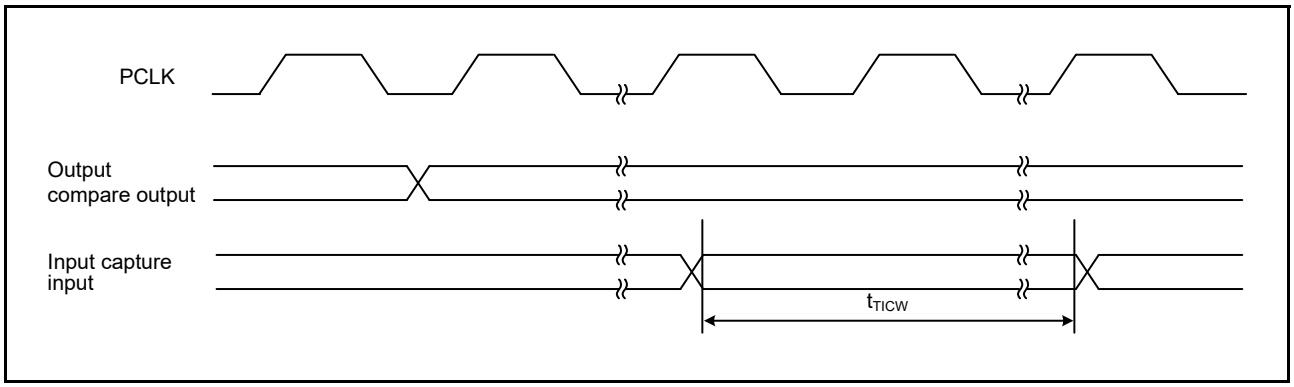


Figure 5.46 MTU2 Input/Output Timing

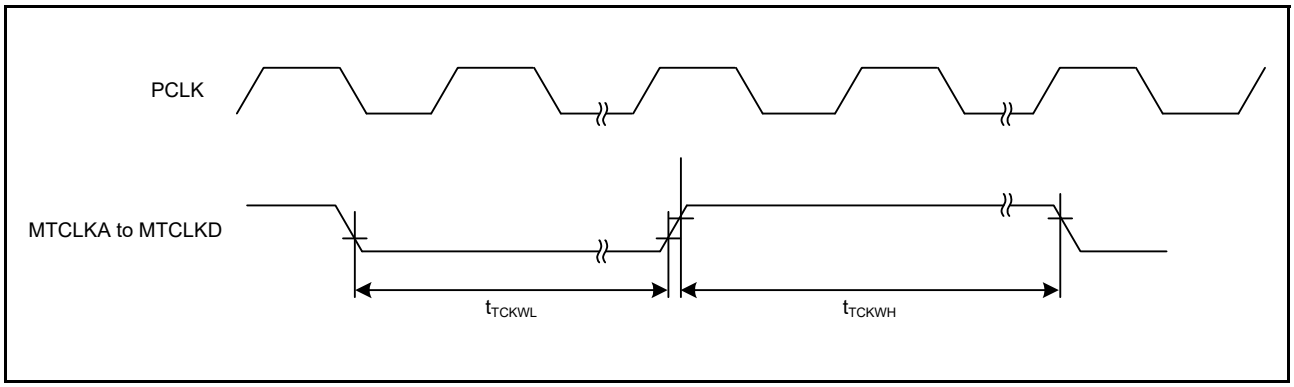


Figure 5.47 MTU2 Clock Input Timing

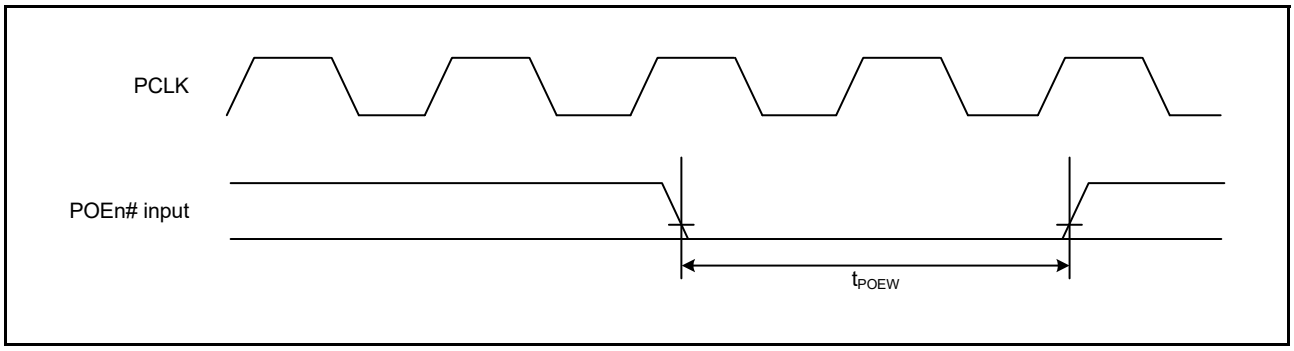


Figure 5.48 POE# Input Timing

Table 5.50 A/D Conversion Characteristics (5)

Conditions: 1.8V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5V, 1.8V ≤ VREFH0 ≤ AVCC0, VSS = AVSS0 = VSS_USB = 0V, reference voltage = VREFH0 selected, Ta = –40 to +105°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	8	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 8 MHz)	Permissible signal source impedance (Max.) = 5 kΩ	6.75	—	—	µs	High-precision channel The ADCSR.ADHSC bit is 1 The ADSSTRn register is 0Dh
		10.13	—	—		Normal-precision channel The ADCSR.ADHSC bit is 1 The ADSSTRn register is 28h
Analog input capacitance	Cs	—	—	15	pF	Pin capacitance included Figure 5.68
Analog input resistance	Rs	—	—	2.5	kΩ	Figure 5.68
Offset error		—	±1	±7.5	LSB	
Full-scale error		—	±1.5	±7.5	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±3.0	±8.0	LSB	
DNL differential non-linearity error		—	±1.0	—	LSB	
INL integral non-linearity error		—	±1.25	±3.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential non-linearity error, and INL integral non-linearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 5.51 A/D Converter Channel Classification

Classification	Channel	Conditions	Remarks
High-precision channel	AN000 to AN007	AVCC0 = 1.8 to 5.5 V	Pins AN000 to AN007 cannot be used as digital outputs when the A/D converter is in use.
Normal-precision channel	AN016 to AN031		
Internal reference voltage input channel	Internal reference voltage	AVCC0 = 2.0 to 5.5 V	
Temperature sensor input channel	Temperature sensor output	AVCC0 = 2.0 to 5.5 V	

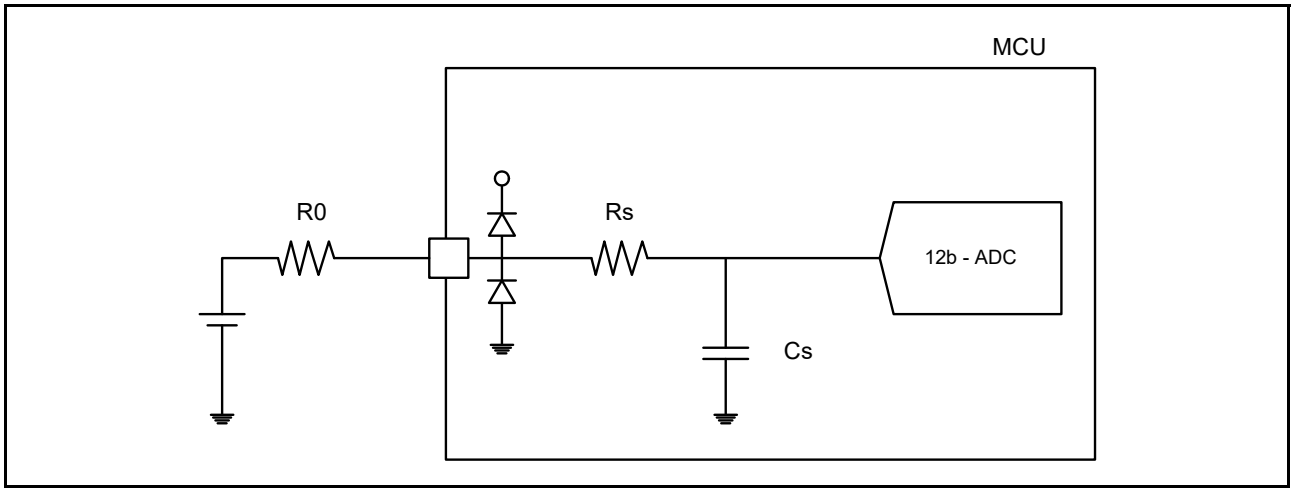


Figure 5.68 Equivalent Circuit

Differential non-linearity error (DNL)

The differential non-linearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

Offset error

An offset error is the difference between a transition point of the ideal first output code and the actual first output code.

Full-scale error

A full-scale error is the difference between a transition point of the ideal last output code and the actual last output code.

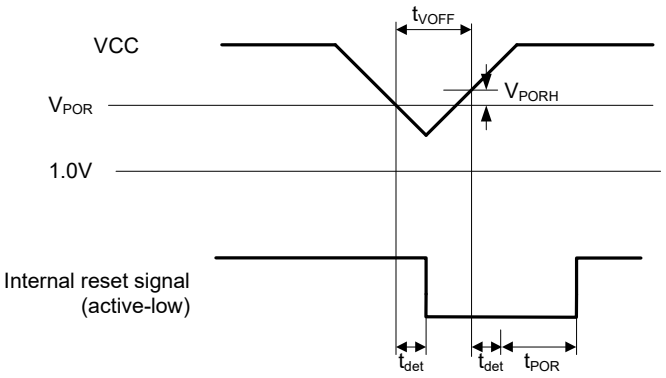
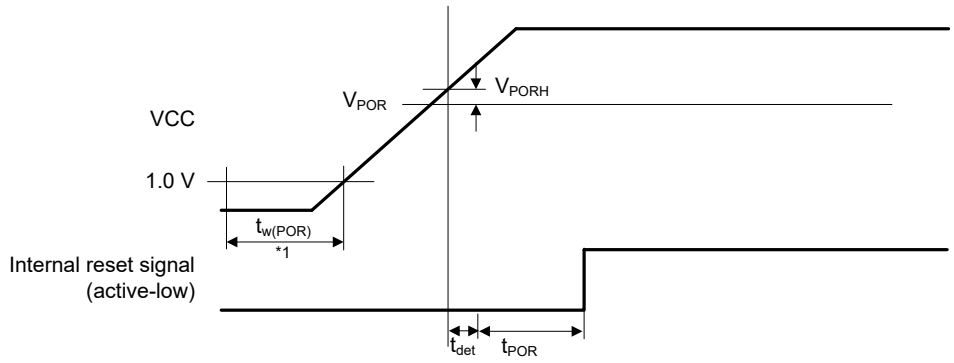


Figure 5.73 Voltage Detection Reset Timing



Note 1. $t_{w(POR)}$ is the time required for a power-on reset to be enabled while the external power VCC is being held below the valid voltage (1.0 V).
When turning the VCC on, maintain a voltage below 1.0V for at least 1.0ms.

Figure 5.74 Power-On Reset Timing

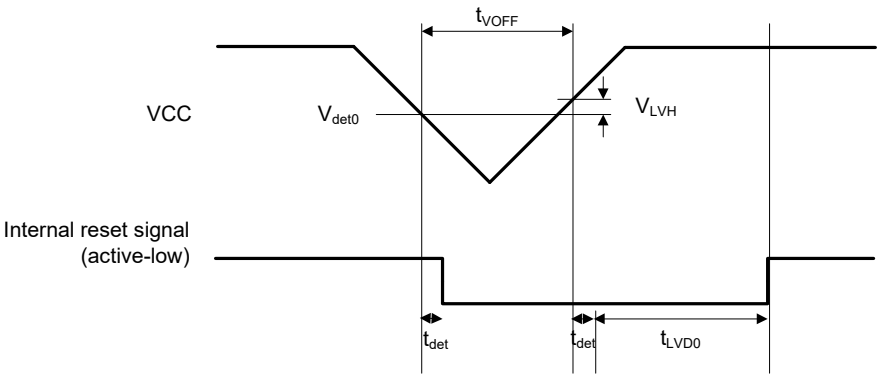
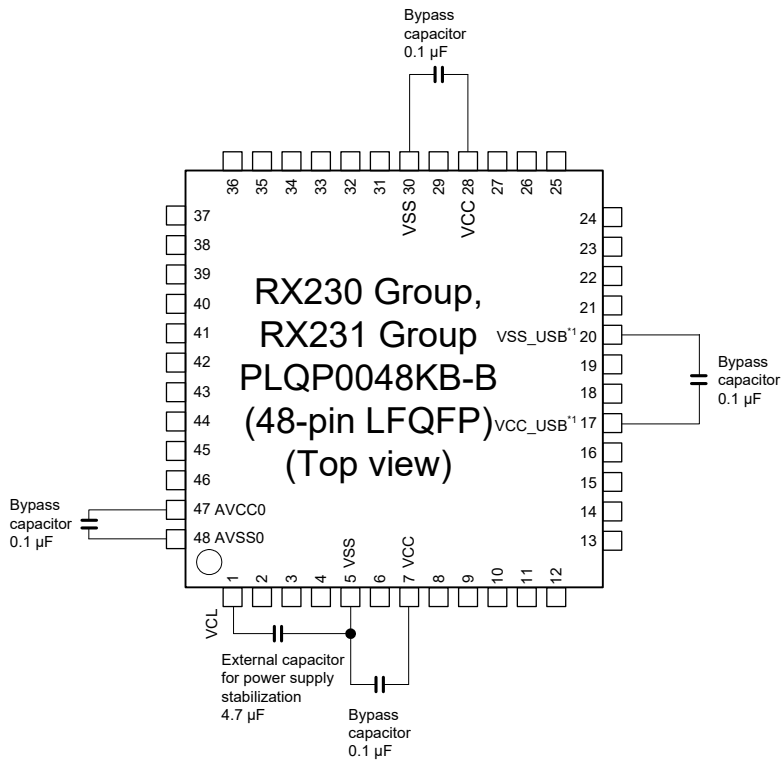


Figure 5.75 Voltage Detection Circuit Timing (Vdet0)



Note: Do not apply the power supply voltage to the VCL pin.
Use a 4.7-µF multilayer ceramic capacitor for the VCL pin and place it close to the pin.
A recommended value is shown for the capacitance of the bypass capacitors.

Note 1. As the products of the RX230 group do not have VCC_USB or VSS_USB, a bypass capacitor is not required.

Figure 5.82 Connecting Capacitors (48 Pins)

Rev.	Date	Description		Classification
		Page	Summary	
1.10	Oct 30, 2015	142	Table 5.45 A/D Conversion Characteristics (1): Conditions and Voltage Range of Analog Input (Max.), changed	
		143	Table 5.46 A/D Conversion Characteristics (2): Conditions changed	
		144	Table 5.47 A/D Conversion Characteristics (3): Conditions changed	
		145	Table 5.48 A/D Conversion Characteristics (4): Conditions changed	
		146	Table 5.49 A/D Conversion Characteristics (5): Conditions changed and Absolute accuracy (Test Conditions) deleted	
		153	Table 5.57 Characteristics of Power-On Reset Circuit and Voltage Detection Circuit (1), changed	TN-RX*-A137A/E
		154	Table 5.58 Characteristics of Power-On Reset Circuit and Voltage Detection Circuit (2), changed	
		155	Figure 5.73 Power-On Reset Timing and Figure 5.74 Voltage Detection Circuit Timing (Vdet0), changed	
		159	Table 5.62 ROM (Flash Memory for Code Storage) Characteristics (2) High-Speed Operating Mode: Note changed	
		160	Table 5.63 ROM (Flash Memory for Code Storage) Characteristics (3) Middle-Speed Operating Mode: Note changed	
		161	Table 5.65 E2 DataFlash Characteristics (2): high-speed operating mode, Note changed	
		161	Table 5.66 E2 DataFlash Characteristics (3): middle-speed operating mode, Conditions and Note changed	
		163	Figure 5.79 Connecting Capacitors (100 Pins), changed	
		164	Figure 5.80 Connecting Capacitors (64 Pins), changed	
		165	Figure 5.81 Connecting Capacitors (48 Pins), changed	
		Appendix 1. Package Dimensions		
		167	Figure B 100 -Pin LQFP (PLQP0100KB-B), changed	TN-RX*-A137A/E
		170	Figure E 64 -Pin LQFP (PLQP0064KB-C), changed	TN-RX*-A137A/E
		172	Figure G 48 -Pin LQFP (PLQP0048KB-B), changed	TN-RX*-A137A/E
1.20	Sep 28, 2018	Features		
		1	SD host interface (optional: one channel) SD memory/ SDIO 1-bit or 4-bit SD bus supported, Note deleted	TN-RX*-A145A/E
		1. Overview		
		6	Table 1.2 Comparison of Functions for Different Packages, changed (deletion of IRQ2 on 64-pin package)	
		6	Table 1.2 Comparison of Functions for Different Packages, Note 1 added	TN-RX*-A145A/E
		7	Table 1.3 List of Products: D Version (Ta = –40 to +85°C) (1/2), changed	TN-RX*-A145A/E
		9	Table 1.4 List of Products: G Version (Ta = –40 to +105°C) (1/2), changed	TN-RX*-A145A/E
		11	Figure 1.1 How to Read the Product Part Number, changed	TN-RX*-A145A/E
		16	Table 1.5 Pin Functions (4/4), changed (changes in description for VCC_USB)	TN-RX*-A201A/E
		24	Table 1.6 List of Pins and Pin Functions (100-Pin TFLGA) (2/3), changed (UPSEL was added to the column of P35)	
		24	Table 1.6 List of Pins and Pin Functions (100-Pin TFLGA) (2/3), changed (USB0_VBUS was added to the column of PB5)	
		26	Table 1.7 List of Pins and Pin Functions (100-Pin LFQFP) (1/3), changed (UPSEL was added to the column of P35)	
		29	Table 1.8 List of Pins and Pin Functions (64-Pin WFLGA) (1/2), changed (UPSEL was added to the column of P35)	
		30	Table 1.8 List of Pins and Pin Functions (64-Pin WFLGA) (2/2), changed (USB0_VBUS was added to the column of PB5)	
		31	Table 1.9 List of Pins and Pin Functions (64-Pin LFQFP/HWQFN) (1/2), changed (UPSEL was added to the column of P35)	
		31	Table 1.9 List of Pins and Pin Functions (64-Pin LQFP/HWQFN) (1/2), changed (USB0_VBUS was added to the column of PB5)	
		33	Table 1.10 List of Pins and Pin Functions (48-Pin LFQFP/HWQFN) (1/2), changed (UPSEL was added to the column of P35)	
		33	Table 1.10 List of Pins and Pin Functions (48-Pin LFQFP/HWQFN) (1/2), changed	TN-RX*-A145A/E
		5. Electrical Characteristics		
		92	Table 5.18 Output Values of Voltage (1), changed	TN-RX*-A201A/E
		92	Table 5.19 Output Values of Voltage (2), changed	TN-RX*-A201A/E