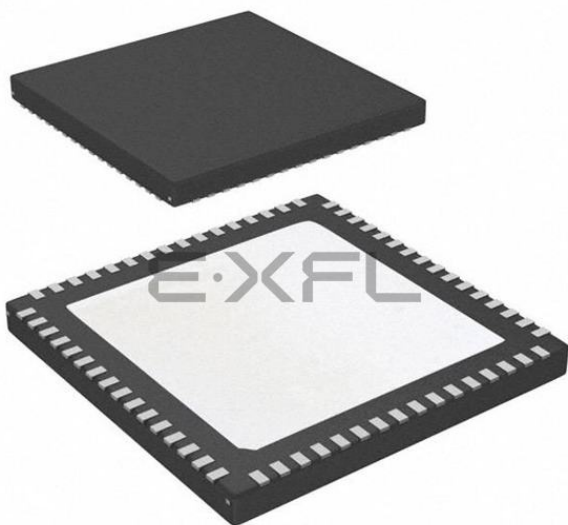




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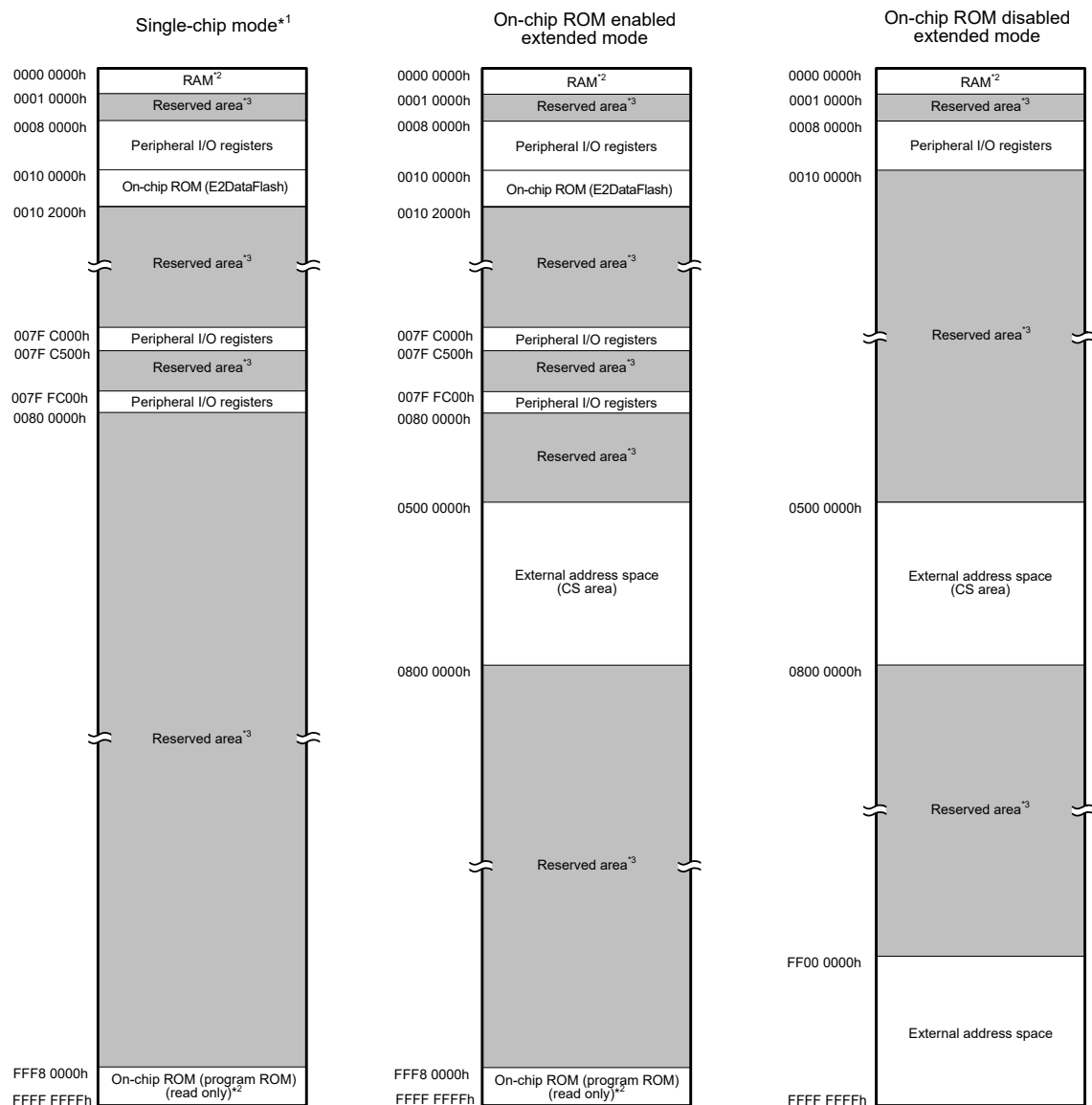
What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	54MHz
Connectivity	CANbus, I ² C, IrDA, SCI, SD/SDIO, SPI, SSI, USB OTG
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	43
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-WFQFN Exposed Pad
Supplier Device Package	64-HWQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f52318adnd-u0



Note 1. The address space in boot mode and USB boot mode is the same as the address space in single-chip mode.

Note 2. The capacity of ROM/RAM differs depending on the products.

ROM (bytes)		RAM (bytes)	
Capacity	Address	Capacity	Address
512 Kbytes	FFF8 0000h to FFFF FFFFh	64 Kbytes	0000 0000h to 0000 FFFFh
384 Kbytes	FFFA 0000h to FFFF FFFFh		
256 Kbytes	FFFC 0000h to FFFF FFFFh		
128 Kbytes	FFFE 0000h to FFFF FFFFh	32 Kbytes	0000 0000h to 0000 7FFFh

Note: See Table 1.3 and Table 1.4 List of Products, for the product type name.

Note 3. Reserved areas should not be accessed.

Figure 3.1 Memory Map in Each Operating Mode

Table 4.1 List of I/O Registers (Address Order) (5/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK $\geq$ PCLK	ICLK < PCLK
0008 8100h	TPU	Timer Start Register	TSTR	8	8	2 or 3 PCLKB	2 ICLK
0008 8101h	TPU	Timer Synchronous Register	TSYR	8	8	2 or 3 PCLKB	2 ICLK
0008 8108h	TPU0	Noise Filter Control Register	NFCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8109h	TPU1	Noise Filter Control Register	NFCR	8	8	2 or 3 PCLKB	2 ICLK
0008 810Ah	TPU2	Noise Filter Control Register	NFCR	8	8	2 or 3 PCLKB	2 ICLK
0008 810Bh	TPU3	Noise Filter Control Register	NFCR	8	8	2 or 3 PCLKB	2 ICLK
0008 810Ch	TPU4	Noise Filter Control Register	NFCR	8	8	2 or 3 PCLKB	2 ICLK
0008 810Dh	TPU5	Noise Filter Control Register	NFCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8110h	TPU0	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8111h	TPU0	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB	2 ICLK
0008 8112h	TPU0	Timer I/O Control Register H	TIORH	8	8	2 or 3 PCLKB	2 ICLK
0008 8113h	TPU0	Timer I/O Control Register L	TIORL	8	8	2 or 3 PCLKB	2 ICLK
0008 8114h	TPU0	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB	2 ICLK
0008 8115h	TPU0	Timer Status Register	TSR	8	8	2 or 3 PCLKB	2 ICLK
0008 8116h	TPU0	Timer Counter	TCNT	16	16	2 or 3 PCLKB	2 ICLK
0008 8118h	TPU0	Timer General Register A	TGRA	16	16	2 or 3 PCLKB	2 ICLK
0008 811Ah	TPU0	Timer General Register B	TGRB	16	16	2 or 3 PCLKB	2 ICLK
0008 811Ch	TPU0	Timer General Register C	TGRC	16	16	2 or 3 PCLKB	2 ICLK
0008 811Eh	TPU0	Timer General Register D	TGRD	16	16	2 or 3 PCLKB	2 ICLK
0008 8120h	TPU1	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8121h	TPU1	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB	2 ICLK
0008 8122h	TPU1	Timer I/O Control Register	TIOR	8	8	2 or 3 PCLKB	2 ICLK
0008 8124h	TPU1	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB	2 ICLK
0008 8125h	TPU1	Timer Status Register	TSR	8	8	2 or 3 PCLKB	2 ICLK
0008 8126h	TPU1	Timer Counter	TCNT	16	16	2 or 3 PCLKB	2 ICLK
0008 8128h	TPU1	Timer General Register A	TGRA	16	16	2 or 3 PCLKB	2 ICLK
0008 812Ah	TPU1	Timer General Register B	TGRB	16	16	2 or 3 PCLKB	2 ICLK
0008 8130h	TPU2	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8131h	TPU2	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB	2 ICLK
0008 8132h	TPU2	Timer I/O Control Register	TIOR	8	8	2 or 3 PCLKB	2 ICLK
0008 8134h	TPU2	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB	2 ICLK
0008 8135h	TPU2	Timer Status Register	TSR	8	8	2 or 3 PCLKB	2 ICLK
0008 8136h	TPU2	Timer Counter	TCNT	16	16	2 or 3 PCLKB	2 ICLK
0008 8138h	TPU2	Timer General Register A	TGRA	16	16	2 or 3 PCLKB	2 ICLK
0008 813Ah	TPU2	Timer General Register B	TGRB	16	16	2 or 3 PCLKB	2 ICLK
0008 8140h	TPU3	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8141h	TPU3	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB	2 ICLK
0008 8142h	TPU3	Timer I/O Control Register H	TIORH	8	8	2 or 3 PCLKB	2 ICLK
0008 8143h	TPU3	Timer I/O Control Register L	TIORL	8	8	2 or 3 PCLKB	2 ICLK
0008 8144h	TPU3	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB	2 ICLK
0008 8145h	TPU3	Timer Status Register	TSR	8	8	2 or 3 PCLKB	2 ICLK
0008 8146h	TPU3	Timer Counter	TCNT	16	16	2 or 3 PCLKB	2 ICLK
0008 8148h	TPU3	Timer General Register A	TGRA	16	16	2 or 3 PCLKB	2 ICLK
0008 814Ah	TPU3	Timer General Register B	TGRB	16	16	2 or 3 PCLKB	2 ICLK
0008 814Ch	TPU3	Timer General Register C	TGRC	16	16	2 or 3 PCLKB	2 ICLK
0008 814Eh	TPU3	Timer General Register D	TGRD	16	16	2 or 3 PCLKB	2 ICLK
0008 8150h	TPU4	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8151h	TPU4	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB	2 ICLK
0008 8152h	TPU4	Timer I/O Control Register	TIOR	8	8	2 or 3 PCLKB	2 ICLK
0008 8154h	TPU4	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB	2 ICLK
0008 8155h	TPU4	Timer Status Register	TSR	8	8	2 or 3 PCLKB	2 ICLK
0008 8156h	TPU4	Timer Counter	TCNT	16	16	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (20/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
0008 C42Eh	RTC	Time Error Adjustment Register	RADJ	8	8	2 or 3 PCLKB	2 ICLK
0008 C440h	RTC	Time Capture Control Register 0	RTCCR0	8	8	2 or 3 PCLKB	2 ICLK
0008 C442h	RTC	Time Capture Control Register 1	RTCCR1	8	8	2 or 3 PCLKB	2 ICLK
0008 C444h	RTC	Time Capture Control Register 2	RTCCR2	8	8	2 or 3 PCLKB	2 ICLK
0008 C452h	RTC	Second Capture Register 0	RSECCP0	8	8	2 or 3 PCLKB	2 ICLK
0008 C452h	RTC	BCNT0 Capture Register 0	BCNT0CP0	8	8	2 or 3 PCLKB	2 ICLK
0008 C454h	RTC	Minute Capture Register 0	RMINCP0	8	8	2 or 3 PCLKB	2 ICLK
0008 C454h	RTC	BCNT1 Capture Register 0	BCNT1CP0	8	8	2 or 3 PCLKB	2 ICLK
0008 C456h	RTC	Hour Capture Register 0	RHRCP0	8	8	2 or 3 PCLKB	2 ICLK
0008 C456h	RTC	BCNT2 Capture Register 0	BCNT2CP0	8	8	2 or 3 PCLKB	2 ICLK
0008 C45Ah	RTC	Date Capture Register 0	RDAYCP0	8	8	2 or 3 PCLKB	2 ICLK
0008 C45Ah	RTC	BCNT3 Capture Register 0	BCNT3CP0	8	8	2 or 3 PCLKB	2 ICLK
0008 C45Ch	RTC	Month Capture Register 0	RMONCP0	8	8	2 or 3 PCLKB	2 ICLK
0008 C462h	RTC	Second Capture Register 1	RSECCP1	8	8	2 or 3 PCLKB	2 ICLK
0008 C462h	RTC	BCNT0 Capture Register 1	BCNT0CP1	8	8	2 or 3 PCLKB	2 ICLK
0008 C464h	RTC	Minute Capture Register 1	RMINCP1	8	8	2 or 3 PCLKB	2 ICLK
0008 C464h	RTC	BCNT1 Capture Register 1	BCNT1CP1	8	8	2 or 3 PCLKB	2 ICLK
0008 C466h	RTC	Hour Capture Register 1	RHRCP1	8	8	2 or 3 PCLKB	2 ICLK
0008 C466h	RTC	BCNT2 Capture Register 1	BCNT2CP1	8	8	2 or 3 PCLKB	2 ICLK
0008 C46Ah	RTC	Date Capture Register 1	RDAYCP1	8	8	2 or 3 PCLKB	2 ICLK
0008 C46Ah	RTC	BCNT3 Capture Register 1	BCNT3CP1	8	8	2 or 3 PCLKB	2 ICLK
0008 C46Ch	RTC	Month Capture Register 1	RMONCP1	8	8	2 or 3 PCLKB	2 ICLK
0008 C472h	RTC	Second Capture Register 2	RSECCP2	8	8	2 or 3 PCLKB	2 ICLK
0008 C472h	RTC	BCNT0 Capture Register 2	BCNT0CP2	8	8	2 or 3 PCLKB	2 ICLK
0008 C474h	RTC	Minute Capture Register 2	RMINCP2	8	8	2 or 3 PCLKB	2 ICLK
0008 C474h	RTC	BCNT1 Capture Register 2	BCNT1CP2	8	8	2 or 3 PCLKB	2 ICLK
0008 C476h	RTC	Hour Capture Register 2	RHRCP2	8	8	2 or 3 PCLKB	2 ICLK
0008 C476h	RTC	BCNT2 Capture Register 2	BCNT2CP2	8	8	2 or 3 PCLKB	2 ICLK
0008 C47Ah	RTC	Date Capture Register 2	RDAYCP2	8	8	2 or 3 PCLKB	2 ICLK
0008 C47Ah	RTC	BCNT3 Capture Register 2	BCNT3CP2	8	8	2 or 3 PCLKB	2 ICLK
0008 C47Ch	RTC	Month Capture Register 2	RMONCP2	8	8	2 or 3 PCLKB	2 ICLK
0008 C580h	CMPB	Comparator B Control Register 1	CPBCNT1	8	8	2 or 3 PCLKB	2 ICLK
0008 C581h	CMPB	Comparator B Control Register 2	CPBCNT2	8	8	2 or 3 PCLKB	2 ICLK
0008 C582h	CMPB	Comparator B Flag Register	CPBFLG	8	8	2 or 3 PCLKB	2 ICLK
0008 C583h	CMPB	Comparator B Interrupt Control Register	CPBINT	8	8	2 or 3 PCLKB	2 ICLK
0008 C584h	CMPB	Comparator B Filter Select Register	CPBF	8	8	2 or 3 PCLKB	2 ICLK
0008 C585h	CMPB	Comparator B Mode Select Register	CPBMD	8	8	2 or 3 PCLKB	2 ICLK
0008 C586h	CMPB	Comparator B Reference Input Voltage Select Register	CPBREF	8	8	2 or 3 PCLKB	2 ICLK
0008 C587h	CMPB	Comparator B Output Control Register	CPBOCR	8	8	2 or 3 PCLKB	2 ICLK
0008 C5A0h	CMPB	Comparator B1 Control Register 1	CPB1CNT1	8	8	2 or 3 PCLKB	2 ICLK
0008 C5A1h	CMPB	Comparator B1 Control Register 2	CPB1CNT2	8	8	2 or 3 PCLKB	2 ICLK
0008 C5A2h	CMPB	Comparator B1 Flag Register	CPB1FLG	8	8	2 or 3 PCLKB	2 ICLK
0008 C5A3h	CMPB	Comparator B1 Interrupt Control Register	CPB1INT	8	8	2 or 3 PCLKB	2 ICLK
0008 C5A4h	CMPB	Comparator B1 Filter Select Register	CPB1F	8	8	2 or 3 PCLKB	2 ICLK
0008 C5A5h	CMPB	Comparator B1 Mode Select Register	CPB1MD	8	8	2 or 3 PCLKB	2 ICLK
0008 C5A6h	CMPB	Comparator B1 Reference Input Voltage Select Register	CPB1REF	8	8	2 or 3 PCLKB	2 ICLK
0008 C5A7h	CMPB	Comparator B1 Output Control Register	CPB1OCR	8	8	2 or 3 PCLKB	2 ICLK
000A 0000h	USB0	System Configuration Control Register	SYSCFG	16	16	3, 4 PCLKB	2 ICLK
000A 0004h	USB0	System Configuration Status Register 0	SYSSTS0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than $1 + 9 \times (\text{frequency ratio of ICLK/PCLK})^2$

Table 4.1 List of I/O Registers (Address Order) (23/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
000A 00B0h	USB0	BC Control Register 0	USBBCCTRL0	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ²
000A 00CCh	USB0	USB Module Control Register	USBMC	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ²
000A 00D0h	USB0	Device Address 0 Configuration Register	DEVADD0	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ²
000A 00D2h	USB0	Device Address 1 Configuration Register	DEVADD1	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ²
000A 00D4h	USB0	Device Address 2 Configuration Register	DEVADD2	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ²
000A 00D6h	USB0	Device Address 3 Configuration Register	DEVADD3	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ²
000A 00D8h	USB0	Device Address 4 Configuration Register	DEVADD4	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ²
000A 00DAh	USB0	Device Address 5 Configuration Register	DEVADD5	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ²
000A 0900h	CTSU	CTSU Control Register 0	CTSUCR0	8	8	2 or 3 PCLKB	2 ICLK
000A 0901h	CTSU	CTSU Control Register 1	CTSUCR1	8	8	2 or 3 PCLKB	2 ICLK
000A 0902h	CTSU	CTSU Synchronous Noise Reduction Setting Register	CTSUSDPRS	8	8	2 or 3 PCLKB	2 ICLK
000A 0903h	CTSU	CTSU Sensor Stabilization Wait Control Register	CTSUSST	8	8	2 or 3 PCLKB	2 ICLK
000A 0904h	CTSU	CTSU Measurement Channel Register 0	CTSUMCH0	8	8	2 or 3 PCLKB	2 ICLK
000A 0905h	CTSU	CTSU Measurement Channel Register 1	CTSUMCH1	8	8	2 or 3 PCLKB	2 ICLK
000A 0906h	CTSU	CTSU Channel Enable Control Register 0	CTSUCHAC0	8	8	2 or 3 PCLKB	2 ICLK
000A 0907h	CTSU	CTSU Channel Enable Control Register 1	CTSUCHAC1	8	8	2 or 3 PCLKB	2 ICLK
000A 0908h	CTSU	CTSU Channel Enable Control Register 2	CTSUCHAC2	8	8	2 or 3 PCLKB	2 ICLK
000A 0909h	CTSU	CTSU Channel Enable Control Register 3	CTSUCHAC3	8	8	2 or 3 PCLKB	2 ICLK
000A 090Ah	CTSU	CTSU Channel Enable Control Register 4	CTSUCHAC4	8	8	2 or 3 PCLKB	2 ICLK
000A 090Bh	CTSU	CTSU Channel Transmit/Receive Control Register 0	CTSUCHTRC0	8	8	2 or 3 PCLKB	2 ICLK
000A 090Ch	CTSU	CTSU Channel Transmit/Receive Control Register 1	CTSUCHTRC1	8	8	2 or 3 PCLKB	2 ICLK
000A 090Dh	CTSU	CTSU Channel Transmit/Receive Control Register 2	CTSUCHTRC2	8	8	2 or 3 PCLKB	2 ICLK
000A 090Eh	CTSU	CTSU Channel Transmit/Receive Control Register 3	CTSUCHTRC3	8	8	2 or 3 PCLKB	2 ICLK
000A 090Fh	CTSU	CTSU Channel Transmit/Receive Control Register 4	CTSUCHTRC4	8	8	2 or 3 PCLKB	2 ICLK
000A 0910h	CTSU	CTSU High-Pass Noise Reduction Control Register	CTSUDCLKC	8	8	2 or 3 PCLKB	2 ICLK
000A 0911h	CTSU	CTSU Status Register	CTSUST	8	8	2 or 3 PCLKB	2 ICLK
000A 0912h	CTSU	CTSU High-Pass Noise Reduction Spectrum Diffusion Control Register	CTSUSSC	16	16	2 or 3 PCLKB	2 ICLK
000A 0914h	CTSU	CTSU Sensor Offset Register 0	CTSUSO0	16	16	2 or 3 PCLKB	2 ICLK
000A 0916h	CTSU	CTSU Sensor Offset Register 1	CTSUSO1	16	16	2 or 3 PCLKB	2 ICLK
000A 0918h	CTSU	CTSU Sensor Counter	CTSUSC	16	16	2 or 3 PCLKB	2 ICLK
000A 091Ah	CTSU	CTSU Reference Counter	CTSURC	16	16	2 or 3 PCLKB	2 ICLK
000A 091Ch	CTSU	CTSU Error Status Register	CTSUERRS	16	16	2 or 3 PCLKB	2 ICLK
000A 8300h	RSCAN0	Bit Configuration Register L	CFGL	16	16	2 or 3 PCLKB	2 ICLK
000A 8302h	RSCAN0	Bit Configuration Register H	CFGH	16	16	2 or 3 PCLKB	2 ICLK
000A 8304h	RSCAN0	Control Register L	CTRL	16	16	2 or 3 PCLKB	2 ICLK
000A 8306h	RSCAN0	Control Register H	CTRH	16	16	2 or 3 PCLKB	2 ICLK
000A 8308h	RSCAN0	Status Register L	STSL	16	16	2 or 3 PCLKB	2 ICLK
000A 830Ah	RSCAN0	Status Register H	STSH	16	16	2 or 3 PCLKB	2 ICLK
000A 830Ch	RSCAN0	Error Flag Register L	ERFLL	16	16	2 or 3 PCLKB	2 ICLK
000A 830Eh	RSCAN0	Error Flag Register H	ERFLH	16	16	2 or 3 PCLKB	2 ICLK
000A 8322h	RSCAN	Global Configuration Register L	GCFGFL	16	16	2 or 3 PCLKB	2 ICLK
000A 8324h	RSCAN	Global Configuration Register H	GCFGH	16	16	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (26/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
000A 83DEh	RSCAN	Receive Rule Entry Register 5AH	GAFLIDH5	16	16	2 or 3 PCLKB	2 ICLK
000A 83DEh	RSCAN	Receive Buffer Register 3DH	RMDF33	16	16	2 or 3 PCLKB	2 ICLK
000A 83E0h	RSCAN	Receive Rule Entry Register 5BL	GAFLML5	16	16	2 or 3 PCLKB	2 ICLK
000A 83E0h	RSCAN	Receive Buffer Register 4AL	RMIDL4	16	16	2 or 3 PCLKB	2 ICLK
000A 83E2h	RSCAN	Receive Rule Entry Register 5BH	GAFLMH5	16	16	2 or 3 PCLKB	2 ICLK
000A 83E2h	RSCAN	Receive Buffer Register 4AH	RMIDH4	16	16	2 or 3 PCLKB	2 ICLK
000A 83E4h	RSCAN	Receive Rule Entry Register 5CL	GAFLPL5	16	16	2 or 3 PCLKB	2 ICLK
000A 83E4h	RSCAN	Receive Buffer Register 4BL	RMTS4	16	16	2 or 3 PCLKB	2 ICLK
000A 83E6h	RSCAN	Receive Rule Entry Register 5CH	GAFLPH5	16	16	2 or 3 PCLKB	2 ICLK
000A 83E6h	RSCAN	Receive Buffer Register 4BH	RMPTR4	16	16	2 or 3 PCLKB	2 ICLK
000A 83E8h	RSCAN	Receive Rule Entry Register 6AL	GAFLIDL6	16	16	2 or 3 PCLKB	2 ICLK
000A 83E8h	RSCAN	Receive Buffer Register 4CL	RMDF04	16	16	2 or 3 PCLKB	2 ICLK
000A 83EAh	RSCAN	Receive Rule Entry Register 6AH	GAFLIDH6	16	16	2 or 3 PCLKB	2 ICLK
000A 83EAh	RSCAN	Receive Buffer Register 4CH	RMDF14	16	16	2 or 3 PCLKB	2 ICLK
000A 83ECh	RSCAN	Receive Rule Entry Register 6BL	GAFLML6	16	16	2 or 3 PCLKB	2 ICLK
000A 83ECh	RSCAN	Receive Buffer Register 4DL	RMDF24	16	16	2 or 3 PCLKB	2 ICLK
000A 83EEh	RSCAN	Receive Rule Entry Register 6BH	GAFLMH6	16	16	2 or 3 PCLKB	2 ICLK
000A 83EEh	RSCAN	Receive Buffer Register 4DH	RMDF34	16	16	2 or 3 PCLKB	2 ICLK
000A 83F0h	RSCAN	Receive Rule Entry Register 6CL	GAFLPL6	16	16	2 or 3 PCLKB	2 ICLK
000A 83F0h	RSCAN	Receive Buffer Register 5AL	RMIDL5	16	16	2 or 3 PCLKB	2 ICLK
000A 83F2h	RSCAN	Receive Rule Entry Register 6CH	GAFLPH6	16	16	2 or 3 PCLKB	2 ICLK
000A 83F2h	RSCAN	Receive Buffer Register 5AH	RMIDH5	16	16	2 or 3 PCLKB	2 ICLK
000A 83F4h	RSCAN	Receive Rule Entry Register 7AL	GAFLIDL7	16	16	2 or 3 PCLKB	2 ICLK
000A 83F4h	RSCAN	Receive Buffer Register 5BL	RMTS5	16	16	2 or 3 PCLKB	2 ICLK
000A 83F6h	RSCAN	Receive Rule Entry Register 7AH	GAFLIDH7	16	16	2 or 3 PCLKB	2 ICLK
000A 83F6h	RSCAN	Receive Buffer Register 5BH	RMPTR5	16	16	2 or 3 PCLKB	2 ICLK
000A 83F8h	RSCAN	Receive Rule Entry Register 7BL	GAFLML7	16	16	2 or 3 PCLKB	2 ICLK
000A 83F8h	RSCAN	Receive Buffer Register 5CL	RMDF05	16	16	2 or 3 PCLKB	2 ICLK
000A 83FAh	RSCAN	Receive Rule Entry Register 7BH	GAFLMH7	16	16	2 or 3 PCLKB	2 ICLK
000A 83FAh	RSCAN	Receive Buffer Register 5CH	RMDF15	16	16	2 or 3 PCLKB	2 ICLK
000A 83FCh	RSCAN	Receive Rule Entry Register 7CL	GAFLPL7	16	16	2 or 3 PCLKB	2 ICLK
000A 83FCh	RSCAN	Receive Buffer Register 5DL	RMDF25	16	16	2 or 3 PCLKB	2 ICLK
000A 83FEh	RSCAN	Receive Rule Entry Register 7CH	GAFLPH7	16	16	2 or 3 PCLKB	2 ICLK
000A 83FEh	RSCAN	Receive Buffer Register 5DH	RMDF35	16	16	2 or 3 PCLKB	2 ICLK
000A 8400h	RSCAN	Receive Rule Entry Register 8AL	GAFLIDL8	16	16	2 or 3 PCLKB	2 ICLK
000A 8400h	RSCAN	Receive Buffer Register 6AL	RMIDL6	16	16	2 or 3 PCLKB	2 ICLK
000A 8402h	RSCAN	Receive Rule Entry Register 8AH	GAFLIDH8	16	16	2 or 3 PCLKB	2 ICLK
000A 8402h	RSCAN	Receive Buffer Register 6AH	RMIDH6	16	16	2 or 3 PCLKB	2 ICLK
000A 8404h	RSCAN	Receive Rule Entry Register 8BL	GAFLML8	16	16	2 or 3 PCLKB	2 ICLK
000A 8404h	RSCAN	Receive Buffer Register 6BL	RMTS6	16	16	2 or 3 PCLKB	2 ICLK
000A 8406h	RSCAN	Receive Rule Entry Register 8BH	GAFLMH8	16	16	2 or 3 PCLKB	2 ICLK
000A 8406h	RSCAN	Receive Buffer Register 6BH	RMPTR6	16	16	2 or 3 PCLKB	2 ICLK
000A 8408h	RSCAN	Receive Rule Entry Register 8CL	GAFLPL8	16	16	2 or 3 PCLKB	2 ICLK
000A 8408h	RSCAN	Receive Buffer Register 6CL	RMDF06	16	16	2 or 3 PCLKB	2 ICLK
000A 840Ah	RSCAN	Receive Rule Entry Register 8CH	GAFLPH8	16	16	2 or 3 PCLKB	2 ICLK
000A 840Ah	RSCAN	Receive Buffer Register 6CH	RMDF16	16	16	2 or 3 PCLKB	2 ICLK
000A 840Ch	RSCAN	Receive Rule Entry Register 9AL	GAFLIDL9	16	16	2 or 3 PCLKB	2 ICLK
000A 840Ch	RSCAN	Receive Buffer Register 6DL	RMDF26	16	16	2 or 3 PCLKB	2 ICLK
000A 840Eh	RSCAN	Receive Rule Entry Register 9AH	GAFLIDH9	16	16	2 or 3 PCLKB	2 ICLK
000A 840Eh	RSCAN	Receive Buffer Register 6DH	RMDF36	16	16	2 or 3 PCLKB	2 ICLK
000A 8410h	RSCAN	Receive Rule Entry Register 9BL	GAFLML9	16	16	2 or 3 PCLKB	2 ICLK
000A 8410h	RSCAN	Receive Buffer Register 7AL	RMIDL7	16	16	2 or 3 PCLKB	2 ICLK

Item					Symbol	Typ. *4	Max.	Unit	Test Conditions	
Supply current	Middle-speed operating mode	Normal operating mode	All peripheral operation: Max.*7	ICLK = 12 MHz	I _{CC}	—	16.7	mA		
		Sleep mode	No peripheral operation*6	ICLK = 12 MHz		1.9	—			
				ICLK = 8 MHz		1.2	—			
				ICLK = 4 MHz		1.1	—			
				ICLK = 1 MHz		1.0	—			
			All peripheral operation: Normal*7	ICLK = 12 MHz		6.1	—			
				ICLK = 8 MHz		4.4	—			
				ICLK = 4 MHz		3.0	—			
				ICLK = 1 MHz		2.0	—			
		Deep sleep mode	No peripheral operation*6	ICLK = 12 MHz		1.6	—			
				ICLK = 8 MHz		1.0	—			
				ICLK = 4 MHz		0.9	—			
				ICLK = 1 MHz		0.8	—			
			All peripheral operation: Normal*7	ICLK = 12 MHz		5.1	—			
				ICLK = 8 MHz		3.7	—			
				ICLK = 4 MHz		2.6	—			
				ICLK = 1 MHz		1.8	—			
		Increase during BGO operation*5				2.5	—			
		Low-speed operating mode	Normal operating mode	No peripheral operation*8		ICLK = 32 kHz	I _{CC}			5.2
	All peripheral operation: Normal *9, *10			ICLK = 32 kHz	22.3	—				
	All peripheral operation: Max.*9, *10			ICLK = 32 kHz	—	74.4				
	Sleep mode		No peripheral operation*8	ICLK = 32 kHz	3.0	—				
			All peripheral operation: Normal*9	ICLK = 32 kHz	13.1	—				
	Deep sleep mode		No peripheral operation*8	ICLK = 32 kHz	2.4	—				
			All peripheral operation: Normal*9	ICLK = 32 kHz	10.5	—				

Note 1. Supply current values do not include the output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is PLL. BCLK, FCLK, and PCLK are set to divided by 64.

Note 3. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL. BCLK, FCLK, and PCLK are the same frequency as that of ICLK.

Note 4. Values when VCC is 3.3 V.

Note 5. This is the increase when data is programmed to or erased from the ROM or E2 DataFlash during program execution.

Note 6. Clock supply to the peripheral functions is stopped. The clock source is PLL when ICLK is 12 MHz and HOCO for other cases. BCLK, FCLK, and PCLK are set to divided by 64.

Note 7. Clocks are supplied to the peripheral functions. The clock source is PLL when ICLK is 12 MHz and HOCO for other cases. BCLK, FCLK, and PCLK are the same frequency of that of the ICLK.

Note 8. Clock supply to the peripheral functions is stopped. The clock source is the sub oscillation circuit. BCLK, FCLK, and PCLK are set to divided by 64.

Note 9. Clocks are supplied to the peripheral functions. The clock source is the sub oscillation circuit. BCLK, FCLK, and PCLK are the same frequency as that of ICLK.

Note 10. This is the value when the MSTPCRA.MSTPA17 (12-bit A/D converter module stop bit) is in the module stop state.

Note 11. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL. BCLK, FCLK, and PCLKB are set to divided by 2 and PCLKA and PCLKD are the same frequency as that of ICLK.

5.2.1 Normal I/O Pin Output Characteristics (1)

Figure 5.8 to Figure 5.12 show the characteristics when normal output is selected by the drive capacity control register.

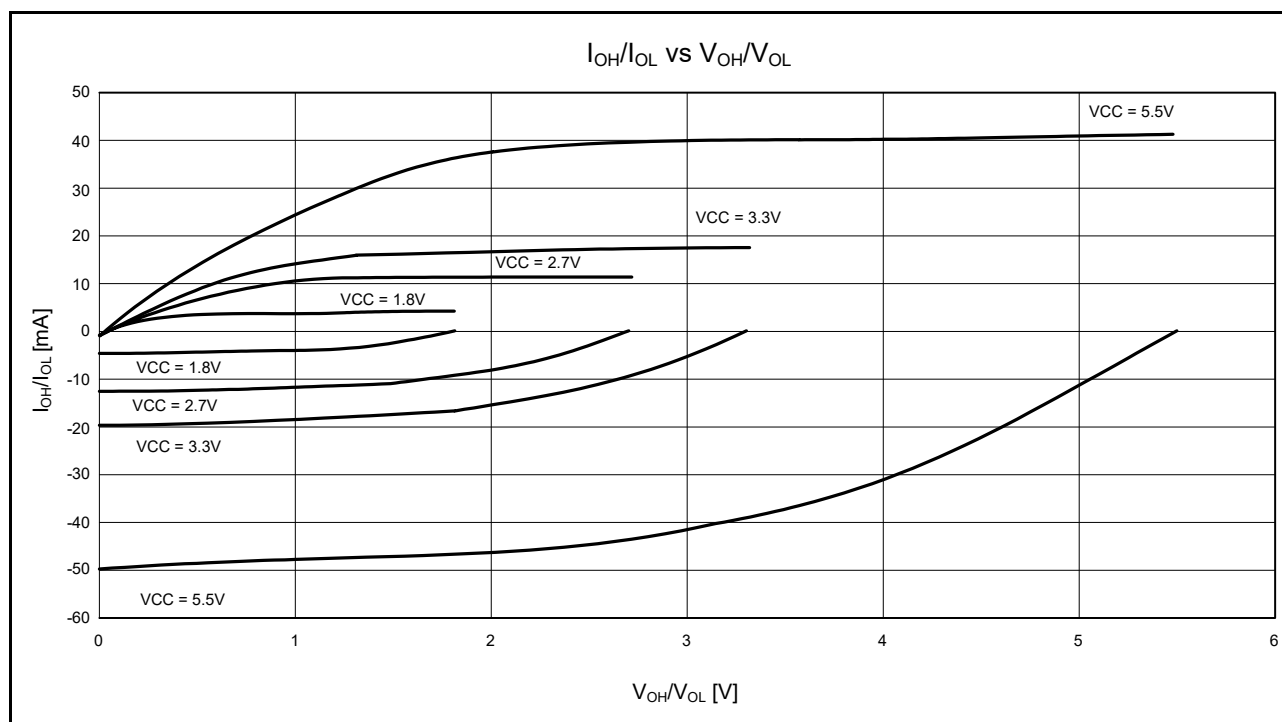


Figure 5.8 V_{OH}/V_{OL} and I_{OH}/I_{OL} Voltage Characteristics at $T_a = 25^\circ\text{C}$ When Normal Output is Selected (Reference Data)

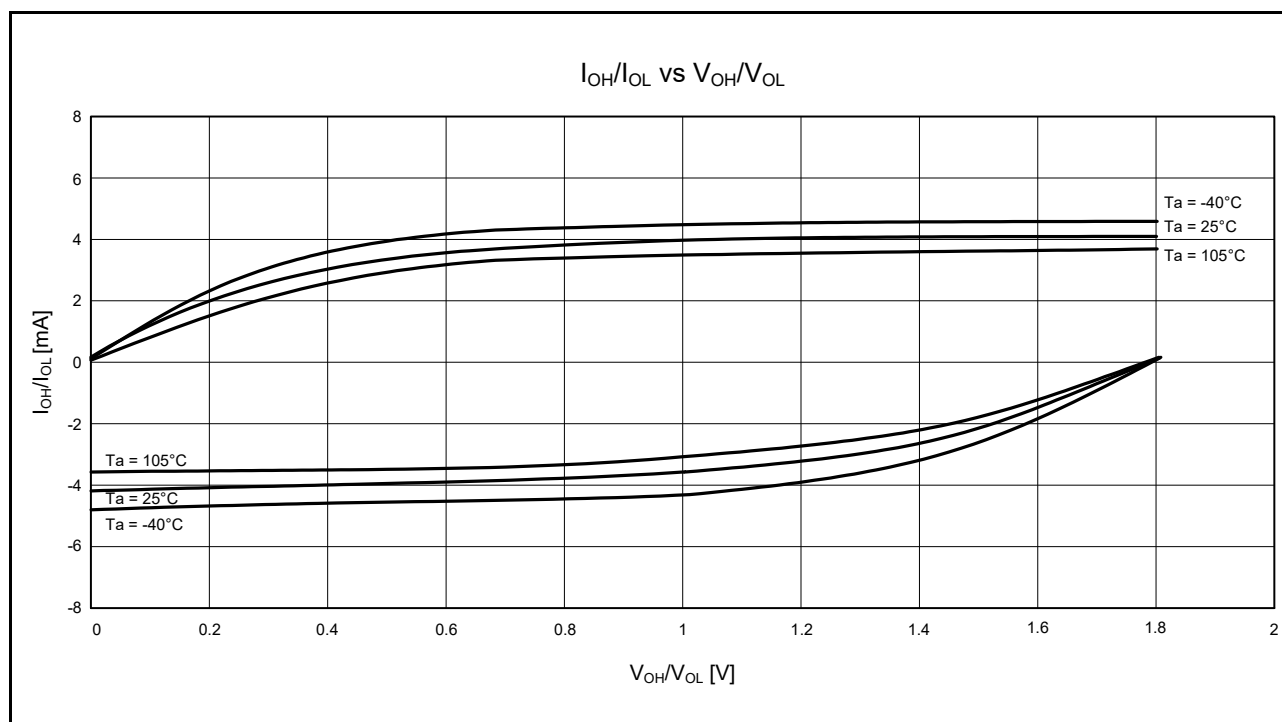


Figure 5.9 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at $V_{CC} = 1.8\text{ V}$ When Normal Output is Selected (Reference Data)

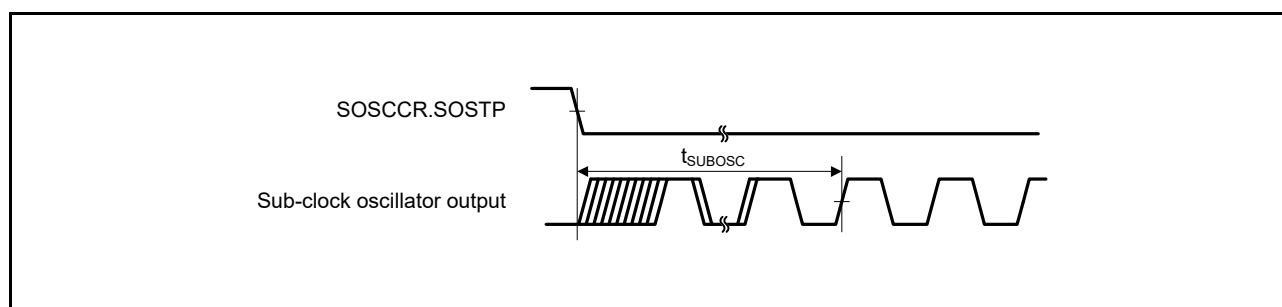


Figure 5.30 Sub-Clock Oscillation Start Timing

5.3.4 Control Signal Timing

Table 5.33 Control Signal Timing

Conditions: $1.8\text{ V} \leq VCC = VCC_USB = AVCC0 \leq 5.5\text{ V}$, $VSS = AVSS0 = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

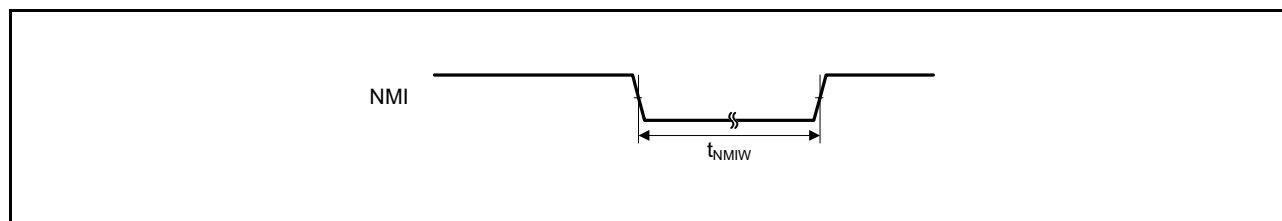
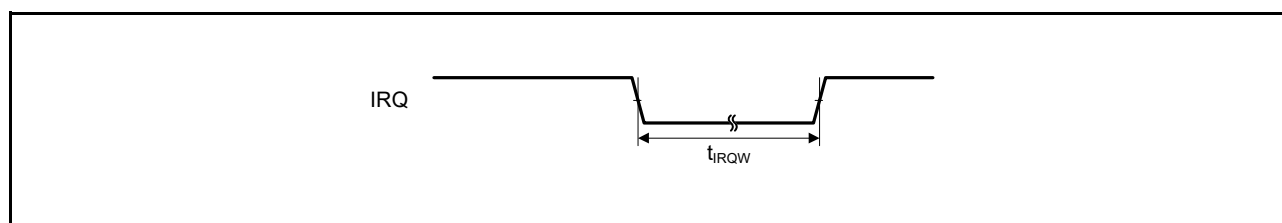
Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
NMI pulse width	t_{NMIW}	200	—	—	ns	NMI digital filter is disabled (NMIFLTE.NFLTEN = 0)	$t_{Pcyc} \times 2 \leq 200\text{ ns}$
		$t_{Pcyc} \times 2^{*1}$	—	—			$t_{Pcyc} \times 2 > 200\text{ ns}$
		200	—	—		NMI digital filter is enabled (NMIFLTE.NFLTEN = 1)	$t_{NMICK} \times 3 \leq 200\text{ ns}$
		$t_{NMICK} \times 3.5^{*2}$	—	—			$t_{NMICK} \times 3 > 200\text{ ns}$
IRQ pulse width	t_{IRQW}	200	—	—	ns	IRQ digital filter is disabled (IRQFLTE0.FLTENi = 0)	$t_{Pcyc} \times 2 \leq 200\text{ ns}$
		$t_{Pcyc} \times 2^{*1}$	—	—			$t_{Pcyc} \times 2 > 200\text{ ns}$
		200	—	—		IRQ digital filter is enabled (IRQFLTE0.FLTENi = 1)	$t_{IRQCK} \times 3 \leq 200\text{ ns}$
		$t_{IRQCK} \times 3.5^{*3}$	—	—			$t_{IRQCK} \times 3 > 200\text{ ns}$

Note: 200 ns minimum in software standby mode.

Note 1. t_{Pcyc} indicates the cycle of PCLKB.

Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.

Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 7).

**Figure 5.36 NMI Interrupt Input Timing****Figure 5.37 IRQ Interrupt Input Timing**

5.3.5 Bus Timing

Table 5.34 Bus Timing (1)

Conditions: $2.7\text{ V} \leq V_{CC} = V_{CC_USB} = AV_{CC0} \leq 5.5\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$,
 $f_{BCLK} \leq 32\text{ MHz}$ (BCLK pin output frequency $\leq 16\text{ MHz}$), $T_a = -40\text{ to }+105^\circ\text{C}$, $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$,
 $I_{OH} = -1.0\text{ mA}$, $I_{OL} = 1.0\text{ mA}$, $C_L = 30\text{ pF}$, when normal output is selected by the drive capacity control register

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	55	ns	Figure 5.38 to Figure 5.41
Byte control delay time	t_{BCD}	—	55	ns	
CS# delay time	t_{CSD}	—	55	ns	
RD# delay time	t_{RSD}	—	55	ns	
Read data setup time	t_{RDS}	40	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	55	ns	
Write data delay time	t_{WDD}	—	55	ns	
Write data hold time	t_{WDH}	0	—	ns	Figure 5.42
WAIT# setup time	t_{WTS}	40	—	ns	
WAIT# hold time	t_{WTH}	0	—	ns	

Table 5.35 Bus Timing (2)

Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} = AV_{CC0} < 2.7\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$,
 $f_{BCLK} \leq 16\text{ MHz}$ (BCLK pin output frequency $\leq 8\text{ MHz}$), $T_a = -40\text{ to }+105^\circ\text{C}$, $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$,
 $I_{OH} = -1.0\text{ mA}$, $I_{OL} = 1.0\text{ mA}$, $C_L = 30\text{ pF}$, when normal output is selected by the drive capacity control register

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	90	ns	Figure 5.38 to Figure 5.41
Byte control delay time	t_{BCD}	—	90	ns	
CS# delay time	t_{CSD}	—	90	ns	
RD# delay time	t_{RSD}	—	90	ns	
Read data setup time	t_{RDS}	60	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	90	ns	
Write data delay time	t_{WDD}	—	90	ns	
Write data hold time	t_{WDH}	0	—	ns	Figure 5.42
WAIT# setup time	t_{WTS}	60	—	ns	
WAIT# hold time	t_{WTH}	0	—	ns	

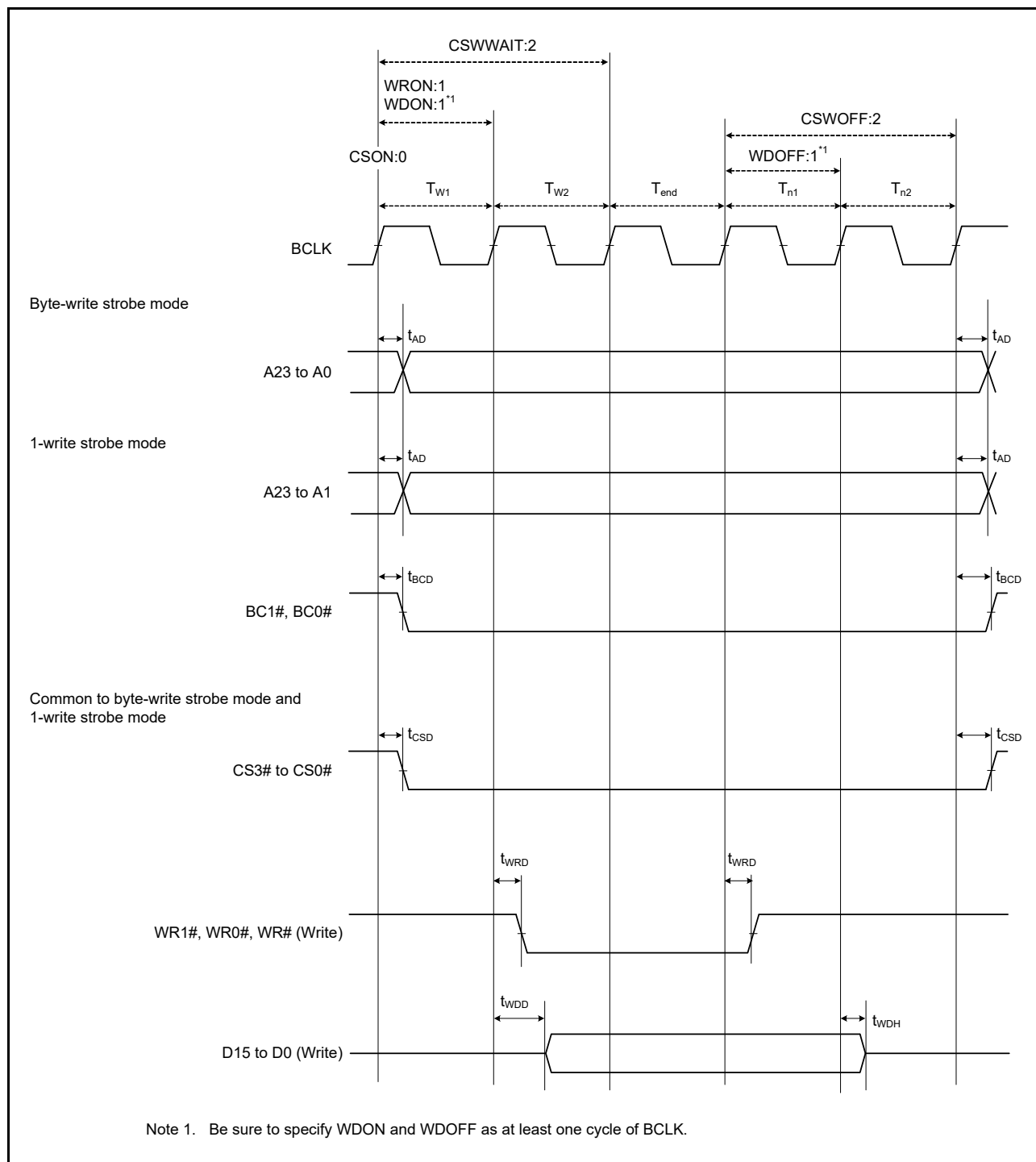


Figure 5.39 External Bus Timing/Normal Write Cycle (Bus Clock Synchronization)

5.3.6 Timing of On-Chip Peripheral Modules

Table 5.38 Timing of On-Chip Peripheral Modules (1)Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} = \text{AVCC0} \leq 5.5\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item				Symbol	Min.	Max.	Unit *1	Test Conditions
I/O ports	Input data pulse width			t _{PRW}	1.5	—	t _{PCYC}	Figure 5.45
MTU2/TPU	Input capture input pulse width	Single-edge setting	t _{TICW}	1.5	—	t _{PCYC}	Figure 5.46	
		Both-edge setting		2.5	—			
	Timer clock pulse width	Single-edge setting	t _{TCKWH} , t _{TCKWL}	1.5	—	t _{PCYC}	Figure 5.47	
		Both-edge setting		2.5	—			
		Phase counting mode		2.5	—			
POE2	POE# input pulse width			t _{POEW}	1.5	—	t _{PCYC}	Figure 5.48
TMR	Timer clock pulse width	Single-edge setting	t _{TMCWH} , t _{TMCWL}	1.5	—	t _{PCYC}	Figure 5.49	
		Both-edge setting	2.5	—				
SCI	Input clock cycle time	Asynchronous	t _{SCYC}	4	—	t _{PCYC}	Figure 5.50	
		Clock synchronous		6	—			
	Input clock pulse width			t _{SCKW}	0.4	0.6	t _{SCYC}	Figure 5.51
	Input clock rise time			t _{SCKr}	—	20	ns	
	Input clock fall time			t _{SCKf}	—	20	ns	
	Output clock cycle time	Asynchronous	t _{SCYC}	16	—	t _{PCYC}		
		Clock synchronous		4	—			
	Output clock pulse width			t _{SCKW}	0.4	0.6	t _{SCYC}	
	Output clock rise time			t _{SCKr}	—	20	ns	
	Output clock fall time			t _{SCKf}	—	20	ns	
	Transmit data delay time (master)	Clock synchronous		t _{TXD}	—	40	ns	
	Transmit data delay time (slave)	Clock synchronous	2.7 V or above		—	65	ns	
			1.8 V or above		—	100	ns	
	Receive data setup time (master)	Clock synchronous	2.7 V or above	t _{RXS}	65	—	ns	
			1.8 V or above		90	—	ns	
	Receive data setup time (slave)	Clock synchronous			40	—	ns	
	Receive data hold time	Clock synchronous		t _{RXH}	40	—	ns	
	A/D converter	Trigger input pulse width			t _{TRGW}	1.5	—	
CAC	CACREF input pulse width	t _{PCYC} ≤ t _{CAC} ^{*2}	t _{CACREF}	4.5 t _{CAC} + 3 t _{PCYC}	—	ns		
		t _{PCYC} > t _{CAC} ^{*2}		5 t _{CAC} + 6.5 t _{PCYC}	—			
CLKOUT	CLKOUT pin output cycle*4	VCC = 2.7 V or above	t _{CCYC}	62.5	—	ns	Figure 5.53	
		VCC = 1.8 V or above		125				
	CLKOUT pin high pulse width*3	VCC = 2.7 V or above	t _{CH}	15	—	ns		
		VCC = 1.8 V or above		30				
	CLKOUT pin low pulse width*3	VCC = 2.7 V or above	t _{CL}	15	—	ns		
		VCC = 1.8 V or above		30				
	CLKOUT pin output rise time	VCC = 2.7 V or above	t _{Cr}	—	12	ns		
		VCC = 1.8 V or above			25			
	CLKOUT pin output fall time	VCC = 2.7 V or above	t _{Cf}	—	12	ns		
		VCC = 1.8 V or above			25			

Note 1. t_{Pcyc} : PCLK cycleNote 2. t_{cac} : CAC count clock source cycle

Note 3. When the LOCO is selected as the clock output source (the CKOCR.CKOSEL[2:0] bits are 000b), set the clock output division ratio selection to divided by 2 (the CKOCR.CKODIV[2:0] bits are 001b).

Note 4. When the EXTAL external clock input or an oscillator is used with divided by 1 (the CKOCR.CKOSEL[2:0] bits are 010b and the CKOCR.CKODIV[2:0] bits are 000b) to output from CLKOUT, the above should be satisfied with an input duty cycle of 45 to 55%.

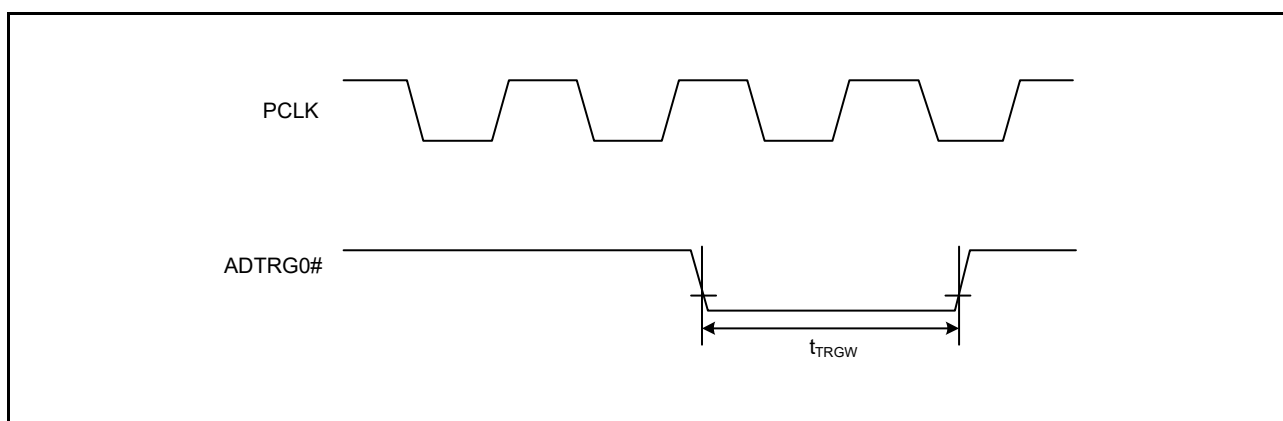


Figure 5.52 A/D Converter External Trigger Input Timing

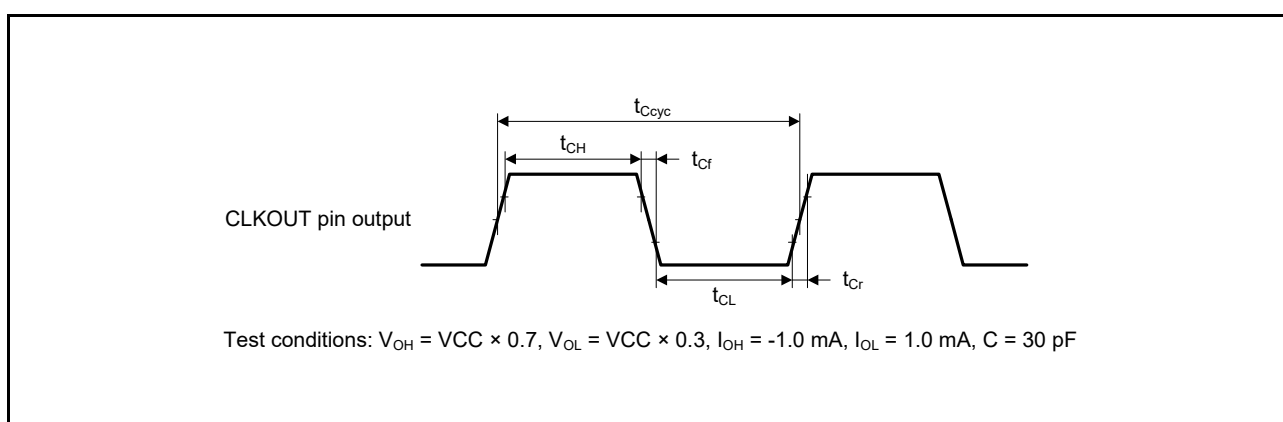


Figure 5.53 CLKOUT Output Timing

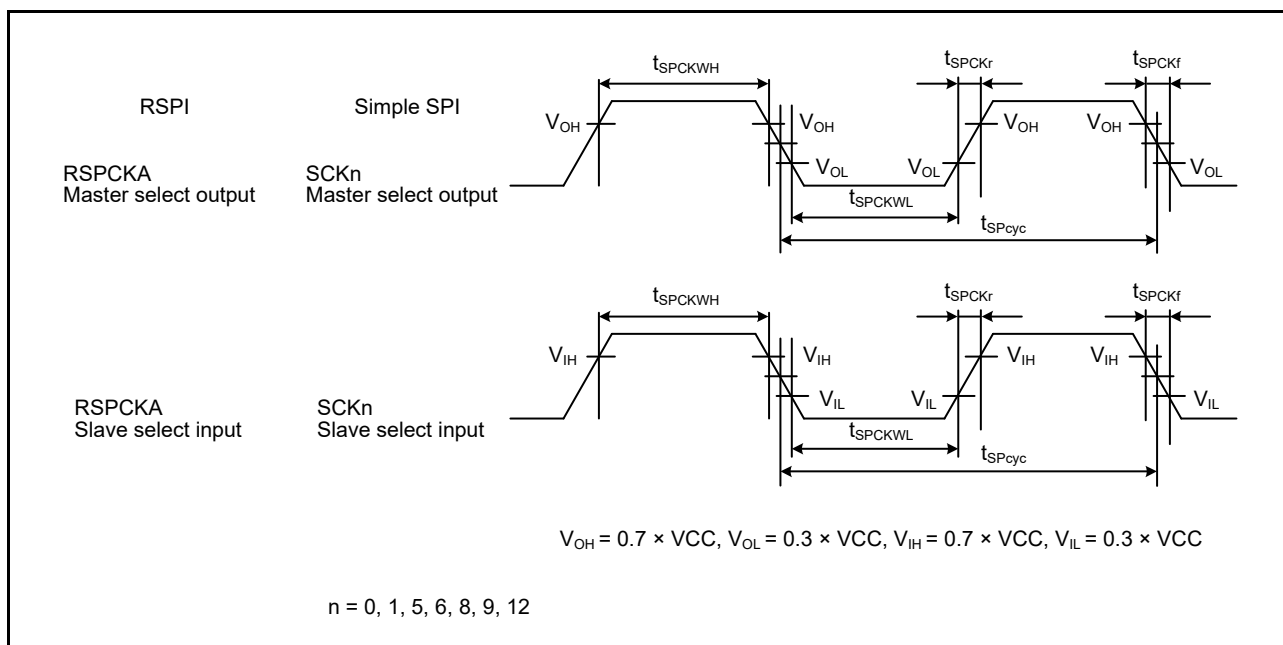


Figure 5.54 RSPI Clock Timing and Simple SPI Clock Timing

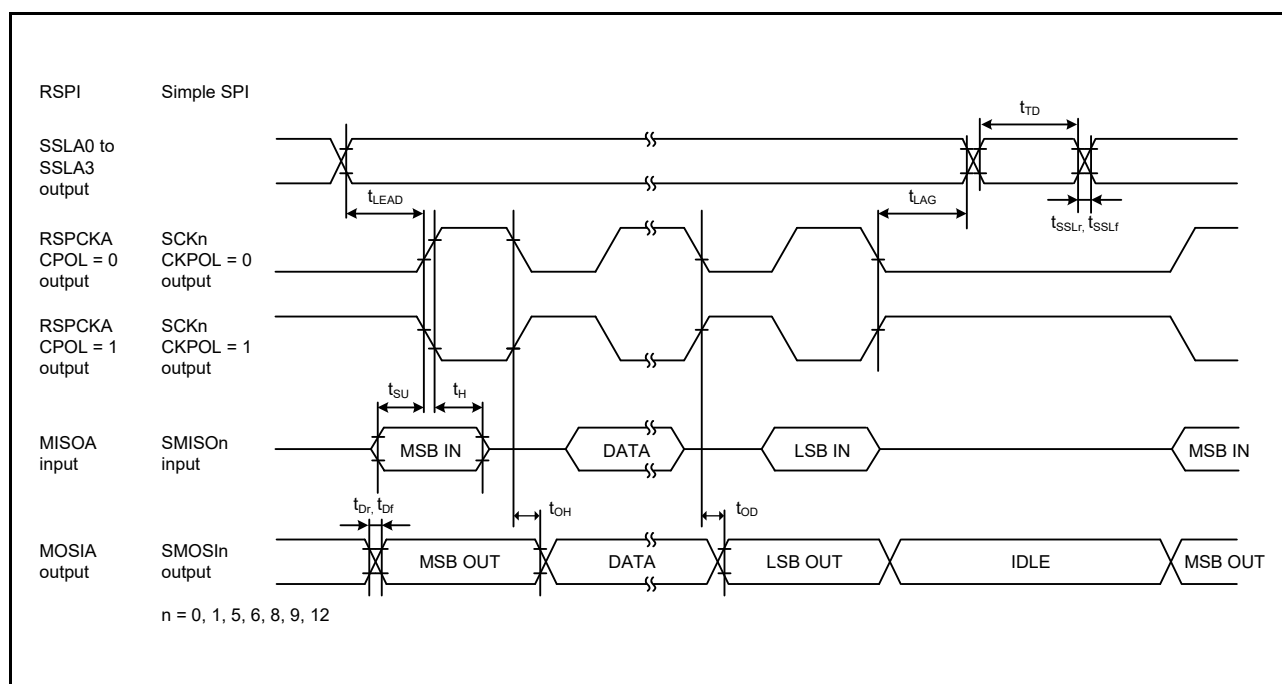


Figure 5.55 RSPI Timing (Master, CPHA = 0) and Simple SPI Clock Timing (Master, CKPH = 1)

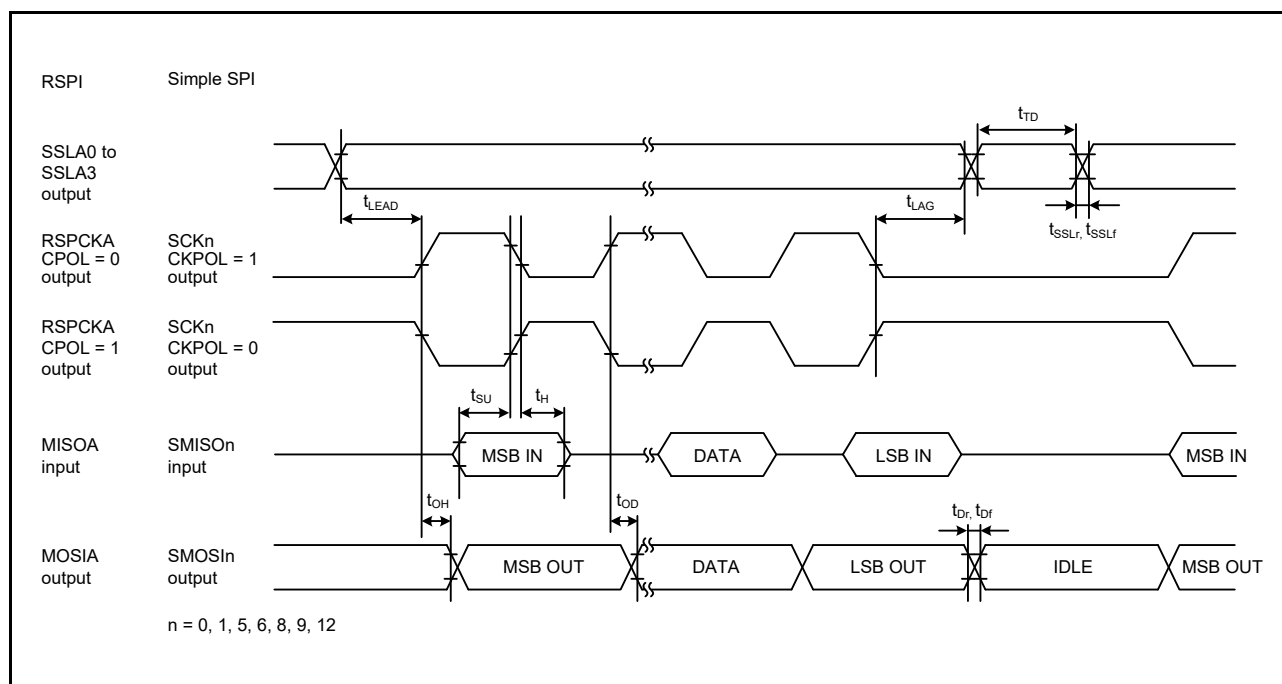


Figure 5.56 RSPI Timing (Master, CPHA = 1) and Simple SPI Clock Timing (Master, CKPH = 0)

Table 5.50 A/D Conversion Characteristics (5)

Conditions: $1.8\text{V} \leq V_{CC} = V_{CC_USB} = AVCC0 \leq 5.5\text{V}$, $1.8\text{V} \leq V_{REFH0} \leq AVCC0$, $V_{SS} = AVSS0 = V_{SS_USB} = 0\text{V}$,
reference voltage = V_{REFH0} selected, $T_a = -40$ to $+105^\circ\text{C}$

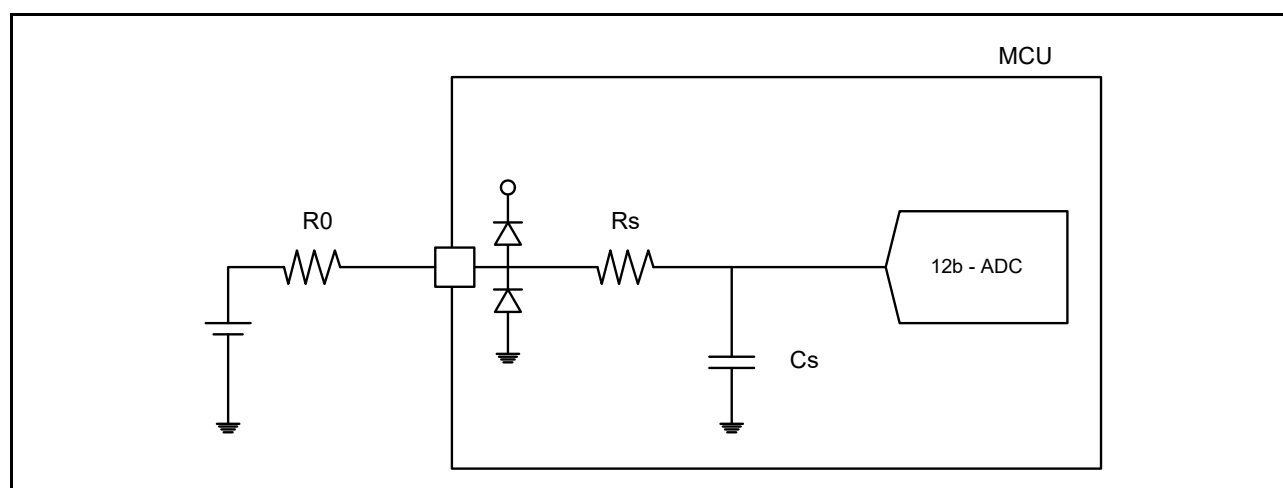
Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	8	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 8 MHz)	Permissible signal source impedance (Max.) = 5 k Ω	6.75	—	—	μs	High-precision channel The ADCSR.ADHSC bit is 1 The ADSSTRn register is 0Dh
		10.13	—	—		Normal-precision channel The ADCSR.ADHSC bit is 1 The ADSSTRn register is 28h
Analog input capacitance	Cs	—	—	15	pF	Pin capacitance included Figure 5.68
Analog input resistance	Rs	—	—	2.5	k Ω	Figure 5.68
Offset error		—	± 1	± 7.5	LSB	
Full-scale error		—	± 1.5	± 7.5	LSB	
Quantization error		—	± 0.5	—	LSB	
Absolute accuracy		—	± 3.0	± 8.0	LSB	
DNL differential non-linearity error		—	± 1.0	—	LSB	
INL integral non-linearity error		—	± 1.25	± 3.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential non-linearity error, and INL integral non-linearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 5.51 A/D Converter Channel Classification

Classification	Channel	Conditions	Remarks
High-precision channel	AN000 to AN007	$AVCC0 = 1.8$ to 5.5V	Pins AN000 to AN007 cannot be used as digital outputs when the A/D converter is in use.
Normal-precision channel	AN016 to AN031		
Internal reference voltage input channel	Internal reference voltage	$AVCC0 = 2.0$ to 5.5V	
Temperature sensor input channel	Temperature sensor output	$AVCC0 = 2.0$ to 5.5V	

**Figure 5.68 Equivalent Circuit**

Differential non-linearity error (DNL)

The differential non-linearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

Offset error

An offset error is the difference between a transition point of the ideal first output code and the actual first output code.

Full-scale error

A full-scale error is the difference between a transition point of the ideal last output code and the actual last output code.

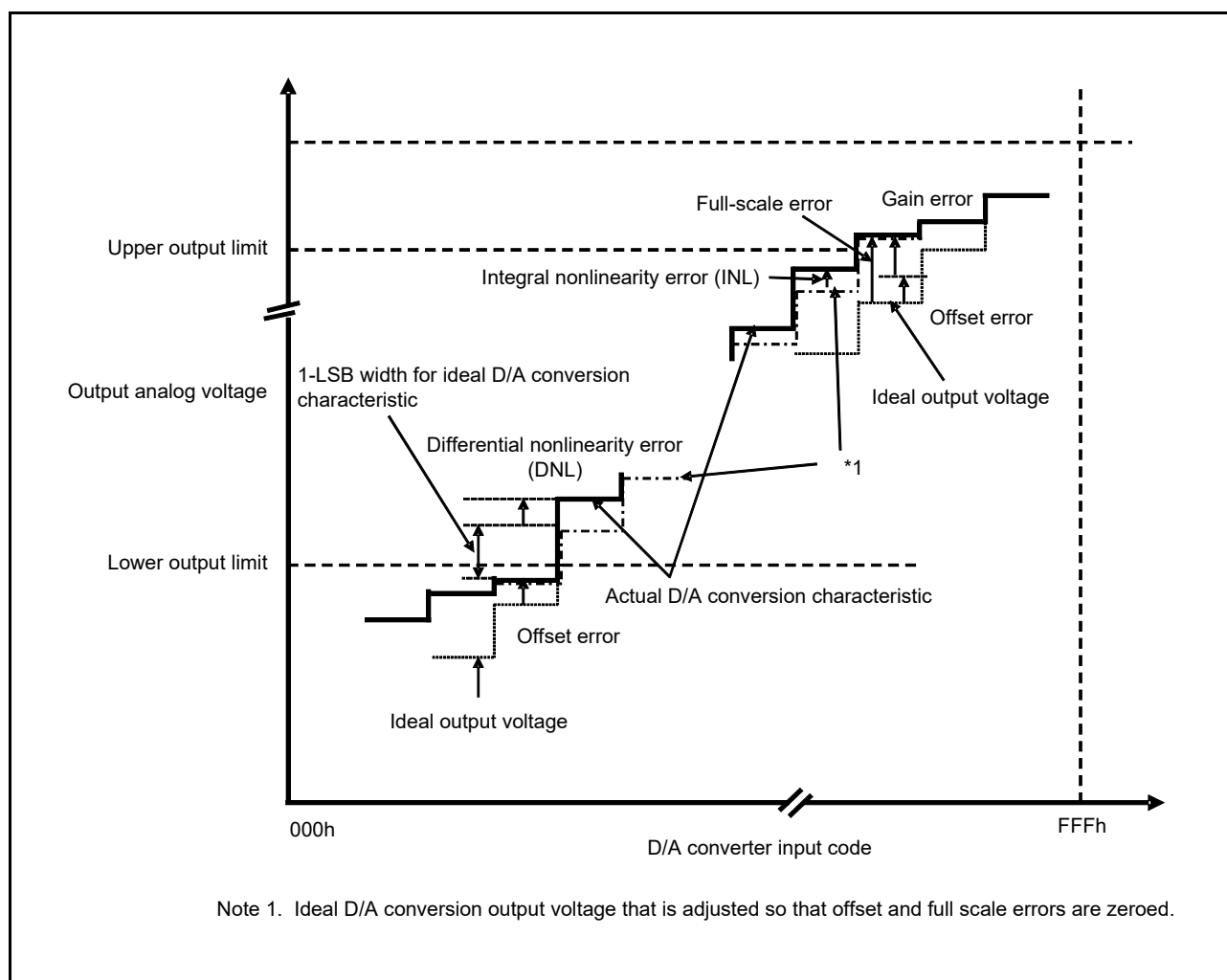


Figure 5.70 Illustration of D/A Converter Characteristic Terms

Integral non-linearity error (INL)

The integral non-linearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential non-linearity error (DNL)

The differential non-linearity error is the difference between 1-LSB width based on the ideal D/A conversion characteristics and the width of the actually output code.

Offset error

An offset error is the difference between a transition point of the ideal first output code and the actual first output code.

Full-scale error

A full-scale error is the difference between a transition point of the ideal last output code and the actual last output code.

5.9 CTSU Characteristics

Table 5.57 CTSU Characteristics

Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} = AV_{CC0} \leq 5.5\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
External capacitance connected to TSCAP pin	C_{tscap}	9	10	11	nF	
TS pin capacitive load	C_{base}	—	—	50	pF	
Permissible output high current	ΣI_{OH}	—	—	−24	mA	When the mutual capacitance method is applied

5.10 Characteristics of Power-On Reset Circuit and Voltage Detection Circuit

Table 5.58 Characteristics of Power-On Reset Circuit and Voltage Detection Circuit (1)

Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} = AV_{CC0} \leq 5.5\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

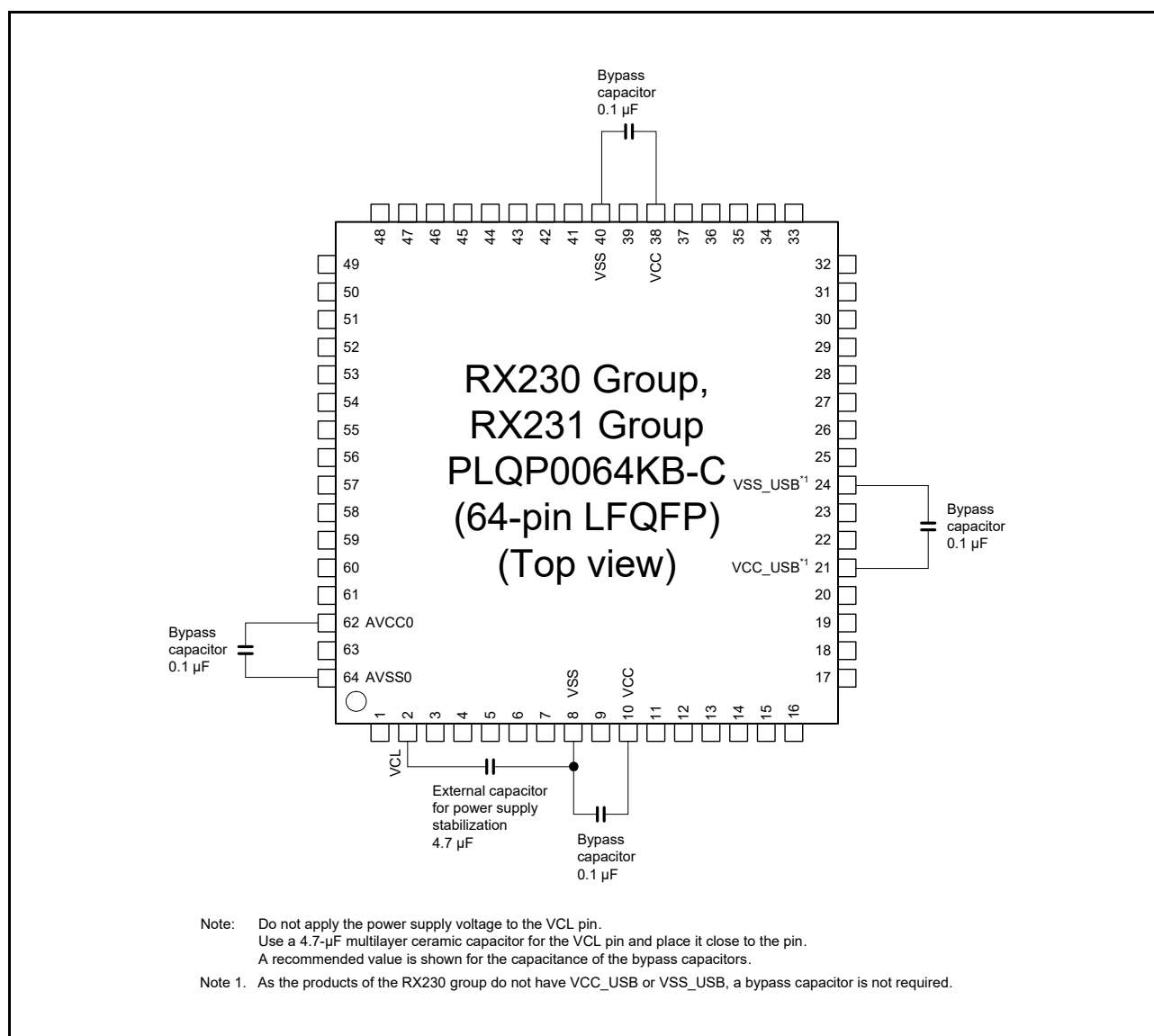
Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V _{POR}	1.35	1.50	1.65	V	Figure 5.73, Figure 5.74
	Voltage detection circuit (LVD0)* ¹	V _{det0_0}	3.67	3.84	3.97	V	Figure 5.75 At falling edge VCC
		V _{det0_1}	2.70	2.82	3.00		
		V _{det0_2}	2.37	2.51	2.67		
		V _{det0_3}	1.80	1.90	1.99		
	Voltage detection circuit (LVD1)* ²	V _{det1_0}	4.12	4.29	4.42	V	Figure 5.76 At falling edge VCC
		V _{det1_1}	3.98	4.14	4.28		
		V _{det1_2}	3.86	4.02	4.16		
		V _{det1_3}	3.68	3.84	3.98		
		V _{det1_4}	2.99	3.10	3.29		
		V _{det1_5}	2.89	3.00	3.19		
		V _{det1_6}	2.79	2.90	3.09		
		V _{det1_7}	2.68	2.79	2.98		
		V _{det1_8}	2.57	2.68	2.87		
		V _{det1_9}	2.47	2.58	2.67		
		V _{det1_A}	2.37	2.48	2.57		
		V _{det1_B}	2.10	2.20	2.30		
		V _{det1_C}	1.86	1.96	2.06		
		V _{det1_D}	1.80	1.86	1.96		
	Voltage detection circuit (LVD2)* ³	V _{det2_0}	4.08	4.29	4.48	V	Figure 5.77 At falling edge VCC
		V _{det2_1}	3.95	4.14	4.35		
		V _{det2_2}	3.82	4.02	4.22		
		V _{det2_3}	3.62	3.84	4.02		

Note: These characteristics apply when noise is not superimposed on the power supply. When a setting is made so that the voltage detection level overlaps with that of the voltage detection circuit (LVD2), it cannot be specified which of LVD1 and LVD2 is used for voltage detection.

Note 1. n in the symbol V_{det0_n} denotes the value of the OFS1.VDSEL[1:0] bits.

Note 2. n in the symbol V_{det1_n} denotes the value of the LVDLVLRLVD1LVL[3:0] bits.

Note 3. n in the symbol V_{det2_n} denotes the value of the LVDLVLRLVD2LVL[1:0] bits.

**Figure 5.81 Connecting Capacitors (64 Pins)**

Rev.	Date	Description		Classification
		Page	Summary	
1.10	Oct 30, 2015	142	Table 5.45 A/D Conversion Characteristics (1): Conditions and Voltage Range of Analog Input (Max.), changed	
		143	Table 5.46 A/D Conversion Characteristics (2): Conditions changed	
		144	Table 5.47 A/D Conversion Characteristics (3): Conditions changed	
		145	Table 5.48 A/D Conversion Characteristics (4): Conditions changed	
		146	Table 5.49 A/D Conversion Characteristics (5): Conditions changed and Absolute accuracy (Test Conditions) deleted	
		153	Table 5.57 Characteristics of Power-On Reset Circuit and Voltage Detection Circuit (1), changed	TN-RX*-A137A/E
		154	Table 5.58 Characteristics of Power-On Reset Circuit and Voltage Detection Circuit (2), changed	
		155	Figure 5.73 Power-On Reset Timing and Figure 5.74 Voltage Detection Circuit Timing (Vdet0), changed	
		159	Table 5.62 ROM (Flash Memory for Code Storage) Characteristics (2) High-Speed Operating Mode: Note changed	
		160	Table 5.63 ROM (Flash Memory for Code Storage) Characteristics (3) Middle-Speed Operating Mode: Note changed	
		161	Table 5.65 E2 DataFlash Characteristics (2): high-speed operating mode, Note changed	
		161	Table 5.66 E2 DataFlash Characteristics (3): middle-speed operating mode, Conditions and Note changed	
		163	Figure 5.79 Connecting Capacitors (100 Pins), changed	
		164	Figure 5.80 Connecting Capacitors (64 Pins), changed	
		165	Figure 5.81 Connecting Capacitors (48 Pins), changed	
		Appendix 1. Package Dimensions		
		167	Figure B 100 -Pin LQFP (PLQP0100KB-B), changed	TN-RX*-A137A/E
		170	Figure E 64 -Pin LQFP (PLQP0064KB-C), changed	TN-RX*-A137A/E
		172	Figure G 48 -Pin LQFP (PLQP0048KB-B), changed	TN-RX*-A137A/E
1.20	Sep 28, 2018	Features		
		1	SD host interface (optional: one channel) SD memory/ SDIO 1-bit or 4-bit SD bus supported, Note deleted	TN-RX*-A145A/E
		1. Overview		
		6	Table 1.2 Comparison of Functions for Different Packages, changed (deletion of IRQ2 on 64-pin package)	
		6	Table 1.2 Comparison of Functions for Different Packages, Note 1 added	TN-RX*-A145A/E
		7	Table 1.3 List of Products: D Version (Ta = -40 to +85°C) (1/2), changed	TN-RX*-A145A/E
		9	Table 1.4 List of Products: G Version (Ta = -40 to +105°C) (1/2), changed	TN-RX*-A145A/E
		11	Figure 1.1 How to Read the Product Part Number, changed	TN-RX*-A145A/E
		16	Table 1.5 Pin Functions (4/4), changed (changes in description for VCC_USB)	TN-RX*-A201A/E
		24	Table 1.6 List of Pins and Pin Functions (100-Pin TFLGA) (2/3), changed (UPSEL was added to the column of P35)	
		24	Table 1.6 List of Pins and Pin Functions (100-Pin TFLGA) (2/3), changed (USB0_VBUS was added to the column of PB5)	
		26	Table 1.7 List of Pins and Pin Functions (100-Pin LQFP) (1/3), changed (UPSEL was added to the column of P35)	
		29	Table 1.8 List of Pins and Pin Functions (64-Pin WFLGA) (1/2), changed (UPSEL was added to the column of P35)	
		30	Table 1.8 List of Pins and Pin Functions (64-Pin WFLGA) (2/2), changed (USB0_VBUS was added to the column of PB5)	
		31	Table 1.9 List of Pins and Pin Functions (64-Pin LQFP/HWQFN) (1/2), changed (UPSEL was added to the column of P35)	
		31	Table 1.9 List of Pins and Pin Functions (64-Pin LQFP/HWQFN) (1/2), changed (USB0_VBUS was added to the column of PB5)	
		33	Table 1.10 List of Pins and Pin Functions (48-Pin LQFP/HWQFN) (1/2), changed (UPSEL was added to the column of P35)	
		33	Table 1.10 List of Pins and Pin Functions (48-Pin LQFP/HWQFN) (1/2), changed	TN-RX*-A145A/E
		5. Electrical Characteristics		
		92	Table 5.18 Output Values of Voltage (1), changed	TN-RX*-A201A/E
		92	Table 5.19 Output Values of Voltage (2), changed	TN-RX*-A201A/E