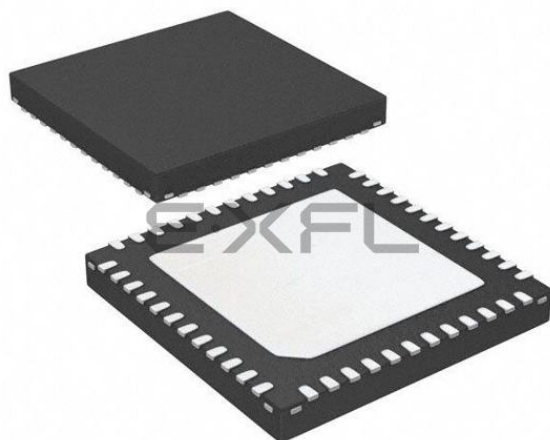




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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	54MHz
Connectivity	CANbus, I ² C, IrDA, SCI, SD/SDIO, SPI, SSI, USB OTG
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	30
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-WFQFN Exposed Pad
Supplier Device Package	48-HWQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f52318adne-u0

1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications, and Table 1.2 gives a comparison of the functions of the products in different packages.

Table 1.1 is for products with the greatest number of functions, so the number of peripheral modules and channels will differ in accordance with the package type. For details, see Table 1.2, Comparison of Functions for Different Packages.

Table 1.1 Outline of Specifications (1/4)

Classification	Module/Function	Description
CPU	CPU	- Maximum operating frequency: 54 MHz 32-bit RX CPU (RX v2) - Minimum instruction execution time: One instruction per clock cycle - Address space: 4-Gbyte linear - Register set - General purpose: Sixteen 32-bit registers - Control: Ten 32-bit registers - Accumulator: Two 72-bit registers - Basic instructions: 75 (variable-length instruction format) - Floating-point instructions: 11 - DSP instructions: 23 - Addressing modes: 10 - Data arrangement - Instructions: Little endian - Data: Selectable as little endian or big endian - On-chip 32-bit multiplier: 32-bit × 32-bit → 64-bit - On-chip divider: 32-bit ÷ 32-bit → 32 bits - Barrel shifter: 32 bits - Memory protection unit (MPU)
	FPU	- Single precision (32-bit) floating point - Data types and floating-point exceptions in conformance with the IEEE754 standard
Memory	ROM	- Capacity: 128/256/384/512 Kbytes - Up to 32 MHz: No-wait memory access 32 to 54 MHz: Wait state required. No wait state if the instruction is served by a ROM accelerator hit. - Programming/erasing method: - Serial programming (asynchronous serial communication/USB communication), self-programming
	RAM	- Capacity: 32/64 Kbytes 54 MHz, no-wait memory access
	E2 DataFlash	- Capacity: 8 Kbytes - Number of erase/write cycles: 1,000,000 (typ)
MCU operating mode		Single-chip mode, on-chip ROM enabled expansion mode, and on-chip ROM disabled expansion mode (software switching)
Clock	Clock generation circuit	- Main clock oscillator, sub-clock oscillator, low-speed on-chip oscillator, high-speed on-chip oscillator, PLL frequency synthesizer, USB-dedicated PLL frequency synthesizer, and IWDG-dedicated on-chip oscillator - Oscillation stop detection: Available - Clock frequency accuracy measurement circuit (CAC) - Independent settings for the system clock (ICLK), peripheral module clock (PCLK), external bus clock (BCLK), and FlashIF clock (FCLK) - The CPU and system sections such as other bus masters run in synchronization with the system clock (ICLK): 54 MHz (at max.) - MTU2a runs in synchronization with the PCLKA: 54 MHz (at max.) - The ADCLK for the S12AD runs in synchronization with the PCLKD: 54 MHz (at max.) - Peripheral modules other than MTU2a and S12ADE run in synchronization with the PCLKB: 32 MHz (at max.) - Devices connected to external buses run in synchronization with the BCLK: 32 MHz (at max.) - The flash peripheral circuit runs in synchronization with the FCLK: 32 MHz (at max.)
Resets		RES# pin reset, power-on reset, voltage monitoring reset, watchdog timer reset, independent watchdog timer reset, and software reset
Voltage detection	Voltage detection circuit (LVDAb)	- When the voltage on VCC falls below the voltage detection level, an internal reset or internal interrupt is generated. - Voltage detection circuit 0 is capable of selecting the detection voltage from 4 levels - Voltage detection circuit 1 is capable of selecting the detection voltage from 14 levels - Voltage detection circuit 2 is capable of selecting the detection voltage from 4 levels

Table 1.2 Comparison of Functions for Different Packages

Module/Functions		RX230 Group			RX231 Group		
		100 Pins	64 Pins	48 Pins	100 Pins	64 Pins	48 Pins
External bus	External bus	16 bit	Not supported		16 bit	Not supported	
Interrupts	External interrupts	NMI, IRQ0 to IRQ7	NMI, IRQ0, IRQ1, IRQ4 to IRQ7	NMI, IRQ0, IRQ1, IRQ4 to IRQ7	NMI, IRQ0 to IRQ7	NMI, IRQ0, IRQ1, IRQ4 to IRQ7	NMI, IRQ0, IRQ1, IRQ4 to IRQ7
DMA	DMA controller	4 channels (DMAC0 to DMAC3)			4 channels (DMAC0 to DMAC3)		
	Data transfer controller	Available			Available		
Timers	16-bit timer pulse unit	6 channels (TPU0 to TPU5)			6 channels (TPU0 to TPU5)		
	Multi-function timer pulse unit 2	6 channels (MTU0 to MTU5)			6 channels (MTU0 to MTU5)		
	Port output enable 2	POE0# to POE3#, POE8#			POE0# to POE3#, POE8#		
	8-bit timer	2 channels× 2 units			2 channels× 2 units		
	Compare match timer	2 channels× 2 units			2 channels× 2 units		
	Low power timer	1 channel			1 channel		
	Realtime clock	Available		Not supported	Available		Not supported
	Watchdog timer	Available			Available		
	Independent watchdog timer	Available			Available		
Communication functions	Serial communications interfaces (SCIg)	6 channels (SCI0, 1, 5, 6, 8, 9)	5 channels (SCI1, 5, 6, 8, 9)	4 channels (SCI1, 5, 6, 8)	6 channels (SCI0, 1, 5, 6, 8, 9)	5 channels (SCI1, 5, 6, 8, 9)	4 channels (SCI1, 5, 6, 8)
	IrDA interface	1 channel (SCI5)			1 channel (SCI5)		
	Serial communications interfaces (SCIh)	1 channel (SCI12)			1 channel (SCI12)		
	I ² C bus interface	1 channel			1 channel		
	CAN module	Not supported			1 channel*1		
	Serial peripheral interface	1 channel			1 channel		
	USB 2.0 host/function module	Not supported			1 channel		
	Serial sound interface	1 channel			1 channel		
	SD Host Interface	Not supported			1 channel*1		Not supported
Capacitive touch sensing unit		24 channels	10 channels	6 channels	24 channels	10 channels	6 channels
12-bit A/D converter (including high-precision channels)		24 channels (8 channels)	12 channels (6 channels)	8 channels (4 channels)	24 channels (8 channels)	12 channels (6 channels)	8 channels (4 channels)
Temperature sensor		Available			Available		
D/A converter		2 channels		Not supported	2 channels		Not supported
CRC calculator		Available			Available		
Event link controller		Available			Available		
Comparator B		4 channels			4 channels		
Packages		100-pin TFLGA 100-pin LFQFP	64-pin WFLGA 64-pin HWQFN 64-pin LFQFP	48-pin HWQFN 48-pin LFQFP	100-pin TFLGA 100-pin LFQFP	64-pin WFLGA 64-pin HWQFN 64-pin LFQFP	48-pin HWQFN 48-pin LFQFP

Note 1. Only for chip version B

1.2 List of Products

Table 1.3 and Table 1.4 are a list of products, and Figure 1.1 shows how to read the product part no., memory capacity, and package type.

Table 1.3 List of Products: D Version (T_a = –40 to +85°C) (1/2)

Group	Part No.	Order Part No.	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency	Security Function	SDHI	CAN	Operating Temperature
RX231	R5F52318ADLA	R5F52318ADLA#20	PTLG0100KA-A	512 Kbytes	64 Kbytes	8 Kbytes	54 MHz	Not available	Not available	Available	–40 to +85°C
	R5F52318BDLA	R5F52318BDLA#20						Available	Available	Available	
	R5F52318ADFP	R5F52318ADFP#30	PLQP0100KB-B					Not available	Not available	Available	
	R5F52318BDFP	R5F52318BDFP#30						Available	Available	Available	
	R5F52318ADND	R5F52318ADND#U0	PWQN0064KC-A					Not available	Not available	Available	
	R5F52318BDND	R5F52318BDND#U0						Available	Available	Available	
	R5F52318ADFM	R5F52318ADFM#30	PLQP0064KB-C					Not available	Not available	Available	
	R5F52318BDFM	R5F52318BDFM#30						Available	Available	Available	
	R5F52318ADNE	R5F52318ADNE#U0	PWQN0048KB-A					Not available	Not available	Available	
	R5F52318BDNE	R5F52318BDNE#U0						Available	Not available	Available	
	R5F52318ADFL	R5F52318ADFL#30	PLQP0048KB-B					Not available	Not available	Available	
	R5F52318BDFL	R5F52318BDFL#30						Available	Not available	Available	
	R5F52317ADLA	R5F52317ADLA#20	PTLG0100KA-A	384 Kbytes				Not available	Not available	Available	
	R5F52317BDLA	R5F52317BDLA#20						Available	Available	Available	
	R5F52317ADFP	R5F52317ADFP#30	PLQP0100KB-B					Not available	Not available	Available	
	R5F52317BDFP	R5F52317BDFP#30						Available	Available	Available	
	R5F52317ADND	R5F52317ADND#U0	PWQN0064KC-A					Not available	Not available	Available	
	R5F52317BDND	R5F52317BDND#U0						Available	Available	Available	
	R5F52317ADFM	R5F52317ADFM#30	PLQP0064KB-C					Not available	Not available	Available	
	R5F52317BDFM	R5F52317BDFM#30						Available	Available	Available	
	R5F52317ADNE	R5F52317ADNE#U0	PWQN0048KB-A					Not available	Not available	Available	
	R5F52317BDNE	R5F52317BDNE#U0						Available	Not available	Available	
	R5F52317ADFL	R5F52317ADFL#30	PLQP0048KB-B					Not available	Not available	Available	
	R5F52317BDFL	R5F52317BDFL#30						Available	Not available	Available	
	R5F52316ADLA	R5F52316ADLA#20	PTLG0100KA-A	256 Kbytes	32 Kbytes			Not available	Not available	Available	
	R5F52316CDLA	R5F52316CDLA#20						Not available	Not available	Not available	
	R5F52316ADFP	R5F52316ADFP#30	PLQP0100KB-B					Not available	Not available	Available	
	R5F52316CDFP	R5F52316CDFP#30						Not available	Not available	Not available	
	R5F52316CDLF	R5F52316CDLF#U0	PWL0064KA-A					Not available	Not available	Not available	
	R5F52316ADND	R5F52316ADND#U0	PWQN0064KC-A					Not available	Not available	Available	
	R5F52316CDND	R5F52316CDND#U0						Not available	Not available	Not available	
	R5F52316ADFM	R5F52316ADFM#30	PLQP0064KB-C					Not available	Not available	Available	
	R5F52316CDFM	R5F52316CDFM#30						Not available	Not available	Not available	
	R5F52316ADNE	R5F52316ADNE#U0	PWQN0048KB-A					Not available	Not available	Available	
	R5F52316CDNE	R5F52316CDNE#U0						Not available	Not available	Not available	

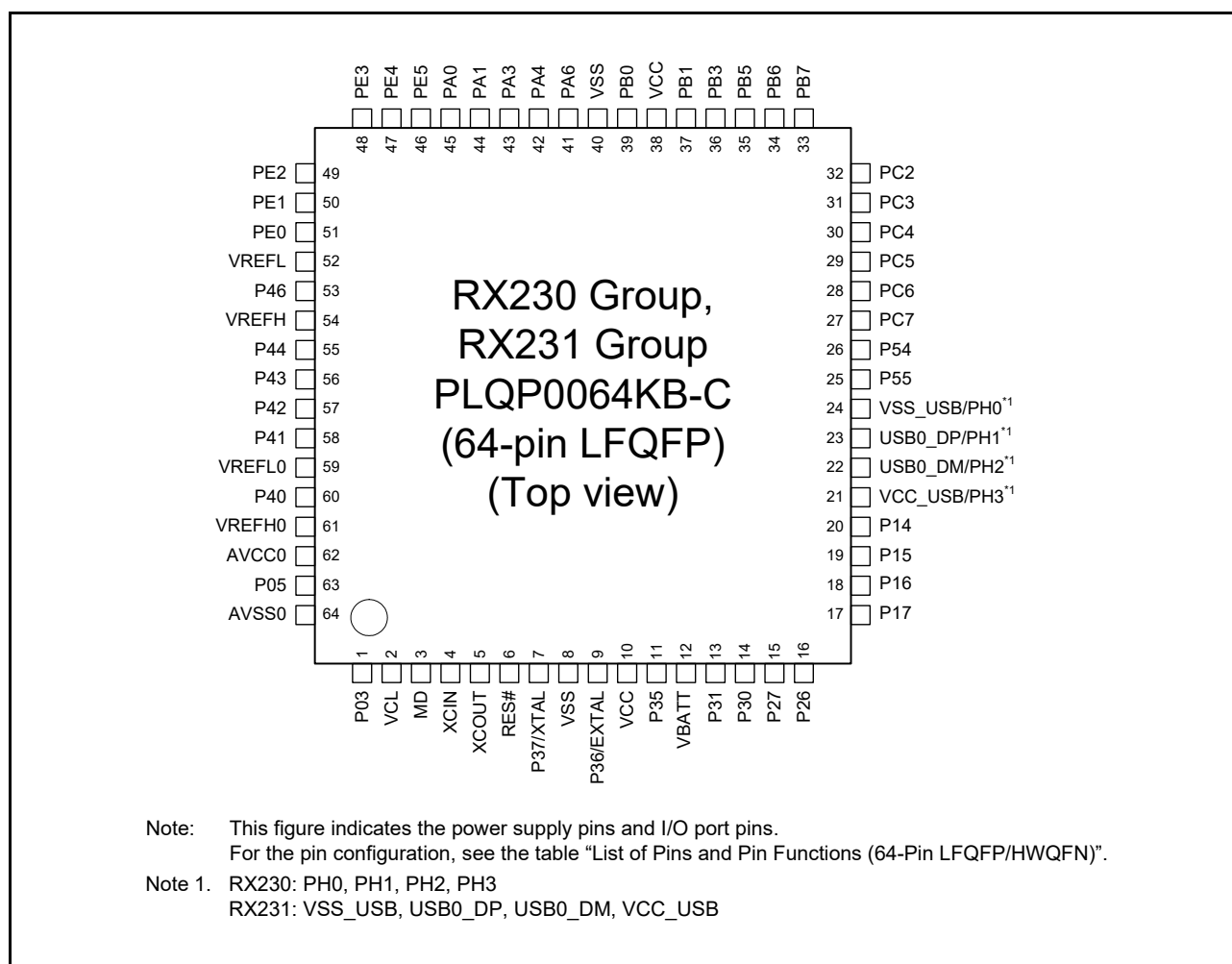
**Figure 1.7 Pin Assignments of the 64-Pin LFQFP**

Table 1.9 List of Pins and Pin Functions (64-Pin LFQFP/HWQFN) (1/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCI, RSPI, IIC, RSCAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
1		P03					DA0
2	VCL						
3	MD						FINED
4	XCIN						
5	XCOUT						
6	RES#						
7	XTAL	P37					
8	VSS						
9	EXTAL	P36					
10	VCC						
11	UPSEL	P35					NMI
12	VBATT						
13		P31	MTIOC4D/TMC12/RTCIC1	CTS1#/RTS1#/SS1#/SSISCK0			IRQ1
14		P30	MTIOC4B/TMRI3/POE8#/RTCIC0	RXD1/SMISO1/SSCL1/AUDIO_MCLK			IRQ0/CMPOB3
15		P27	MTIOC2B/TMC13	SCK1/SSIWS0		TS2	CVREFB3
16		P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1/USB0_VBUSEN/SSIRXD0		TS3	CMPB3
17		P17	MTIOC3A/MTIOC3B/TMO1/POE8#/TIOCB0/TCLKD	SCK1/MISOA/SDA/SSITXD0			IRQ7/ CMPOB2
18		P16	MTIOC3C/MTIOC3D/TMO2/TIOCB1/TCLKC/RTXCOUT	TXD1/SMOSI1/SSDA1/MOSIA/SCL/USB0_VBUS/USB0_VBUSEN/USB0_OVRCURB			IRQ6/ADTRG0#
19		P15	MTIOC0B/MTCLKB/TMC12/TIOCB2/TCLKB	RXD1/SMISO1/SSCL1/CRXD0		TS12	IRQ5/CMPB2
20		P14	MTIOC3A/MTCLKA/TMRI2/TIOCB5/TCLKA	CTS1#/RTS1#/SS1#/CTXD0/USB0_OVRCURA		TS13	IRQ4/CVREFB2
21	VCC_USB*1	PH3*1	TMC10*1				
22		PH2*1	TMRI0*1	USB0_DM*1			IRQ1*1
23		PH1*1	TMO0*1	USB0_DP*1			IRQ0*1
24	VSS_USB*1	PH0*1					CACREF*1
25		P55	MTIOC4D/TMO3	CRXD0		TS15	
26		P54	MTIOC4B/TMC11	CTXD0		TS16	
27	UB	PC7	MTIOC3A/MTCLKB/TMO2	TXD8/SMOSI8/SSDA8/MISOA			CACREF
28		PC6	MTIOC3C/MTCLKA/TMC12	RXD8/SMISO8/SSCL8/MOSIA/USB0_EXICEN		TS22	
29		PC5	MTIOC3B/MTCLKD/TMRI2	SCK8/RSPCKA/USB0_ID		TS23	
30		PC4	MTIOC3D/MTCLKC/TMC11/POE0#	SCK5/CTS8#/RTS8#/SS8#/SSLA0	SDHI_D1	TSCAP	
31		PC3	MTIOC4D/TCLKB	TXD5/SMOSI5/SSDA5/ IRTXD5	SDHI_D0	TS27	
32		PC2	MTIOC4B/TCLKA	RXD5/SMISO5/SSCL5/SSLA3/IRRXD5	SDHI_D3	TS30	
33		PB7/PC1	MTIOC3B/TIOCB5	TXD9/SMOSI9/SSDA9	SDHI_D2		
34		PB6/PC0	MTIOC3D/TIOCA5	RXD9/SMISO9/SSCL9	SDHI_D1		
35		PB5	MTIOC2A/MTIOC1B/TMRI1/POE1#/TIOCB4	SCK9/USB0_VBUS	SDHI_CD		
36		PB3	MTIOC0A/MTIOC4A/TMO0/POE3#/TIOCD3/TCLKD	SCK6	SDHI_W P		
37		PB1	MTIOC0C/MTIOC4C/TMC10/TIOCB3	TXD6/SMOSI6/SSDA6	SDHI_CL K		IRQ4/ CMPOB1
38	VCC						
39		PB0	MTIC5W/TIOCA3	RXD6/SMISO6/SSCL6/RSPCKA	SDHI_C MD		
40	VSS						
41		PA6	MTIC5V/MTCLKB/TMC13/POE2#/TIOCA2	CTS5#/RTS5#/SS5#/MOSIA/SSIWS0			

Table 1.10 List of Pins and Pin Functions (48-Pin LFQFP/HWQFN) (1/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCI, RSPI, IIC, RSCAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
1	VCL						
2	MD						FINED
3	RES#						
4	XTAL	P37					
5	VSS						
6	EXTAL	P36					
7	VCC						
8	UPSEL	P35					NMI
9		P31	MTIOC4D/TMC12	CTS1#/RTS1#/SS1#/SSISCK0			IRQ1
10		P30	MTIOC4B/TMRI3/POE8#	RXD1/SMISO1/SSCL1/AUDIO_MCLK			IRQ0/CMPOB3
11		P27	MTIOC2B/TMC13	SCK1/SSIWS0		TS2	CVREFB3
12		P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1/USB0_VBUSEN/SSIRXD0		TS3	CMPB3
13		P17	MTIOC3A/MTIOC3B/TMO1/POE8#/TIOCB0/TCLKD	SCK1/MISOA/SDA/ SSITXD0			IRQ7/ CMPOB2
14		P16	MTIOC3C/MTIOC3D/TMO2/TIOCB1/TCLKC	TXD1/SMOSI1/SSDA1/MOSIA/SCL/USB0_VBUS/USB0_VBUSEN/USB0_OVRCURB			IRQ6/ADTRG0#
15		P15	MTIOC0B/MTCLKB/TMC12/TIOCB2/TCLKB	RXD1/SMISO1/SSCL1/CRXD0		TS12	IRQ5/CMPB2
16		P14	MTIOC3A/MTCLKA/TMRI2/TIOCB5/TCLKA	CTS1#/RTS1#/SS1#/CTXD0/USB0_OVRCURA		TS13	IRQ4/CVREFB2
17	VCC_USB*1	PH3*1	TMC10*1				
18		PH2*1	TMRI0*1	USB0_DM*1			IRQ1*1
19		PH1*1	TMO0*1	USB0_DP*1			IRQ0*1
20	VSS_USB*1	PH0*1					CACREF*1
21	UB	PC7	MTIOC3A/MTCLKB/TMO2	TXD8/SMOSI8/SSDA8/MISOA			CACREF
22		PC6	MTIOC3C/MTCLKA/TMC12	RXD8/SMISO8/SSCL8/MOSIA/USB0_EXICEN		TS22	
23		PC5	MTIOC3B/MTCLKD/TMRI2	SCK8/RSPCKA/USB0_ID		TS23	
24		PC4	MTIOC3D/MTCLKC/TMC11/POE0#	SCK5/CTS8#/RTS8#/SS8#/SSLA0		TSCAP	
25		PB5/PC3	MTIOC2A/MTIOC1B/TMRI1/POE1#/TIOCB4	USB0_VBUS			
26		PB3/PC2	MTIOC0A/MTIOC4A/TMO0/POE3#/TIOCD3/TCLKD	SCK6			
27		PB1/PC1	MTIOC0C/MTIOC4C/TMC10/TIOCB3	TXD6/SMOSI6/SSDA6			IRQ4/ CMPOB1
28	VCC						
29		PB0/PC0	MTIC5W/TIOCA3	RXD6/SMISO6/SSCL6/RSPCKA			
30	VSS						
31		PA6	MTIC5V/MTCLKB/TMC13/POE2#/TIOCA2	CTS5#/RTS5#/SS5#/MOSIA/SSIWS0			
32		PA4	MTIC5U/MTCLKA/TMRI0/TIOCA1	TXD5/SMOSI5/SSDA5/SSLA0/SSITXD0/IRTXD5			IRQ5 /CVREFB1
33		PA3	MTIOC0D/MTCLKD/TIOCD0/TCLKB	RXD5/SMISO5/SSCL5/SSIRXD0/IRRXD5			IRQ6 /CMPB1
34		PA1	MTIOC0B/MTCLKC/TIOCB0	SCK5/SSLA2/SSISCK0			
35		PE4	MTIOC4D/MTIOC1A				AN020/CMPA2/CLKOUT
36		PE3	MTIOC4B/POE8#	CTS12#/RTS12#/AUDIO_MCLK			AN019/CLKOUT
37		PE2	MTIOC4A	RXD12/RXDX12/SSCL12			IRQ7/AN018/CVREFB0
38		PE1	MTIOC4C	TXD12/TXDX12/SIOX12/SSDA12			AN017/CMPB0
39	VREFL						
40		P46					AN006
41	VREFH						

2. CPU

Figure 2.1 shows register set of the CPU.

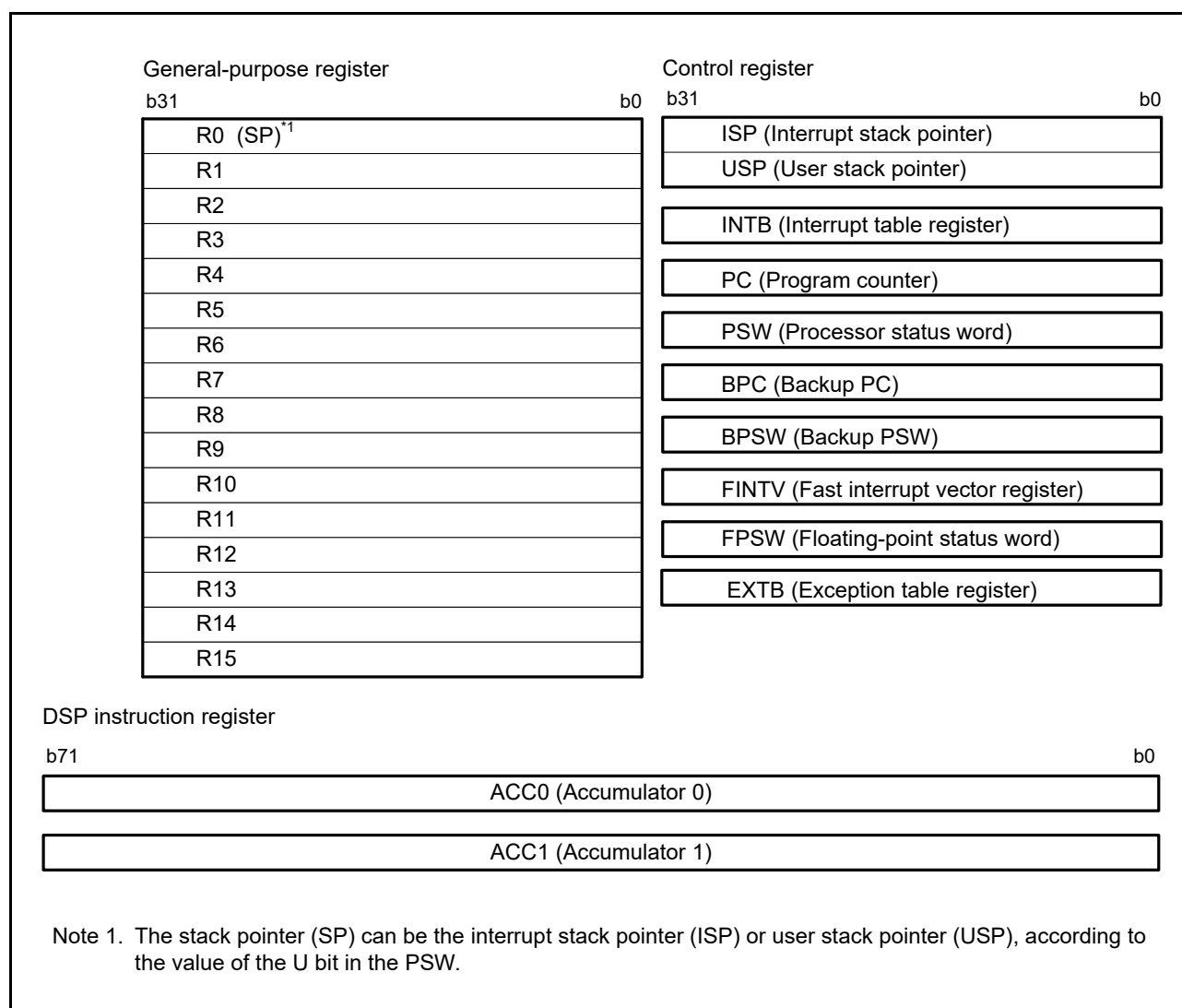


Figure 2.1 Register Set of the CPU

Table 4.1 List of I/O Registers (Address Order) (6/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
0008 8158h	TPU4	Timer General Register A	TGRA	16	16	2 or 3 PCLKB	2 ICLK
0008 815Ah	TPU4	Timer General Register B	TGRB	16	16	2 or 3 PCLKB	2 ICLK
0008 8160h	TPU5	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8161h	TPU5	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB	2 ICLK
0008 8162h	TPU5	Timer I/O Control Register	TIOR	8	8	2 or 3 PCLKB	2 ICLK
0008 8164h	TPU5	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB	2 ICLK
0008 8165h	TPU5	Timer Status Register	TSR	8	8	2 or 3 PCLKB	2 ICLK
0008 8166h	TPU5	Timer Counter	TCNT	16	16	2 or 3 PCLKB	2 ICLK
0008 8168h	TPU5	Timer General Register A	TGRA	16	16	2 or 3 PCLKB	2 ICLK
0008 816Ah	TPU5	Timer General Register B	TGRB	16	16	2 or 3 PCLKB	2 ICLK
0008 8200h	TMR0	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8201h	TMR1	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8202h	TMR0	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB	2 ICLK
0008 8203h	TMR1	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB	2 ICLK
0008 8204h	TMR0	Time Constant Register A	TCORA	8	8	2 or 3 PCLKB	2 ICLK
0008 8205h	TMR1	Time Constant Register A	TCORA	8	8*1	2 or 3 PCLKB	2 ICLK
0008 8206h	TMR0	Time Constant Register B	TCORB	8	8	2 or 3 PCLKB	2 ICLK
0008 8207h	TMR1	Time Constant Register B	TCORB	8	8*1	2 or 3 PCLKB	2 ICLK
0008 8208h	TMR0	Timer Counter	TCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 8209h	TMR1	Timer Counter	TCNT	8	8*1	2 or 3 PCLKB	2 ICLK
0008 820Ah	TMR0	Timer Counter Control Register	TCCR	8	8	2 or 3 PCLKB	2 ICLK
0008 820Bh	TMR1	Timer Counter Control Register	TCCR	8	8*1	2 or 3 PCLKB	2 ICLK
0008 820Ch	TMR0	Timer Count Start Register	TCSTR	8	8	2 or 3 PCLKB	2 ICLK
0008 8210h	TMR2	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8211h	TMR3	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8212h	TMR2	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB	2 ICLK
0008 8213h	TMR3	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB	2 ICLK
0008 8214h	TMR2	Time Constant Register A	TCORA	8	8	2 or 3 PCLKB	2 ICLK
0008 8215h	TMR3	Time Constant Register A	TCORA	8	8*1	2 or 3 PCLKB	2 ICLK
0008 8216h	TMR2	Time Constant Register B	TCORB	8	8	2 or 3 PCLKB	2 ICLK
0008 8217h	TMR3	Time Constant Register B	TCORB	8	8*1	2 or 3 PCLKB	2 ICLK
0008 8218h	TMR2	Timer Counter	TCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 8219h	TMR3	Timer Counter	TCNT	8	8*1	2 or 3 PCLKB	2 ICLK
0008 821Ah	TMR2	Timer Counter Control Register	TCCR	8	8	2 or 3 PCLKB	2 ICLK
0008 821Bh	TMR3	Timer Counter Control Register	TCCR	8	8*1	2 or 3 PCLKB	2 ICLK
0008 821Ch	TMR2	Timer Count Start Register	TCSTR	8	8	2 or 3 PCLKB	2 ICLK
0008 8280h	CRC	CRC Control Register	CRCCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8281h	CRC	CRC Data Input Register	CRCDIR	8	8	2 or 3 PCLKB	2 ICLK
0008 8282h	CRC	CRC Data Output Register	CRCDOR	16	16	2 or 3 PCLKB	2 ICLK
0008 8300h	RIIC0	I ² C-Bus Control Register 1	ICCR1	8	8	2 or 3 PCLKB	2 ICLK
0008 8301h	RIIC0	I ² C-Bus Control Register 2	ICCR2	8	8	2 or 3 PCLKB	2 ICLK
0008 8302h	RIIC0	I ² C-Bus Mode Register 1	ICMR1	8	8	2 or 3 PCLKB	2 ICLK
0008 8303h	RIIC0	I ² C-Bus Mode Register 2	ICMR2	8	8	2 or 3 PCLKB	2 ICLK
0008 8304h	RIIC0	I ² C-Bus Mode Register 3	ICMR3	8	8	2 or 3 PCLKB	2 ICLK
0008 8305h	RIIC0	I ² C-Bus Function Enable Register	ICFER	8	8	2 or 3 PCLKB	2 ICLK
0008 8306h	RIIC0	I ² C-Bus Status Enable Register	ICSER	8	8	2 or 3 PCLKB	2 ICLK
0008 8307h	RIIC0	I ² C-Bus Interrupt Enable Register	ICIER	8	8	2 or 3 PCLKB	2 ICLK
0008 8308h	RIIC0	I ² C-Bus Status Register 1	ICSR1	8	8	2 or 3 PCLKB	2 ICLK
0008 8309h	RIIC0	I ² C-Bus Status Register 2	ICSR2	8	8	2 or 3 PCLKB	2 ICLK
0008 830Ah	RIIC0	Slave Address Register L0	SARL0	8	8	2 or 3 PCLKB	2 ICLK
0008 830Bh	RIIC0	Slave Address Register U0	SARU0	8	8	2 or 3 PCLKB	2 ICLK
0008 830Ch	RIIC0	Slave Address Register L1	SARL1	8	8	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (8/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
0008 901Eh	S12AD	A/D Self-Diagnosis Data Register	ADDRD	16	16	2 or 3 PCLKB	2 ICLK
0008 9020h	S12AD	A/D Data Register 0	ADDR0	16	16	2 or 3 PCLKB	2 ICLK
0008 9022h	S12AD	A/D Data Register 1	ADDR1	16	16	2 or 3 PCLKB	2 ICLK
0008 9024h	S12AD	A/D Data Register 2	ADDR2	16	16	2 or 3 PCLKB	2 ICLK
0008 9026h	S12AD	A/D Data Register 3	ADDR3	16	16	2 or 3 PCLKB	2 ICLK
0008 9028h	S12AD	A/D Data Register 4	ADDR4	16	16	2 or 3 PCLKB	2 ICLK
0008 902Ah	S12AD	A/D Data Register 5	ADDR5	16	16	2 or 3 PCLKB	2 ICLK
0008 902Ch	S12AD	A/D Data Register 6	ADDR6	16	16	2 or 3 PCLKB	2 ICLK
0008 902Eh	S12AD	A/D Data Register 7	ADDR7	16	16	2 or 3 PCLKB	2 ICLK
0008 9040h	S12AD	A/D Data Register 16	ADDR16	16	16	2 or 3 PCLKB	2 ICLK
0008 9042h	S12AD	A/D Data Register 17	ADDR17	16	16	2 or 3 PCLKB	2 ICLK
0008 9044h	S12AD	A/D Data Register 18	ADDR18	16	16	2 or 3 PCLKB	2 ICLK
0008 9046h	S12AD	A/D Data Register 19	ADDR19	16	16	2 or 3 PCLKB	2 ICLK
0008 9048h	S12AD	A/D Data Register 20	ADDR20	16	16	2 or 3 PCLKB	2 ICLK
0008 904Ah	S12AD	A/D Data Register 21	ADDR21	16	16	2 or 3 PCLKB	2 ICLK
0008 904Ch	S12AD	A/D Data Register 22	ADDR22	16	16	2 or 3 PCLKB	2 ICLK
0008 904Eh	S12AD	A/D Data Register 23	ADDR23	16	16	2 or 3 PCLKB	2 ICLK
0008 9050h	S12AD	A/D Data Register 24	ADDR24	16	16	2 or 3 PCLKB	2 ICLK
0008 9052h	S12AD	A/D Data Register 25	ADDR25	16	16	2 or 3 PCLKB	2 ICLK
0008 9055h	S12AD	A/D Data Register 26	ADDR26	16	16	2 or 3 PCLKB	2 ICLK
0008 9056h	S12AD	A/D Data Register 27	ADDR27	16	16	2 or 3 PCLKB	2 ICLK
0008 9058h	S12AD	A/D Data Register 28	ADDR28	16	16	2 or 3 PCLKB	2 ICLK
0008 905Ah	S12AD	A/D Data Register 29	ADDR29	16	16	2 or 3 PCLKB	2 ICLK
0008 905Ch	S12AD	A/D Data Register 30	ADDR30	16	16	2 or 3 PCLKB	2 ICLK
0008 905Eh	S12AD	A/D Data Register 31	ADDR31	16	16	2 or 3 PCLKB	2 ICLK
0008 907Ah	S12AD	A/D Disconnection Detection Control Register	ADDISCR	8	8	2 or 3 PCLKB	2 ICLK
0008 907Dh	S12AD	A/D Event Link Control Register	ADELCCR	8	8	2 or 3 PCLKB	2 ICLK
0008 9080h	S12AD	A/D Group Scan Priority Control Register	ADGSPCR	16	16	2 or 3 PCLKB	2 ICLK
0008 908Ah	S12AD	A/D High-Side/Low-Side Reference Voltage Control Register	ADHVREFCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 908Ch	S12AD	A/D Compare Function Window A/B Status Monitor Register	ADWINMON	8	8	2 or 3 PCLKB	2 ICLK
0008 9090h	S12AD	A/D Compare Function Control Register	ADCMPCR	16	16	2 or 3 PCLKB	2 ICLK
0008 9092h	S12AD	A/D Compare Function Window A Extended Input Select Register	ADCMPSER	8	8	2 or 3 PCLKB	2 ICLK
0008 9093h	S12AD	A/D Compare Function Window A Extended Input Comparison Condition Setting Register	ADCMPLER	8	8	2 or 3 PCLKB	2 ICLK
0008 9094h	S12AD	A/D Compare Function Window A Channel Select Register 0	ADCMPSR0	16	16	2 or 3 PCLKB	2 ICLK
0008 9096h	S12AD	A/D Compare Function Window A Channel Select Register 1	ADCMPSR1	16	16	2 or 3 PCLKB	2 ICLK
0008 9098h	S12AD	A/D Compare Function Window A Comparison Condition Setting Register 0	ADCMPLR0	16	16	2 or 3 PCLKB	2 ICLK
0008 909Ah	S12AD	A/D Compare Function Window A Comparison Condition Setting Register 1	ADCMPLR1	16	16	2 or 3 PCLKB	2 ICLK
0008 909Ch	S12AD	A/D Compare Function Window A Lower-Side Level Setting Register	ADCMPSR0	16	16	2 or 3 PCLKB	2 ICLK
0008 909Eh	S12AD	A/D Compare Function Window A Upper-Side Level Setting Register	ADCMPSR1	16	16	2 or 3 PCLKB	2 ICLK
0008 90A0h	S12AD	A/D Compare Function Window A Channel Status Register 0	ADCMPSR0	16	16	2 or 3 PCLKB	2 ICLK
0008 90A2h	S12AD	A/D Compare Function Window A Channel Status Register 1	ADCMPSR1	16	16	2 or 3 PCLKB	2 ICLK
0008 90A4h	S12AD	A/D Compare Function Window A Extended Input Channel Status Register	ADCMPSER	16	16	2 or 3 PCLKB	2 ICLK
0008 90A6h	S12AD	A/D Compare Function Window B Channel Select Register	ADCMPSNR	8	8	2 or 3 PCLKB	2 ICLK
0008 90A8h	S12AD	A/D Compare Function Window B Lower-Side Level Setting Register	ADWINLLB	16	16	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (19/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK $\geq$ PCLK	ICLK < PCLK
0008 C1B3h	MPC	PE3 Pin Function Control Register	PE3PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1B4h	MPC	PE4 Pin Function Control Register	PE4PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1B5h	MPC	PE5 Pin Function Control Register	PE5PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1B6h	MPC	PE6 Pin Function Control Register	PE6PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1B7h	MPC	PE7 Pin Function Control Register	PE7PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1C8h	MPC	PH0 Pin Function Control Register	PH0PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1C9h	MPC	PH1 Pin Function Control Register	PH1PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1CAh	MPC	PH2 Pin Function Control Register	PH2PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1CBh	MPC	PH3 Pin Function Control Register	PH3PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C1D3h	MPC	PJ3 Pin Function Control Register	PJ3PFS	8	8	2 or 3 PCLKB	2 ICLK
0008 C290h	SYSTEM	Reset Status Register 0	RSTSR0	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C291h	SYSTEM	Reset Status Register 1	RSTSR1	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C293h	SYSTEM	Main Clock Oscillator Forced Oscillation Control Register	MOFCR	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C297h	SYSTEM	Voltage Monitoring Circuit Control Register	LVCMPCR	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C298h	SYSTEM	Voltage Detection Level Select Register	LVDLVL	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C29Ah	SYSTEM	Voltage Monitoring 1 Circuit Control Register 0	LVD1CR0	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C29Bh	SYSTEM	Voltage Monitoring 2 Circuit Control Register 0	LVD2CR0	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C29Dh	SYSTEM	VBATT Control Register	VBATTCT	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C29Eh	SYSTEM	VBATT Status Register	VBATTST	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C29Fh	SYSTEM	VBATT Pin Voltage Drop Detection Interrupt Control Register	VBTLVDICR	8	8	4 or 5 PCLKB	2 or 3 ICLK
0008 C400h	RTC	64-Hz Counter	R64CNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C402h	RTC	Second Counter	RSECCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C402h	RTC	Binary Counter 0	BCNT0	8	8	2 or 3 PCLKB	2 ICLK
0008 C404h	RTC	Minute Counter	RMINCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C404h	RTC	Binary Counter 1	BCNT1	8	8	2 or 3 PCLKB	2 ICLK
0008 C406h	RTC	Hour Counter	RHRCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C406h	RTC	Binary Counter 2	BCNT2	8	8	2 or 3 PCLKB	2 ICLK
0008 C408h	RTC	Day-of-Week Counter	RWKCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C408h	RTC	Binary Counter 3	BCNT3	8	8	2 or 3 PCLKB	2 ICLK
0008 C40Ah	RTC	Date Counter	RDAYCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C40Ch	RTC	Month Counter	RMONCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 C40Eh	RTC	Year Counter	RYRCNT	16	16	2 or 3 PCLKB	2 ICLK
0008 C410h	RTC	Second Alarm Register	RSECAR	8	8	2 or 3 PCLKB	2 ICLK
0008 C410h	RTC	Binary Counter 0 Alarm Register	BCNT0AR	8	8	2 or 3 PCLKB	2 ICLK
0008 C412h	RTC	Minute Alarm Register	RMINAR	8	8	2 or 3 PCLKB	2 ICLK
0008 C412h	RTC	Binary Counter 1 Alarm Register	BCNT1AR	8	8	2 or 3 PCLKB	2 ICLK
0008 C414h	RTC	Hour Alarm Register	RHRAR	8	8	2 or 3 PCLKB	2 ICLK
0008 C414h	RTC	Binary Counter 2 Alarm Register	BCNT2AR	8	8	2 or 3 PCLKB	2 ICLK
0008 C416h	RTC	Day-of-Week Alarm Register	RWKAR	8	8	2 or 3 PCLKB	2 ICLK
0008 C416h	RTC	Binary Counter 3 Alarm Register	BCNT3AR	8	8	2 or 3 PCLKB	2 ICLK
0008 C418h	RTC	Date Alarm Register	RDAYAR	8	8	2 or 3 PCLKB	2 ICLK
0008 C418h	RTC	Binary Counter 0 Alarm Enable Register	BCNT0AER	8	8	2 or 3 PCLKB	2 ICLK
0008 C41Ah	RTC	Month Alarm Register	RMONAR	8	8	2 or 3 PCLKB	2 ICLK
0008 C41Ah	RTC	Binary Counter 1 Alarm Enable Register	BCNT1AER	8	8	2 or 3 PCLKB	2 ICLK
0008 C41Ch	RTC	Year Alarm Register	RYRAR	16	16	2 or 3 PCLKB	2 ICLK
0008 C41Ch	RTC	Binary Counter 2 Alarm Enable Register	BCNT2AER	16	16	2 or 3 PCLKB	2 ICLK
0008 C41Eh	RTC	Year Alarm Enable Register	RYRAREN	8	8	2 or 3 PCLKB	2 ICLK
0008 C41Eh	RTC	Binary Counter 3 Alarm Enable Register	BCNT3AER	8	8	2 or 3 PCLKB	2 ICLK
0008 C422h	RTC	RTC Control Register 1	RCR1	8	8	2 or 3 PCLKB	2 ICLK
0008 C424h	RTC	RTC Control Register 2	RCR2	8	8	2 or 3 PCLKB	2 ICLK
0008 C426h	RTC	RTC Control Register 3	RCR3	8	8	2 or 3 PCLKB	2 ICLK

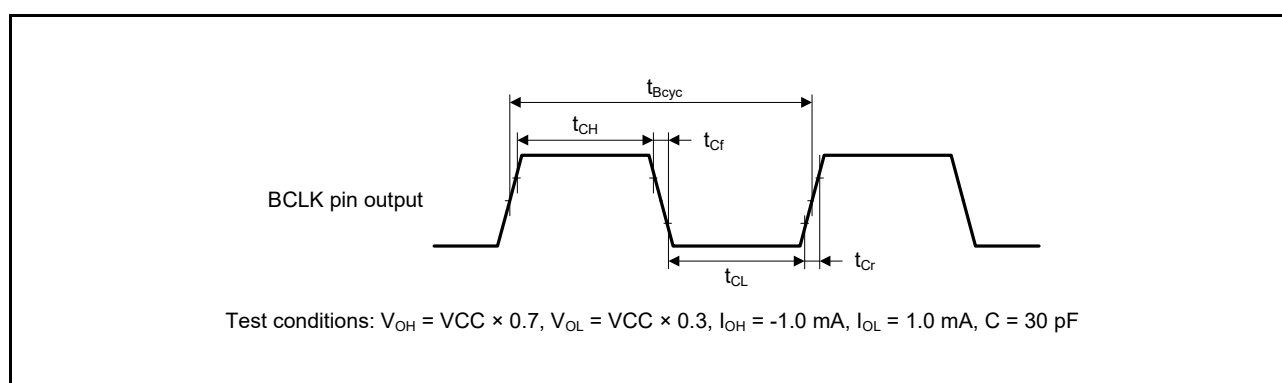


Figure 5.22 BCLK Pin Output Timing

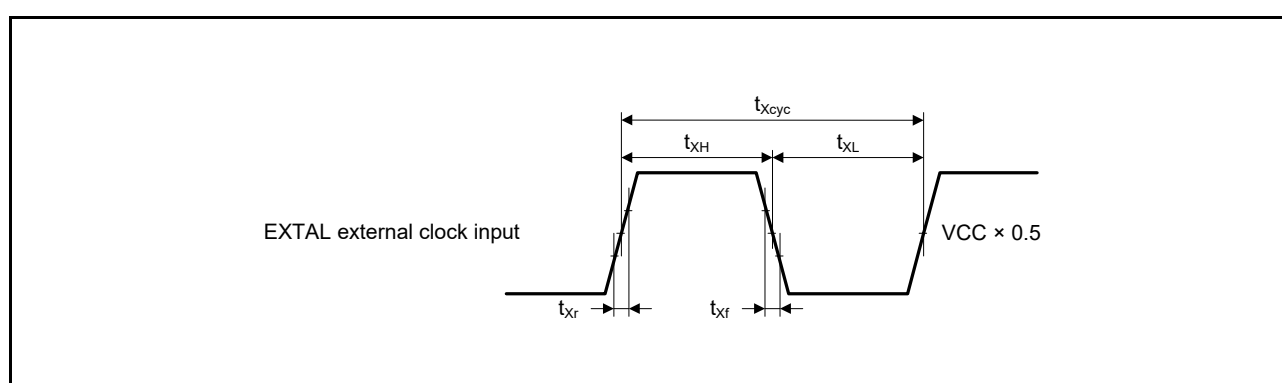


Figure 5.23 EXTAL External Clock Input Timing

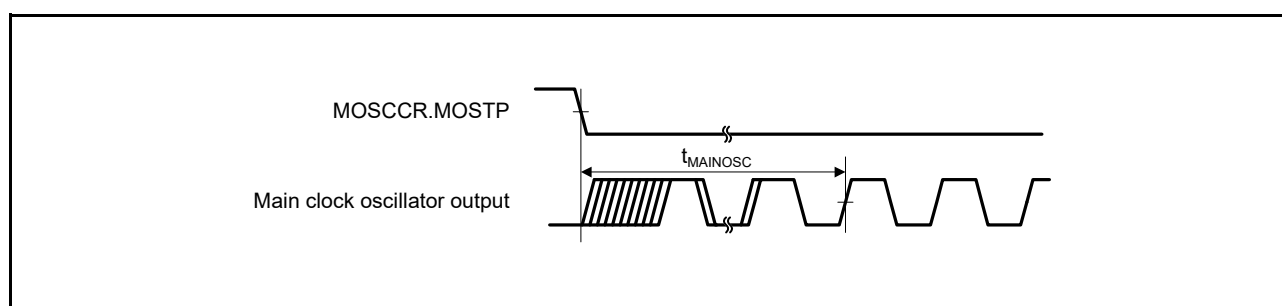


Figure 5.24 Main Clock Oscillation Start Timing

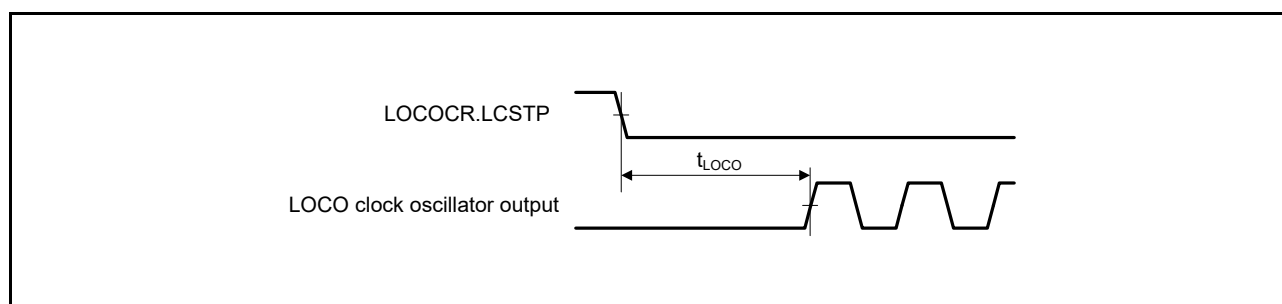


Figure 5.25 LOCO Clock Oscillation Start Timing

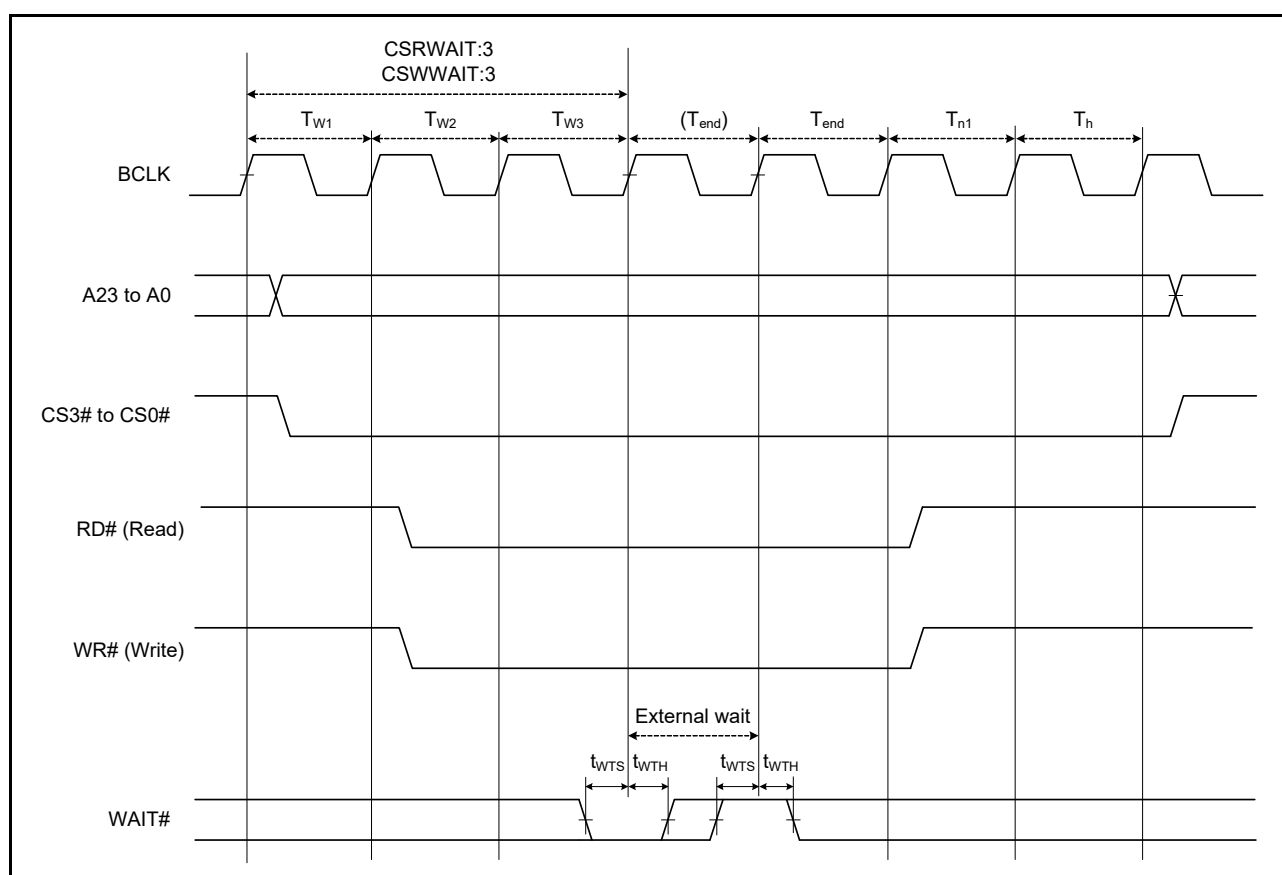


Figure 5.42 External Bus Timing/External Wait Control

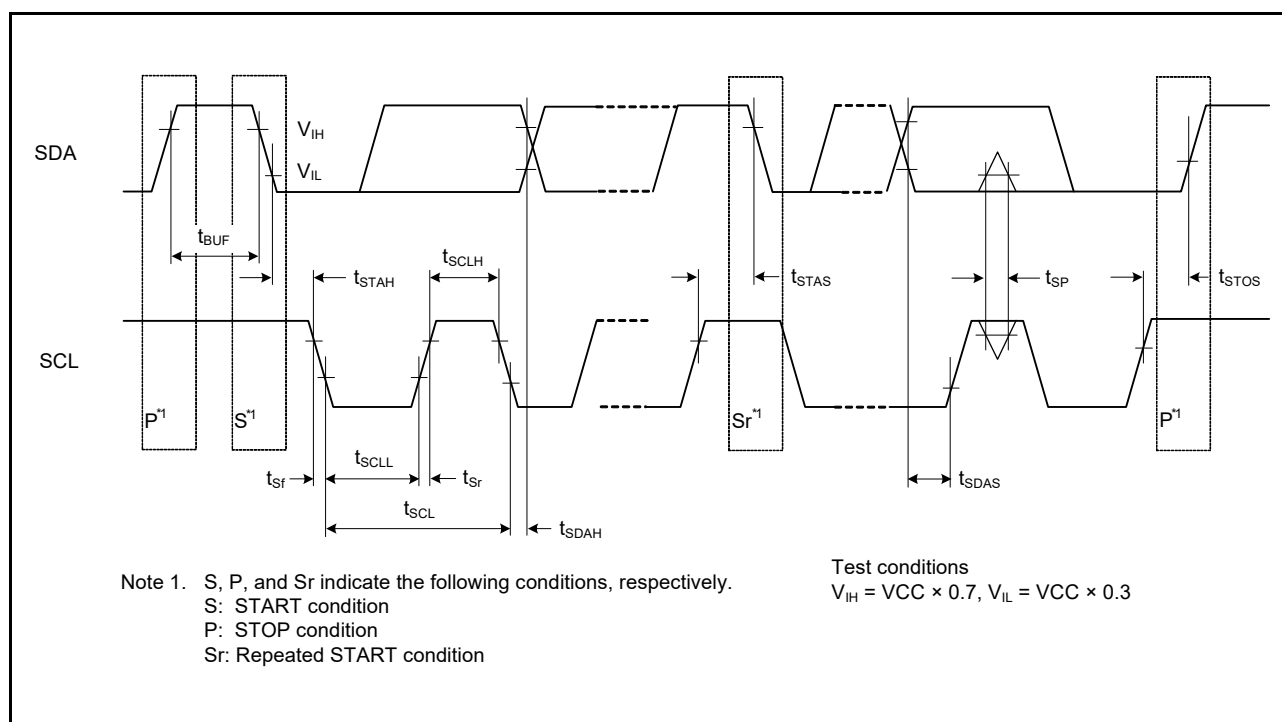
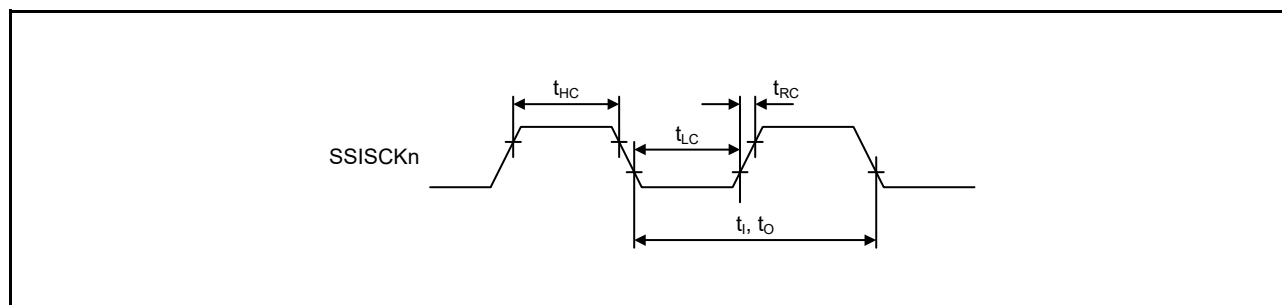
Figure 5.59 RIIC Bus Interface Input/Output Timing and Simple I²C Bus Interface Input/Output Timing

Figure 5.60 SSI Clock Input/Output Timing

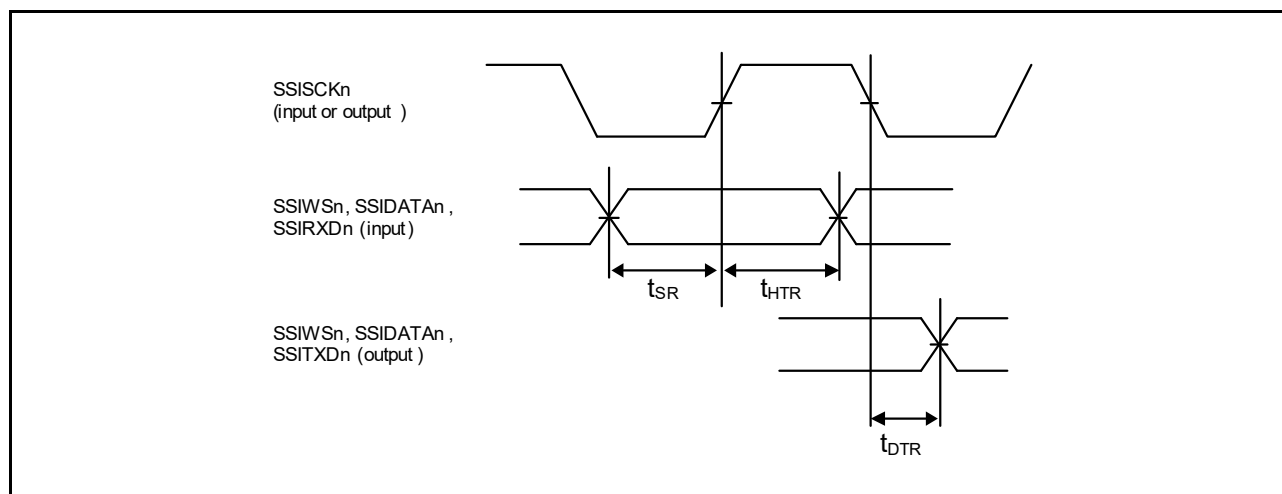


Figure 5.61 SSI Transmission/Reception Timing (SSICR.SCKP=0)

Table 5.48 A/D Conversion Characteristics (3)

Conditions: $2.7V \leq VCC = VCC_USB = AVCC0 \leq 5.5V$, $2.7V \leq VREFH0 \leq AVCC0$, reference voltage = VREFH0 selected, $VSS = AVSS0 = VREFL0 = VSS_USB = 0V$, $T_a = -40$ to $+105^\circ C$

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	27	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 27 MHz)	Permissible signal source impedance (Max.) = 1.1 kΩ	2	—	—	μs	High-precision channel The ADCSR.ADHSC bit is 1 The ADSSTRn.SST[7:0] bits are 0Dh
		3	—	—		Normal-precision channel The ADCSR.ADHSC bit is 1 The ADSSTRn.SST[7:0] bits are 28h
Analog input capacitance	Cs	—	—	15	pF	Pin capacitance included Figure 5.68
Analog input resistance	Rs	—	—	2.5	kΩ	Figure 5.68
Offset error		—	±0.5	±4.5	LSB	
Full-scale error		—	±0.75	±4.5	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential non-linearity error		—	±1.0	—	LSB	
INL integral non-linearity error		—	±1.0	±3.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential non-linearity error, and INL integral non-linearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 5.49 A/D Conversion Characteristics (4)

Conditions: $2.4V \leq VCC = VCC_USB = AVCC0 \leq 5.5V$, $2.4V \leq VREFH0 \leq AVCC0$, $VSS = AVSS0 = VSS_USB = 0V$,
reference voltage = VREFH0 selected, $T_a = -40$ to $+105^\circ C$

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	16	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 16 MHz)	Permissible signal source impedance (Max.) = 2.2 kΩ	3.38	—	—	μs	High-precision channel The ADCSR.ADHSC bit is 1 The ADSSTRn register is 0Dh
		5.06	—	—		Normal-precision channel The ADCSR.ADHSC bit is 1 The ADSSTRn register is 28h
Analog input capacitance	Cs	—	—	15	pF	Pin capacitance included Figure 5.68
Analog input resistance	Rs	—	—	2.5	kΩ	Figure 5.68
Offset error		—	±0.5	±4.5	LSB	
Full-scale error		—	±0.75	±4.5	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential non-linearity error		—	±1.0	—	LSB	
INL integral non-linearity error		—	±1.0	±3.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential non-linearity error, and INL integral non-linearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

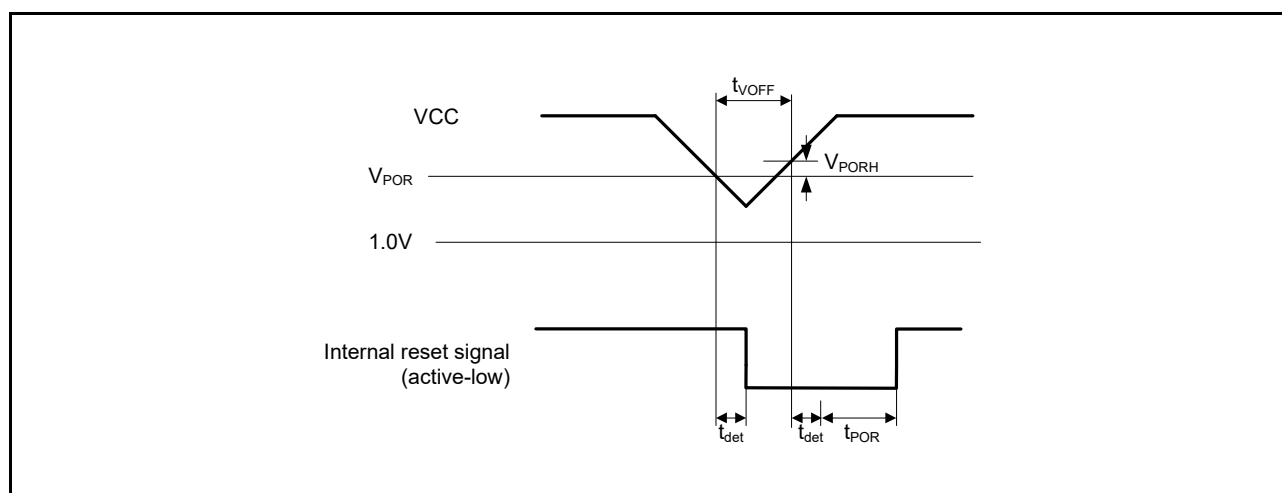


Figure 5.73 Voltage Detection Reset Timing

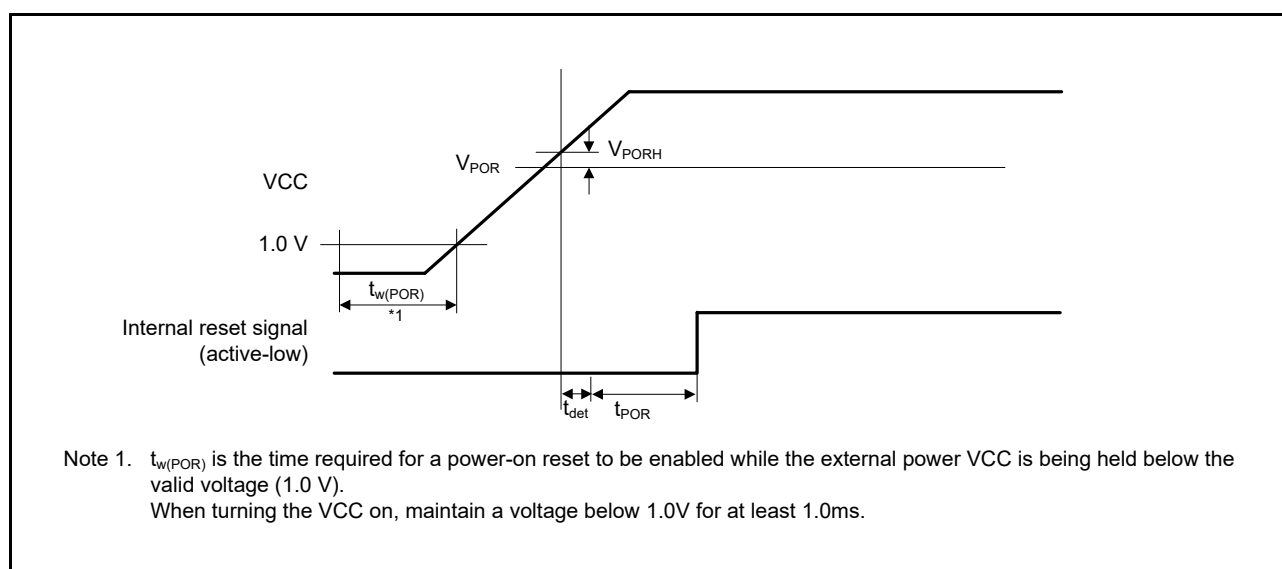


Figure 5.74 Power-On Reset Timing

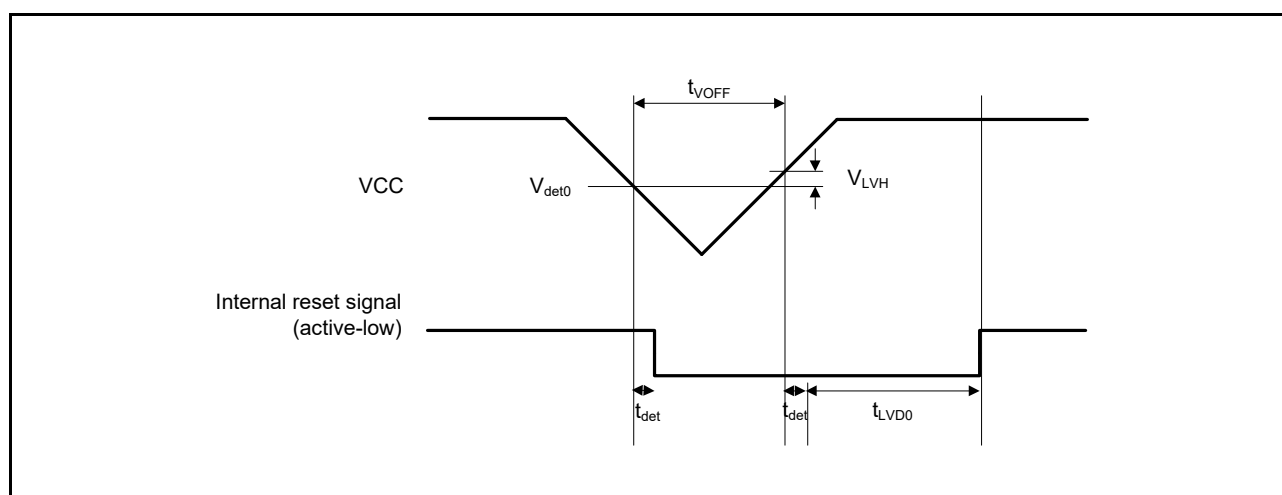


Figure 5.75 Voltage Detection Circuit Timing (Vdet0)

5.15 Usage Notes

5.15.1 Connecting VCL Capacitor and Bypass Capacitors

This MCU integrates an internal voltage-down circuit, which is used for lowering the power supply voltage in the internal MCU automatically to the optimum level. A 4.7- μ F capacitor needs to be connected between this internal voltage-down power supply (VCL pin) and the VSS pin. Figure 5.80 to Figure 5.82 shows how to connect external capacitors. Place an external capacitor close to the pins. Do not apply the power supply voltage to the VCL pin.

Insert a multilayer ceramic capacitor as a bypass capacitor between each pair of the power supply pins. Implement a bypass capacitor as closer to the MCU power supply pins as possible. Use a recommended value of 0.1 μ F as the capacitance of the capacitors. For the capacitors related to crystal oscillation, see section 9, Clock Generation Circuit in the User's Manual: Hardware. For the capacitors related to analog modules, also see section 43, 12-Bit A/D Converter (S12ADE) in the User's Manual: Hardware.

For notes on designing the printed circuit board, see the descriptions of the application note, the Hardware Design Guide (R01AN1411EJ). The latest version can be downloaded from the Renesas Electronics website.

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

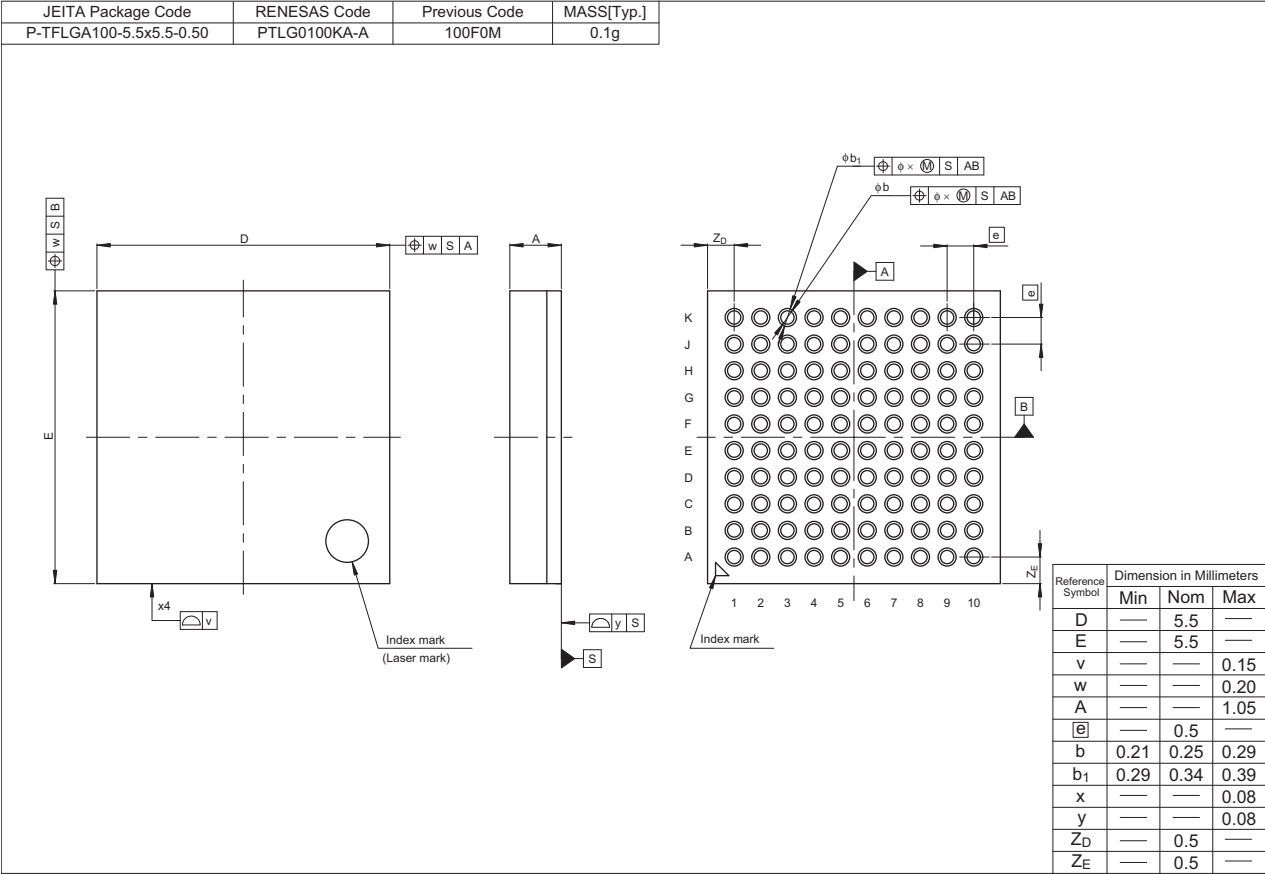


Figure A 100 -Pin TFLGA (PTLG0100KA-A)

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HWQFN64-9x9-0.50	PWQN0064KC-A	P64K8-50-6B4-5	0.21

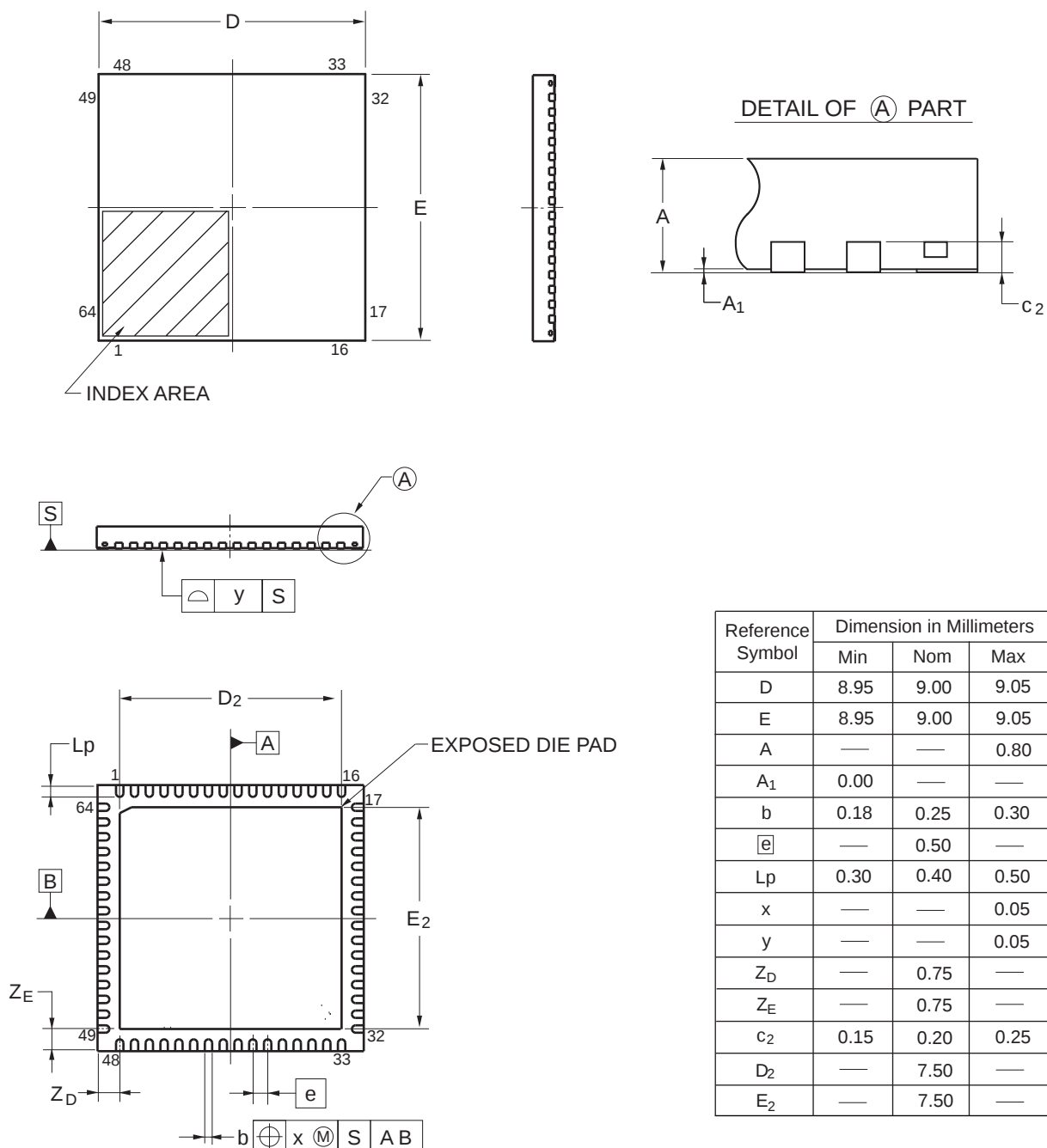


Figure D 64-Pin HWQFN (PWQN0064KC-A)

Rev.	Date	Description		Classification
		Page	Summary	
1.20	Sep 28, 2018	95	Figure 5.12 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 5.5 V When Normal Output is Selected (Reference Data), changed	TN-RX*-A201A/E
		124	Table 5.44 Timing of On-Chip Peripheral Modules (7), added	TN-RX*-A197A/E
		131	Figure 5.64 SD Host Interface Input/Output Signal Timing, added	TN-RX*-A197A/E
		132	Table 5.45 USB Characteristics (USB0_DP and USB0_DM Pin Characteristics) conditions, changed	

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