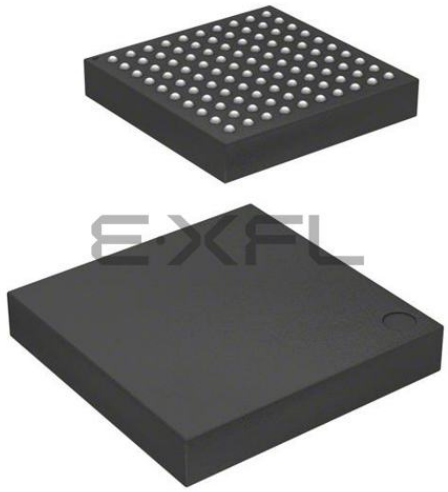
Renesas Electronics America Inc - R5F52318BDLA#20 Datasheet



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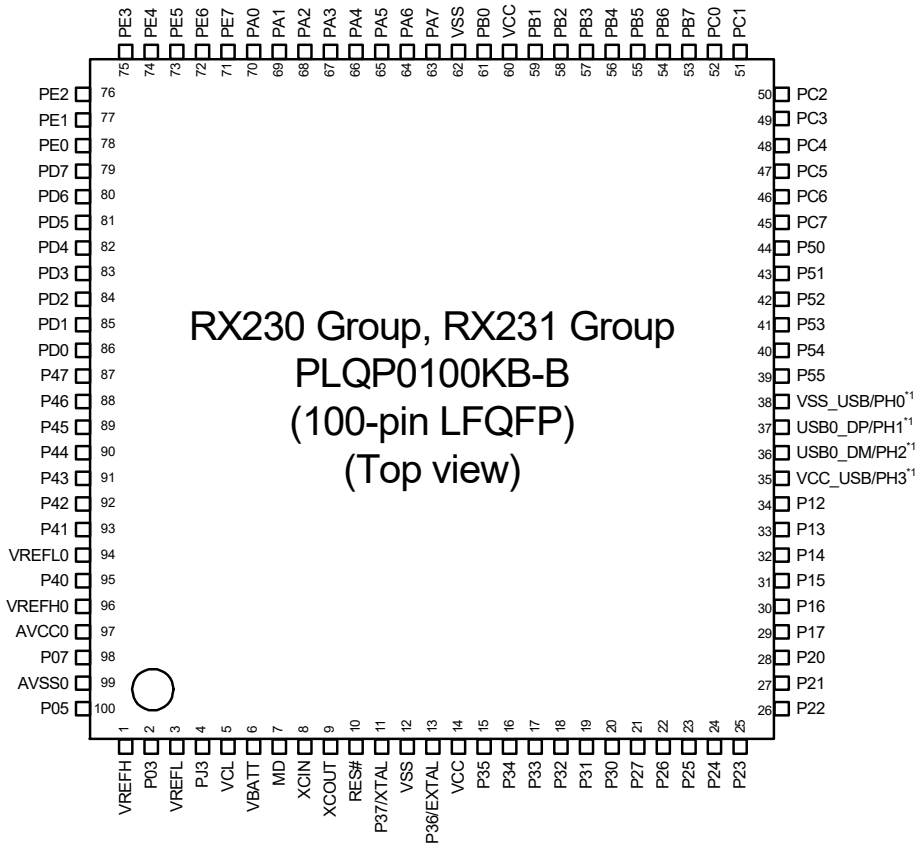
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	54MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, SCI, SD/SDIO, SPI, SSI, USB OTG
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	79
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFLGA
Supplier Device Package	100-TFLGA (5.5x5.5)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f52318bdla-20

Table 1.1 Outline of Specifications (2/4)

Classification	Module/Function	Description
Low power consumption	Low power consumption functions	• Module stop function • Three low power consumption modes Sleep mode, deep sleep mode, and software standby mode • Low power timer that operates during the software standby state
	Function for lower operating power consumption	• Operating power control modes High-speed operating mode, middle-speed operating mode, and low-speed operating mode
Interrupt	Interrupt controller (ICUb)	• Interrupt vectors: 167 • External interrupts: 9 (NMI, IRQ0 to IRQ7 pins) • Non-maskable interrupts: 7 (NMI pin, oscillation stop detection interrupt, voltage monitoring 1 interrupt, voltage monitoring 2 interrupt, WDT interrupt, IWDT interrupt, and VBATT power monitoring interrupt) • 16 levels specifiable for the order of priority
External bus extension		• The external address space can be divided into four areas (CS0 to CS3), each with independent control of access settings. Capacity of each area: 16 Mbytes (CS0 to CS3) A chip-select signal (CS0# to CS3#) can be output for each area. Each area is specifiable as an 8-bit or 16-bit bus space The data arrangement in each area is selectable as little or big endian (only for data). Bus format: Separate bus, multiplex bus • Wait control • Write buffer facility
DMA	DMA controller (DMACA)	• 4 channels • Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions
	Data transfer controller (DTCa)	• Transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Interrupts • Chain transfer function
I/O ports	General I/O ports	100-pin/64-pin/48-pin I/O: 79/43/30 (RX231 Group), 83/47/34 (RX230 Group) • Input: 1/1/1 Pull-up resistors: 79/43/30(RX231 Group), 83/47/34 (RX230 Group) • Open-drain outputs: 58/34/26 • 5-V tolerance: 8/5/5
Event link controller (ELC)		• Event signals of 61 types can be directly connected to the module • Operations of timer modules are selectable at event input • Capable of event link operation for port B and port E
Multi-function pin controller (MPC)		Capable of selecting the input/output function from multiple pins
Timers	16-bit timer pulse unit (TPUa)	• (16 bits × 6 channels) × 1 unit • Maximum of 16 pulse-input/output possible • Select from among seven or eight counter-input clock signals for each channel • Supports the input capture/output compare function • Output of PWM waveforms in up to 15 phases in PWM mode • Support for buffered operation, phase-counting mode (two-phase encoder input) and cascade connected operation (32 bits × 2 channels) depending on the channel. • Capable of generating conversion start triggers for the A/D converters • Signals from the input capture pins are input via a digital filter • Clock frequency measuring method
	Multi-function timer pulse unit 2 (MTU2a)	• (16 bits × 6 channels) × 1 unit • Up to 16 pulse-input/output lines and three pulse-input lines are available based on the six 16-bit timer channels • Select from among eight or seven counter-input clock signals for each channel (PCLK/1, PCLK/4, PCLK/16, PCLK/64, PCLK/256, PCLK/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD) other than channel 5, for which only four signals are available. • Input capture function • 21 output compare/input capture registers • Pulse output mode • Complementary PWM output mode • Reset synchronous PWM mode • Phase-counting mode • Capable of generating conversion start triggers for the A/D converter
	Port output enable 2 (POE2a)	Controls the high-impedance state of the MTU's waveform output pins
	Compare match timer (CMT)	• (16 bits × 2 channels) × 2 units • Select from among four clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512)
	Watchdog timer (WDTA)	• 14 bits x 1 channel • Select from among six counter-input clock signals (PCLK/4, PCLK/64, PCLK/128, PCLK/512, PCLK/2048, PCLK/8192)

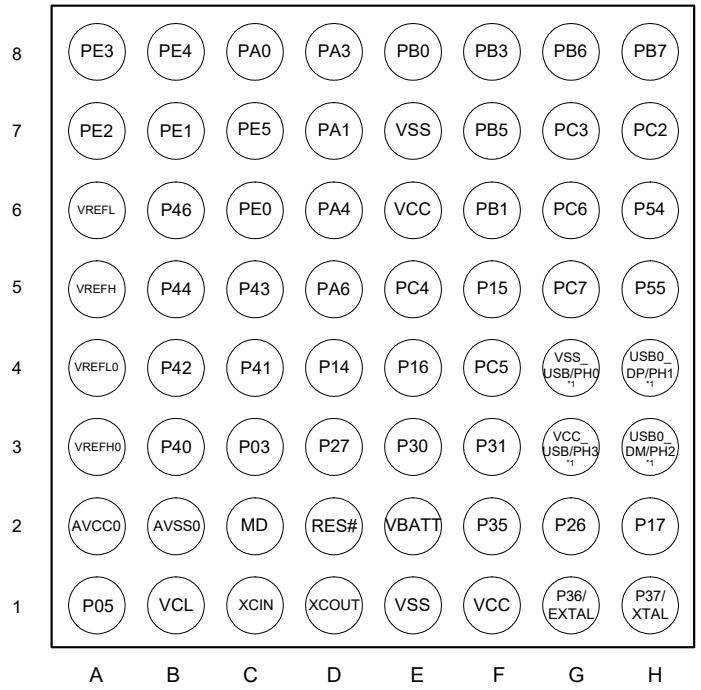


Note: This figure indicates the power supply pins and I/O port pins.
For the pin configuration, see the table “List of Pins and Pin Functions (100-Pin LFQFP)”.

Note 1. RX230: PH0, PH1, PH2, PH3
RX231: VSS_USB, USB0_DP, USB0_DM, VCC_USB

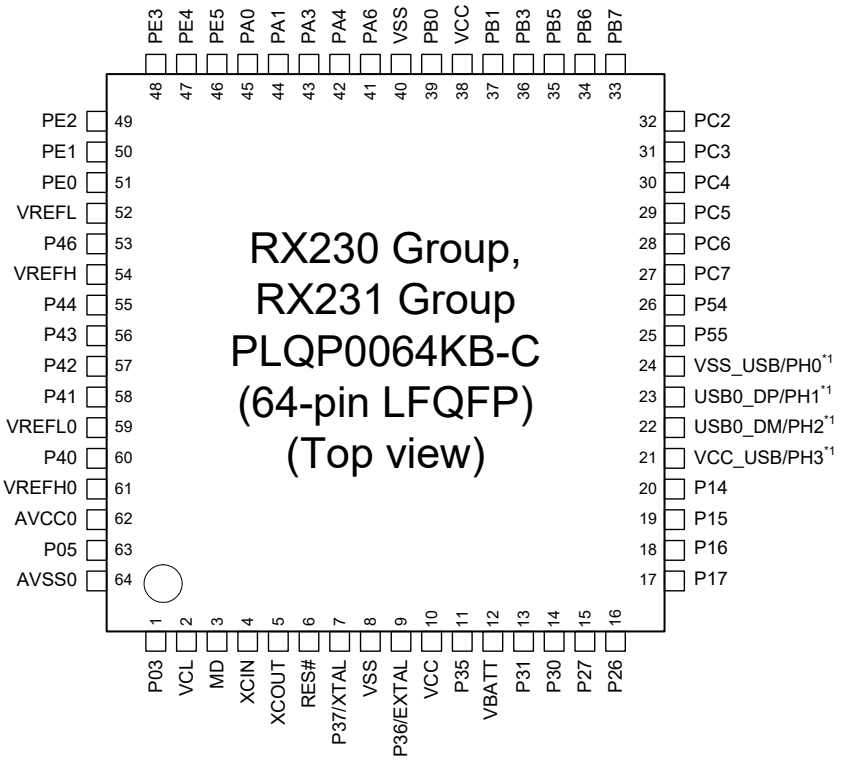
Figure 1.4 Pin Assignments of the 100-Pin LFQFP

RX230 Group, RX231 Group
PWLG0064KA-A
(64-pin WFLGA)
(Upper perspective view)



Note: This figure indicates the power supply pins and I/O port pins.
For the pin configuration, see the table “List of Pins and Pin Functions (64-Pin WFLGA)”.
Note: For the position of A1 pin in the package, see “Package Dimensions”.
Note 1. RX230: PH0, PH1, PH2, PH3
RX231: VSS_USB, USB0_DP, USB0_DM, VCC_USB

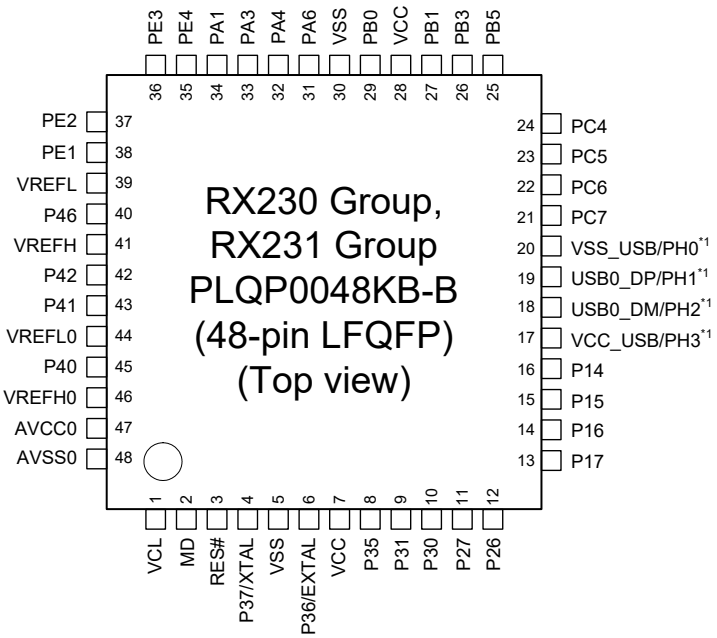
Figure 1.5 Pin Assignments of the 64-Pin WFLGA



Note: This figure indicates the power supply pins and I/O port pins.
For the pin configuration, see the table “List of Pins and Pin Functions (64-Pin LFQFP/HWQFN)”.

Note 1. RX230: PH0, PH1, PH2, PH3
RX231: VSS_USB, USB0_DP, USB0_DM, VCC_USB

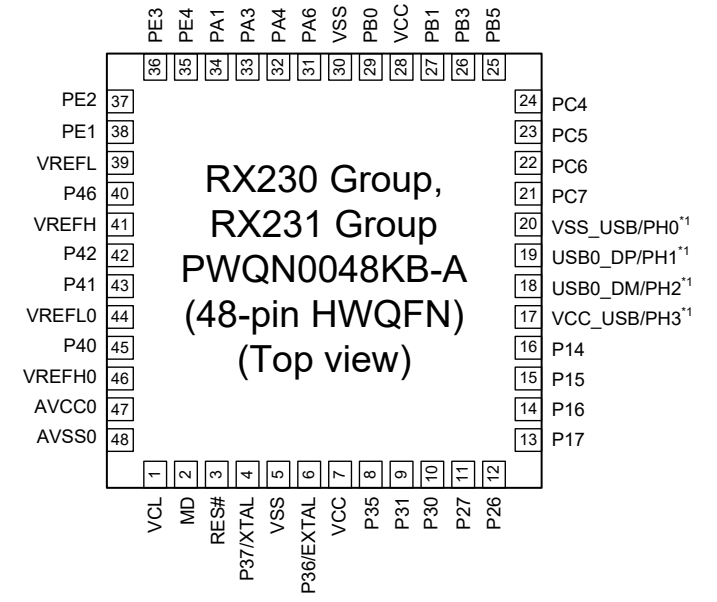
Figure 1.7 Pin Assignments of the 64-Pin LFQFP



Note: This figure indicates the power supply pins and I/O port pins.
For the pin configuration, see the table “List of Pins and Pin Functions (48-Pin LFQFP/HWQFN)”.

Note 1. RX230: PH0, PH1, PH2, PH3
RX231: VSS_USB, USB0_DP, USB0_DM, VCC_USB

Figure 1.8 Pin Assignments of the 48-Pin LFQFP



Note: It is recommended to connect an exposed die pad to VSS.

Note: This figure indicates the power supply pins and I/O port pins.
For the pin configuration, see the table “List of Pins and Pin Functions (48-Pin LFQFP/HWQFN)”.

Note 1. RX230: PH0, PH1, PH2, PH3
RX231: VSS_USB, USB0_DP, USB0_DM, VCC_USB

Figure 1.9 Pin Assignments of the 48-Pin HWQFN

Table 4.1 List of I/O Registers (Address Order) (6/33)

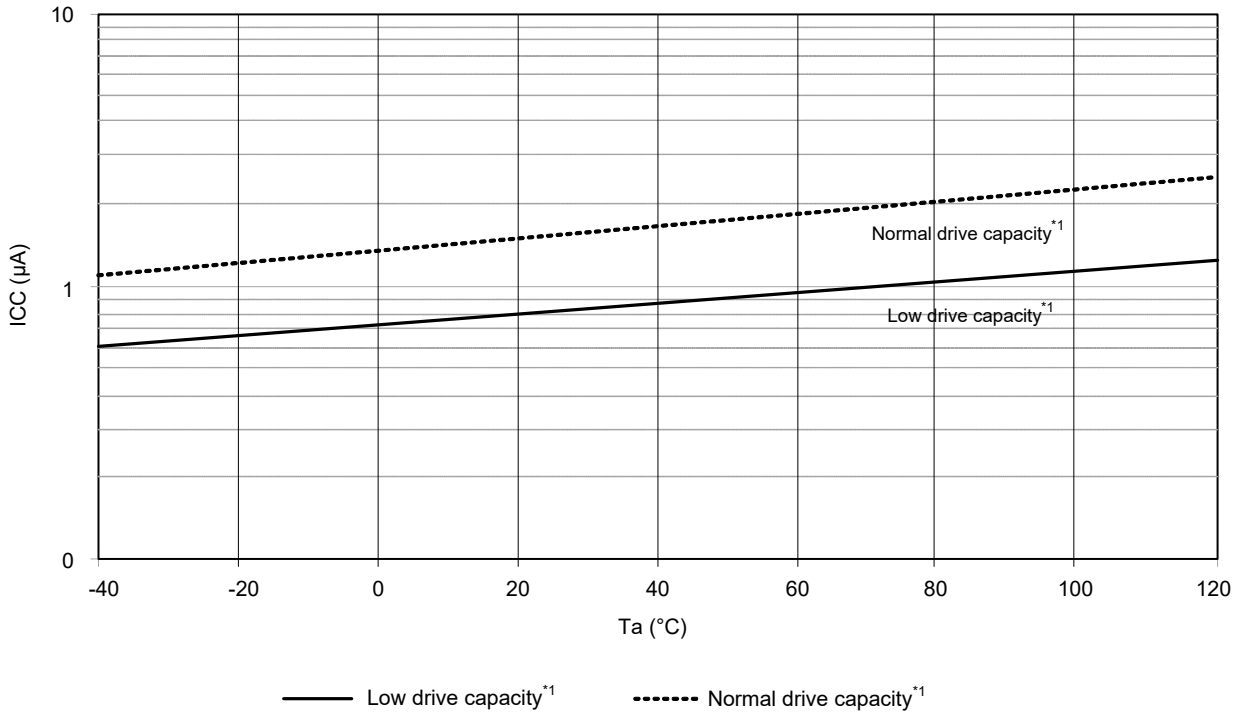
Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK <PCLK
0008 8158h	TPU4	Timer General Register A	TGRA	16	16	2 or 3 PCLKB	2 ICLK
0008 815Ah	TPU4	Timer General Register B	TGRB	16	16	2 or 3 PCLKB	2 ICLK
0008 8160h	TPU5	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8161h	TPU5	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB	2 ICLK
0008 8162h	TPU5	Timer I/O Control Register	TIOR	8	8	2 or 3 PCLKB	2 ICLK
0008 8164h	TPU5	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB	2 ICLK
0008 8165h	TPU5	Timer Status Register	TSR	8	8	2 or 3 PCLKB	2 ICLK
0008 8166h	TPU5	Timer Counter	TCNT	16	16	2 or 3 PCLKB	2 ICLK
0008 8168h	TPU5	Timer General Register A	TGRA	16	16	2 or 3 PCLKB	2 ICLK
0008 816Ah	TPU5	Timer General Register B	TGRB	16	16	2 or 3 PCLKB	2 ICLK
0008 8200h	TMR0	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8201h	TMR1	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8202h	TMR0	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB	2 ICLK
0008 8203h	TMR1	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB	2 ICLK
0008 8204h	TMR0	Time Constant Register A	TCORA	8	8	2 or 3 PCLKB	2 ICLK
0008 8205h	TMR1	Time Constant Register A	TCORA	8	8*1	2 or 3 PCLKB	2 ICLK
0008 8206h	TMR0	Time Constant Register B	TCORB	8	8	2 or 3 PCLKB	2 ICLK
0008 8207h	TMR1	Time Constant Register B	TCORB	8	8*1	2 or 3 PCLKB	2 ICLK
0008 8208h	TMR0	Timer Counter	TCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 8209h	TMR1	Timer Counter	TCNT	8	8*1	2 or 3 PCLKB	2 ICLK
0008 820Ah	TMR0	Timer Counter Control Register	TCCR	8	8	2 or 3 PCLKB	2 ICLK
0008 820Bh	TMR1	Timer Counter Control Register	TCCR	8	8*1	2 or 3 PCLKB	2 ICLK
0008 820Ch	TMR0	Timer Count Start Register	TCSTR	8	8	2 or 3 PCLKB	2 ICLK
0008 8210h	TMR2	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8211h	TMR3	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8212h	TMR2	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB	2 ICLK
0008 8213h	TMR3	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB	2 ICLK
0008 8214h	TMR2	Time Constant Register A	TCORA	8	8	2 or 3 PCLKB	2 ICLK
0008 8215h	TMR3	Time Constant Register A	TCORA	8	8*1	2 or 3 PCLKB	2 ICLK
0008 8216h	TMR2	Time Constant Register B	TCORB	8	8	2 or 3 PCLKB	2 ICLK
0008 8217h	TMR3	Time Constant Register B	TCORB	8	8*1	2 or 3 PCLKB	2 ICLK
0008 8218h	TMR2	Timer Counter	TCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 8219h	TMR3	Timer Counter	TCNT	8	8*1	2 or 3 PCLKB	2 ICLK
0008 821Ah	TMR2	Timer Counter Control Register	TCCR	8	8	2 or 3 PCLKB	2 ICLK
0008 821Bh	TMR3	Timer Counter Control Register	TCCR	8	8*1	2 or 3 PCLKB	2 ICLK
0008 821Ch	TMR2	Timer Count Start Register	TCSTR	8	8	2 or 3 PCLKB	2 ICLK
0008 8280h	CRC	CRC Control Register	CRCCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8281h	CRC	CRC Data Input Register	CRCDIR	8	8	2 or 3 PCLKB	2 ICLK
0008 8282h	CRC	CRC Data Output Register	CRCDOR	16	16	2 or 3 PCLKB	2 ICLK
0008 8300h	RIIC0	I^2C-Bus Control Register 1	ICCR1	8	8	2 or 3 PCLKB	2 ICLK
0008 8301h	RIIC0	I^2C-Bus Control Register 2	ICCR2	8	8	2 or 3 PCLKB	2 ICLK
0008 8302h	RIIC0	I^2C-Bus Mode Register 1	ICMR1	8	8	2 or 3 PCLKB	2 ICLK
0008 8303h	RIIC0	I^2C-Bus Mode Register 2	ICMR2	8	8	2 or 3 PCLKB	2 ICLK
0008 8304h	RIIC0	I^2C-Bus Mode Register 3	ICMR3	8	8	2 or 3 PCLKB	2 ICLK
0008 8305h	RIIC0	I^2C-Bus Function Enable Register	ICFER	8	8	2 or 3 PCLKB	2 ICLK
0008 8306h	RIIC0	I^2C-Bus Status Enable Register	ICSER	8	8	2 or 3 PCLKB	2 ICLK
0008 8307h	RIIC0	I^2C-Bus Interrupt Enable Register	ICIER	8	8	2 or 3 PCLKB	2 ICLK
0008 8308h	RIIC0	I^2C-Bus Status Register 1	ICSR1	8	8	2 or 3 PCLKB	2 ICLK
0008 8309h	RIIC0	I^2C-Bus Status Register 2	ICSR2	8	8	2 or 3 PCLKB	2 ICLK
0008 830Ah	RIIC0	Slave Address Register L0	SARL0	8	8	2 or 3 PCLKB	2 ICLK
0008 830Bh	RIIC0	Slave Address Register U0	SARU0	8	8	2 or 3 PCLKB	2 ICLK
0008 830Ch	RIIC0	Slave Address Register L1	SARL1	8	8	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (27/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK <PCLK
000A 8412h	RSCAN	Receive Rule Entry Register 9BH	GAFLMH9	16	16	2 or 3 PCLKB	2 ICLK
000A 8412h	RSCAN	Receive Buffer Register 7AH	RMIDH7	16	16	2 or 3 PCLKB	2 ICLK
000A 8414h	RSCAN	Receive Rule Entry Register 9CL	GAFLPL9	16	16	2 or 3 PCLKB	2 ICLK
000A 8414h	RSCAN	Receive Buffer Register 7BL	RMTS7	16	16	2 or 3 PCLKB	2 ICLK
000A 8416h	RSCAN	Receive Rule Entry Register 9CH	GAFLPH9	16	16	2 or 3 PCLKB	2 ICLK
000A 8416h	RSCAN	Receive Buffer Register 7BH	RMPTR7	16	16	2 or 3 PCLKB	2 ICLK
000A 8418h	RSCAN	Receive Rule Entry Register 10AL	GAFLIDL10	16	16	2 or 3 PCLKB	2 ICLK
000A 8418h	RSCAN	Receive Buffer Register 7CL	RMDF07	16	16	2 or 3 PCLKB	2 ICLK
000A 841Ah	RSCAN	Receive Rule Entry Register 10AH	GAFLIDH10	16	16	2 or 3 PCLKB	2 ICLK
000A 841Ah	RSCAN	Receive Buffer Register 7CH	RMDF17	16	16	2 or 3 PCLKB	2 ICLK
000A 841Ch	RSCAN	Receive Rule Entry Register 10BL	GAFLML10	16	16	2 or 3 PCLKB	2 ICLK
000A 841Ch	RSCAN	Receive Buffer Register 7DL	RMDF27	16	16	2 or 3 PCLKB	2 ICLK
000A 841Eh	RSCAN	Receive Rule Entry Register 10BH	GAFLMH10	16	16	2 or 3 PCLKB	2 ICLK
000A 841Eh	RSCAN	Receive Buffer Register 7DH	RMDF37	16	16	2 or 3 PCLKB	2 ICLK
000A 8420h	RSCAN	Receive Rule Entry Register 10CL	GAFLPL10	16	16	2 or 3 PCLKB	2 ICLK
000A 8420h	RSCAN	Receive Buffer Register 8AL	RMIDL8	16	16	2 or 3 PCLKB	2 ICLK
000A 8422h	RSCAN	Receive Rule Entry Register 10CH	GAFLPH10	16	16	2 or 3 PCLKB	2 ICLK
000A 8422h	RSCAN	Receive Buffer Register 8AH	RMIDH8	16	16	2 or 3 PCLKB	2 ICLK
000A 8424h	RSCAN	Receive Rule Entry Register 11AL	GAFLIDL11	16	16	2 or 3 PCLKB	2 ICLK
000A 8424h	RSCAN	Receive Buffer Register 8BL	RMTS8	16	16	2 or 3 PCLKB	2 ICLK
000A 8426h	RSCAN	Receive Rule Entry Register 11AH	GAFLIDH11	16	16	2 or 3 PCLKB	2 ICLK
000A 8426h	RSCAN	Receive Buffer Register 8BH	RMPTR8	16	16	2 or 3 PCLKB	2 ICLK
000A 8428h	RSCAN	Receive Rule Entry Register 11BL	GAFLML11	16	16	2 or 3 PCLKB	2 ICLK
000A 8428h	RSCAN	Receive Buffer Register 8CL	RMDF08	16	16	2 or 3 PCLKB	2 ICLK
000A 842Ah	RSCAN	Receive Rule Entry Register 11BH	GAFLMH11	16	16	2 or 3 PCLKB	2 ICLK
000A 842Ah	RSCAN	Receive Buffer Register 8CH	RMDF18	16	16	2 or 3 PCLKB	2 ICLK
000A 842Ch	RSCAN	Receive Rule Entry Register 11CL	GAFLPL11	16	16	2 or 3 PCLKB	2 ICLK
000A 842Ch	RSCAN	Receive Buffer Register 8DL	RMDF28	16	16	2 or 3 PCLKB	2 ICLK
000A 842Eh	RSCAN	Receive Rule Entry Register 11CH	GAFLPH11	16	16	2 or 3 PCLKB	2 ICLK
000A 842Eh	RSCAN	Receive Buffer Register 8DH	RMDF38	16	16	2 or 3 PCLKB	2 ICLK
000A 8430h	RSCAN	Receive Rule Entry Register 12AL	GAFLIDL12	16	16	2 or 3 PCLKB	2 ICLK
000A 8430h	RSCAN	Receive Buffer Register 9AL	RMIDL9	16	16	2 or 3 PCLKB	2 ICLK
000A 8432h	RSCAN	Receive Rule Entry Register 12AH	GAFLIDH12	16	16	2 or 3 PCLKB	2 ICLK
000A 8432h	RSCAN	Receive Buffer Register 9AH	RMIDH9	16	16	2 or 3 PCLKB	2 ICLK
000A 8434h	RSCAN	Receive Rule Entry Register 12BL	GAFLML12	16	16	2 or 3 PCLKB	2 ICLK
000A 8434h	RSCAN	Receive Buffer Register 9BL	RMTS9	16	16	2 or 3 PCLKB	2 ICLK
000A 8436h	RSCAN	Receive Rule Entry Register 12BH	GAFLMH12	16	16	2 or 3 PCLKB	2 ICLK
000A 8436h	RSCAN	Receive Buffer Register 9BH	RMPTR9	16	16	2 or 3 PCLKB	2 ICLK
000A 8438h	RSCAN	Receive Rule Entry Register 12CL	GAFLPL12	16	16	2 or 3 PCLKB	2 ICLK
000A 8438h	RSCAN	Receive Buffer Register 9CL	RMDF09	16	16	2 or 3 PCLKB	2 ICLK
000A 843Ah	RSCAN	Receive Rule Entry Register 12CH	GAFLPH12	16	16	2 or 3 PCLKB	2 ICLK
000A 843Ah	RSCAN	Receive Buffer Register 9CH	RMDF19	16	16	2 or 3 PCLKB	2 ICLK
000A 843Ch	RSCAN	Receive Rule Entry Register 13AL	GAFLIDL13	16	16	2 or 3 PCLKB	2 ICLK
000A 843Ch	RSCAN	Receive Buffer Register 9DL	RMDF29	16	16	2 or 3 PCLKB	2 ICLK
000A 843Eh	RSCAN	Receive Rule Entry Register 13AH	GAFLIDH13	16	16	2 or 3 PCLKB	2 ICLK
000A 843Eh	RSCAN	Receive Buffer Register 9DH	RMDF39	16	16	2 or 3 PCLKB	2 ICLK
000A 8440h	RSCAN	Receive Rule Entry Register 13BL	GAFLML13	16	16	2 or 3 PCLKB	2 ICLK
000A 8440h	RSCAN	Receive Buffer Register 10AL	RMIDL10	16	16	2 or 3 PCLKB	2 ICLK
000A 8442h	RSCAN	Receive Rule Entry Register 13BH	GAFLMH13	16	16	2 or 3 PCLKB	2 ICLK
000A 8442h	RSCAN	Receive Buffer Register 10AH	RMIDH10	16	16	2 or 3 PCLKB	2 ICLK
000A 8444h	RSCAN	Receive Rule Entry Register 13CL	GAFLPL13	16	16	2 or 3 PCLKB	2 ICLK
000A 8444h	RSCAN	Receive Buffer Register 10BL	RMTS10	16	16	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (31/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK <PCLK
000A 862Eh	RSCAN	RAM Test Register 87	RPGACC87	16	16	2 or 3 PCLKB	2 ICLK
000A 8630h	RSCAN0	Transmit Buffer Register 3AL	TMIDL3	16	16	2 or 3 PCLKB	2 ICLK
000A 8630h	RSCAN	RAM Test Register 88	RPGACC88	16	16	2 or 3 PCLKB	2 ICLK
000A 8632h	RSCAN0	Transmit Buffer Register 3AH	TMIDH3	16	16	2 or 3 PCLKB	2 ICLK
000A 8632h	RSCAN	RAM Test Register 89	RPGACC89	16	16	2 or 3 PCLKB	2 ICLK
000A 8634h	RSCAN	RAM Test Register 90	RPGACC90	16	16	2 or 3 PCLKB	2 ICLK
000A 8636h	RSCAN0	Transmit Buffer Register 3BH	TMPTR3	16	16	2 or 3 PCLKB	2 ICLK
000A 8636h	RSCAN	RAM Test Register 91	RPGACC91	16	16	2 or 3 PCLKB	2 ICLK
000A 8638h	RSCAN0	Transmit Buffer Register 3CL	TMDF03	16	16	2 or 3 PCLKB	2 ICLK
000A 8638h	RSCAN	RAM Test Register 92	RPGACC92	16	16	2 or 3 PCLKB	2 ICLK
000A 863Ah	RSCAN0	Transmit Buffer Register 3CH	TMDF13	16	16	2 or 3 PCLKB	2 ICLK
000A 863Ah	RSCAN	RAM Test Register 93	RPGACC93	16	16	2 or 3 PCLKB	2 ICLK
000A 863Ch	RSCAN0	Transmit Buffer Register 3DL	TMDF23	16	16	2 or 3 PCLKB	2 ICLK
000A 863Ch	RSCAN	RAM Test Register 94	RPGACC94	16	16	2 or 3 PCLKB	2 ICLK
000A 863Eh	RSCAN0	Transmit Buffer Register 3DH	TMDF33	16	16	2 or 3 PCLKB	2 ICLK
000A 863Eh	RSCAN	RAM Test Register 95	RPGACC95	16	16	2 or 3 PCLKB	2 ICLK
000A 8640h to 000A 867Eh	RSCAN	RAM Test Register 96 to RAM Test Register 127	RPGACC96 to RPGACC127	16	16	2 or 3 PCLKB	2 ICLK
000A 8680h	RSCAN0	Transmit History Buffer Access Register	THLACC0	16	16	2 or 3 PCLKB	2 ICLK
000D 0A00h	MTU3	Timer Control Register	TCR	8	8	2 or 3 PCLKA	2 ICLK
000D 0A01h	MTU4	Timer Control Register	TCR	8	8	2 or 3 PCLKA	2 ICLK
000D 0A02h	MTU3	Timer Mode Register	TMDR	8	8	2 or 3 PCLKA	2 ICLK
000D 0A03h	MTU4	Timer Mode Register	TMDR	8	8	2 or 3 PCLKA	2 ICLK
000D 0A04h	MTU3	Timer I/O Control Register H	TIORH	8	8	2 or 3 PCLKA	2 ICLK
000D 0A05h	MTU3	Timer I/O Control Register L	TIORL	8	8	2 or 3 PCLKA	2 ICLK
000D 0A06h	MTU4	Timer I/O Control Register H	TIORH	8	8	2 or 3 PCLKA	2 ICLK
000D 0A07h	MTU4	Timer I/O Control Register L	TIORL	8	8	2 or 3 PCLKA	2 ICLK
000D 0A08h	MTU3	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKA	2 ICLK
000D 0A09h	MTU4	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKA	2 ICLK
000D 0A0Ah	MTU	Timer Output Master Enable Register	TOER	8	8	2 or 3 PCLKA	2 ICLK
000D 0A0Dh	MTU	Timer Gate Control Register	TGCR	8	8	2 or 3 PCLKA	2 ICLK
000D 0A0Eh	MTU	Timer Output Control Register 1	TOCR1	8	8	2 or 3 PCLKA	2 ICLK
000D 0A0Fh	MTU	Timer Output Control Register 2	TOCR2	8	8	2 or 3 PCLKA	2 ICLK
000D 0A10h	MTU3	Timer Counter	TCNT	16	16	2 or 3 PCLKA	2 ICLK
000D 0A12h	MTU4	Timer Counter	TCNT	16	16	2 or 3 PCLKA	2 ICLK
000D 0A14h	MTU	Timer Cycle Data Register	TCDR	16	16	2 or 3 PCLKA	2 ICLK
000D 0A16h	MTU	Timer Dead Time Data Register	TDDR	16	16	2 or 3 PCLKA	2 ICLK
000D 0A18h	MTU3	Timer General Register A	TGRA	16	16	2 or 3 PCLKA	2 ICLK
000D 0A1Ah	MTU3	Timer General Register B	TGRB	16	16	2 or 3 PCLKA	2 ICLK
000D 0A1Ch	MTU4	Timer General Register A	TGRA	16	16	2 or 3 PCLKA	2 ICLK
000D 0A1Eh	MTU4	Timer General Register B	TGRB	16	16	2 or 3 PCLKA	2 ICLK
000D 0A20h	MTU	Timer Subcounters	TCNTS	16	16	2 or 3 PCLKA	2 ICLK
000D 0A22h	MTU	Timer Cycle Buffer Register	TCBR	16	16	2 or 3 PCLKA	2 ICLK
000D 0A24h	MTU3	Timer General Register C	TGRC	16	16	2 or 3 PCLKA	2 ICLK
000D 0A26h	MTU3	Timer General Register D	TGRD	16	16	2 or 3 PCLKA	2 ICLK
000D 0A28h	MTU4	Timer General Register C	TGRC	16	16	2 or 3 PCLKA	2 ICLK
000D 0A2Ah	MTU4	Timer General Register D	TGRD	16	16	2 or 3 PCLKA	2 ICLK
000D 0A2Ch	MTU3	Timer Status Register	TSR	8	8	2 or 3 PCLKA	2 ICLK
000D 0A2Dh	MTU4	Timer Status Register	TSR	8	8	2 or 3 PCLKA	2 ICLK
000D 0A30h	MTU	Timer Interrupt Skipping Set Register	TITCR	8	8	2 or 3 PCLKA	2 ICLK
000D 0A31h	MTU	Timer Interrupt Skipping Counters	TITCNT	8	8	2 or 3 PCLKA	2 ICLK
000D 0A32h	MTU	Timer Buffer Transfer Set Register	TBTER	8	8	2 or 3 PCLKA	2 ICLK



Note 1. Indicates the average of the typical samples through actual measurement during product evaluation.

Figure 5.6 Temperature Dependency of RTC Operation with VCC Off (Reference Data)

Table 5.10 DC Characteristics (8)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VSS_USB = 0 V

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Permissible total power consumption*1	Pd	—	—	350	mW	D-version product
Permissible total power consumption*1	Pd	—	—	130	mW	G-version product

Note: Please contact a Renesas Electronics sales office for information on the derating of the G-version product. Derating is the systematic reduction of load to improve reliability.

Note 1. Total power dissipated by the entire chip (including output currents)

Table 5.11 DC Characteristics (9)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.*7	Max.	Unit	Test Conditions
Analog power supply current	During A/D conversion (at high-speed conversion)	I_{AVCC}	—	0.7	1.7	mA	
	During A/D conversion (in low-current mode)		—	0.6	1.0		
	During D/A conversion (per channel)*1		—	0.4	0.8		
	Waiting for A/D and D/A conversion (all units)		—	—	0.4	μA	
Reference power supply current	During A/D conversion (at high-speed conversion)	I_{REFH0}	—	25	150	μA	
	Waiting for A/D conversion (all units)		—	—	60	nA	
	During D/A conversion (per channel)	I_{REFH}	—	50	100	μA	
	Waiting for D/A conversion (all units)		—	—	100	nA	
LVD1, 2	per channel	I_{LVD}	—	0.15	—	μA	
Temperature sensor*6	—	I_{TEMP}	—	75	—	μA	
Comparator B operating current*6	Window mode	I_{CMP}*5	—	12.5	28.6	μA	
	Comparator high-speed mode (per channel)		—	3.2	16.2	μA	
	Comparator low-speed mode (per channel)		—	1.7	4.4	μA	
CTSU operating current	When sleep mode Base clock frequency: 2MHz Pin capacitance: 50pF	I_{CTSU}	—	150	—	μA	
USB operating current*4	During USB communication operation under the following settings and conditions • Host controller operation is set to full-speed mode Bulk OUT transfer (64 bytes) × 1, bulk IN transfer (64 bytes) × 1 • Connect peripheral devices via a 1-meter USB cable from the USB port.	I_{USBH}*2	—	4.3 (VCC) 0.9 (VCC_USB)	—	mA	
	During USB communication operation under the following settings and conditions • Function controller operation is set to full-speed mode Bulk OUT transfer (64 bytes) × 1, bulk IN transfer (64 bytes) × 1 • Connect the host device via a 1-meter USB cable from the USB port.	I_{USBF}*2	—	3.6 (VCC) 1.1 (VCC_USB)	—	mA	
	During suspended state under the following setting and conditions • Function controller operation is set to full-speed mode (pull up the USB0_DP pin) • Software standby mode • Connect the host device via a 1-meter USB cable from the USB port.	I_{SUSP}*3	—	0.35 (VCC) 170 (VCC_USB)	—	μA	

Note 1. The value of the D/A converter is the value of the power supply current including the reference current.
Note 2. Current consumed only by the USB module.
Note 3. Includes the current supplied from the pull-up resistor of the USB0_DP pin to the pull-down resistor of the host device, in addition to the current consumed by this MCU during the suspended state.
Note 4. Current consumed by the power supplies (VCC and VCC_USB).
Note 5. Current consumed only by the comparator B module.
Note 6. Current consumed by the power supply (VCC).
Note 7. When VCC = AVCC0 = VCC_USB = 3.3 V.

Table 5.12 DC Characteristics (10)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RAM standby voltage	V_{RAM}	1.8	—	—	V	

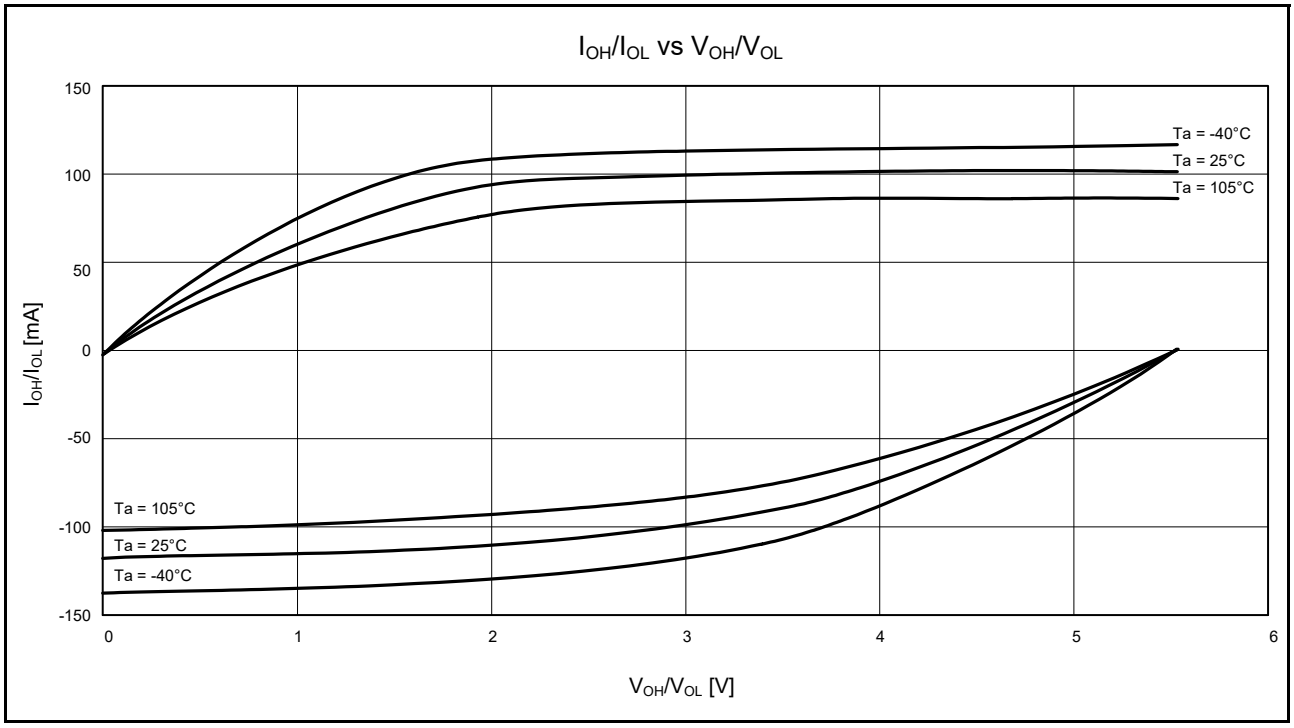


Figure 5.17 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 5.5 V When High-Drive Output is Selected (Reference Data)

5.2.3 Normal I/O Pin Output Characteristics (3)

Figure 5.18 to Figure 5.21 show the characteristics of the RIIC output pin.

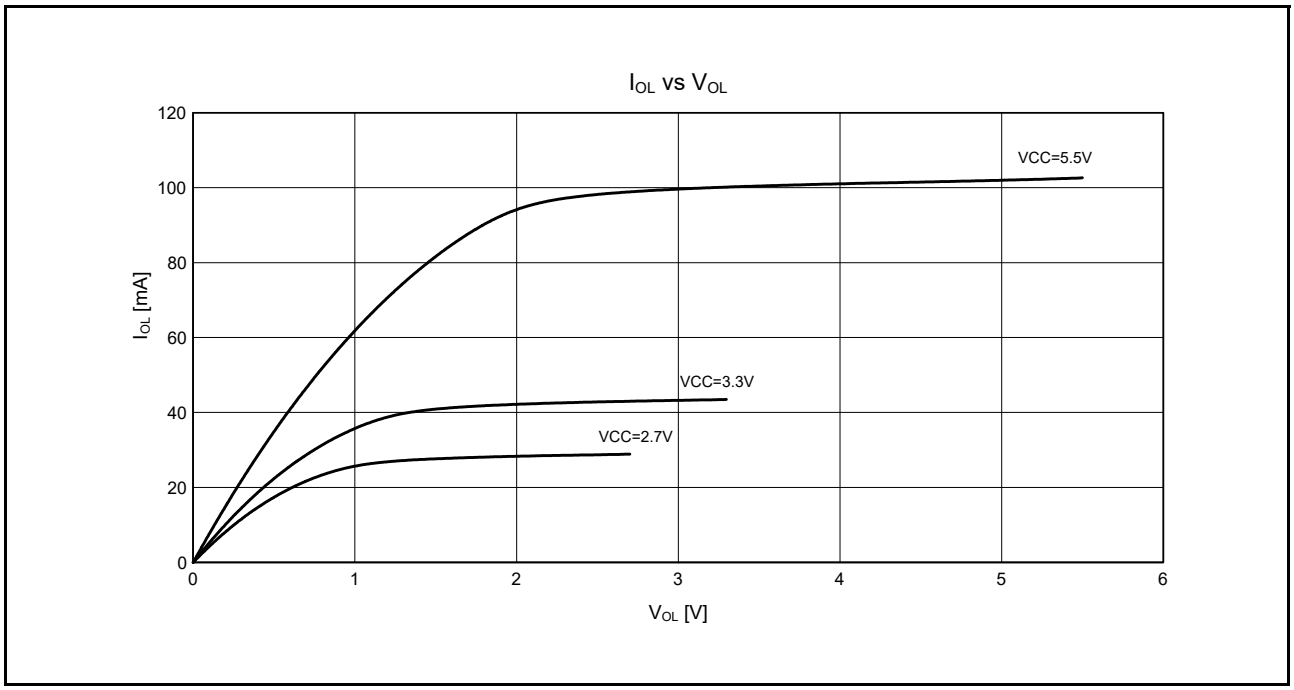


Figure 5.18 V_{OL} and I_{OL} Voltage Characteristics of RIIC Output Pin at T_a = 25°C (Reference Data)

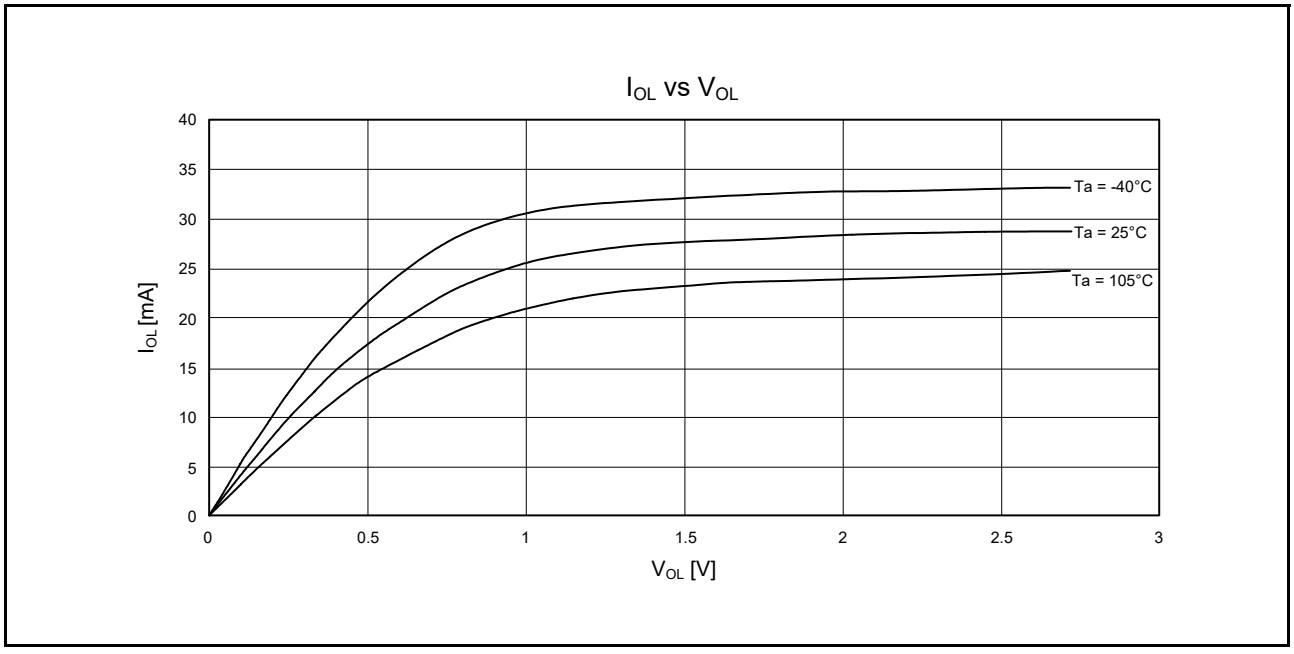


Figure 5.19 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at VCC = 2.7 V (Reference Data)

Table 5.26 Clock Timing

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VREFL0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
EXTAL external clock input cycle time		t_{Xcyc}	50	—	—	ns	Figure 5.23
EXTAL external clock input high pulse width		t_{XH}	20	—	—	ns	
EXTAL external clock input low pulse width		t_{XL}	20	—	—	ns	
EXTAL external clock rise time		t_{Xr}	—	—	5	ns	
EXTAL external clock fall time		t_{Xf}	—	—	5	ns	
EXTAL external clock input wait time*1		t_{XWT}	0.5	—	—	μs	
Main clock oscillator oscillation frequency*2	2.4 ≤ VCC ≤ 5.5	f_{MAIN}	1	—	20	MHz	
	1.8 ≤ VCC < 2.4		1	—	8		
Main clock oscillation stabilization time (crystal)*2		$t_{MAINOSC}$	—	3	—	ms	Figure 5.24
Main clock oscillation stabilization time (ceramic resonator)*2		$t_{MAINOSC}$	—	50	—	μs	
LOCO clock oscillation frequency		f_{LOCO}	3.44	4.0	4.56	MHz	
LOCO clock oscillation stabilization time		t_{LOCO}	—	—	0.5	μs	Figure 5.25
IWDT-dedicated clock oscillation frequency		f_{ILOCO}	12.75	15	17.25	kHz	
IWDT-dedicated clock oscillation stabilization time		t_{ILOCO}	—	—	50	μs	Figure 5.26
HOCO clock oscillation frequency		f_{HOCO} (32 MHz)	31.52	32	32.48	MHz	T_a = –40 to + 85°C
			31.68	32	32.32		T_a = 0 to + 55°C
			31.36	32	32.64		T_a = –40 to +105°C
		f_{HOCO} (54 MHz)	53.19	54	54.81	MHz	T_a = –40 to + 85°C
			53.46	54	54.54		T_a = 0 to + 55°C
			52.92	54	55.08		T_a = –40 to +105°C
HOCO clock oscillation stabilization time		t_{HOCO}	—	—	30	μs	Figure 5.28
PLL input frequency*3		f_{PLLIN}	4	—	12.5	MHz	
PLL circuit oscillation frequency*3		f_{PLL}	24	—	54	MHz	
PLL clock oscillation stabilization time		t_{PLL}	—	—	50	μs	Figure 5.29
PLL free-running oscillation frequency		f_{PLLFR}	—	8	—	MHz	
USBPLL input frequency*5		f_{PLLIN}	—	6, 8*6	—	MHz	
USBPLL circuit oscillation frequency*5		f_{PLL}	—	48*6	—	MHz	
USBPLL clock oscillation stabilization time		t_{PLL}	—	—	50	μs	Figure 5.29
Sub-clock oscillator oscillation frequency*7		f_{SUB}	—	32.768	—	kHz	
Sub-clock oscillation stabilization time*4		t_{SUBOSC}	—	0.5	—	s	Figure 5.30

Note 1. Time until the clock can be used after the main clock oscillator stop bit (MOSCCR.MOSTP) is set to 0 (operating).

Note 2. Reference values when an 8-MHz resonator is used.
When specifying the main clock oscillator stabilization time, set the MOSCWTCR register with a stabilization time value that is equal to or greater than the resonator-manufacturer-recommended value.
After the MOSCCR.MOSTP bit is changed to enable the main clock oscillator, confirm that the OSCOVFSR.MOOVF flag has become 1, and then start using the main clock.

Note 3. The VCC range should be 2.4 to 5.5 V when the PLL is used.

Note 4. Reference values when a 32.768-kHz resonator is used.
After the setting of the SOSCCR.SOSTP bit or RCR3.RTCEN bit is changed to operate the sub-clock oscillator, only start using the sub-clock after the sub-clock oscillation stabilization wait time that is equal to or greater than the oscillator-manufacturer-recommended value has elapsed.

Note 5. The VCC range should be 3.0 to 5.5 V when the USBPLL is used.

Note 6. The input frequency can be set to 6 or 8 MHz and the oscillation frequency can be set to 48 MHz only.

Note 7. Only 32.768 kHz can be used.

Table 5.36 Bus Timing (Multiplex bus) (1)

Conditions: 2.7 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VSS_USB = 0 V,
fBCLK ≤ 32 MHz (BCLK pin output frequency ≤ 16 MHz), T_a = –40 to +105°C, V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5,
I_{OH} = –1.0 mA, I_{OL} = 1.0 mA, C_L = 30 pF, when normal output is selected by the drive capacity control register

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	55	ns	Figure 5.43, Figure 5.44
Byte control delay time	t_{BCD}	—	55	ns	
CS# delay time	t_{CSD}	—	55	ns	
RD# delay time	t_{RSD}	—	55	ns	
ALE delay time	t_{ALED}	—	55	ns	
Read data setup time	t_{RDS}	40	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	55	ns	
Write data delay time	t_{WDD}	—	55	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	40	—	ns	Figure 5.42
WAIT# hold time	t_{WTH}	0	—	ns	

Table 5.37 Bus Timing (Multiplex bus) (2)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 < 5.5 V, VSS = AVSS0 = VSS_USB = 0 V,
fBCLK ≤ 16 MHz (BCLK pin output frequency ≤ 8 MHz), T_a = –40 to +105°C, V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5,
I_{OH} = –1.0 mA, I_{OL} = 1.0 mA, C_L = 30 pF, when normal output is selected by the drive capacity control register

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	90	ns	Figure 5.43, Figure 5.44
Byte control delay time	t_{BCD}	—	90	ns	
CS# delay time	t_{CSD}	—	90	ns	
RD# delay time	t_{RSD}	—	90	ns	
ALE delay time	t_{ALED}	—	90	ns	
Read data setup time	t_{RDS}	60	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	90	ns	
Write data delay time	t_{WDD}	—	90	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	60	—	ns	Figure 5.42
WAIT# hold time	t_{WTH}	0	—	ns	

Table 5.44 Timing of On-Chip Peripheral Modules (7)

Conditions: 2.7 V ≤ VCC = VCC_USB = AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, fPCLKB ≤ 32 MHz,
T_a = –40 to +105°C,
when high-drive output is selected by the drive capacity control register

Item		Symbol	Min.	Max.	Unit	Test Conditions
SDHI	SDHI_CLK pin output cycle time	$t_{PP(SD)}$	62.5	—	ns	Figure 5.64
	SDHI_CLK pin output high pulse width	$t_{WH(SD)}$	18.25	—	ns	
	SDHI_CLK pin output low pulse width	$t_{WL(SD)}$	18.25	—	ns	
	SDHI_CLK pin output rise time	$t_{TLH(SD)}$	—	10	ns	
	SDHI_CLK pin output fall time	$t_{THL(SD)}$	—	10	ns	
	Output data delay time (data transfer mode) for SDHI_CMD and SDHI_D0 to SDHI_D3 pins	$t_{ODLY(SD)}$	–18.25	18.25	ns	
	Input data setup time for SDHI_CMD and SDHI_D0 to SDHI_D3 pins	$t_{ISU(SD)}$	9.25	—	ns	
	Input data hold time for SDHI_CMD and SDHI_D0 to SDHI_D3 pins	$t_{IH(SD)}$	8.3	—	ns	

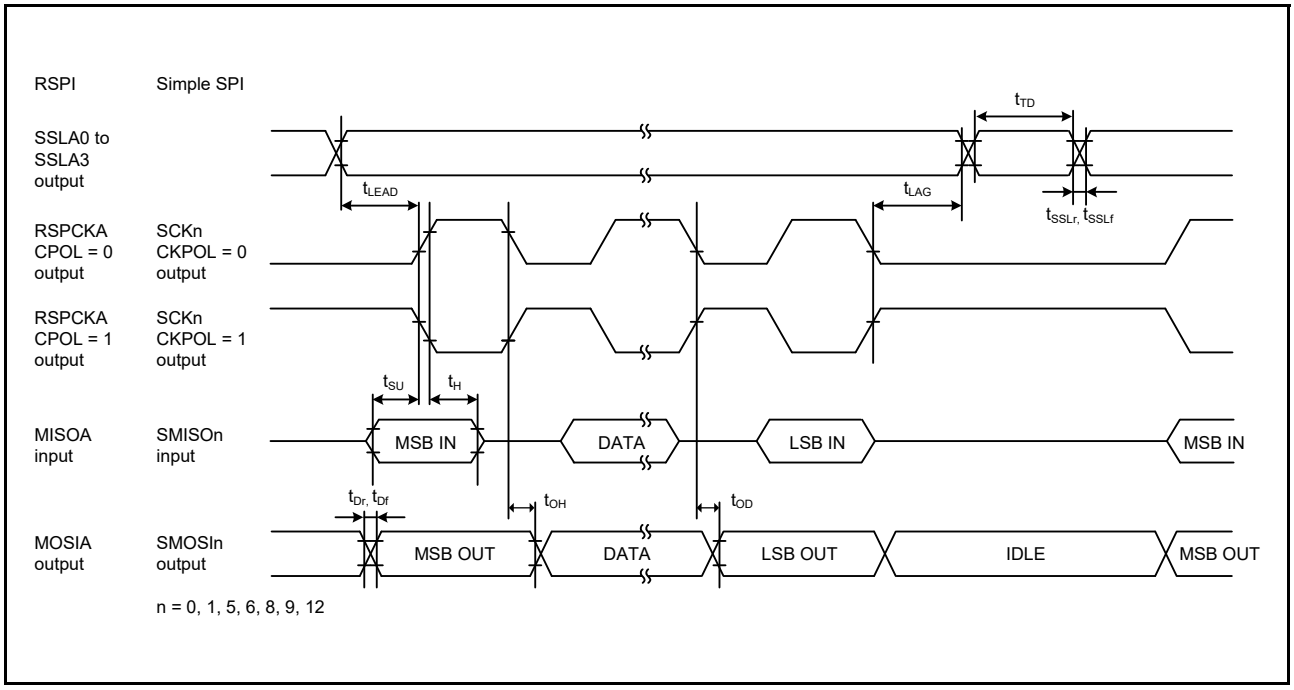


Figure 5.55 RSPI Timing (Master, CPHA = 0) and Simple SPI Clock Timing (Master, CKPH = 1)

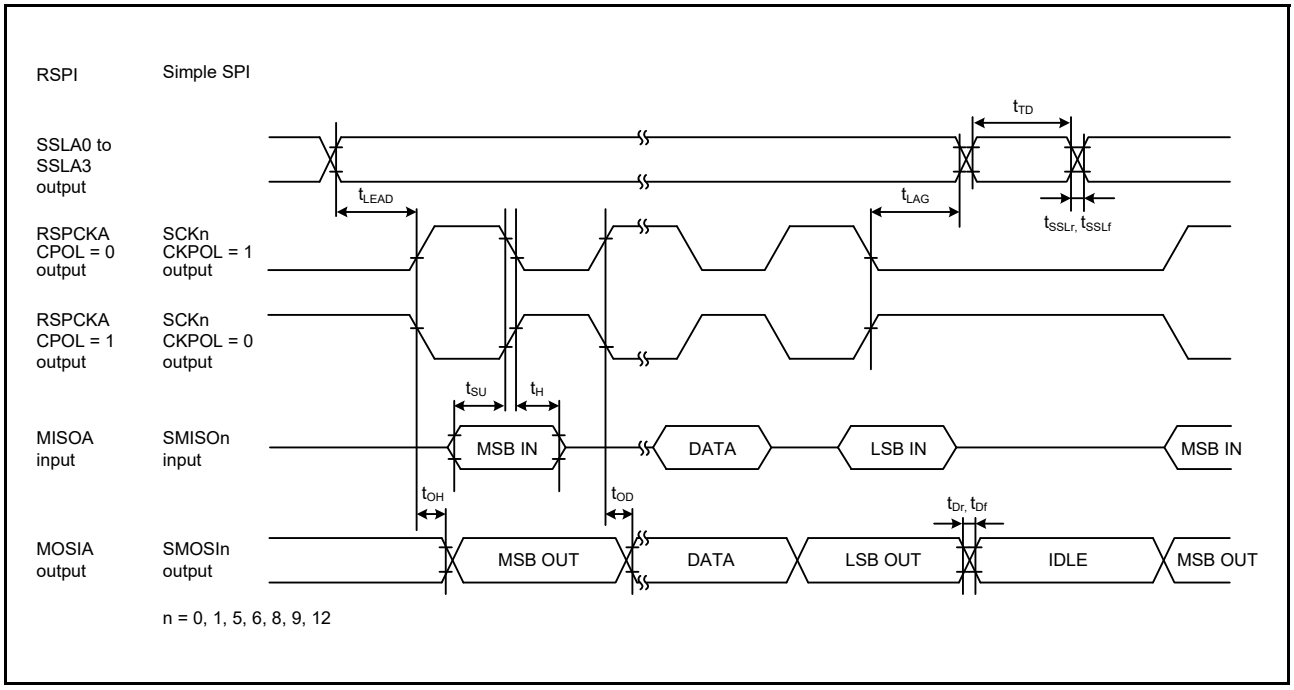


Figure 5.56 RSPI Timing (Master, CPHA = 1) and Simple SPI Clock Timing (Master, CKPH = 0)

Table 5.49 A/D Conversion Characteristics (4)

Conditions: 2.4V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5V, 2.4V ≤ VREFH0 ≤ AVCC0, VSS = AVSS0 = VSS_USB = 0V, reference voltage = VREFH0 selected, Ta = –40 to +105°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	16	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 16 MHz)	Permissible signal source impedance (Max.) = 2.2 kΩ	3.38	—	—	µs	High-precision channel The ADCSR.ADHSC bit is 1 The ADSSTRn register is 0Dh
		5.06	—	—		Normal-precision channel The ADCSR.ADHSC bit is 1 The ADSSTRn register is 28h
Analog input capacitance	Cs	—	—	15	pF	Pin capacitance included Figure 5.68
Analog input resistance	Rs	—	—	2.5	kΩ	Figure 5.68
Offset error		—	±0.5	±4.5	LSB	
Full-scale error		—	±0.75	±4.5	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential non-linearity error		—	±1.0	—	LSB	
INL integral non-linearity error		—	±1.0	±3.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential non-linearity error, and INL integral non-linearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

5.6 D/A Conversion Characteristics

Table 5.52 D/A Conversion Characteristics (1)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C
Reference voltage = VREFH or VREFL selected

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	—	—	12	Bit	
Resistive load	30	—	—	kΩ	
Capacitive load	—	—	50	pF	
Output voltage range	0.35	—	AVCC0 - 0.47	V	
DNL differential non-linearity error	—	±0.5	±1.0	LSB	
INL integral non-linearity error	—	±2.0	±8.0	LSB	
Offset error	—	—	±20	mV	
Full-scale error	—	—	±20	mV	
Output resistance	—	5	—	Ω	
Conversion time	—	—	30	μs	

Table 5.53 D/A Conversion Characteristics (2)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VREFL = VSS_USB = 0 V, T_a = –40 to +105°C
Reference voltage = AVCC0 or AVSS0 selected

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	—	—	12	Bit	
Resistive load	30	—	—	kΩ	
Capacitive load	—	—	50	pF	
Output voltage range	0.35	—	AVCC0 - 0.47	V	
DNL differential non-linearity error	—	±0.5	±2.0	LSB	
INL integral non-linearity error	—	±2.0	±8.0	LSB	
Offset error	—	—	±30	mV	
Full-scale error	—	—	±30	mV	
Output resistance	—	5	—	Ω	
Conversion time	—	—	30	μs	

Table 5.54 D/A Conversion Characteristics (3)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C
Reference voltage = internal reference voltage selected

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	—	—	12	Bit	
Internal reference voltage (Vbgr)	1.36	1.43	1.50	V	
Resistive load	30	—	—	kΩ	
Capacitive load	—	—	50	pF	
Output voltage range	0.35	—	Vbgr	V	
DNL differential non-linearity error	—	±2.0	±16.0	LSB	
INL integral non-linearity error	—	±8.0	±16.0	LSB	
Offset error	—	—	30	mV	
Output resistance	—	5	—	Ω	
Conversion time	—	—	30	μs	

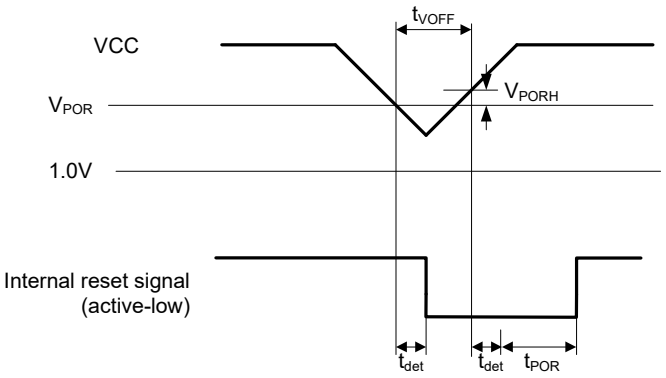
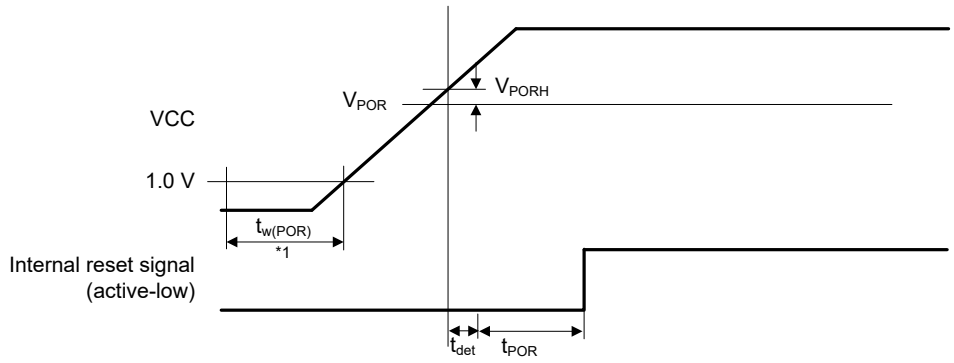


Figure 5.73 Voltage Detection Reset Timing



Note 1. $t_{w(POR)}$ is the time required for a power-on reset to be enabled while the external power VCC is being held below the valid voltage (1.0 V).
When turning the VCC on, maintain a voltage below 1.0V for at least 1.0ms.

Figure 5.74 Power-On Reset Timing

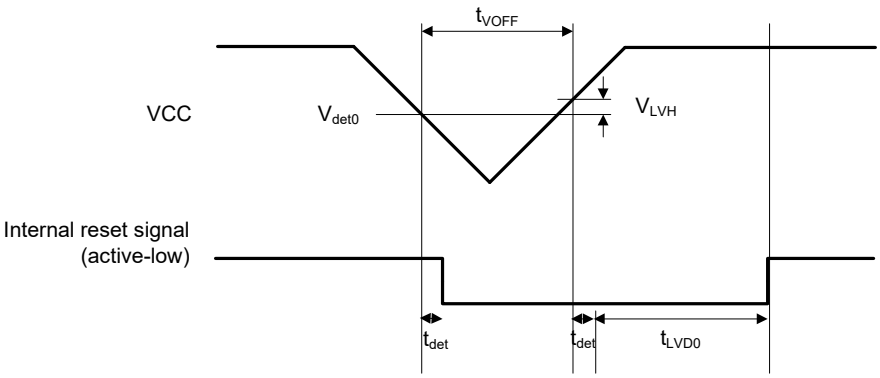
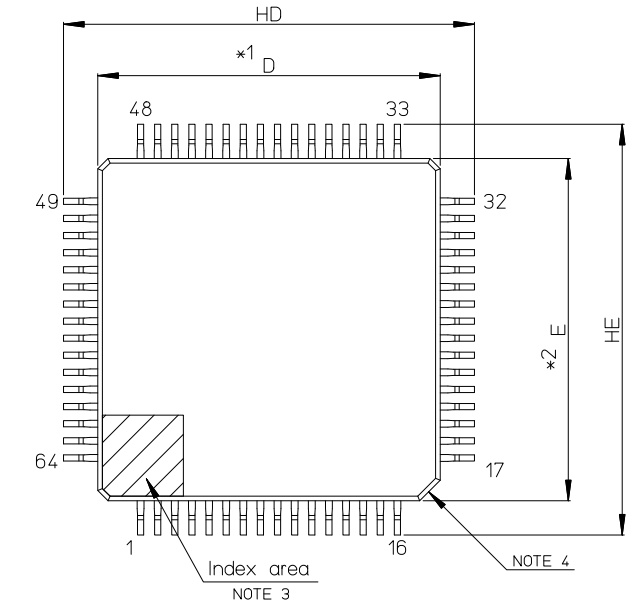
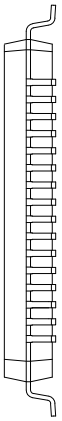
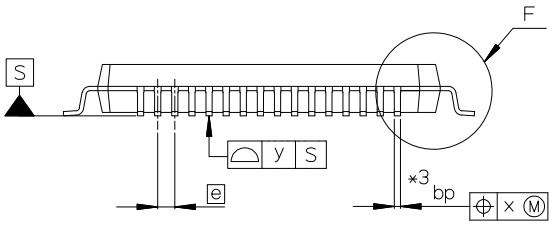


Figure 5.75 Voltage Detection Circuit Timing (Vdet0)

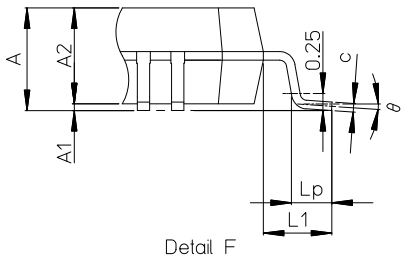
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP64-10x10-0.50	PLQP0064KB-C	——	0.3g







NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL; SIZE MAY VARY.



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A2	——	1.4	——
HD	11.8	12.0	12.2
HE	11.8	12.0	12.2
A	——	——	1.7
A1	0.05	——	0.15
bp	0.15	0.20	0.27
c	0.09	——	0.20
θ	0°	3.5°	8°
e	——	0.5	——
x	——	——	0.08
y	——	——	0.08
Lp	0.45	0.6	0.75
L1	——	1.0	——

Figure E 64 -Pin LFQFP (PLQP0064KB-C)