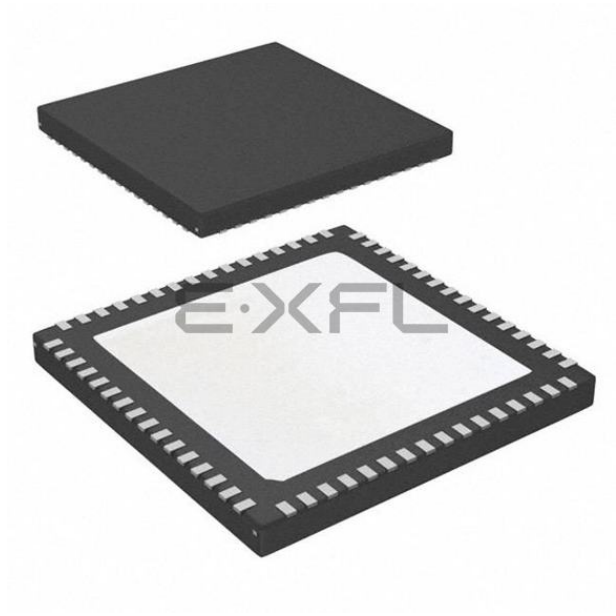
Renesas Electronics America Inc - R5F52318BDND#U0 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	54MHz
Connectivity	CANbus, I²C, IrDA, SCI, SD/SDIO, SPI, SSI, USB OTG
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	43
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-WFQFN Exposed Pad
Supplier Device Package	64-HWQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f52318bdnd-u0

Table 1.1 Outline of Specifications (2/4)

Classification	Module/Function	Description
Low power consumption	Low power consumption functions	• Module stop function • Three low power consumption modes Sleep mode, deep sleep mode, and software standby mode • Low power timer that operates during the software standby state
	Function for lower operating power consumption	• Operating power control modes High-speed operating mode, middle-speed operating mode, and low-speed operating mode
Interrupt	Interrupt controller (ICUb)	• Interrupt vectors: 167 • External interrupts: 9 (NMI, IRQ0 to IRQ7 pins) • Non-maskable interrupts: 7 (NMI pin, oscillation stop detection interrupt, voltage monitoring 1 interrupt, voltage monitoring 2 interrupt, WDT interrupt, IWDT interrupt, and VBATT power monitoring interrupt) • 16 levels specifiable for the order of priority
External bus extension		• The external address space can be divided into four areas (CS0 to CS3), each with independent control of access settings. Capacity of each area: 16 Mbytes (CS0 to CS3) A chip-select signal (CS0# to CS3#) can be output for each area. Each area is specifiable as an 8-bit or 16-bit bus space The data arrangement in each area is selectable as little or big endian (only for data). Bus format: Separate bus, multiplex bus • Wait control • Write buffer facility
DMA	DMA controller (DMACA)	• 4 channels • Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions
	Data transfer controller (DTCa)	• Transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Interrupts • Chain transfer function
I/O ports	General I/O ports	100-pin/64-pin/48-pin I/O: 79/43/30 (RX231 Group), 83/47/34 (RX230 Group) • Input: 1/1/1 Pull-up resistors: 79/43/30(RX231 Group), 83/47/34 (RX230 Group) • Open-drain outputs: 58/34/26 • 5-V tolerance: 8/5/5
Event link controller (ELC)		• Event signals of 61 types can be directly connected to the module • Operations of timer modules are selectable at event input • Capable of event link operation for port B and port E
Multi-function pin controller (MPC)		Capable of selecting the input/output function from multiple pins
Timers	16-bit timer pulse unit (TPUa)	• (16 bits × 6 channels) × 1 unit • Maximum of 16 pulse-input/output possible • Select from among seven or eight counter-input clock signals for each channel • Supports the input capture/output compare function • Output of PWM waveforms in up to 15 phases in PWM mode • Support for buffered operation, phase-counting mode (two-phase encoder input) and cascade connected operation (32 bits × 2 channels) depending on the channel. • Capable of generating conversion start triggers for the A/D converters • Signals from the input capture pins are input via a digital filter • Clock frequency measuring method
	Multi-function timer pulse unit 2 (MTU2a)	• (16 bits × 6 channels) × 1 unit • Up to 16 pulse-input/output lines and three pulse-input lines are available based on the six 16-bit timer channels • Select from among eight or seven counter-input clock signals for each channel (PCLK/1, PCLK/4, PCLK/16, PCLK/64, PCLK/256, PCLK/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD) other than channel 5, for which only four signals are available. • Input capture function • 21 output compare/input capture registers • Pulse output mode • Complementary PWM output mode • Reset synchronous PWM mode • Phase-counting mode • Capable of generating conversion start triggers for the A/D converter
	Port output enable 2 (POE2a)	Controls the high-impedance state of the MTU's waveform output pins
	Compare match timer (CMT)	• (16 bits × 2 channels) × 2 units • Select from among four clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512)
	Watchdog timer (WDTA)	• 14 bits x 1 channel • Select from among six counter-input clock signals (PCLK/4, PCLK/64, PCLK/128, PCLK/512, PCLK/2048, PCLK/8192)

Table 1.4 List of Products: G Version (T_a = –40 to +105°C) (2/2)

Group	Part No.	Order Part No.	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency	Security Function	SDHI	CAN	Operating Temperature
RX231	R5F52315AGFL	R5F52315AGFL#30	PLQP0048KB-B	128 Kbytes	32 Kbytes	8 Kbytes	54 MHz	Not available	Not available	Available	–40 to +105°C
	R5F52315CGFL	R5F52315CGFL#30						Not available	Not available	Not available	
RX230	R5F52306AGFP	R5F52306AGFP#30	PLQP0100KB-B	256 Kbytes	32 Kbytes	8 Kbytes	54 MHz	Not available	Not available	Not available	–40 to +105°C
	R5F52306AGND	R5F52306AGND#U0	PWQN0064KC-A					Not available	Not available	Not available	
	R5F52306AGFM	R5F52306AGFM#30	PLQP0064KB-C					Not available	Not available	Not available	
	R5F52306AGNE	R5F52306AGNE#U0	PWQN0048KB-A					Not available	Not available	Not available	
	R5F52306AGFL	R5F52306AGFL#30	PLQP0048KB-B					Not available	Not available	Not available	
	R5F52305AGFP	R5F52305AGFP#30	PLQP0100KB-B	128 Kbytes				Not available	Not available	Not available	
	R5F52305AGND	R5F52305AGND#U0	PWQN0064KC-A					Not available	Not available	Not available	
	R5F52305AGFM	R5F52305AGFM#30	PLQP0064KB-C					Not available	Not available	Not available	
	R5F52305AGNE	R5F52305AGNE#U0	PWQN0048KB-A					Not available	Not available	Not available	
	R5F52305AGFL	R5F52305AGFL#30	PLQP0048KB-B					Not available	Not available	Not available	

Table 1.5 Pin Functions (2/4)

Classifications	Pin Name	I/O	Description
16-bit timer pulse unit	TIOCA0, TIOCB0 TIOCC0, TIOCD0	I/O	The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins.
	TIOCA1, TIOCB1	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins.
	TIOCA2, TIOCB2	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins.
	TIOCA3, TIOCB3 TIOCC3, TIOCD3	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins.
	TIOCA4, TIOCB4	I/O	The TGRA4 and TGRB4 input capture input/output compare output/PWM output pins.
	TIOCA5, TIOCB5	I/O	The TGRA5 and TGRB5 input capture input/output compare output/PWM output pins.
	TCLKA, TCLKB TCLKC, TCLKD	Input	Input pins for external clock signals.
Multi-function timer pulse unit 2	MTIOC0A, MTIOC0B MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins.
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins.
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins.
	MTIOC3A, MTIOC3B MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins.
	MTIOC4A, MTIOC4B MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/PWM output pins.
	MTIC5U, MTIC5V, MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/external pulse input pins.
	MTCLKA, MTCLKB, MTCLKC, MTCLKD	Input	Input pins for the external clock.
Port output enable 2	POE0# to POE3#, POE8#	Input	Input pins for request signals to place the MTU pins in the high impedance state.
Realtime clock	RTCOUT	Output	Output pin for the 1-Hz/64-Hz clock.
	RTCIC0 to RTCIC2	Input	Time capture event input pins.
8-bit timer	TMO0 to TMO3	Output	Compare match output pins.
	TMCI0 to TMCI3	Input	Input pins for the external clock to be input to the counter.
	TMRI0 to TMRI3	Input	Counter reset input pins.
Serial communications interface (SCIg)	• Asynchronous mode/clock synchronous mode		
	SCK0, SCK1, SCK5, SCK6, SCK8, SCK9	I/O	Input/output pins for the clock.
	RXD0, RXD1, RXD5, RXD6, RXD8, RXD9	Input	Input pins for received data.
	TXD0, TXD1, TXD5, TXD6, TXD8, TXD9	Output	Output pins for transmitted data.
	CTS0#, CTS1#, CTS5#, CTS6#, CTS8#, CTS9#	Input	Input pins for controlling the start of transmission and reception.
	RTS0#, RTS1#, RTS5#, RTS6#, RTS8#, RTS9#	Output	Output pins for controlling the start of transmission and reception.
	• Simple I^2C mode		
	SSCL0, SSCL1, SSCL5, SSCL6, SSCL8, SSCL9	I/O	Input/output pins for the I^2C clock.
	SSDA0, SSDA1, SSDA5, SSDA6, SSDA8, SSDA9	I/O	Input/output pins for the I^2C data.

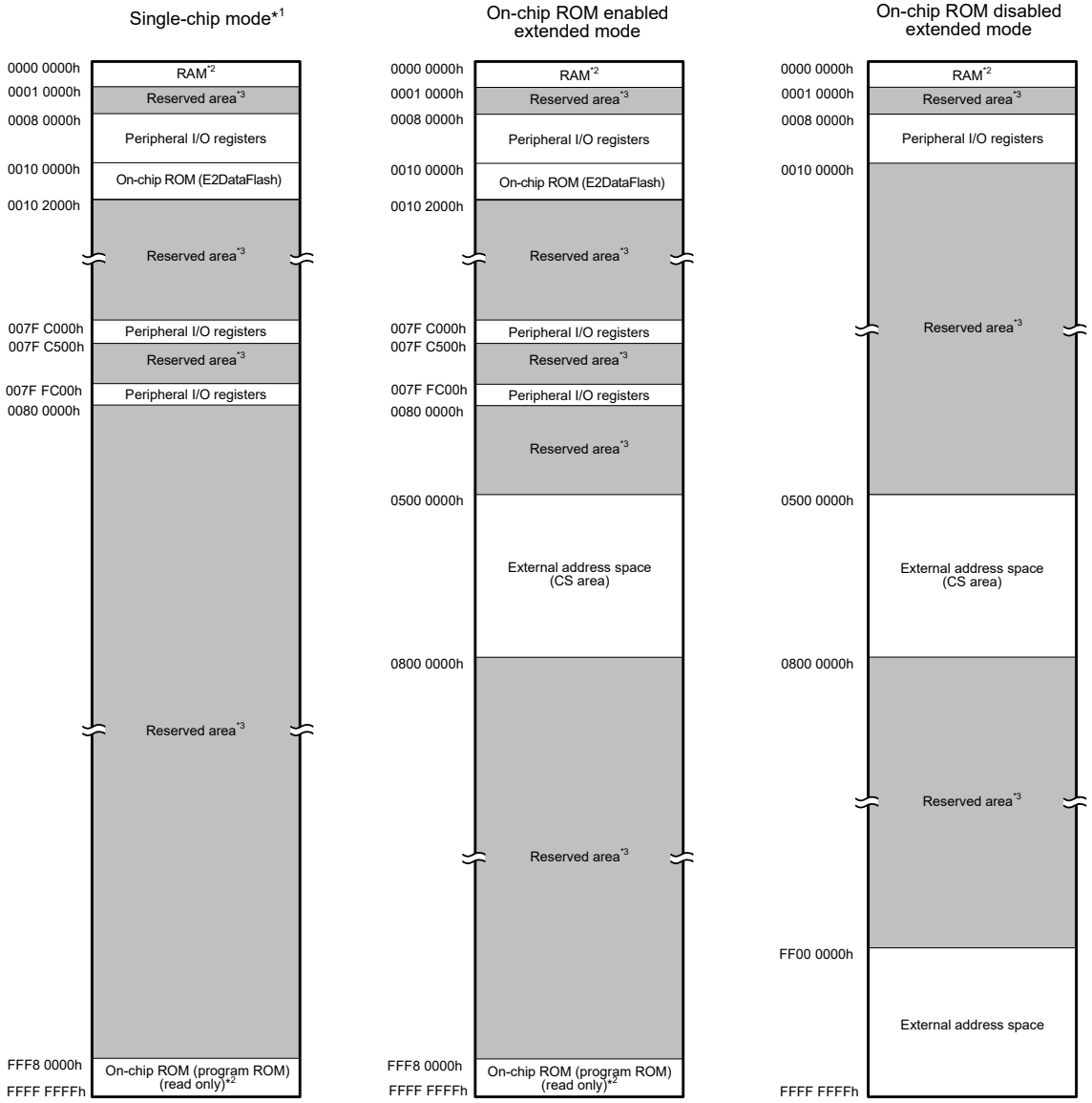
Table 1.6 List of Pins and Pin Functions (100-Pin TFLGA) (1/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCI, RSPI, RIIC, RSCAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
A1		P05						DA1
A2	VREFH							
A3		P07						ADTRG0#
A4	VREFL0							
A5		P43						AN003
A6		PD0	D0[A0/D0]					IRQ0/AN024
A7		PD4	D4[A4/D4]	POE3#				IRQ4/AN028
A8		PE0	D8[A8/D8]		SCK12			AN016
A9		PE1	D9[A9/D9]	MTIOC4C	TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12			AN017/ CMPB0
A10		PE2	D10[A10/D10]	MTIOC4A	RXD12/RXDX12/ SMISO12/SSCL12			IRQ7/AN018/ CVREFB0
B1		P03						DA0
B2	AVSS0							
B3	AVCC0							
B4		P40						AN000
B5		P44						AN004
B6		PD1	D1[A1/D1]	MTIOC4B				IRQ1/AN025
B7		PD3	D3[A3/D3]	POE8#				IRQ3/AN027
B8		PD6	D6[A6/D6]	MTIC5V/POE1#				IRQ6/AN030
B9		PD7	D7[A7/D7]	MTIC5U/POE0#				IRQ7/AN031
B10		PE3	D11[A11/D11]	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#/ AUDIO_MCLK			AN019/ CLKOUT
C1	VCL							
C2	VREFL							
C3		PJ3		MTIOC3C	CTS6#/RTS6#/SS6#			
C4	VREFH0							
C5		P42						AN002
C6		P47						AN007
C7		PD2	D2[A2/D2]	MTIOC4D				IRQ2/AN026
C8		PD5	D5[A5/D5]	MTIC5W/POE2#				IRQ5/AN029
C9		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B				IRQ5/AN021/ CMPOB0
C10		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A				AN020/ CMPA2/ CLKOUT
D1	XCIN							
D2	XCOUT							
D3	MD							FINED
D4	VBATT							
D5		P45						AN005
D6		P46						AN006
D7		PE6	D14[A14/D14]					IRQ6/AN022
D8		PE7	D15[A15/D15]					IRQ7/AN023
D9		PA1	A1	MTIOC0B/MTCLKC/ TIOCB0	SCK5/SSLA2/SSISCK0			
D10		PA0	A0/BC0#	MTIOC4A/TIOCA0	SSLA1			CACREF
E1	XTAL	P37						
E2	VSS							
E3	RES#							
E4		P34		MTIOC0A/TMCI3/POE2#	SCK6		TS0	IRQ4
E5		P41						AN001
E6		PA2	A2		RXD5/SMISO5/SSCL5/ SSLA3/IRRXD5			
E7		PA6	A6	MTIC5V/MTCLKB/TMCI3/ POE2#/TIOCA2	CTS5#/RTS5#/SS5#/ MOSIA/SSIWS0			

Table 1.6 List of Pins and Pin Functions (100-Pin TFLGA) (3/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCI, RSPI, RIIC, RSCAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
J6	VCC_USB*1	PH3*1		TMCI0*1				
J7		P50	WR0#/WR#				TS20	
J8		PC4	A20/CS3#	MTIOC3D/MTCLKC/TMCI1/ POE0#	SCK5/CTS8#/RTS8#/ SS8#/SSLA0	SDHI_D1	TSCAP	
J9		PC0	A16	MTIOC3C/TCLKC	CTS5#/RTS5#/SS5#/ SSLA1		TS35	
J10		PC1	A17	MTIOC3A/TCLKD	SCK5/SSLA2		TS33	
K1		P23		MTIOC3D/MTCLKD/ TIOCD3	CTS0#/RTS0#/SS0#/ SSISCK0		TS6	
K2		P22		MTIOC3B/MTCLKC/TMO0/ TIOCC3	SCK0/ USB0_OVRCURB/ AUDIO_MCLK		TS7	
K3		P20		MTIOC1A/TMRI0/TIOCB3	TXD0/SMOSI0/SSDA0/ USB0_ID/SSIRXD0		TS9	
K4		P14		MTIOC3A/MTCLKA/TMRI2/ TIOCB5/TCLKA	CTS1#/RTS1#/SS1#/ CTXD0/USB0_OVRCURA		TS13	IRQ4/ CVREFB2
K5		PH2*1		TMRI0*1	USB0_DM*1			IRQ1*1
K6		PH1*1		TMO0*1	USB0_DP*1			IRQ0*1
K7		P51	WR1#/BC1#/ WAIT#				TS19	
K8		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/TMRI2	SCK8/RSPCKA		TS23	
K9		PC3	A19	MTIOC4D/TCLKB	TXD5/SMOSI5/SSDA5/ IRTXD5	SDHI_D0	TS27	
K10		PC2	A18	MTIOC4B/TCLKA	RXD5/SMISO5/SSCL5/ SSLA3/ IRRXD5	SDHI_D3	TS30	

Note 1. RX230: PH0/CACREF, PH1/IRQ0/TMO0, PH2/IRQ1/TMRI0, PH3/TMCI0
RX231: VSS_USB, USB0_DP, USB0_DM, VCC_USB



Note 1. The address space in boot mode and USB boot mode is the same as the address space in single-chip mode.
Note 2. The capacity of ROM/RAM differs depending on the products.

ROM (bytes)		RAM (bytes)	
Capacity	**Address**	**Capacity**	**Address**
512 Kbytes	FFF8 0000h to FFFF FFFFh	64 Kbytes	0000 0000h to 0000 FFFFh
384 Kbytes	FFFA 0000h to FFFF FFFFh		
256 Kbytes	FFFC 0000h to FFFF FFFFh	32 Kbytes	0000 0000h to 0000 7FFFh
128 Kbytes	FFFE 0000h to FFFF FFFFh		

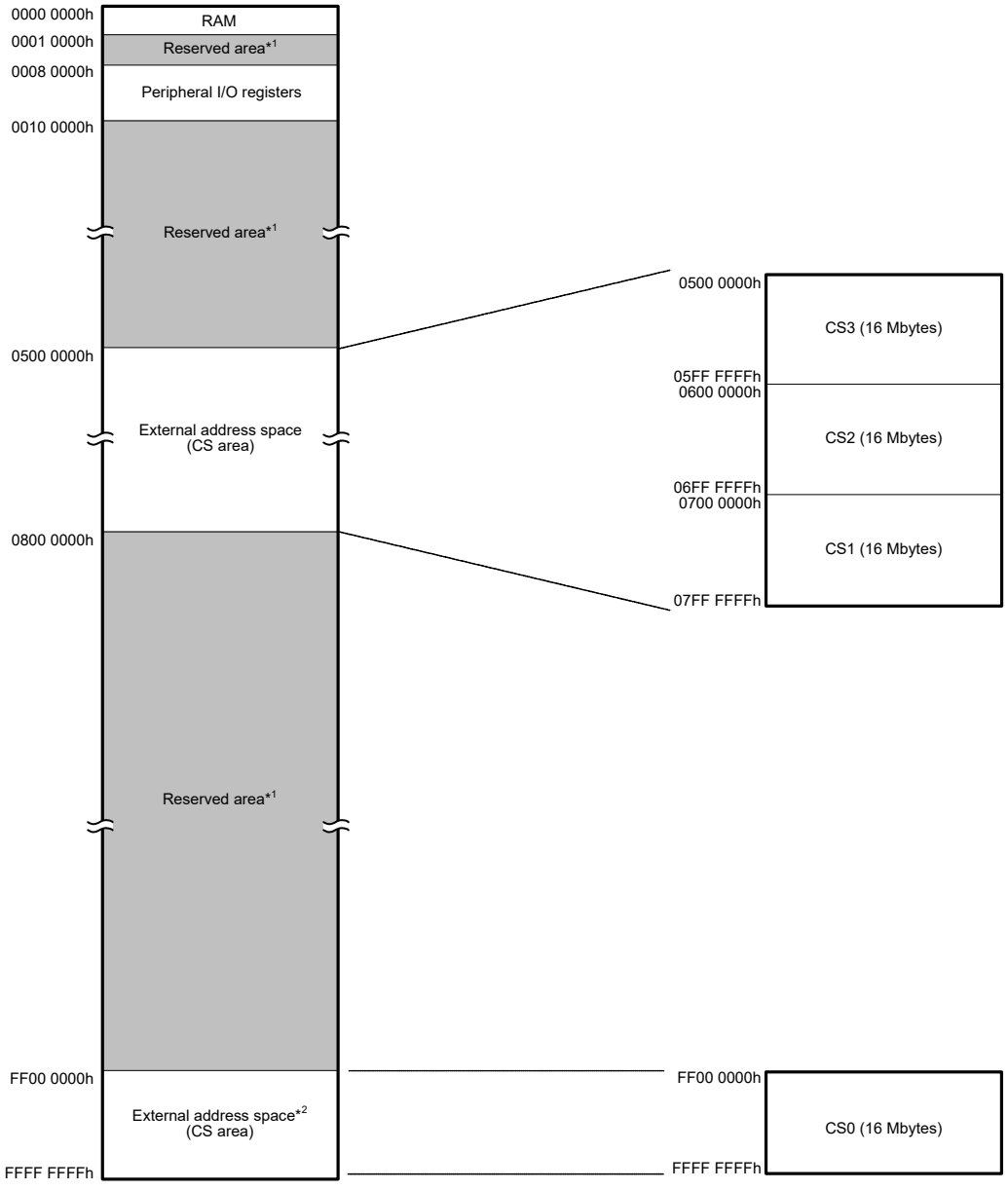
Note: See Table 1.3 and Table 1.4 List of Products, for the product type name.

Note 3. Reserved areas should not be accessed.

Figure 3.1 Memory Map in Each Operating Mode

3.2 External Address Space

The external address space is divided into up to four CS areas (CS0 to CS3), each corresponding to the CSn# signal output from a CSn# (n = 0 to 3) pin. Figure 3.2 shows the address ranges corresponding to the individual CS areas (CS0 to CS3) in on-chip ROM disabled extended mode.



Note 1. Reserved areas should not be accessed.
Note 2. The CS0 area is disabled in on-chip ROM enabled extended mode.
In this mode, the address space for addresses above 1000 0000h is as shown in figure on this section, Memory Map in Each Operating Mode.

Figure 3.2 Correspondence between External Address Spaces and CS Areas (In On-Chip ROM Disabled Extended Mode)

Table 4.1 List of I/O Registers (Address Order) (4/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK <PCLK
0008 711Bh to 0008 71FFh	ICU	DTC Activation Enable Register 027 to DTC Activation Enable Register 255	DTCER027 to DTCER255	8	8	2 ICLK	
0008 7202h to 0008 721Fh	ICU	Interrupt Request Enable Register 02 to Interrupt Request Enable Register 1F	IER02 to IER1F	8	8	2 ICLK	
0008 72E0h	ICU	Software Interrupt Generation Register	SWINTR	8	8	2 ICLK	
0008 72F0h	ICU	Fast Interrupt Set Register	FIR	16	16	2 ICLK	
0008 7300h to 0008 73FFh	ICU	Interrupt Source Priority Register 000 to Interrupt Source Priority Register 255	IPR000 to IPR255	8	8	2 ICLK	
0008 7400h	ICU	DMAC Activation Request Select Register 0	DMRSR0	8	8	2 ICLK	
0008 7404h	ICU	DMAC Activation Request Select Register 1	DMRSR1	8	8	2 ICLK	
0008 7408h	ICU	DMAC Activation Request Select Register 2	DMRSR2	8	8	2 ICLK	
0008 740Ch	ICU	DMAC Activation Request Select Register 3	DMRSR3	8	8	2 ICLK	
0008 7500h to 0008 7507h	ICU	IRQ Control Register 0 to IRQ Control Register 7	IRQCR0 to IRQCR7	8	8	2 ICLK	
0008 7510h	ICU	IRQ Pin Digital Filter Enable Register 0	IRQFLTE0	8	8	2 ICLK	
0008 7514h	ICU	IRQ Pin Digital Filter Setting Register 0	IRQFLTC0	16	16	2 ICLK	
0008 7580h	ICU	Non-Maskable Interrupt Status Register	NMISR	8	8	2 ICLK	
0008 7581h	ICU	Non-Maskable Interrupt Enable Register	NMIER	8	8	2 ICLK	
0008 7582h	ICU	Non-Maskable Interrupt Status Clear Register	NMICLR	8	8	2 ICLK	
0008 7583h	ICU	NMI Pin Interrupt Control Register	NMICR	8	8	2 ICLK	
0008 7590h	ICU	NMI Pin Digital Filter Enable Register	NMIFLTE	8	8	2 ICLK	
0008 7594h	ICU	NMI Pin Digital Filter Setting Register	NMIFLTC	8	8	2 ICLK	
0008 8000h	CMT	Compare Match Timer Start Register 0	CMSTR0	16	16	2 or 3 PCLKB	2 ICLK
0008 8002h	CMT0	Compare Match Timer Control Register	CMCR	16	16	2 or 3 PCLKB	2 ICLK
0008 8004h	CMT0	Compare Match Counter	CMCNT	16	16	2 or 3 PCLKB	2 ICLK
0008 8006h	CMT0	Compare Match Constant Register	CMCOR	16	16	2 or 3 PCLKB	2 ICLK
0008 8008h	CMT1	Compare Match Timer Control Register	CMCR	16	16	2 or 3 PCLKB	2 ICLK
0008 800Ah	CMT1	Compare Match Counter	CMCNT	16	16	2 or 3 PCLKB	2 ICLK
0008 800Ch	CMT1	Compare Match Constant Register	CMCOR	16	16	2 or 3 PCLKB	2 ICLK
0008 8010h	CMT	Compare Match Timer Start Register 1	CMSTR1	16	16	2 or 3 PCLKB	2 ICLK
0008 8012h	CMT2	Compare Match Timer Control Register	CMCR	16	16	2 or 3 PCLKB	2 ICLK
0008 8014h	CMT2	Compare Match Counter	CMCNT	16	16	2 or 3 PCLKB	2 ICLK
0008 8016h	CMT2	Compare Match Constant Register	CMCOR	16	16	2 or 3 PCLKB	2 ICLK
0008 8018h	CMT3	Compare Match Timer Control Register	CMCR	16	16	2 or 3 PCLKB	2 ICLK
0008 801Ah	CMT3	Compare Match Counter	CMCNT	16	16	2 or 3 PCLKB	2 ICLK
0008 801Ch	CMT3	Compare Match Constant Register	CMCOR	16	16	2 or 3 PCLKB	2 ICLK
0008 8020h	WDT	WDT Refresh Register	WDTRR	8	8	2 or 3 PCLKB	2 ICLK
0008 8022h	WDT	WDT Control Register	WDTCR	16	16	2 or 3 PCLKB	2 ICLK
0008 8024h	WDT	WDT Status Register	WDTSR	16	16	2 or 3 PCLKB	2 ICLK
0008 8026h	WDT	WDT Reset Control Register	WDTRCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8030h	IWDT	IWDT Refresh Register	IWDTRR	8	8	2 or 3 PCLKB	2 ICLK
0008 8032h	IWDT	IWDT Control Register	IWDTCR	16	16	2 or 3 PCLKB	2 ICLK
0008 8034h	IWDT	IWDT Status Register	IWDTSR	16	16	2 or 3 PCLKB	2 ICLK
0008 8036h	IWDT	IWDT Reset Control Register	IWDTRCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8038h	IWDT	IWDT Count Stop Control Register	IWDTCSTPR	8	8	2 or 3 PCLKB	2 ICLK
0008 8040h	DA	D/A Data Register 0	DADR0	16	16	2 or 3 PCLKB	2 ICLK
0008 8042h	DA	D/A Data Register 1	DADR1	16	16	2 or 3 PCLKB	2 ICLK
0008 8044h	DA	D/A Control Register	DACR	8	8	2 or 3 PCLKB	2 ICLK
0008 8045h	DA	DADRm Format Select Register	DADPR	8	8	2 or 3 PCLKB	2 ICLK
0008 8046h	DA	D/A A/D Synchronous Start Control Register	DAADSCR	8	8	2 or 3 PCLKB	2 ICLK
0008 8047h	DA	D/A VREF Control Register	DAVREFCR	8	8	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (8/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK <PCLK
0008 901Eh	S12AD	A/D Self-Diagnosis Data Register	ADRD	16	16	2 or 3 PCLKB	2 ICLK
0008 9020h	S12AD	A/D Data Register 0	ADDR0	16	16	2 or 3 PCLKB	2 ICLK
0008 9022h	S12AD	A/D Data Register 1	ADDR1	16	16	2 or 3 PCLKB	2 ICLK
0008 9024h	S12AD	A/D Data Register 2	ADDR2	16	16	2 or 3 PCLKB	2 ICLK
0008 9026h	S12AD	A/D Data Register 3	ADDR3	16	16	2 or 3 PCLKB	2 ICLK
0008 9028h	S12AD	A/D Data Register 4	ADDR4	16	16	2 or 3 PCLKB	2 ICLK
0008 902Ah	S12AD	A/D Data Register 5	ADDR5	16	16	2 or 3 PCLKB	2 ICLK
0008 902Ch	S12AD	A/D Data Register 6	ADDR6	16	16	2 or 3 PCLKB	2 ICLK
0008 902Eh	S12AD	A/D Data Register 7	ADDR7	16	16	2 or 3 PCLKB	2 ICLK
0008 9040h	S12AD	A/D Data Register 16	ADDR16	16	16	2 or 3 PCLKB	2 ICLK
0008 9042h	S12AD	A/D Data Register 17	ADDR17	16	16	2 or 3 PCLKB	2 ICLK
0008 9044h	S12AD	A/D Data Register 18	ADDR18	16	16	2 or 3 PCLKB	2 ICLK
0008 9046h	S12AD	A/D Data Register 19	ADDR19	16	16	2 or 3 PCLKB	2 ICLK
0008 9048h	S12AD	A/D Data Register 20	ADDR20	16	16	2 or 3 PCLKB	2 ICLK
0008 904Ah	S12AD	A/D Data Register 21	ADDR21	16	16	2 or 3 PCLKB	2 ICLK
0008 904Ch	S12AD	A/D Data Register 22	ADDR22	16	16	2 or 3 PCLKB	2 ICLK
0008 904Eh	S12AD	A/D Data Register 23	ADDR23	16	16	2 or 3 PCLKB	2 ICLK
0008 9050h	S12AD	A/D Data Register 24	ADDR24	16	16	2 or 3 PCLKB	2 ICLK
0008 9052h	S12AD	A/D Data Register 25	ADDR25	16	16	2 or 3 PCLKB	2 ICLK
0008 9055h	S12AD	A/D Data Register 26	ADDR26	16	16	2 or 3 PCLKB	2 ICLK
0008 9056h	S12AD	A/D Data Register 27	ADDR27	16	16	2 or 3 PCLKB	2 ICLK
0008 9058h	S12AD	A/D Data Register 28	ADDR28	16	16	2 or 3 PCLKB	2 ICLK
0008 905Ah	S12AD	A/D Data Register 29	ADDR29	16	16	2 or 3 PCLKB	2 ICLK
0008 905Ch	S12AD	A/D Data Register 30	ADDR30	16	16	2 or 3 PCLKB	2 ICLK
0008 905Eh	S12AD	A/D Data Register 31	ADDR31	16	16	2 or 3 PCLKB	2 ICLK
0008 907Ah	S12AD	A/D Disconnection Detection Control Register	ADDISCR	8	8	2 or 3 PCLKB	2 ICLK
0008 907Dh	S12AD	A/D Event Link Control Register	ADELCCR	8	8	2 or 3 PCLKB	2 ICLK
0008 9080h	S12AD	A/D Group Scan Priority Control Register	ADGSPCR	16	16	2 or 3 PCLKB	2 ICLK
0008 908Ah	S12AD	A/D High-Side/Low-Side Reference Voltage Control Register	ADHVREFCNT	8	8	2 or 3 PCLKB	2 ICLK
0008 908Ch	S12AD	A/D Compare Function Window A/B Status Monitor Register	ADWINMON	8	8	2 or 3 PCLKB	2 ICLK
0008 9090h	S12AD	A/D Compare Function Control Register	ADCMPCR	16	16	2 or 3 PCLKB	2 ICLK
0008 9092h	S12AD	A/D Compare Function Window A Extended Input Select Register	ADCMPANSER	8	8	2 or 3 PCLKB	2 ICLK
0008 9093h	S12AD	A/D Compare Function Window A Extended Input Comparison Condition Setting Register	ADCMPLER	8	8	2 or 3 PCLKB	2 ICLK
0008 9094h	S12AD	A/D Compare Function Window A Channel Select Register 0	ADCMPANSR0	16	16	2 or 3 PCLKB	2 ICLK
0008 9096h	S12AD	A/D Compare Function Window A Channel Select Register 1	ADCMPANSR1	16	16	2 or 3 PCLKB	2 ICLK
0008 9098h	S12AD	A/D Compare Function Window A Comparison Condition Setting Register 0	ADCMPLR0	16	16	2 or 3 PCLKB	2 ICLK
0008 909Ah	S12AD	A/D Compare Function Window A Comparison Condition Setting Register 1	ADCMPLR1	16	16	2 or 3 PCLKB	2 ICLK
0008 909Ch	S12AD	A/D Compare Function Window A Lower-Side Level Setting Register	ADCMPDR0	16	16	2 or 3 PCLKB	2 ICLK
0008 909Eh	S12AD	A/D Compare Function Window A Upper-Side Level Setting Register	ADCMPDR1	16	16	2 or 3 PCLKB	2 ICLK
0008 90A0h	S12AD	A/D Compare Function Window A Channel Status Register 0	ADCMPSR0	16	16	2 or 3 PCLKB	2 ICLK
0008 90A2h	S12AD	A/D Compare Function Window A Channel Status Register 1	ADCMPSR1	16	16	2 or 3 PCLKB	2 ICLK
0008 90A4h	S12AD	A/D Compare Function Window A Extended Input Channel Status Register	ADCMPSER	16	16	2 or 3 PCLKB	2 ICLK
0008 90A6h	S12AD	A/D Compare Function Window B Channel Select Register	ADCMPBNSR	8	8	2 or 3 PCLKB	2 ICLK
0008 90A8h	S12AD	A/D Compare Function Window B Lower-Side Level Setting Register	ADWINLLB	16	16	2 or 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (33/33)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK <PCLK
000D 0C80h	MTU5	Timer Counter U	TCNTU	16	16	2 or 3 PCLKA	2 ICLK
000D 0C82h	MTU5	Timer General Register U	TGRU	16	16	2 or 3 PCLKA	2 ICLK
000D 0C84h	MTU5	Timer Control Register U	TCRU	8	8	2 or 3 PCLKA	2 ICLK
000D 0C86h	MTU5	Timer I/O Control Register U	TIORU	8	8	2 or 3 PCLKA	2 ICLK
000D 0C90h	MTU5	Timer Counter V	TCNTV	16	16	2 or 3 PCLKA	2 ICLK
000D 0C92h	MTU5	Timer General Register V	TGRV	16	16	2 or 3 PCLKA	2 ICLK
000D 0C94h	MTU5	Timer Control Register V	TCRV	8	8	2 or 3 PCLKA	2 ICLK
000D 0C96h	MTU5	Timer I/O Control Register V	TIORV	8	8	2 or 3 PCLKA	2 ICLK
000D 0CA0h	MTU5	Timer Counter W	TCNTW	16	16	2 or 3 PCLKA	2 ICLK
000D 0CA2h	MTU5	Timer General Register W	TGRW	16	16	2 or 3 PCLKA	2 ICLK
000D 0CA4h	MTU5	Timer Control Register W	TCRW	8	8	2 or 3 PCLKA	2 ICLK
000D 0CA6h	MTU5	Timer I/O Control Register W	TIORW	8	8	2 or 3 PCLKA	2 ICLK
000D 0CB2h	MTU5	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKA	2 ICLK
000D 0CB4h	MTU5	Timer Start Register	TSTR	8	8	2 or 3 PCLKA	2 ICLK
000D 0CB6h	MTU5	Timer Compare Match Clear Register	TCNTCMPCLR	8	8	2 or 3 PCLKA	2 ICLK
007F C090h	FLASH	E2 DataFlash Control Register	DFLCTL	8	8	2 or 3 FCLK	2 ICLK
007F C0ACh	TEMPSA	Temperature Sensor Calibration Data Register L	TSCDRL	8	8	2 or 3 PCLKA	2ICLK
007F C0ADh	TEMPSA	Temperature Sensor Calibration Data Register H	TSCDRH	8	8	2 or 3 PCLKA	2ICLK
007F C100h	FLASH	Flash P/E Mode Control Register	FPMCR	8	8	2 or 3 FCLK	2 ICLK
007F C104h	FLASH	Flash Area Select Register	FASR	8	8	2 or 3 FCLK	2 ICLK
007F C108h	FLASH	Flash Processing Start Address Register L	FSARL	16	16	2 or 3 FCLK	2 ICLK
007F C110h	FLASH	Flash Processing Start Address Register H	FSARH	16	16	2 or 3 FCLK	2 ICLK
007F C114h	FLASH	Flash Control Register	FCR	8	8	2 or 3 FCLK	2 ICLK
007F C118h	FLASH	Flash Processing End Address Register L	FEARL	16	16	2 or 3 FCLK	2 ICLK
007F C120h	FLASH	Flash Processing End Address Register H	FEARH	16	16	2 or 3 FCLK	2 ICLK
007F C124h	FLASH	Flash Reset Register	FRESETR	8	8	2 or 3 FCLK	2 ICLK
007F C12Ch	FLASH	Flash Status Register 1	FSTATR1	8	8	2 or 3 FCLK	2 ICLK
007F C130h	FLASH	Flash Write Buffer Register 0	FWB0	16	16	2 or 3 FCLK	2 ICLK
007F C138h	FLASH	Flash Write Buffer Register 1	FWB1	16	16	2 or 3 FCLK	2 ICLK
007F C140h	FLASH	Flash Write Buffer Register 2	FWB2	16	16	2 or 3 FCLK	2 ICLK
007F C144h	FLASH	Flash Write Buffer Register 3	FWB3	16	16	2 or 3 FCLK	2 ICLK
007F C180h	FLASH	Protection Unlock Register	FPR	8	8	2 or 3 FCLK	2 ICLK
007F C184h	FLASH	Protection Unlock Status Register	FPSR	8	8	2 or 3 FCLK	2 ICLK
007F C1C0h	FLASH	Flash Start-Up Setting Monitor Register	FSCMR	16	16	2 or 3 FCLK	2 ICLK
007F C1C8h	FLASH	Flash Access Window Start Address Monitor Register	FAWSMR	16	16	2 or 3 FCLK	2 ICLK
007F C1D0h	FLASH	Flash Access Window End Address Monitor Register	FAWEMR	16	16	2 or 3 FCLK	2 ICLK
007F C1D8h	FLASH	Flash Initial Setting Register	FISR	8	8	2 or 3 FCLK	2 ICLK
007F C1DCh	FLASH	Flash Extra Area Control Register	FEXCR	8	8	2 or 3 FCLK	2 ICLK
007F C1E0h	FLASH	Flash Error Address Monitor Register L	FEAML	16	16	2 or 3 FCLK	2 ICLK
007F C1E8h	FLASH	Flash Error Address Monitor Register H	FEAMH	8	8	2 or 3 FCLK	2 ICLK
007F C1F0h	FLASH	Flash Status Register 0	FSTATR0	8	8	2 or 3 FCLK	2 ICLK
007F C350h	FLASHCONST	Unique ID Register 0	UIDR0	32	32	2 or 3 FCLK	2 ICLK
007F C354h	FLASHCONST	Unique ID Register 1	UIDR1	32	32	2 or 3 FCLK	2 ICLK
007F C358h	FLASHCONST	Unique ID Register 2	UIDR2	32	32	2 or 3 FCLK	2 ICLK
007F C35Ch	FLASHCONST	Unique ID Register 3	UIDR3	32	32	2 or 3 FCLK	2 ICLK
007F FFB2h	FLASH	Flash P/E Mode Entry Register	FENTRYR	16	16	2 or 3 FCLK	2 ICLK

Note 1. Odd addresses cannot be accessed in 16-bit units. Table 26.4 lists register allocation for 16-bit access in the User's Manual: Hardware.
Note 2. When the register is accessed while the USB is operating, a delay may be generated in accessing.

Table 5.2 Recommended Operating Voltage Conditions

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltages	VCC*1, *2	When USB is not used	1.8	—	5.5	V
		When USB is used When USB regulator is not used	3.0	—	3.6	
		When USB is used When USB regulator is used	4.0	—	5.5	
	VSS		—	0	—	
USB power supply voltages	VCC_USB	When USB regulator is not used	—	VCC	—	V
	VSS_USB		—	0	—	
VBATT power supply voltage	VBATT		1.8	—	5.5	V
Analog power supply voltages	AVCC0*1, *2		1.8	—	5.5	V
	AVSS0		—	0	—	
	VREFH0		1.8	—	AVCC0	
	VREFL0		—	0	—	
	VREFH		1.8	—	AVCC0	
	VREFL		—	0	—	

Note 1. Use AVCC0 and VCC under the following conditions:
AVCC0 and VCC can be set individually within the operating range when VCC ≥ 2.0 V
AVCC0 = VCC when VCC < 2.0 V
Note 2. When powering on the VCC and AVCC0 pins, power them on at the same time or the VCC pin first and then the AVCC0 pin.

Table 5.4 DC Characteristics (2)

Conditions: 1.8 V ≤ VCC = VCC_USB < 2.7 V, 1.8 V ≤ AVCC0 < 2.7 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	Ports 12, 13, 16, 17, port B5 (5 V tolerant)	V_{IH}	VCC × 0.8	—	5.8	V	
	Ports 14 to 15, ports 20 to 27, ports 30 to 37, ports 50 to 55, ports A0 to A7, ports B0 to B4, B6, B7, ports C0 to C7, ports D0 to D7, ports E0 to E7, port J3, RES#		VCC × 0.8	—	VCC + 0.3		
	Ports 03, 05, 07, ports 40 to 47		AVCC0 × 0.8	—	AVCC0 + 0.3		
	Ports 03, 05, 07, ports 40 to 47	V_{IL}	–0.3	—	AVCC0 × 0.2		
	Ports other than above		–0.3	—	VCC × 0.2		
	Ports 03, 05, 07, ports 40 to 47	ΔV_T	AVCC0 × 0.01	—	—		
	Ports other than above		VCC × 0.01	—	—		
Input level voltage (except for Schmitt trigger input pins)	MD	V_{IH}	VCC × 0.9	—	VCC + 0.3	V	
	EXTAL (external clock input)		VCC × 0.8	—	VCC + 0.3		
	MD	V_{IL}	–0.3	—	VCC × 0.1		
	EXTAL (external clock input)		–0.3	—	VCC × 0.2		

Table 5.5 DC Characteristics (3)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input leakage current	RES#, MD, port 35	$\lvert I_{in} \rvert$	—	—	1.0	μA	V_{in} = 0 V, VCC
Three-state leakage current (off-state)	Ports for 5 V tolerant	$\lvert I_{TSI} \rvert$	—	—	1.0	μA	V_{in} = 0 V, 5.8V
	Ports except for 5 V tolerant		—	—	0.2	μA	V_{in} = 0 V, VCC
Input capacitance	All input pins (except for port 35, USB0_DM, USB0_DP)	C_{in}	—	—	15	pF	V_{in} = 0 mV, f = 1 MHz, T_a = 25°C
	Port 35, USB0_DM, USB0_DP		—	—	30		

Table 5.6 DC Characteristics (4)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input pull-up resistor	All ports (except for port 35)	R_U	10	20	50	kΩ	V_{in} = 0 V

Table 5.18 Output Values of Voltage (1)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 < 2.7 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item				Symbol	Min.	Max.	Unit	Test Conditions
Output low	All output ports	Normal output mode		V_{OL}	—	0.3	V	I_{OL} = 0.5 mA
		High-drive output mode			—	0.3		I_{OL} = 1.0 mA
Output high	All output ports	Normal output mode	Ports 03, 05, 07, Ports 40 to 47	V_{OH}	AVCC0 – 0.3	—	V	I_{OH} = –0.5 mA
			Ports other than above		VCC – 0.3	—		
		High-drive output mode			VCC – 0.3	—		I_{OH} = –1.0 mA

Table 5.19 Output Values of Voltage (2)

Conditions: 2.7 V ≤ VCC = VCC_USB = AVCC0 < 4.0 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item				Symbol	Min.	Max.	Unit	Test Conditions
Output low	All output ports (except for RIIC)	Normal output mode		V_{OL}	—	0.5	V	I_{OL} = 1.0 mA
		High-drive output mode			—	0.5		I_{OL} = 2.0 mA
	RIIC pins	Standard mode (Normal output mode)			—	0.4		I_{OL} = 3.0 mA
		Fast mode (High-drive output mode)			—	0.6		I_{OL} = 6.0 mA
Output high	All output ports	Normal output mode	Ports 03, 05, 07, Ports 40 to 47	V_{OH}	AVCC0 – 0.5	—	V	I_{OH} = –1.0 mA
			Ports other than above		VCC – 0.5			
		High-drive output mode			VCC – 0.5	—		I_{OH} = –2.0 mA

Table 5.20 Output Values of Voltage (3)

Conditions: 4.0 V ≤ VCC = VCC_USB = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item				Symbol	Min.	Max.	Unit	Test Conditions
Output low	All output ports (except for RIIC)	Normal output mode		V_{OL}	—	0.8	V	I_{OL} = 2.0 mA
		High-drive output mode			—	0.8		I_{OL} = 4.0 mA
	RIIC pins	Standard mode(Normal output mode)			—	0.4		I_{OL} = 3.0 mA
		Fast mode (High-drive output mode)			—	0.6		I_{OL} = 6.0 mA
Output high	All output ports	Normal output mode	Ports 03, 05, 07, Ports 40 to 47	V_{OH}	AVCC0 – 0.8	—	V	I_{OH} = –2.0 mA
			Ports other than above		VCC – 0.8	—		
		High-drive output mode			VCC – 0.8	—		I_{OH} = –4.0 mA

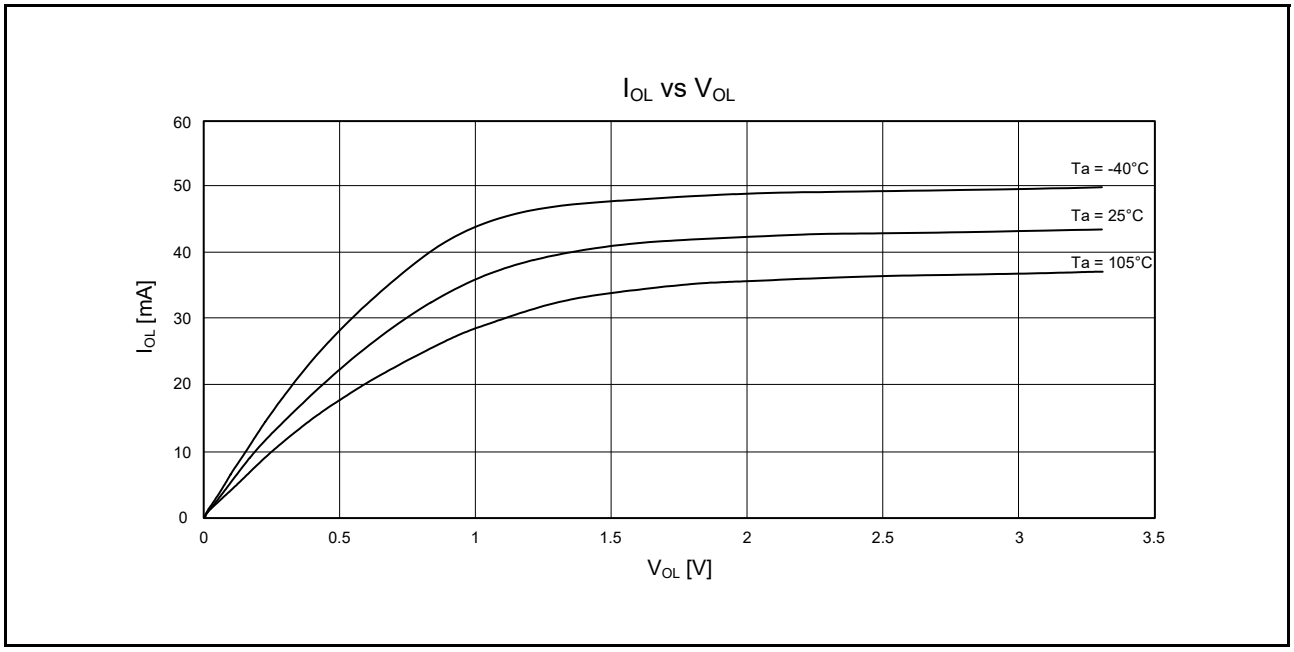


Figure 5.20 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at VCC = 3.3 V (Reference Data)

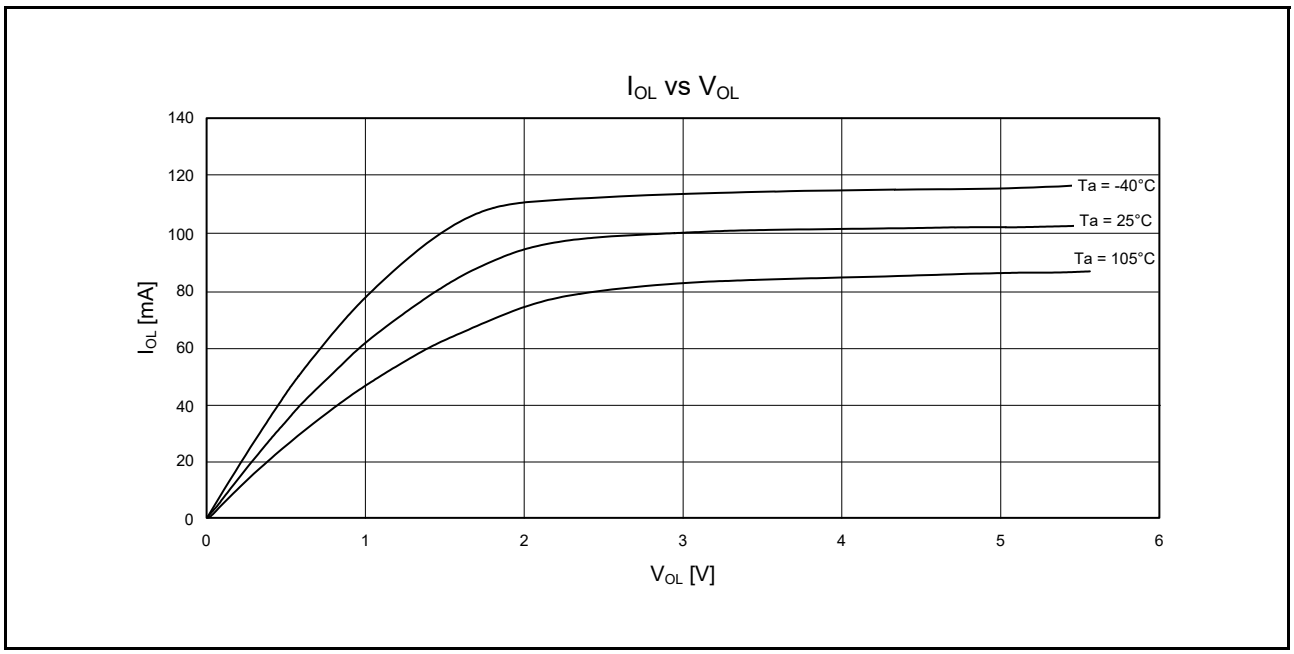


Figure 5.21 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at VCC = 5.5 V (Reference Data)

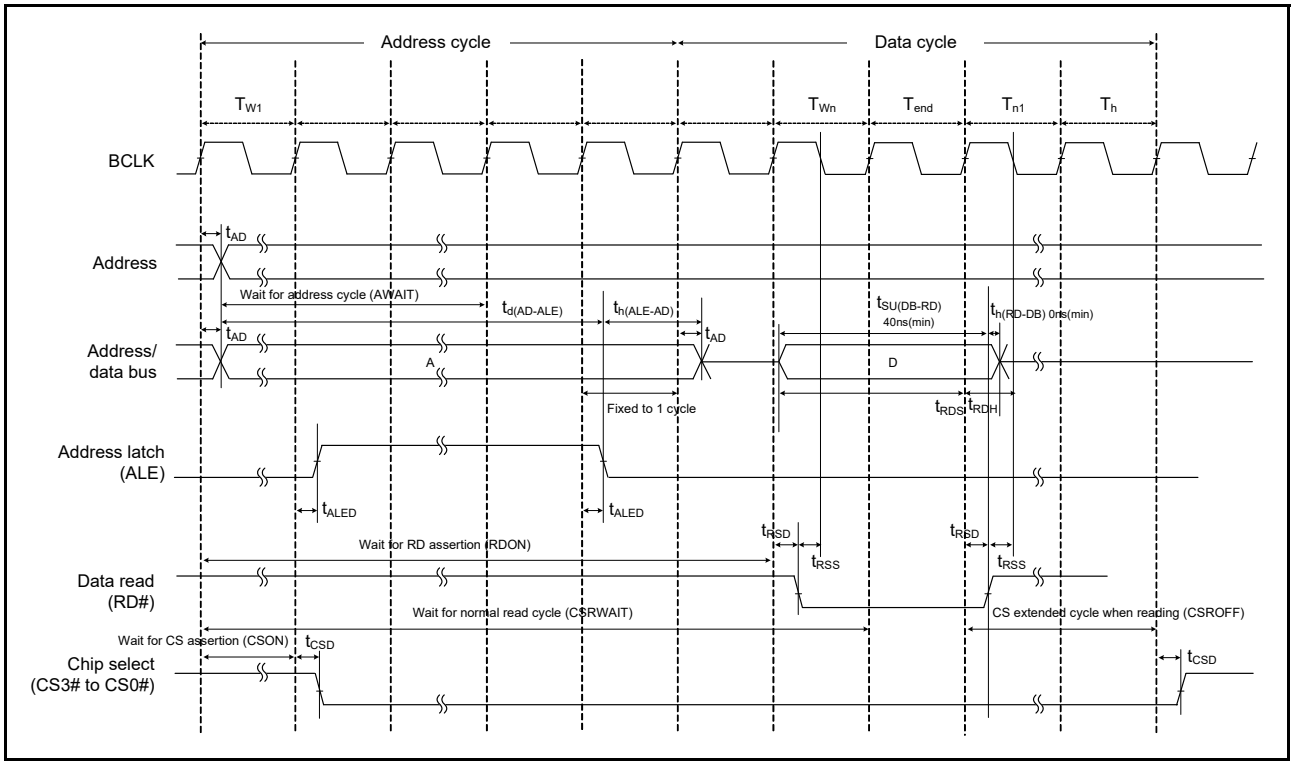


Figure 5.43 External Bus Timing/Read Access Operation Example (Multiplex)

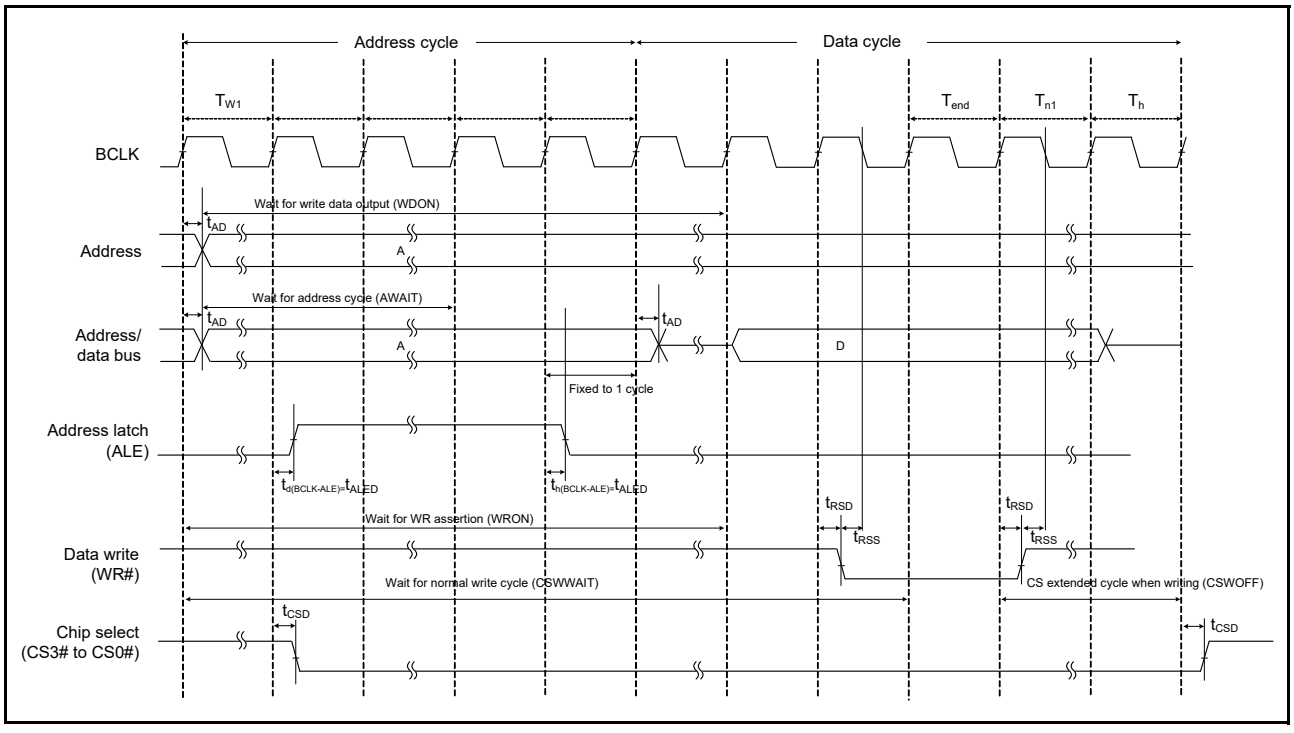


Figure 5.44 External Bus Timing/Write Access Operation Example (Multiplex)

Table 5.44 Timing of On-Chip Peripheral Modules (7)

Conditions: 2.7 V ≤ VCC = VCC_USB = AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, fPCLKB ≤ 32 MHz,
T_a = –40 to +105°C,
when high-drive output is selected by the drive capacity control register

Item		Symbol	Min.	Max.	Unit	Test Conditions
SDHI	SDHI_CLK pin output cycle time	$t_{PP(SD)}$	62.5	—	ns	Figure 5.64
	SDHI_CLK pin output high pulse width	$t_{WH(SD)}$	18.25	—	ns	
	SDHI_CLK pin output low pulse width	$t_{WL(SD)}$	18.25	—	ns	
	SDHI_CLK pin output rise time	$t_{TLH(SD)}$	—	10	ns	
	SDHI_CLK pin output fall time	$t_{THL(SD)}$	—	10	ns	
	Output data delay time (data transfer mode) for SDHI_CMD and SDHI_D0 to SDHI_D3 pins	$t_{ODLY(SD)}$	–18.25	18.25	ns	
	Input data setup time for SDHI_CMD and SDHI_D0 to SDHI_D3 pins	$t_{ISU(SD)}$	9.25	—	ns	
	Input data hold time for SDHI_CMD and SDHI_D0 to SDHI_D3 pins	$t_{IH(SD)}$	8.3	—	ns	

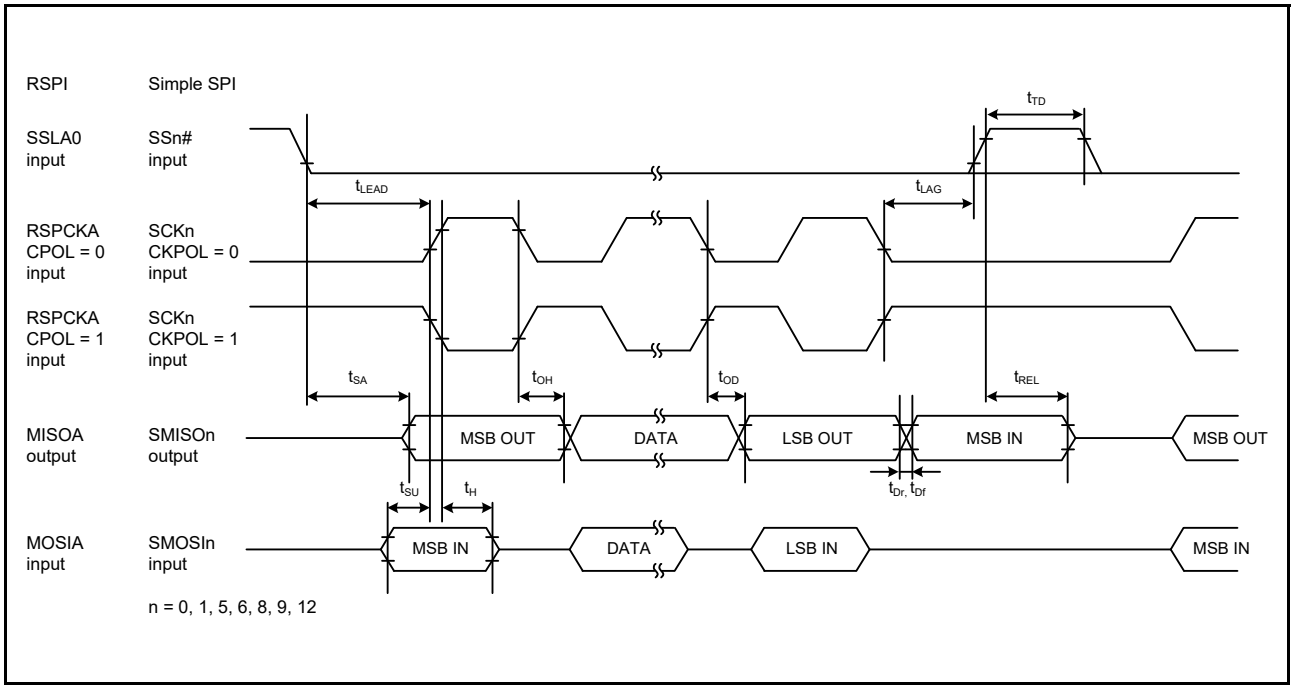


Figure 5.57 RSPI Timing (Slave, CPHA = 0) and Simple SPI Clock Timing (Slave, CKPH = 1)

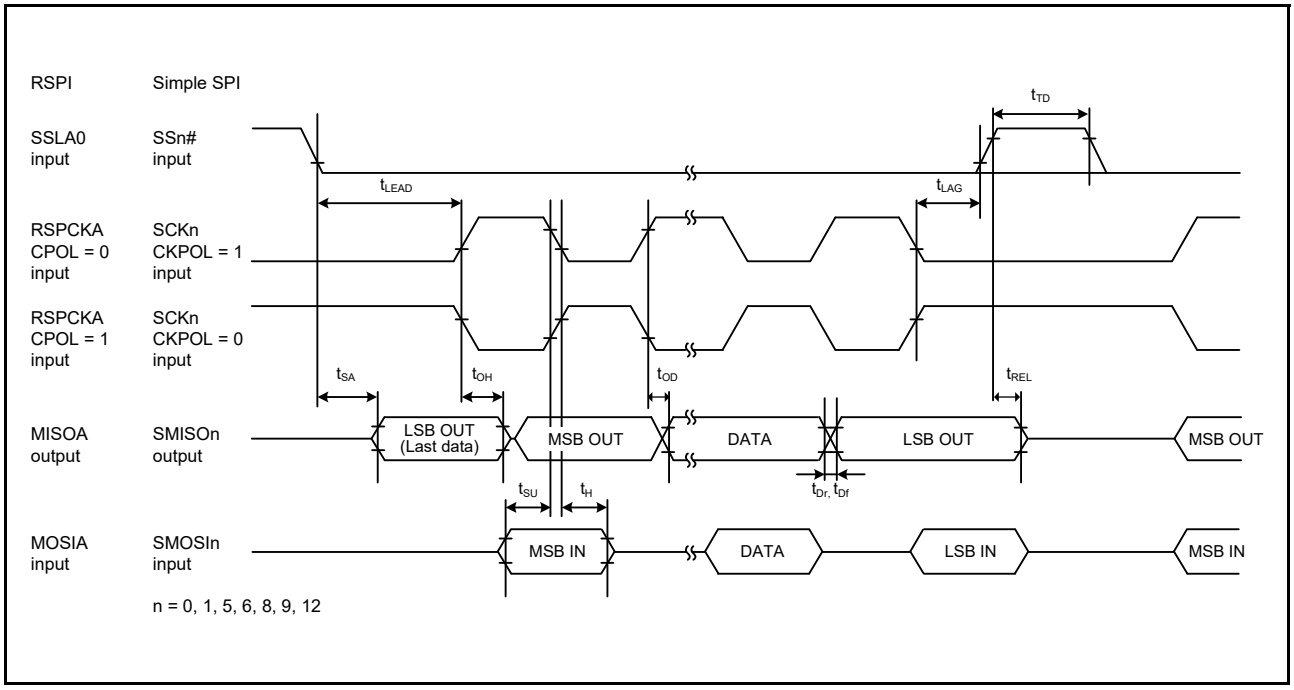


Figure 5.58 RSPI Timing (Slave, CPHA = 1) and Simple SPI Clock Timing (Slave, CKPH = 0)

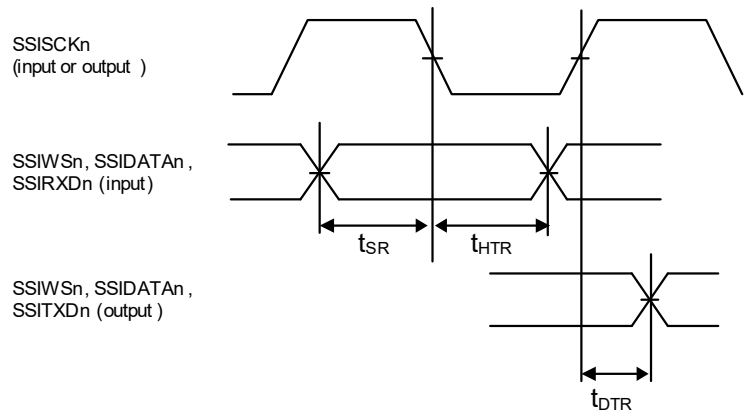
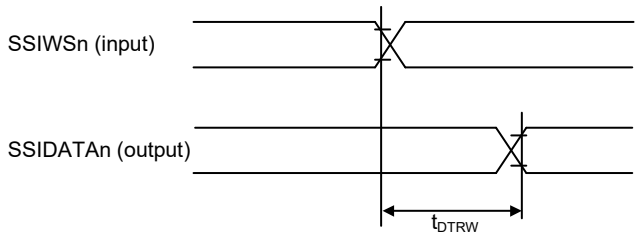


Figure 5.62 SSI Transmission/Reception Timing (SSICR.SCKP=1)



Note. Timing to output the MSB bit during slave transmission from SSIWSn
when DEL = 1 and SDTA = 0 or DEL = 1, SDTA = 1, and SWL[2:0] = DWL[2:0]

Figure 5.63 SSIDATA Output Delay After SSIWSn Changing Edge

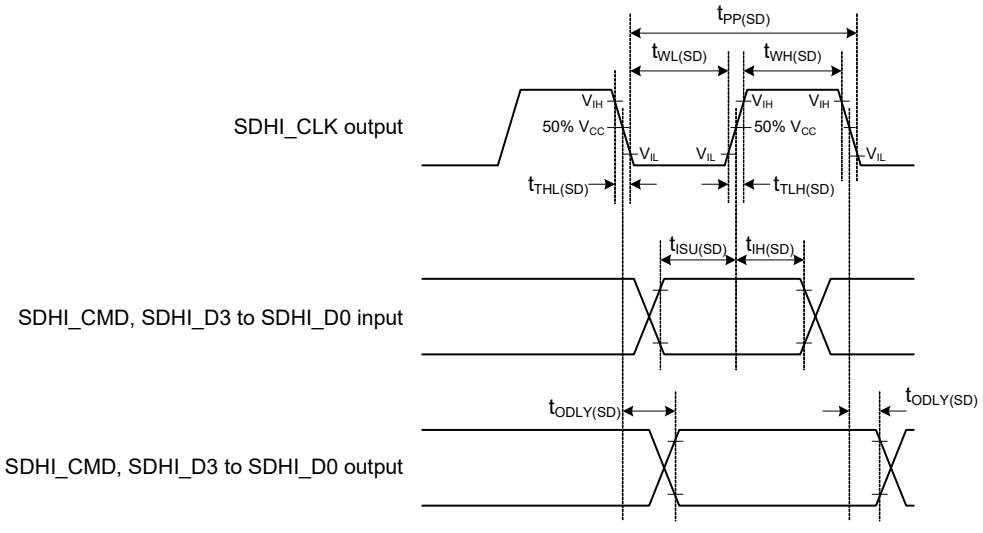
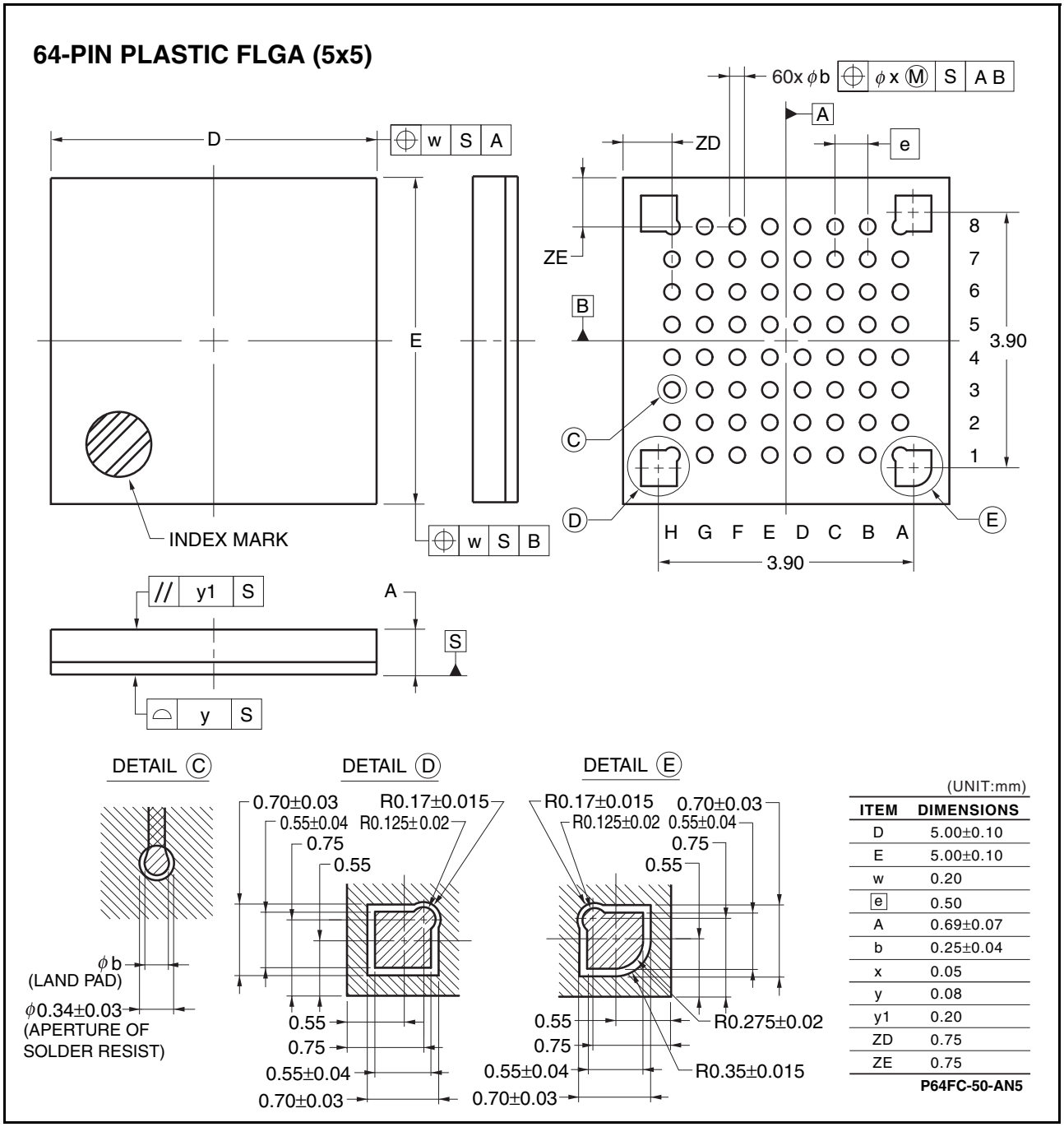


Figure 5.64 SD Host Interface Input/Output Signal Timing



(UNIT:mm)

ITEM	DIMENSIONS
D	5.00±0.10
E	5.00±0.10
w	0.20
e	0.50
A	0.69±0.07
b	0.25±0.04
x	0.05
y	0.08
y1	0.20
ZD	0.75
ZE	0.75

P64FC-50-AN5

Figure C 64 -Pin WFLGA (PWLG0064KA-A)

REVISION HISTORY	RX230 Group, RX231 Group Datasheet

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
1.00	Jun 24, 2015	—	First edition, issued	
1.10	Oct 30, 2015	1. Overview		
		3	Table 1.1 Outline of Specifications (2/4), changed	
		5	Table 1.1 Outline of Specifications (4/4): SD Host Interface (SDHIa) added	
		6	Table 1.2 Comparison of Functions for Different Packages: RX230 Group added	
		3. Address Space		
		39	Figure 3.1 Memory Map in Each Operating Mode, changed	
		4. I/O Registers		
		67	Table 4.1 List of I/O Registers (Address Order) (25 / 42), changed	TN-RX*-A139A/E
		83	Table 4.1 List of I/O Registers (Address Order) (41 / 42), changed	
		5. Electrical Characteristics		
		85	Table 5.1 Absolute Maximum Ratings, changed	TN-RX*-A137A/E
		86	Table 5.2 Recommended Operating Voltage Conditions, changed	
		87	Table 5.3 DC Characteristics (1), changed	TN-RX*-A137A/E
		88	Table 5.4 DC Characteristics (2), changed	
		88	Table 5.5 DC Characteristics (3), changed	
		89	Table 5.7 DC Characteristics (5), changed	
		91	Figure 5.1 Voltage Dependency in High-Speed Operating Mode (Reference Data), changed	
		92	Figure 5.2 Voltage Dependency in Middle-Speed Operating Mode (Reference Data), changed	
		93	Figure 5.3 Voltage Dependency in Low-Speed Operating Mode (Reference Data), changed	TN-RX*-A137A/E
		94	Table 5.8 DC Characteristics (6), changed Figure 5.4 Voltage Dependency in Software Standby Mode (Reference Data), changed	
		95	Figure 5.5 Temperature Dependency in Software Standby Mode (Reference Data), changed	
		96	Figure 5.6 Temperature Dependency of RTC Operation with VCC Off (Reference Data), changed Table 5.10 DC Characteristics (8): Conditions changed	
		97	Table 5.11 DC Characteristics (9), changed	TN-RX*-A137A/E
		99	Table 5.16 Permissible Output Currents (1), changed	TN-RX*-A137A/E
		100	Table 5.17 Permissible Output Currents (2), changed	
		101	Table 5.18 Output Values of Voltage (1), changed	
		101	Table 5.19 Output Values of Voltage (2), changed	TN-RX*-A137A/E
		101	Table 5.20 Output Values of Voltage (3), changed	TN-RX*-A137A/E
		105	Figure 5.13 VOH/VOL and IOH/IOL Voltage Characteristics at Ta = 25°C When High-Drive Output is Selected (Reference Data), changed	TN-RX*-A137A/E
		108	Figure 5.18 V_{OL} and I_{OL} Voltage Characteristics of RIIC Output Pin at Ta = 25°C (Reference Data)	TN-RX*-A137A/E
		110	Table 5.21 Operating Frequency Value (High-Speed Operating Mode) and Table 5.22 Operating Frequency Value (Middle-Speed Operating Mode), changed	TN-RX*-A137A/E
		112	Table 5.26 Clock Timing, changed	TN-RX*-A137A/E
		116	Table 5.27 Reset Timing, changed	
		131	Table 5.41 Timing of On-Chip Peripheral Modules (4): Note changed	
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		138	Figure 5.61 SSI Transmission/Reception Timing (SSICP.SCKP=0), changed	TN-RX*-A137A/E
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		142	Figure 5.66 VREFH0 Voltage Range vs. AVCC0, changed	