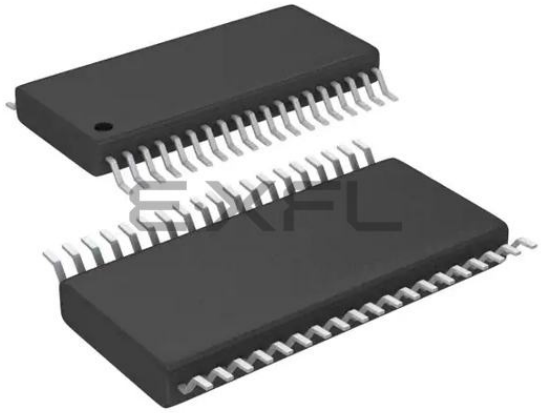
# Infineon Technologies - XMC1201Q040F0064ABXUMA1 Datasheet



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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0 |
| Core Size | 32-Bit Single-Core |
| Speed | 32MHz |
| Connectivity | I²C, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, I²S, POR, PWM, WDT |
| Number of I/O | 27 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V |
| Data Converters | A/D 16x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 38-TFSOP (0.173", 4.40mm Width) |
| Supplier Device Package | PG-TSSOP-38-9 |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/xmc1201q040f0064abxuma1 |

## 2.2 Pin Configuration and Definition

The following figures summarize all pins, showing their locations on the different packages.

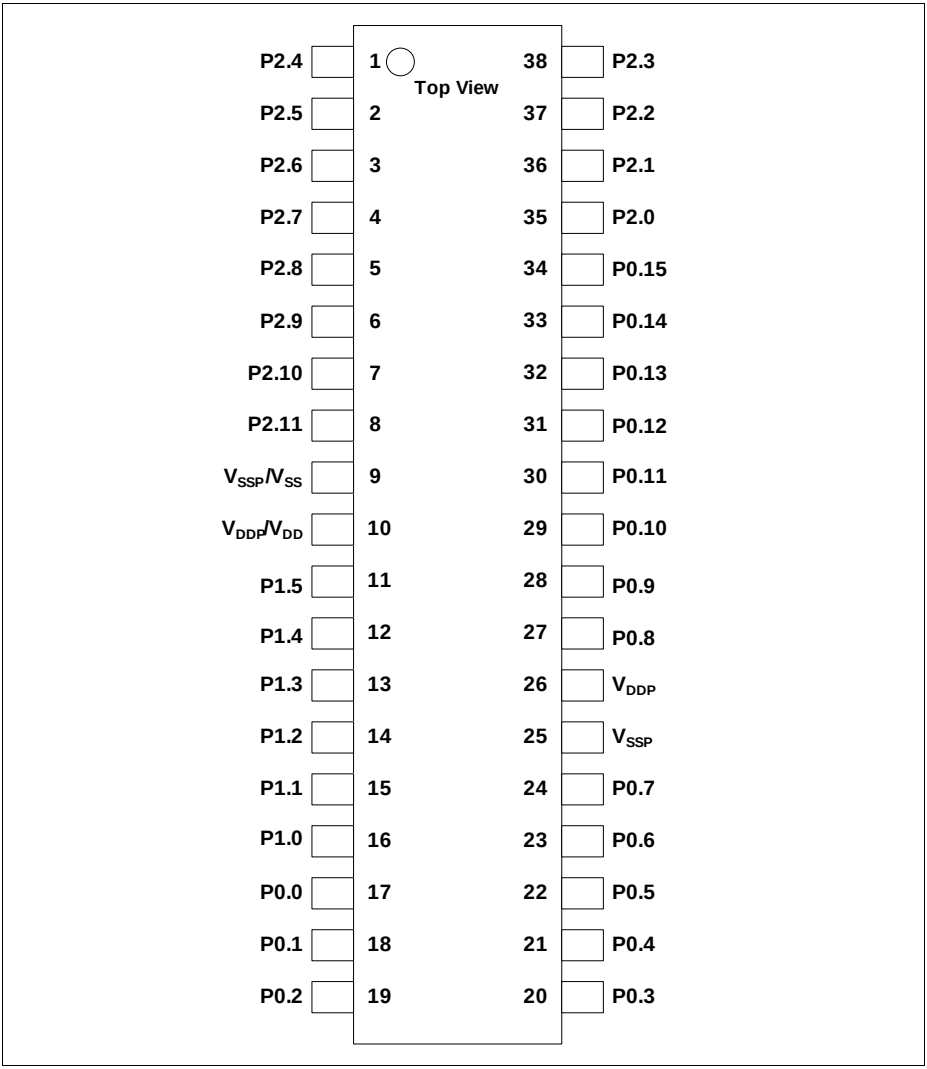



**Figure 4 XMC1200 PG-TSSOP-38 Pin Configuration** (top view)

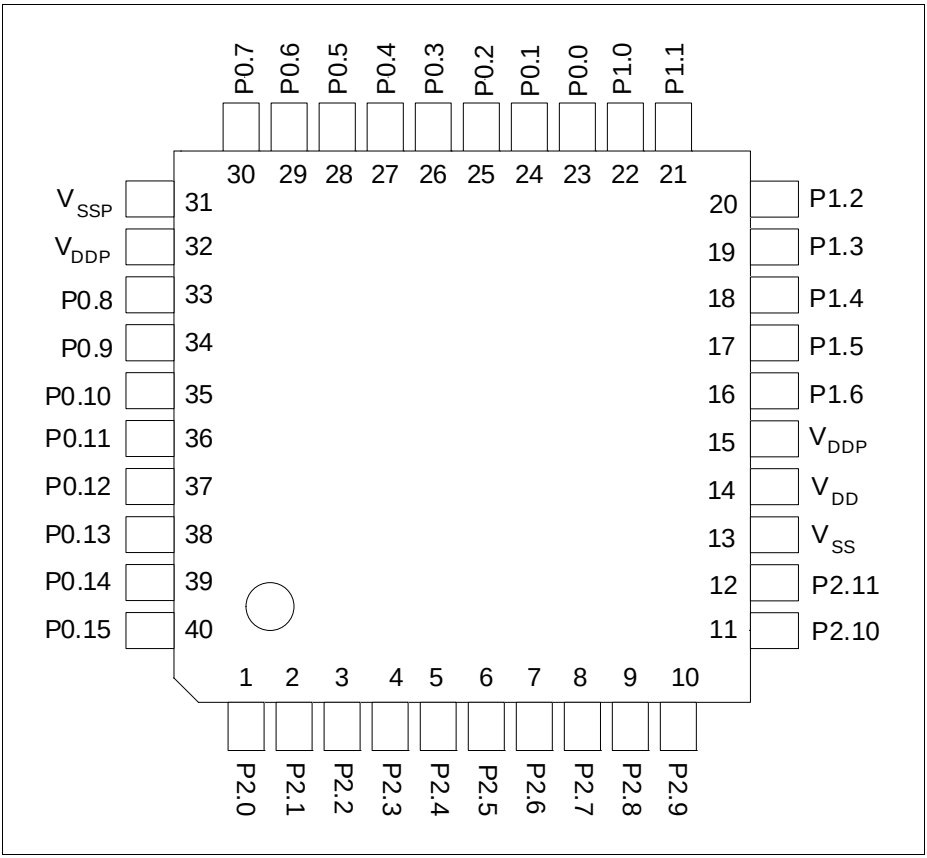



**Figure 8 XMC1200 PG-VQFN-40 Pin Configuration** (top view)

### 2.2.1 Package Pin Summary

The following general building block is used to describe each pin:

**Table 5 Package Pin Mapping Description**

| Function | Package A | Package B | ... | Pad Type |
|---|---|---|---|---|
| Px.y | N | N | | Pad Class |

The table is sorted by the “Function” column, starting with the regular Port pins (Px.y), followed by the supply pins.

The following columns, titled with the supported package variants, lists the package pin number to which the respective function is mapped in that package.

The “Pad Type” indicates the employed pad type:

- STD_INOUT (standard bi-directional pads)
- STD_INOUT/AN (standard bi-directional pads with analog input)
- High Current (high current bi-directional pads)
- STD_IN/AN (standard input pads with analog input)
- Power (power supply)

Details about the pad properties are defined in the Electrical Parameters.

**Table 6 Package Pin Mapping**

| Function | VQFN 40 | TSSOP 38 | TSSOP 28 | VQFN 24 | TSSOP 16 | Pad Type | Notes |
|---|---|---|---|---|---|---|---|
| P0.0 | 23 | 17 | 13 | 15 | 7 | STD_INOUT | |
| P0.1 | 24 | 18 | - | - | - | STD_INOUT | |
| P0.2 | 25 | 19 | - | - | - | STD_INOUT | |
| P0.3 | 26 | 20 | - | - | - | STD_INOUT | |
| P0.4 | 27 | 21 | 14 | - | - | STD_INOUT | |
| P0.5 | 28 | 22 | 15 | 16 | 8 | STD_INOUT | |
| P0.6 | 29 | 23 | 16 | 17 | 9 | STD_INOUT | |

**Table 6 Package Pin Mapping** (cont'd)

| Function | VQFN 40 | TSSOP 38 | TSSOP 28 | VQFN 24 | TSSOP 16 | Pad Type | Notes |
|---|---|---|---|---|---|---|---|
| VSSP | 31 | 25 | - | - | - | Power | I/O port ground |
| VDDP | 32 | 26 | - | - | - | Power | I/O port supply |
| VSSP | Exp. Pad | - | - | Exp. Pad | - | Power | **Exposed Die Pad** The exposed die pad is connected internally to VSSP. For proper operation, it is mandatory to connect the exposed pad to the board ground. For thermal aspects, please refer to the Package and Reliability chapter. |

## Table 10 Hardware Controlled I/O Functions

| Function | Outputs | | Inputs | | Pull Control | | | |
|---|---|---|---|---|---|---|---|---|
| | HWO0 | HWO1 | HWI0 | HWI1 | HW0_PD | HW0_PU | HW1_PD | HW1_PU |
| P1.3 | | USIC0_CH0.DOUT3 | | USIC0_CH0.HWIN3 | BCCU0.OUT5 | BCCU0.OUT5 | | |
| P1.4 | | | | | BCCU0.OUT6 | BCCU0.OUT6 | | |
| P1.5 | | | | | BCCU0.OUT7 | BCCU0.OUT7 | | |
| P1.6 | | | | | BCCU0.OUT8 | BCCU0.OUT8 | | |
| P2.0 | | | | | BCCU0.OUT1 | BCCU0.OUT1 | | |
| P2.1 | | | | | BCCU0.OUT6 | BCCU0.OUT6 | | |
| P2.2 | | | | | BCCU0.OUT0 | BCCU0.OUT0 | CCU40.OUT3 | CCU40.OUT3 |
| P2.3 | | | | | ACMP2.OUT | ACMP2.OUT | | |
| P2.4 | | | | | BCCU0.OUT8 | BCCU0.OUT8 | | |
| P2.5 | | | | | ACMP1.OUT | ACMP1.OUT | | |
| P2.6 | | | | | BCCU0.OUT2 | BCCU0.OUT2 | CCU40.OUT3 | CCU40.OUT3 |
| P2.7 | | | | | BCCU0.OUT8 | BCCU0.OUT8 | CCU40.OUT3 | CCU40.OUT3 |
| P2.8 | | | | | BCCU0.OUT1 | BCCU0.OUT1 | CCU40.OUT2 | CCU40.OUT2 |
| P2.9 | | | | | BCCU0.OUT7 | BCCU0.OUT7 | CCU40.OUT2 | CCU40.OUT2 |
| P2.10 | | | | | BCCU0.OUT4 | BCCU0.OUT4 | | |
| P2.11 | | | | | BCCU0.OUT5 | BCCU0.OUT5 | | |

### 3.1.2 Absolute Maximum Ratings

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Table 11 Absolute Maximum Rating Parameters**

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Junction temperature | $T_J$ | SR | -40 | – | 115 | °C | – |
| Storage temperature | $T_{ST}$ | SR | -40 | – | 125 | °C | – |
| Voltage on power supply pin with respect to $V_{SSP}$ | $V_{DDP}$ | SR | -0.3 | – | 6 | V | – |
| Voltage on any pin with respect to $V_{SSP}$ | $V_{IN}$ | SR | -0.5 | – | $V_{DDP}$ + 0.5 or max. 6 | V | whichever is lower |
| Voltage on any analog input pin with respect to $V_{SSP}$ | $V_{AIN}$ $V_{AREF}$ | SR | -0.5 | – | $V_{DDP}$ + 0.5 or max. 6 | V | – |
| Input current on any pin during overload condition | $I_{IN}$ | SR | -10 | – | 10 | mA | – |
| Absolute maximum sum of all input currents during overload condition | $\Sigma I_{IN}$ | SR | -50 | – | +50 | mA | – |
| Analog comparator input voltage | $V_{CM}$ | SR | -0.3 | – | $V_{DDP}$ + 0.3 | V | |

### 3.1.3 Pin Reliability in Overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.

**Table 12** defines overload conditions that will not cause any negative reliability impact if all the following conditions are met:

- full operation life-time is not exceeded
- **Operating Conditions** are met for
  - pad supply levels ($V_{DDP}$)
  - temperature

## 3.2 DC Parameters

### 3.2.1 Input/Output Characteristics

**Table 16** provides the characteristics of the input/output pins of the XMC1200.

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

*Note: Unless otherwise stated, input DC and AC characteristics, including peripheral timings, assume that the input pads operate with the standard hysteresis.*

**Table 16 Input/Output Characteristics (Operating Conditions apply)**

| Parameter | Symbol | | Limit Values | | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| | | | Min. | Max. | | |
| Output low voltage on port pins (with standard pads) | $V_{OLP}$ | CC | – | 1.0 | V | $I_{OL}$ = 11 mA (5 V)<br>$I_{OL}$ = 7 mA (3.3 V) |
| | | | – | 0.4 | V | $I_{OL}$ = 5 mA (5 V)<br>$I_{OL}$ = 3.5 mA (3.3 V) |
| Output low voltage on high current pads | $V_{OLP1}$ | CC | – | 1.0 | V | $I_{OL}$ = 50 mA (5 V)<br>$I_{OL}$ = 25 mA (3.3 V) |
| | | | – | 0.32 | V | $I_{OL}$ = 10 mA (5 V) |
| | | | – | 0.4 | V | $I_{OL}$ = 5 mA (3.3 V) |
| Output high voltage on port pins (with standard pads) | $V_{OHP}$ | CC | $V_{DDP}$ - 1.0 | – | V | $I_{OH}$ = -10 mA (5 V)<br>$I_{OH}$ = -7 mA (3.3 V) |
| | | | $V_{DDP}$ - 0.4 | – | V | $I_{OH}$ = -4.5 mA (5 V)<br>$I_{OH}$ = -2.5 mA (3.3 V) |
| Output high voltage on high current pads | $V_{OHP1}$ | CC | $V_{DDP}$ - 0.32 | – | V | $I_{OH}$ = -6 mA (5 V) |
| | | | $V_{DDP}$ - 1.0 | – | V | $I_{OH}$ = -8 mA (3.3 V) |
| | | | $V_{DDP}$ - 0.4 | – | V | $I_{OH}$ = -4 mA (3.3 V) |
| Input low voltage on port pins (Standard Hysteresis) | $V_{ILPS}$ | SR | – | 0.19 × $V_{DDP}$ | V | CMOS Mode (5 V, 3.3 V & 2.2 V) |
| Input high voltage on port pins (Standard Hysteresis) | $V_{IHPS}$ | SR | 0.7 × $V_{DDP}$ | – | V | CMOS Mode (5 V, 3.3 V & 2.2 V) |

**Table 16 Input/Output Characteristics (Operating Conditions apply)** (cont'd)

| Parameter | Symbol | | Limit Values | | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| | | | Min. | Max. | | |
| Pin capacitance (digital inputs/outputs) | $C_{IO}$ | CC | – | 10 | pF | |
| Pull-up resistor on port pins | $R_{PUP}$ | CC | 20 | 50 | kohm | $V_{IN} = V_{SSP}$ |
| Pull-down resistor on port pins | $R_{PDP}$ | CC | 20 | 50 | kohm | $V_{IN} = V_{DDP}$ |
| Input leakage current[9)] | $I_{OZP}$ | CC | -1 | 1 | µA | $0 < V_{IN} < V_{DDP}$, $T_A \leq 105$ °C |
| Voltage on any pin during $V_{DDP}$ power off | $V_{PO}$ | SR | – | 0.3 | V | [10)] |
| Maximum current per pin (excluding P1, $V_{DDP}$ and $V_{SS}$) | $I_{MP}$ | SR | -10 | 11 | mA | – |
| Maximum current per high currrent pins | $I_{MP1A}$ | SR | -10 | 50 | mA | – |
| Maximum current into $V_{DDP}$ (TSSOP28/16, VQFN24) | $I_{MVDD1}$ | SR | – | 130 | mA | [10)] |
| Maximum current into $V_{DDP}$ (TSSOP38, VQFN40) | $I_{MVDD2}$ | SR | – | 260 | mA | [10)] |
| Maximum current out of $V_{SS}$ (TSSOP28/16, VQFN24) | $I_{MVSS1}$ | SR | – | 130 | mA | [10)] |
| Maximum current out of $V_{SS}$ (TSSOP38, VQFN40) | $I_{MVSS2}$ | SR | – | 260 | mA | [10)] |

1) Rise/Fall time parameters are taken with 10% - 90% of supply.
2) Additional rise/fall time valid for $C_L$ = 50 pF - $C_L$ = 100 pF @ 0.150 ns/pF at 5 V supply voltage.
3) Additional rise/fall time valid for $C_L$ = 50 pF - $C_L$ = 100 pF @ 0.205 ns/pF at 3.3 V supply voltage.
4) Additional rise/fall time valid for $C_L$ = 50 pF - $C_L$ = 100 pF @ 0.445 ns/pF at 1.8 V supply voltage.
5) Additional rise/fall time valid for $C_L$ = 50 pF - $C_L$ = 100 pF @ 0.225 ns/pF at 5 V supply voltage.
6) Additional rise/fall time valid for $C_L$ = 50 pF - $C_L$ = 100 pF @ 0.288 ns/pF at 3.3 V supply voltage.
7) Additional rise/fall time valid for $C_L$ = 50 pF - $C_L$ = 100 pF @ 0.588 ns/pF at 1.8 V supply voltage.

### 3.2.2 Analog to Digital Converters (ADC)

**Table 17** shows the Analog to Digital Converter (ADC) characteristics.

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 17 ADC Characteristics (Operating Conditions apply)[1)]**

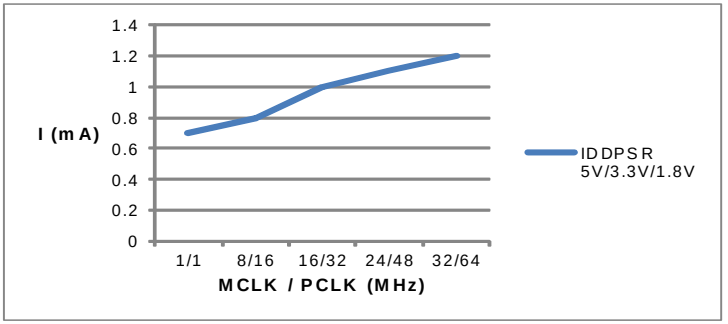
| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Supply voltage range (internal reference) | $V_{DD\_int}$ SR | 2.0 | – | 3.0 | V | SHSCFG.AREF = $11_B$ CALCTR.CALGNSTC = $0C_H$ |
| | | 3.0 | – | 5.5 | V | SHSCFG.AREF = $10_B$ |
| Supply voltage range (external reference) | $V_{DD\_ext}$ SR | 3.0 | – | 5.5 | V | SHSCFG.AREF = $00_B$ |
| Analog input voltage range | $V_{AIN}$ SR | $V_{SSP}$ - 0.05 | – | $V_{DDP}$ + 0.05 | V | |
| Auxiliary analog reference ground | $V_{REFGND}$ SR | $V_{SSP}$ - 0.05 | – | 1.0 | V | G0CH0 |
| | | $V_{SSP}$ - 0.05 | – | 0.2 | V | G1CH0 |
| Internal reference voltage (full scale value) | $V_{REFINT}$ CC | 5 | | | V | |
| Switched capacitance of an analog input | $C_{AINS}$ CC | – | 1.2 | 2 | pF | GNCTRxz.GAINy = $00_B$ (unity gain) |
| | | – | 1.2 | 2 | pF | GNCTRxz.GAINy = $01_B$ (gain g1) |
| | | – | 4.5 | 6 | pF | GNCTRxz.GAINy = $10_B$ (gain g2) |
| | | – | 4.5 | 6 | pF | GNCTRxz.GAINy = $11_B$ (gain g3) |
| Total capacitance of an analog input | $C_{AINT}$ CC | – | – | 10 | pF | |
| Total capacitance of the reference input | $C_{AREFT}$ CC | – | – | 10 | pF | |

**Table 21 Power Supply Parameters; $V_{DDP}$ = 5V**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ.[1] | Max. | | |
| Sleep mode current Peripherals clock disabled Flash active $f_{MCLK}$ / $f_{PCLK}$ in MHz[5] | $I_{DDPSD}$ CC | – | 1.8 | – | mA | 32 / 64 |
| | | | 1.7 | – | mA | 24 / 48 |
| | | | 1.6 | – | mA | 16 / 32 |
| | | | 1.5 | – | mA | 8 / 16 |
| | | | 1.4 | – | mA | 1 / 1 |
| Sleep mode current Peripherals clock disabled Flash powered down $f_{MCLK}$ / $f_{PCLK}$ in MHz[6] | $I_{DDPSR}$ CC | – | 1.2 | – | mA | 32 / 64 |
| | | | 1.1 | – | mA | 24 / 48 |
| | | | 1.0 | – | mA | 16 / 32 |
| | | | 0.8 | – | mA | 8 / 16 |
| | | | 0.7 | – | mA | 1 / 1 |
| Deep Sleep mode current[7] | $I_{DDPDS}$ CC | – | 0.24 | – | mA | |
| Wake-up time from Sleep to Active mode[8] | $t_{SSA}$ CC | – | 6 | – | cycles | |
| Wake-up time from Deep Sleep to Active mode[9] | $t_{DSA}$ CC | – | 280 | – | µsec | |

1) The typical values are measured at $T_A$ = + 25 °C and $V_{DDP}$ = 5 V.
2) CPU and all peripherals clock enabled, Flash is in active mode.
3) CPU enabled, all peripherals clock disabled, Flash is in active mode.
4) CPU in sleep, all peripherals clock enabled and Flash is in active mode.
5) CPU in sleep, Flash is in active mode.
6) CPU in sleep, Flash is powered down and code executed from RAM after wake-up.
7) CPU in sleep, peripherals clock disabled, Flash is powered down and code executed from RAM after wake-up.
8) CPU in sleep, Flash is in active mode during sleep mode.
9) CPU in sleep, Flash is in powered down mode during deep sleep mode.

**Figure 15** shows typical graphs for sleep mode current for $V_{DDP}$ = 5V, $V_{DDP}$ = 3.3V, $V_{DDP}$ = 1.8V across different clock frequencies.




Condition:
1. TA = +25° C

**Figure 15 Sleep mode, peripherals clocks disabled, Flash powered down: Supply current $I_{DDPSR}$ over supply voltage $V_{DDP}$ for different clock frequencies**

**Table 24 Power-Up and Supply Monitoring Parameters (Operating Conditions apply)[1)]** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| $V_{DDP}$ brownout reset voltage | $V_{DDPBO}$ CC | 1.55 | 1.62 | 1.75 | V | calibrated, before user code starts running |
| $V_{DDP}$ voltage to ensure defined pad states | $V_{DDPPA}$ CC | – | 1.0 | – | V | |
| Start-up time from power-on reset | $t_{SSW}$ SR | – | 320 | – | µs | Time to the first user code instruction in all start-up modes[4)] |
| BMI program time | $t_{BMI}$ SR | – | 8.25 | – | ms | Time taken from a user-triggered system reset after BMI installation is is requested |

1) Not all parameters are 100% tested, but are verified by design/characterisation.

2) A capacitor of at least 100 nF has to be added between $V_{DDP}$ and $V_{SSP}$ to fulfill the requirement as stated for this parameter.

3) Valid for a 100 nF buffer capacitor connected to supply pin where current from capacitor is forwarded only to the chip. A larger capacitor value has to be chosen if the power source sink a current.

4) This values does not include the ramp-up time. During startup firmware execution, MCLK is running at 32 MHz and the clocks to peripheral as specified in register CGATSTAT0 are gated.

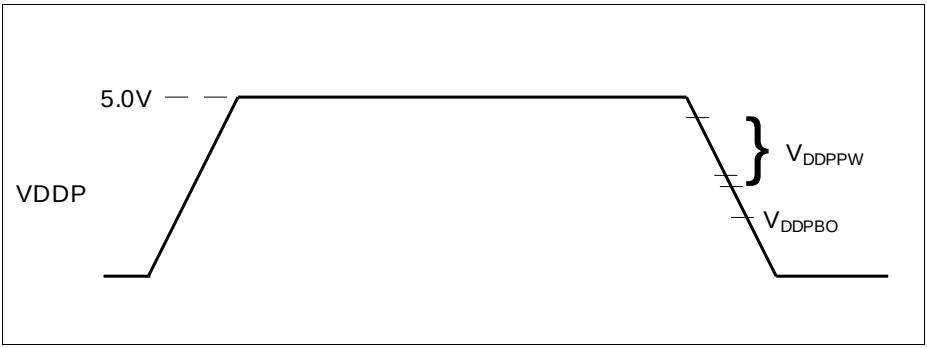



**Figure 19 Supply Threshold Parameters**

### 3.3.3 On-Chip Oscillator Characteristics

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 25** provides the characteristics of the 64 MHz clock output from the digital controlled oscillator, DCO1 in XMC1200.

**Table 25 64 MHz DCO1 Characteristics (Operating Conditions apply)**

| Parameter | Symbol | | Limit Values | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Nominal frequency | $f_{NOM}$ | CC | – | 64 | – | MHz | under nominal conditions[1] after trimming |
| Accuracy[2] | $\Delta f_{LT}$ | CC | -1.7 | – | 3.4 | % | with respect to $f_{NOM}$(typ), over temperature (0 °C to 85 °C) |
| | | | -3.9 | – | 4.0 | % | with respect to $f_{NOM}$(typ), over temperature (-40 °C to 105 °C) |

1) The deviation is relative to the factory trimmed frequency at nominal $V_{DDC}$ and $T_A$ = + 25 °C.

2) The accuracy of the DCO1 oscillator can be further improved through alternative methods, refer to XMC1000 Oscillator Handling Application Note.

**Figure 20** shows the typical curves for the accuracy of DCO1, with and without calibration based on temperature sensor, respectively.

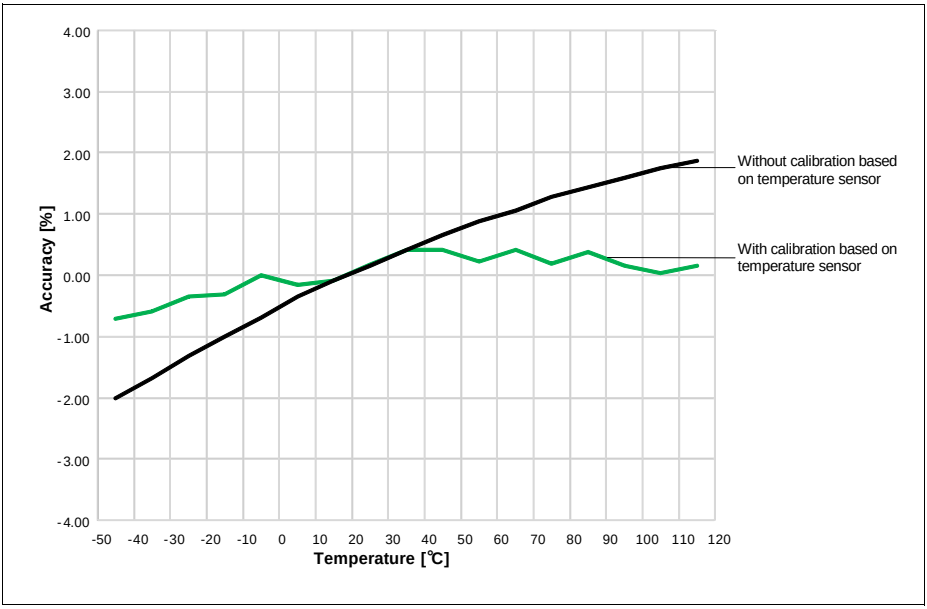



**Figure 20 Typical DCO1 accuracy over temperature**

**Table 26** provides the characteristics of the 32 kHz clock output from digital controlled oscillators, DCO2 in XMC1200.

**Table 26 32 kHz DCO2 Characteristics (Operating Conditions apply)**

| Parameter | Symbol | | Limit Values | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Nominal frequency | $f_{NOM}$ | CC | – | 32.75 | – | kHz | under nominal conditions[1] after trimming |
| Accuracy | $\Delta f_{LT}$ | CC | -1.7 | – | 3.4 | % | with respect to $f_{NOM}$(typ), over temperature (0 °C to 85 °C) |
| | | | -3.9 | – | 4.0 | % | with respect to $f_{NOM}$(typ), over temperature (-40 °C to 105 °C) |

1) The deviation is relative to the factory trimmed frequency at nominal $V_{DDC}$ and $T_A$ = + 25 °C.

### 3.3.4 Serial Wire Debug Port (SW-DP) Timing

The following parameters are applicable for communication through the SW-DP interface.

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 27 SWD Interface Timing Parameters**(Operating Conditions apply)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| SWDCLK high time | $t_1$ SR | 50 | – | 500000 | ns | – |
| SWDCLK low time | $t_2$ SR | 50 | – | 500000 | ns | – |
| SWDIO input setup to SWDCLK rising edge | $t_3$ SR | 10 | – | – | ns | – |
| SWDIO input hold after SWDCLK rising edge | $t_4$ SR | 10 | – | – | ns | – |
| SWDIO output valid time after SWDCLK rising edge | $t_5$ CC | – | – | 68 | ns | $C_L$ = 50 pF |
| | | – | – | 62 | ns | $C_L$ = 30 pF |
| SWDIO output hold time from SWDCLK rising edge | $t_6$ CC | 4 | – | – | ns | |

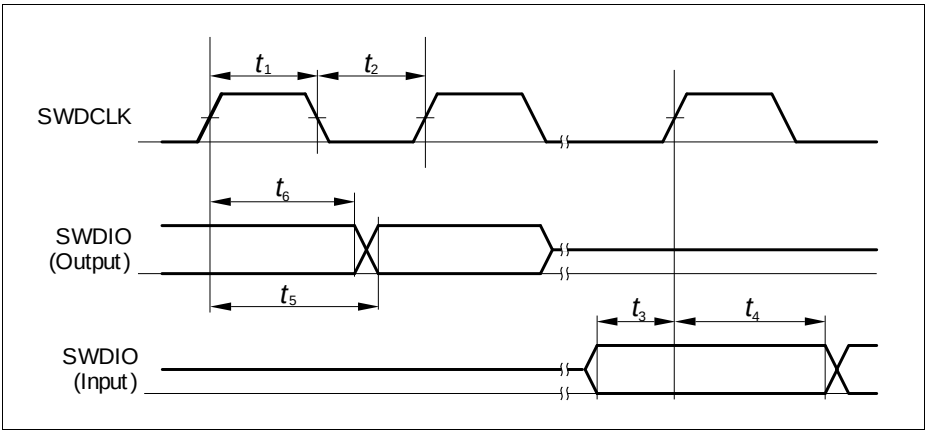



**Figure 21 SWD Timing**

### 3.3.5 SPD Timing Requirements

The optimum SPD decision time between $0_B$ and $1_B$ is 0.75 µs. With this value the system has maximum robustness against frequency deviations of the sampling clock on tool and on device side. However it is not always possible to exactly match this value with the given constraints for the sample clock. For instance for a oversampling rate of 4, the sample clock will be 8 MHz and in this case the closest possible effective decision time is 5.5 clock cycles (0.69 µs).

**Table 28 Optimum Number of Sample Clocks for SPD**

| Sample Freq. | Sampling Factor | Sample Clocks $0_B$ | Sample Clocks $1_B$ | Effective Decision Time[1)] | Remark |
|---|---|---|---|---|---|
| 8 MHz | 4 | 1 to 5 | 6 to 12 | 0.69 µs | The other closest option (0.81 µs) for the effective decision time is less robust. |

1) Nominal sample frequency period multiplied with 0.5 + (max. number of $0_B$ sample clocks)

For a balanced distribution of the timing robustness of SPD between tool and device, the timing requirements for the tool are:

- Frequency deviation of the sample clock is +/- 5%
- Effective decision time is between 0.69 µs and 0.75 µs (calculated with nominal sample frequency)

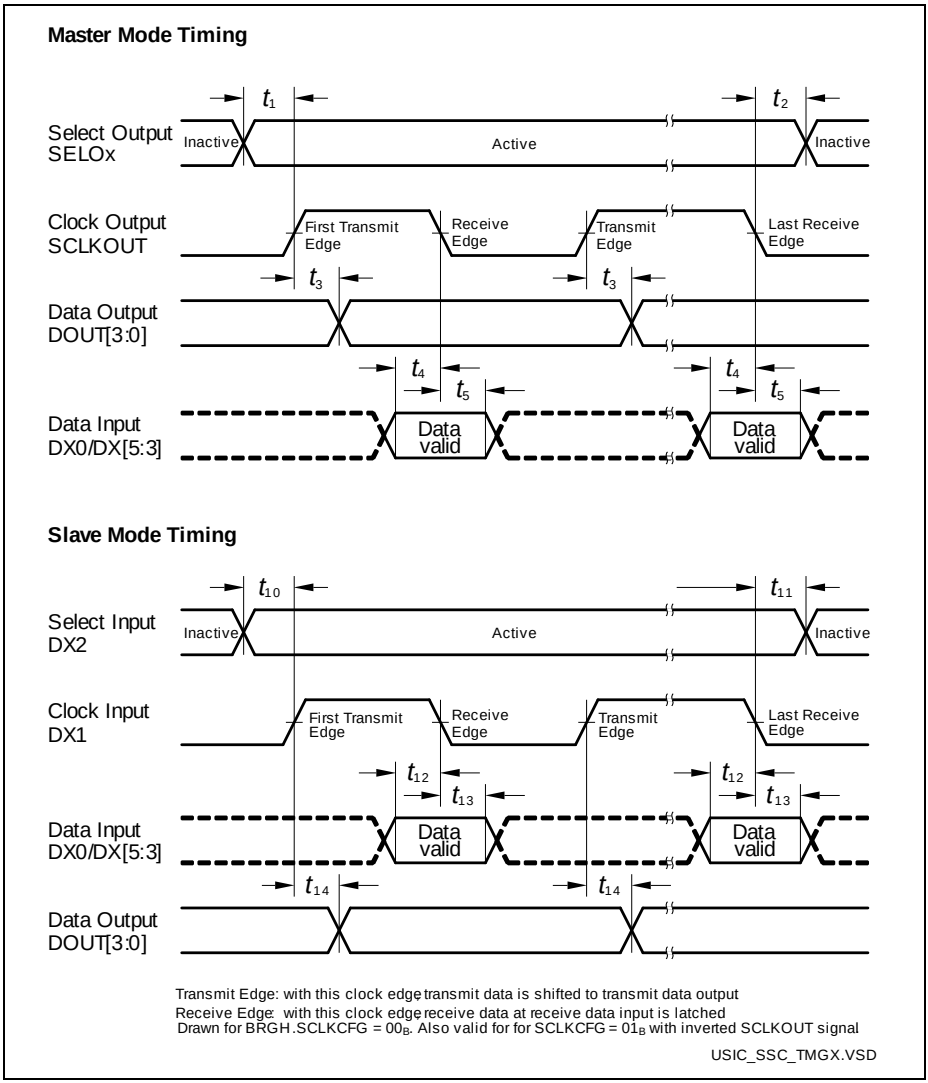



**Figure 22 USIC - SSC Master/Slave Mode Timing**

*Note: This timing diagram shows a standard configuration, for which the slave select signal is low-active, and the serial clock signal is not shifted and not inverted.*

### 3.3.6.2 Inter-IC (IIC) Interface Timing

The following parameters are applicable for a USIC channel operated in IIC mode.

*Note: Operating Conditions apply.*

**Table 31 USIC IIC Standard Mode Timing[1)]**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Fall time of both SDA and SCL | $t_1$ CC/SR | - | - | 300 | ns | |
| Rise time of both SDA and SCL | $t_2$ CC/SR | - | - | 1000 | ns | |
| Data hold time | $t_3$ CC/SR | 0 | - | - | µs | |
| Data set-up time | $t_4$ CC/SR | 250 | - | - | ns | |
| LOW period of SCL clock | $t_5$ CC/SR | 4.7 | - | - | µs | |
| HIGH period of SCL clock | $t_6$ CC/SR | 4.0 | - | - | µs | |
| Hold time for (repeated) START condition | $t_7$ CC/SR | 4.0 | - | - | µs | |
| Set-up time for repeated START condition | $t_8$ CC/SR | 4.7 | - | - | µs | |
| Set-up time for STOP condition | $t_9$ CC/SR | 4.0 | - | - | µs | |
| Bus free time between a STOP and START condition | $t_{10}$ CC/SR | 4.7 | - | - | µs | |
| Capacitive load for each bus line | $C_b$ SR | - | - | 400 | pF | |

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximalely 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

## 4.2 Package Outlines

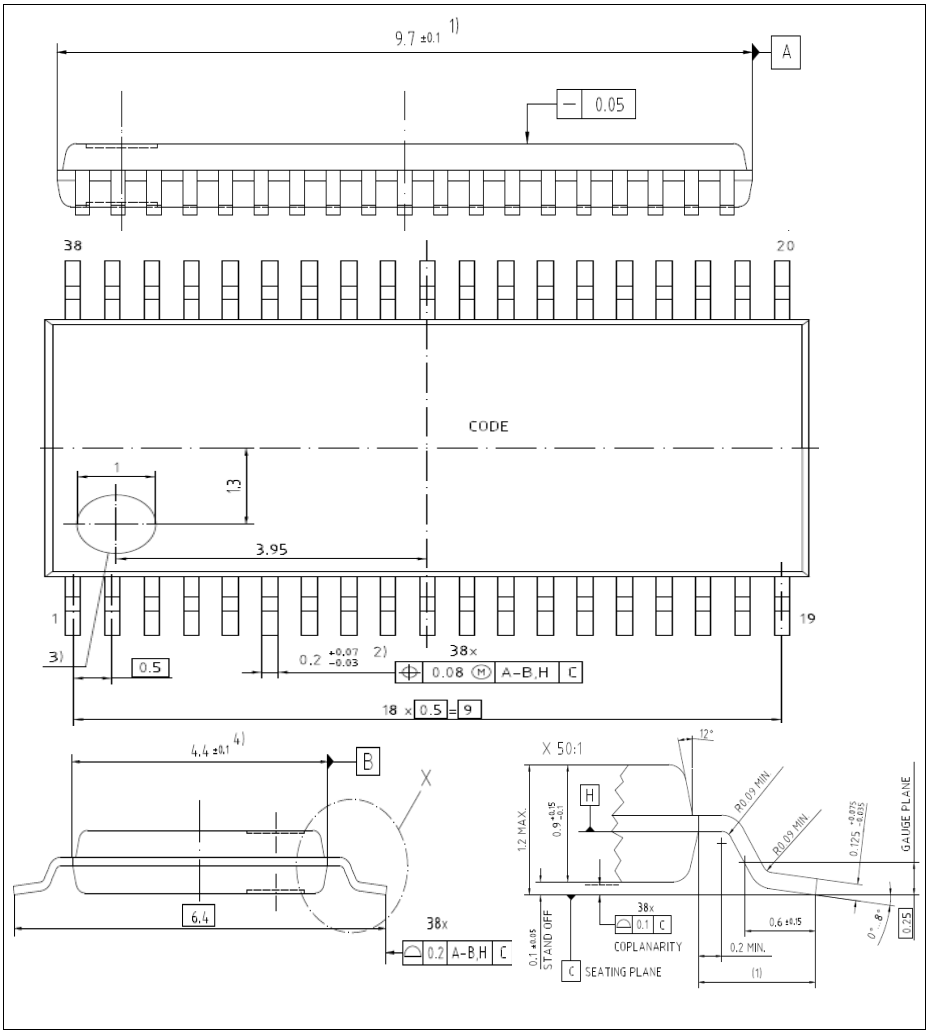



**Figure 26 PG-TSSOP-38-9**

# 5 Quality Declaration

Table 36 shows the characteristics of the quality parameters in the XMC1200.

**Table 36 Quality Parameters**

| Parameter | Symbol | Limit Values | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| ESD susceptibility according to Human Body Model (HBM) | $V_{HBM}$ SR | - | 2000 | V | Conforming to EIA/JESD22-A114-B |
| ESD susceptibility according to Charged Device Model (CDM) pins | $V_{CDM}$ SR | - | 500 | V | Conforming to JESD22-C101-C |
| Moisture sensitivity level | $MSL$ CC | - | 3 | - | JEDEC J-STD-020D |
| Soldering temperature | $T_{SDR}$ SR | - | 260 | °C | Profile according to JEDEC J-STD-020D |