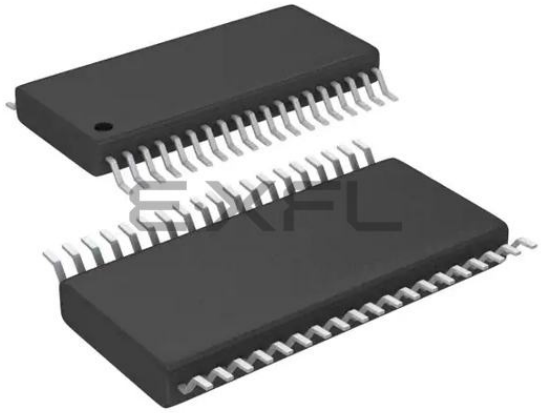
Infineon Technologies - XMC1201T038F0064ABXUMA1 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, I²S, POR, PWM, WDT
Number of I/O	26
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	38-TFSOP (0.173", 4.40mm Width)
Supplier Device Package	PG-TSSOP-38-9
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc1201t038f0064abxuma1

About this Document

This Data Sheet is addressed to embedded hardware and software developers. It provides the reader with detailed descriptions about the ordering designations, available features, electrical and physical characteristics of the XMC1200 series devices.

The document describes the characteristics of a superset of the XMC1200 series devices. For simplicity, the various device types are referred to by the collective term XMC1200 throughout this document.

XMC™1000 Family User Documentation

The set of user documentation includes:

- **Reference Manual**
  – decribes the functionality of the superset of devices.
- **Data Sheets**
  – list the complete ordering designations, available features and electrical characteristics of derivative devices.
- **Errata Sheets**
  – list deviations from the specifications given in the related Reference Manual or Data Sheets. Errata Sheets are provided for the superset of devices.

Attention: Please consult all parts of the documentation set to attain consolidated knowledge about your device.

Application related guidance is provided by **Users Guides** and **Application Notes**.

Please refer to **http://www.infineon.com/xmc1000** to get access to the latest versions of those documents.

2 General Device Information

This section summarizes the logic symbols and package pin configurations with a detailed list of the functional I/O mapping.

2.1 Logic Symbols

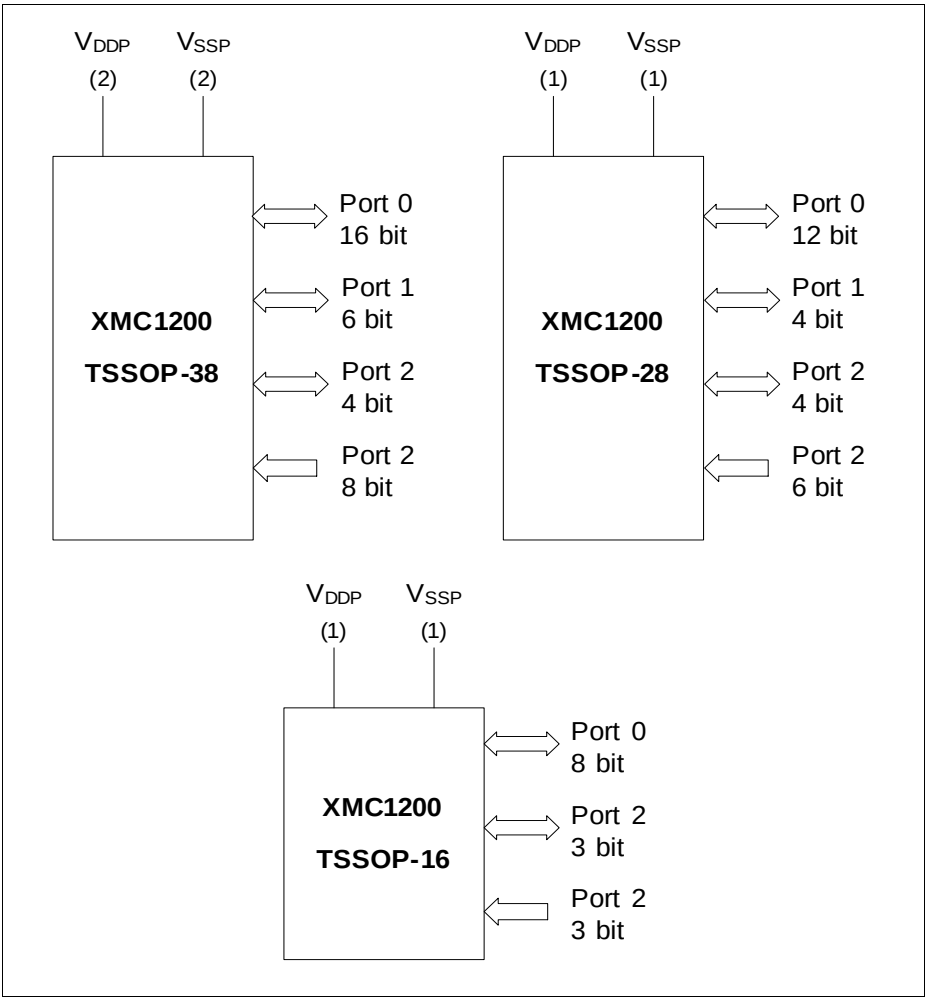

Figure 2 XMC1200 Logic Symbol for TSSOP-38, TSSOP-28 and TSSOP-16

2.2 Pin Configuration and Definition

The following figures summarize all pins, showing their locations on the different packages.

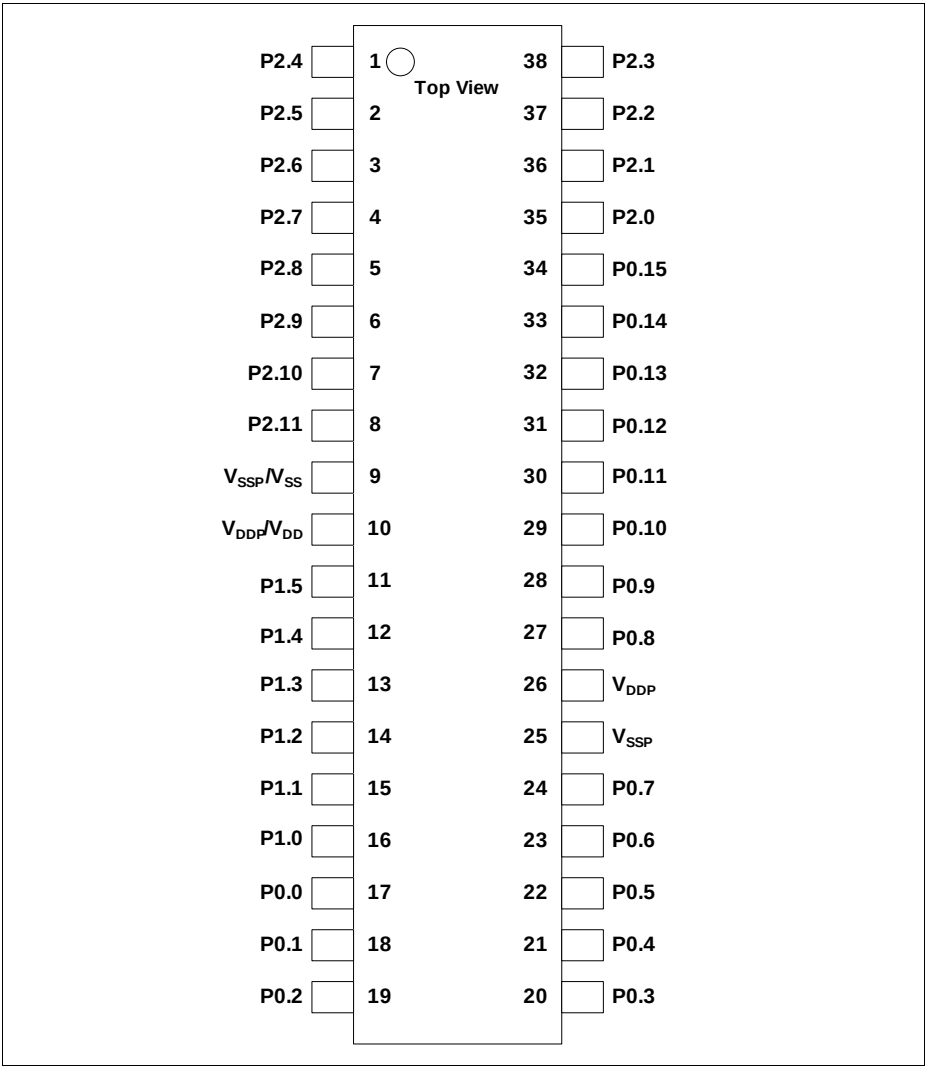

Figure 4 XMC1200 PG-TSSOP-38 Pin Configuration (top view)

2.2.1 Package Pin Summary

The following general building block is used to describe each pin:

Table 5 Package Pin Mapping Description

Function	Package A	Package B	...	Pad Type
Px.y	N	N		Pad Class

The table is sorted by the “Function” column, starting with the regular Port pins (Px.y), followed by the supply pins.

The following columns, titled with the supported package variants, lists the package pin number to which the respective function is mapped in that package.

The “Pad Type” indicates the employed pad type:

- STD_INOUT (standard bi-directional pads)
- STD_INOUT/AN (standard bi-directional pads with analog input)
- High Current (high current bi-directional pads)
- STD_IN/AN (standard input pads with analog input)
- Power (power supply)

Details about the pad properties are defined in the Electrical Parameters.

Table 6 Package Pin Mapping

Function	VQFN 40	TSSOP 38	TSSOP 28	VQFN 24	TSSOP 16	Pad Type	Notes
P0.0	23	17	13	15	7	STD_INOUT	
P0.1	24	18	-	-	-	STD_INOUT	
P0.2	25	19	-	-	-	STD_INOUT	
P0.3	26	20	-	-	-	STD_INOUT	
P0.4	27	21	14	-	-	STD_INOUT	
P0.5	28	22	15	16	8	STD_INOUT	
P0.6	29	23	16	17	9	STD_INOUT	

Table 6 Package Pin Mapping (cont'd)

Function	VQFN 40	TSSOP 38	TSSOP 28	VQFN 24	TSSOP 16	Pad Type	Notes
P2.1	2	36	26	2	-	STD_INOUT/AN	
P2.2	3	37	27	3	-	STD_IN/AN	
P2.3	4	38	-	-	-	STD_IN/AN	
P2.4	5	1	-	-	-	STD_IN/AN	
P2.5	6	2	28	-	-	STD_IN/AN	
P2.6	7	3	1	4	16	STD_IN/AN	
P2.7	8	4	2	5	1	STD_IN/AN	
P2.8	9	5	3	5	1	STD_IN/AN	
P2.9	10	6	4	6	2	STD_IN/AN	
P2.10	11	7	5	7	3	STD_INOUT/AN	
P2.11	12	8	6	8	4	STD_INOUT/AN	
VSS	13	9	7	9	5	Power	Supply GND, ADC reference GND
VDD	14	10	8	10	6	Power	Supply VDD, ADC reference voltage/ ORC reference voltage
VDDP	15	10	8	10	6	Power	When VDD is supplied, VDDP has to be supplied with the same voltage.

Table 10 Hardware Controlled I/O Functions

Function	Outputs		Inputs		Pull Control			
	HWO0	HWO1	HWI0	HWI1	HW0_PD	HW0_PU	HW1_PD	HW1_PU
P0.0	LEDTS0. EXTENDED7		LEDTS0.TSIN7	LEDTS0. TSIN7	Reserved for LEDTS Scheme A: pull-down disabled always	Reserved for LEDTS Scheme A: pull-down enabled always	Reserved for LEDTS Scheme B: pull-up enabled and pull-down disabled, and vice versa	
P0.1	LEDTS0. EXTENDED6		LEDTS0.TSIN6	LEDTS0. TSIN6				
P0.2	LEDTS0. EXTENDED5		LEDTS0.TSIN5	LEDTS0. TSIN5				
P0.3	LEDTS0. EXTENDED4		LEDTS0.TSIN4	LEDTS0. TSIN4				
P0.4	LEDTS0. EXTENDED3		LEDTS0. TSIN3	LEDTS0. TSIN3				
P0.5	LEDTS0. EXTENDED2		LEDTS0. TSIN2	LEDTS0. TSIN2				
P0.6	LEDTS0. EXTENDED1		LEDTS0. TSIN1	LEDTS0. TSIN1				
P0.7	LEDTS0. EXTENDED0		LEDTS0. TSIN0	LEDTS0. TSIN0				
P0.8	LEDTS1. EXTENDED0		LEDTS1. TSIN0	LEDTS1. TSIN0				
P0.9	LEDTS1. EXTENDED1		LEDTS1. TSIN1	LEDTS1. TSIN1				
P0.10	LEDTS1. EXTENDED2		LEDTS1. TSIN2	LEDTS1. TSIN2				
P0.11	LEDTS1. EXTENDED3		LEDTS1. TSIN3	LEDTS1. TSIN3				
P0.12	LEDTS1. EXTENDED4		LEDTS1. TSIN4	LEDTS1. TSIN4				
P0.13	LEDTS1. EXTENDED5		LEDTS1. TSIN5	LEDTS1. TSIN5				
P0.14	LEDTS1. EXTENDED6		LEDTS1. TSIN6	LEDTS1. TSIN6				
P0.15	LEDTS1. EXTENDED7		LEDTS1. TSIN7	LEDTS1. TSIN7				
P1.0		USIC0_CH0.DOUT0		USIC0_CH0.HWIN0	$\overline{\text{BCCU0.OUT2}}$	BCCU0.OUT2		
P1.1		USIC0_CH0.DOUT1		USIC0_CH0.HWIN1	$\overline{\text{BCCU0.OUT3}}$	BCCU0.OUT3		
P1.2		USIC0_CH0.DOUT2		USIC0_CH0.HWIN2	$\overline{\text{BCCU0.OUT4}}$	BCCU0.OUT4		

Table 13 PN-Junction Characterisitics for positive Overload

Pad Type	I_{OV} = 5 mA, T_J = -40 °C	I_{OV} = 5 mA, T_J = 115 °C
Standard, High-current, AN/DIG_IN	$V_{IN} = V_{DDP} + 0.5$ V	$V_{IN} = V_{DDP} + 0.5$ V

Table 14 PN-Junction Characterisitics for negative Overload

Pad Type	I_{OV} = 5 mA, T_J = -40 °C	I_{OV} = 5 mA, T_J = 115 °C
Standard, High-current, AN/DIG_IN	$V_{IN} = V_{SS} - 0.5$ V	$V_{IN} = V_{SS} - 0.5$ V

3.1.4 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the XMC1200. All parameters specified in the following tables refer to these operating conditions, unless noted otherwise.

Table 15 Operating Conditions Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Ambient Temperature	T_A SR	-40	–	85	°C	Temp. Range F
		-40	–	105	°C	Temp. Range X
Digital supply voltage[1)]	V_{DDP} SR	1.8	–	5.5	V	
MCLK Frequency	f_{MCLK} CC	–	–	33.2	MHz	CPU clock
PCLK Frequency	f_{PCLK} CC	–	–	66.4	MHz	Peripherals clock
Short circuit current of digital outputs	I_{SC} SR	-5	–	5	mA	
Absolute sum of short circuit currents of the device	ΣI_{SC_D} SR	–	–	25	mA	

1) See also the Supply Monitoring thresholds, **Chapter 3.3.2**.

3.2 DC Parameters

3.2.1 Input/Output Characteristics

Table 16 provides the characteristics of the input/output pins of the XMC1200.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Unless otherwise stated, input DC and AC characteristics, including peripheral timings, assume that the input pads operate with the standard hysteresis.

Table 16 Input/Output Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Output low voltage on port pins (with standard pads)	V_{OLP}	CC	–	1.0	V	I_{OL} = 11 mA (5 V) I_{OL} = 7 mA (3.3 V)
			–	0.4	V	I_{OL} = 5 mA (5 V) I_{OL} = 3.5 mA (3.3 V)
Output low voltage on high current pads	V_{OLP1}	CC	–	1.0	V	I_{OL} = 50 mA (5 V) I_{OL} = 25 mA (3.3 V)
			–	0.32	V	I_{OL} = 10 mA (5 V)
			–	0.4	V	I_{OL} = 5 mA (3.3 V)
Output high voltage on port pins (with standard pads)	V_{OHP}	CC	V_{DDP} - 1.0	–	V	I_{OH} = -10 mA (5 V) I_{OH} = -7 mA (3.3 V)
			V_{DDP} - 0.4	–	V	I_{OH} = -4.5 mA (5 V) I_{OH} = -2.5 mA (3.3 V)
Output high voltage on high current pads	V_{OHP1}	CC	V_{DDP} - 0.32	–	V	I_{OH} = -6 mA (5 V)
			V_{DDP} - 1.0	–	V	I_{OH} = -8 mA (3.3 V)
			V_{DDP} - 0.4	–	V	I_{OH} = -4 mA (3.3 V)
Input low voltage on port pins (Standard Hysteresis)	V_{ILPS}	SR	–	0.19 × V_{DDP}	V	CMOS Mode (5 V, 3.3 V & 2.2 V)
Input high voltage on port pins (Standard Hysteresis)	V_{IHPS}	SR	0.7 × V_{DDP}	–	V	CMOS Mode (5 V, 3.3 V & 2.2 V)

Table 16 Input/Output Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Input low voltage on port pins (Large Hysteresis)	V_{ILPL}	SR	–	0.08 × V_{DDP}	V	CMOS Mode (5 V, 3.3 V & 2.2 V)[10]
Input high voltage on port pins (Large Hysteresis)	V_{IHPL}	SR	0.85 × V_{DDP}	–	V	CMOS Mode (5 V, 3.3 V & 2.2 V)[10]
Rise time on High Current Pad[1]	t_{HCPR}	CC	–	9	ns	50 pF @ 5 V[2]
			–	12	ns	50 pF @ 3.3 V[3]
			–	25	ns	50 pF @ 1.8 V[4]
Fall time on High Current Pad[1]	t_{HCPF}	CC	–	9	ns	50 pF @ 5 V[2]
			–	12	ns	50 pF @ 3.3 V[3]
			–	25	ns	50 pF @ 1.8 V[4]
Rise time on Standard Pad[1]	t_R	CC	–	12	ns	50 pF @ 5 V[5]
			–	15	ns	50 pF @ 3.3 V[6]
			–	31	ns	50 pF @ 1.8 V[7]
Fall time on Standard Pad[1]	t_F	CC	–	12	ns	50 pF @ 5 V[5]
			–	15	ns	50 pF @ 3.3 V[6]
			–	31	ns	50 pF @ 1.8 V[7]
Input Hysteresis[8]	HYS	CC	0.08 × V_{DDP}	–	V	CMOS Mode (5 V), Standard Hysteresis
			0.03 × V_{DDP}	–	V	CMOS Mode (3.3 V), Standard Hysteresis
			0.02 × V_{DDP}	–	V	CMOS Mode (2.2 V), Standard Hysteresis
			0.5 × V_{DDP}	0.75 × V_{DDP}	V	CMOS Mode(5 V), Large Hysteresis
			0.4 × V_{DDP}	0.75 × V_{DDP}	V	CMOS Mode(3.3 V), Large Hysteresis
			0.2 × V_{DDP}	0.65 × V_{DDP}	V	CMOS Mode(2.2 V), Large Hysteresis

Table 17 ADC Characteristics (Operating Conditions apply)[1] (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Maximum sample rate in 8-bit mode [3]	f_{C8} CC	–	–	f_{ADC} / 38.5	–	1 sample pending
		–	–	f_{ADC} / 54.5	–	2 samples pending
RMS noise [4]	EN_{RMS} CC	–	1.5	–	LSB 12	DC input, V_{DD} = 5.0 V, V_{AIN} = 2.5 V, 25°C
DNL error	EA_{DNL} CC	–	±2.0	–	LSB 12	
INL error	EA_{INL} CC	–	±4.0	–	LSB 12	
Gain error with external reference	EA_{GAIN} CC	–	±0.5	–	%	SHSCFG.AREF = 00_B (calibrated)
Gain error with internal reference [5]	EA_{GAIN} CC	–	±3.6	–	%	SHSCFG.AREF = $1X_B$ (calibrated), -40°C - 105°C
		–	±2.0	–	%	SHSCFG.AREF = $1X_B$ (calibrated), 0°C - 85°C
Offset error	EA_{OFF} CC	–	±8.0	–	mV	Calibrated, V_{DD} = 5.0 V

1) The parameters are defined for ADC clock frequency f_{SH} = 32MHz, SHSCFG.DIVS = 0000_B. Usage of any other frequencies may affect the ADC performance.

2) No pending samples assumed, excluding sampling time and calibration.

3) Includes synchronization and calibration (average of gain and offset calibration).

4) This parameter can also be defined as an SNR value: SNR[dB] = 20 × log(A_{MAXeff} / N_{RMS}).
With $A_{MAXeff} = 2^N / 2$, SNR[dB] = 20 × log (2048 / N_{RMS}) [N = 12].
N_{RMS} = 1.5 LSB12, therefore, equals SNR = 20 × log (2048 / 1.5) = 62.7 dB.

5) Includes error from the reference voltage.

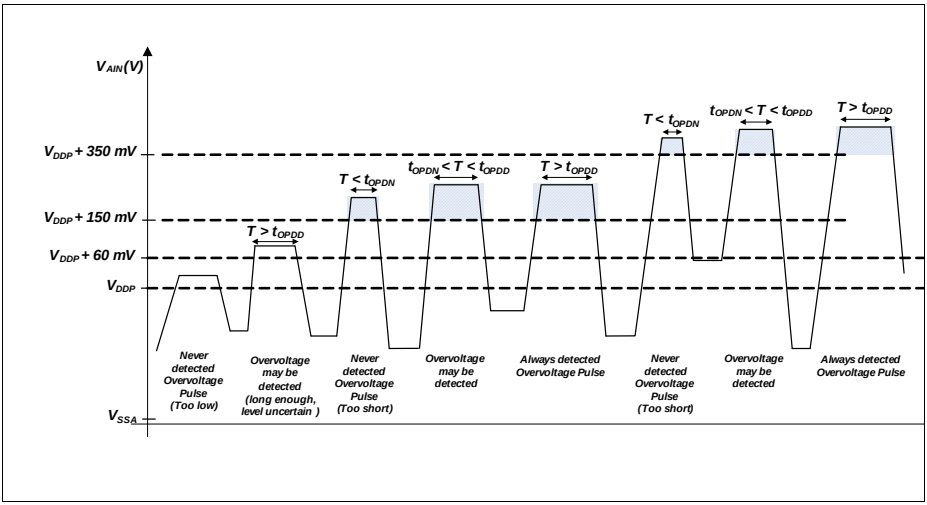

Figure 13 ORC Detection Ranges

3.2.5 Temperature Sensor Characteristics

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 20 Temperature Sensor Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Measurement time	t_M CC	–	–	10	ms	
Temperature sensor range	T_{SR} SR	-40	–	115	°C	
Sensor Accuracy[1)]	T_{TSAL} CC	-6	–	6	°C	T_J > 20°C
		-10	–	10	°C	0°C ≤ T_J ≤ 20°C
		-18	–	18	°C	-25°C ≤ T_J < 0°C
		-31	–	31	°C	-40°C ≤ T_J < -25°C
Start-up time after enabling	t_{TSSTE} SR	–	–	15	µs	

1) The temperature sensor accuracy is independent of the supply voltage.

Table 21 Power Supply Parameters; V_{DDP} = 5V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.[1]	Max.		
Sleep mode current Peripherals clock disabled Flash active f_{MCLK} / f_{PCLK} in MHz[5]	I_{DDPSD} CC	–	1.8	–	mA	32 / 64
			1.7	–	mA	24 / 48
			1.6	–	mA	16 / 32
			1.5	–	mA	8 / 16
			1.4	–	mA	1 / 1
Sleep mode current Peripherals clock disabled Flash powered down f_{MCLK} / f_{PCLK} in MHz[6]	I_{DDPSR} CC	–	1.2	–	mA	32 / 64
			1.1	–	mA	24 / 48
			1.0	–	mA	16 / 32
			0.8	–	mA	8 / 16
			0.7	–	mA	1 / 1
Deep Sleep mode current[7]	I_{DDPDS} CC	–	0.24	–	mA	
Wake-up time from Sleep to Active mode[8]	t_{SSA} CC	–	6	–	cycles	
Wake-up time from Deep Sleep to Active mode[9]	t_{DSA} CC	–	280	–	µsec	

1) The typical values are measured at T_A = + 25 °C and V_{DDP} = 5 V.
2) CPU and all peripherals clock enabled, Flash is in active mode.
3) CPU enabled, all peripherals clock disabled, Flash is in active mode.
4) CPU in sleep, all peripherals clock enabled and Flash is in active mode.
5) CPU in sleep, Flash is in active mode.
6) CPU in sleep, Flash is powered down and code executed from RAM after wake-up.
7) CPU in sleep, peripherals clock disabled, Flash is powered down and code executed from RAM after wake-up.
8) CPU in sleep, Flash is in active mode during sleep mode.
9) CPU in sleep, Flash is in powered down mode during deep sleep mode.

Table 22 provides the active current consumption of some modules operating at 5 V power supply at 25 °C. The typical values shown are used as a reference guide on the current consumption when these modules are enabled.

Table 22 Typical Active Current Consumption

Active Current Consumption	Symbol	Limit Values	Unit	Test Condition
		Typ.		
Baseload current	I_{CPUDDC}	5.04	mA	Modules including Core, SCU, PORT, memories, ANATOP[1)]
VADC and SHS	I_{ADCDDC}	3.4	mA	Set CGATCLR0.VADC to 1[2)]
USIC0	$I_{USIC0DDC}$	0.87	mA	Set CGATCLR0.USIC0 to 1[3)]
CCU40	$I_{CCU40DDC}$	0.94	mA	Set CGATCLR0.CCU40 to 1[4)]
LEDTSx	$I_{LTSxDDC}$	0.76	mA	Set CGATCLR0.LEDTSx to 1[5)]
BCCU0	$I_{BCCU0DDC}$	0.24	mA	Set CGATCLR0.BCCU0 to 1[6)]
WDT	I_{WDTDDC}	0.03	mA	Set CGATCLR0.WDT to 1[7)]
RTC	I_{RTCDDC}	0.01	mA	Set CGATCLR0.RTC to 1[8)]

1) Baseload current is measured with device running in user mode, MCLK=PCLK=32 MHz, with an endless loop in the flash memory. The clock to the modules stated in CGATSTAT0 are gated.

2) Active current is measured with: module enabled, MCLK=32 MHz, running in auto-scan conversion mode

3) Active current is measured with: module enabled, alternating messages sent to PC at 57.6kbaud every 200ms

4) Active current is measured with: module enabled, MCLK=PCLK=32 MHz, 1 CCU4 slice for PWM switching from 1500Hz and 1000Hz at regular intervals, 1 CCU4 slice in capture mode for reading period and duty cycle

5) Active current is measured with: module enabled, MCLK=32 MHz, 1 LED column, 6 LED/TS lines, Pad Scheme A with large pad hysteresis config, time slice duration = 1.048 ms

6) Active current is measured with: module enabled, MCLK=32 MHz, PCLK=64MHz, FCLK=0.8MHz, Normal mode (BCCU Clk = FCLK/4), 3 BCCU Channels and 1 Dimming Engine, change color or dim every 1s

7) Active current is measured with: module enabled, MCLK=32 MHz, time-out mode; WLB = 0, WUB = 0x00008000; WDT serviced every 1s

8) Active current is measured with: module enabled, MCLK=32 MHz, Periodic interrupt enabled

Table 24 Power-Up and Supply Monitoring Parameters (Operating Conditions apply)[1)] (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
V_{DDP} brownout reset voltage	V_{DDPBO} CC	1.55	1.62	1.75	V	calibrated, before user code starts running
V_{DDP} voltage to ensure defined pad states	V_{DDPPA} CC	–	1.0	–	V	
Start-up time from power-on reset	t_{SSW} SR	–	320	–	µs	Time to the first user code instruction in all start-up modes[4)]
BMI program time	t_{BMI} SR	–	8.25	–	ms	Time taken from a user-triggered system reset after BMI installation is is requested

1) Not all parameters are 100% tested, but are verified by design/characterisation.

2) A capacitor of at least 100 nF has to be added between V_{DDP} and V_{SSP} to fulfill the requirement as stated for this parameter.

3) Valid for a 100 nF buffer capacitor connected to supply pin where current from capacitor is forwarded only to the chip. A larger capacitor value has to be chosen if the power source sink a current.

4) This values does not include the ramp-up time. During startup firmware execution, MCLK is running at 32 MHz and the clocks to peripheral as specified in register CGATSTAT0 are gated.

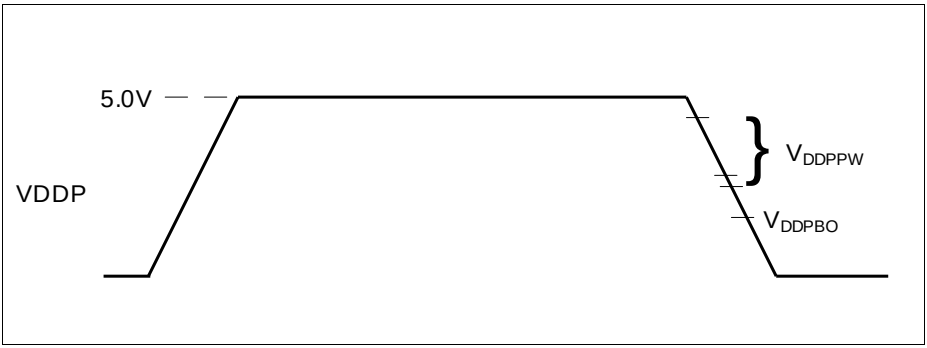

Figure 19 Supply Threshold Parameters

Figure 20 shows the typical curves for the accuracy of DCO1, with and without calibration based on temperature sensor, respectively.

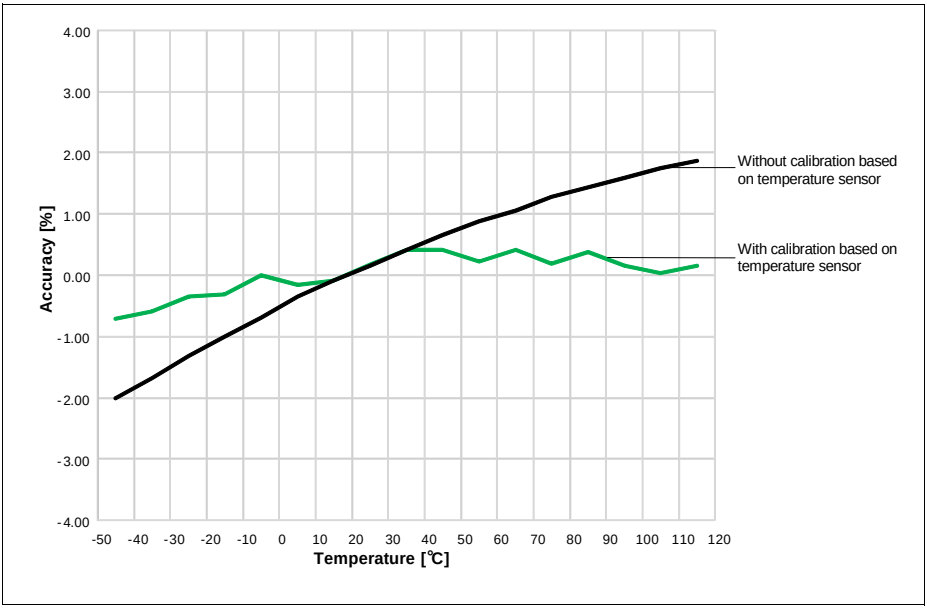

Figure 20 Typical DCO1 accuracy over temperature

Table 26 provides the characteristics of the 32 kHz clock output from digital controlled oscillators, DCO2 in XMC1200.

Table 26 32 kHz DCO2 Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Nominal frequency	f_{NOM}	CC	–	32.75	–	kHz	under nominal conditions[1] after trimming
Accuracy	Δf_{LT}	CC	-1.7	–	3.4	%	with respect to f_{NOM}(typ), over temperature (0 °C to 85 °C)
			-3.9	–	4.0	%	with respect to f_{NOM}(typ), over temperature (-40 °C to 105 °C)

1) The deviation is relative to the factory trimmed frequency at nominal V_{DDC} and T_A = + 25 °C.

3.3.5 SPD Timing Requirements

The optimum SPD decision time between 0_B and 1_B is 0.75 µs. With this value the system has maximum robustness against frequency deviations of the sampling clock on tool and on device side. However it is not always possible to exactly match this value with the given constraints for the sample clock. For instance for a oversampling rate of 4, the sample clock will be 8 MHz and in this case the closest possible effective decision time is 5.5 clock cycles (0.69 µs).

Table 28 Optimum Number of Sample Clocks for SPD

Sample Freq.	Sampling Factor	Sample Clocks 0_B	Sample Clocks 1_B	Effective Decision Time[1)]	Remark
8 MHz	4	1 to 5	6 to 12	0.69 µs	The other closest option (0.81 µs) for the effective decision time is less robust.

1) Nominal sample frequency period multiplied with 0.5 + (max. number of 0_B sample clocks)

For a balanced distribution of the timing robustness of SPD between tool and device, the timing requirements for the tool are:

- Frequency deviation of the sample clock is +/- 5%
- Effective decision time is between 0.69 µs and 0.75 µs (calculated with nominal sample frequency)

3.3.6 Peripheral Timings

Note: These parameters are not subject to production test, but verified by design and/or characterization.

3.3.6.1 Synchronous Serial Interface (USIC SSC) Timing

The following parameters are applicable for a USIC channel operated in SSC mode.

Note: Operating Conditions apply.

Table 29 USIC SSC Master Mode Timing

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
SCLKOUT master clock period	t_{CLK}	CC	62.5	–	–	ns	
Slave select output SELO active to first SCLKOUT transmit edge	t_1	CC	80	–	–	ns	
Slave select output SELO inactive after last SCLKOUT receive edge	t_2	CC	0	–	–	ns	
Data output DOUT[3:0] valid time	t_3	CC	-10	–	10	ns	
Receive data input DX0/DX[5:3] setup time to SCLKOUT receive edge	t_4	SR	80	–	–	ns	
Data input DX0/DX[5:3] hold time from SCLKOUT receive edge	t_5	SR	0	–	–	ns	

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