Infineon Technologies - XMC1202T016X0016ABXUMA1 Datasheet

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Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, I²S, POR, PWM, WDT
Number of I/O	11
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	16-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	PG-TSSOP-16-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc1202t016x0016abxuma1

XMC™1200 AB-Step

Microcontroller Series
for Industrial Applications

XMC™1000 Family

ARM® Cortex®-M0
32-bit processor core

Data Sheet

V1.7 2016-08

Microcontrollers

XMC1200 Data Sheet

Revision History: V1.7 2016-08

Previous Version: V1.6	
Page	Subjects
many	Added XMC™ trademark
10, **11**, **12**	Added new marking variants XMC1201-T028F0016, XMC1201-T028F0032 and XMC1202-T016X0064
53	Flash Memory Parameters Table: • Erase time per page parameter is renamed to Erase time per page / sector. • Erase cycles parameter is renamed to include test condition of sum of page and sector erase cycles. • Added parameter for fixed wait states configuration.

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Table 1 Synopsis of XMC1200 Device Types (cont'd)

Derivative	Package	Flash Kbytes	SRAM Kbytes
XMC1202-T028X0016	PG-TSSOP-28-16	16	16
XMC1202-T028X0032	PG-TSSOP-28-16	32	16
XMC1202-T028X0064	PG-TSSOP-28-16	64	16
XMC1202-T016X0016	PG-TSSOP-16-8	16	16
XMC1202-T016X0032	PG-TSSOP-16-8	32	16
XMC1202-T016X0064	PG-TSSOP-16-8	64	16
XMC1202-Q024X0016	PG-VQFN-24-19	16	16
XMC1202-Q024X0032	PG-VQFN-24-19	32	16
XMC1201-Q040F0016	PG-VQFN-40-13	16	16
XMC1201-Q040F0032	PG-VQFN-40-13	32	16
XMC1201-Q040F0064	PG-VQFN-40-13	64	16
XMC1201-Q040F0128	PG-VQFN-40-13	128	16
XMC1201-Q040F0200	PG-VQFN-40-13	200	16
XMC1202-Q040X0016	PG-VQFN-40-13	16	16
XMC1202-Q040X0032	PG-VQFN-40-13	32	16

1.3 Device Type Features

The following table lists the available features per device type.

Table 2 Features of XMC1200 Device Types[1)]

Derivative	ADC channel	ACMP	BCCU	LEDTS
XMC1200-T038	16	3	1	2
XMC1201-T028	14	-	-	2
XMC1201-T038	16	-	-	2
XMC1202-T028	14	3	1	-
XMC1202-T016	11	2	1	-
XMC1202-Q024	13	3	1	-
XMC1201-Q040	16	-	-	2
XMC1202-Q040	16	3	1	-

1) Features that are not included in this table are available in all the derivatives

Table 4 XMC1200 Chip Identification Number (cont'd)

Derivative	Value	Marking
XMC1202-T028X0016	00012023 01CF00FF 00001FF7 00008000 00000C00 00001000 00005000 201ED083$_H$	AB
XMC1202-T028X0032	00012023 01CF00FF 00001FF7 00008000 00000C00 00001000 00009000 201ED083$_H$	AB
XMC1202-T028X0064	00012023 01CF00FF 00001FF7 00008000 00000C00 00001000 00011000 201ED083$_H$	AB
XMC1202-T016X0016	00012033 01CF00FF 00001FF7 00008000 00000C00 00001000 00005000 201ED083$_H$	AB
XMC1202-T016X0032	00012033 01CF00FF 00001FF7 00008000 00000C00 00001000 00009000 201ED083$_H$	AB
XMC1202-T016X0064	00012033 01CF00FF 00001FF7 00008000 00000C00 00001000 00011000 201ED083$_H$	AB
XMC1202-Q024X0016	00012063 01CF00FF 00001FF7 00008000 00000C00 00001000 00005000 201ED083$_H$	AB
XMC1202-Q024X0032	00012063 01CF00FF 00001FF7 00008000 00000C00 00001000 00009000 201ED083$_H$	AB
XMC1201-Q040F0016	00012042 01CF00FF 00001FF7 00006000 00000C00 00001000 00005000 201ED083$_H$	AB
XMC1201-Q040F0032	00012042 01CF00FF 00001FF7 00006000 00000C00 00001000 00009000 201ED083$_H$	AB
XMC1201-Q040F0064	00012042 01CF00FF 00001FF7 00006000 00000C00 00001000 00011000 201ED083$_H$	AB
XMC1201-Q040F0128	00012042 01CF00FF 00001FF7 00006000 00000C00 00001000 00021000 201ED083$_H$	AB
XMC1201-Q040F0200	00012042 01CF00FF 00001FF7 00006000 00000C00 00001000 00033000 201ED083$_H$	AB
XMC1202-Q040X0016	00012043 01CF00FF 00001FF7 00008000 00000C00 00001000 00005000 201ED083$_H$	AB
XMC1202-Q040X0032	00012043 01CF00FF 00001FF7 00008000 00000C00 00001000 00009000 201ED083$_H$	AB

2 General Device Information

This section summarizes the logic symbols and package pin configurations with a detailed list of the functional I/O mapping.

2.1 Logic Symbols

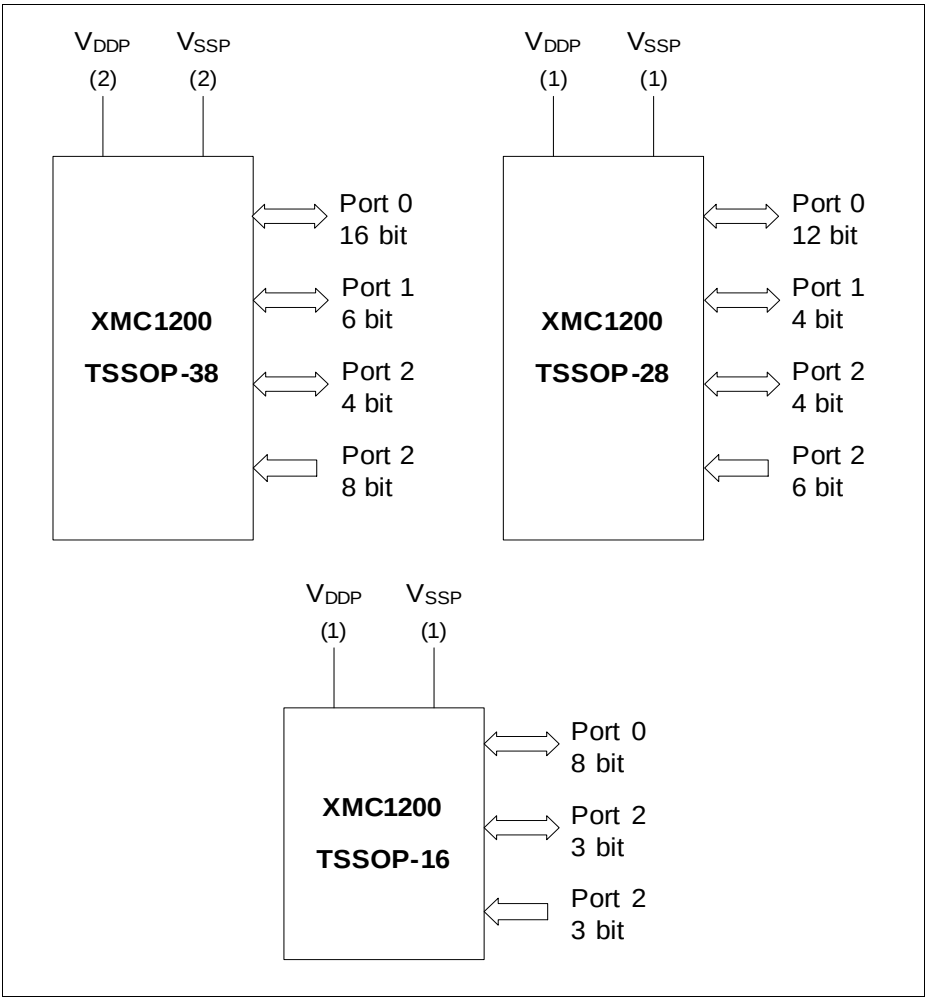

Figure 2 XMC1200 Logic Symbol for TSSOP-38, TSSOP-28 and TSSOP-16

Table 6 Package Pin Mapping (cont'd)

Function	VQFN 40	TSSOP 38	TSSOP 28	VQFN 24	TSSOP 16	Pad Type	Notes
P2.1	2	36	26	2	-	STD_INOUT/AN	
P2.2	3	37	27	3	-	STD_IN/AN	
P2.3	4	38	-	-	-	STD_IN/AN	
P2.4	5	1	-	-	-	STD_IN/AN	
P2.5	6	2	28	-	-	STD_IN/AN	
P2.6	7	3	1	4	16	STD_IN/AN	
P2.7	8	4	2	5	1	STD_IN/AN	
P2.8	9	5	3	5	1	STD_IN/AN	
P2.9	10	6	4	6	2	STD_IN/AN	
P2.10	11	7	5	7	3	STD_INOUT/AN	
P2.11	12	8	6	8	4	STD_INOUT/AN	
VSS	13	9	7	9	5	Power	Supply GND, ADC reference GND
VDD	14	10	8	10	6	Power	Supply VDD, ADC reference voltage/ ORC reference voltage
VDDP	15	10	8	10	6	Power	When VDD is supplied, VDDP has to be supplied with the same voltage.

2.2.2 Port I/O Functions

The following general building block is used to describe each PORT pin:

Table 7 Port I/O Function Description

Function	Outputs		Inputs	
	ALT1	ALTn	Input	Input
P0.0		MODA.OUT	MODC.INA	
Pn.y	MODA.OUT		MODA.INA	MODC.INB

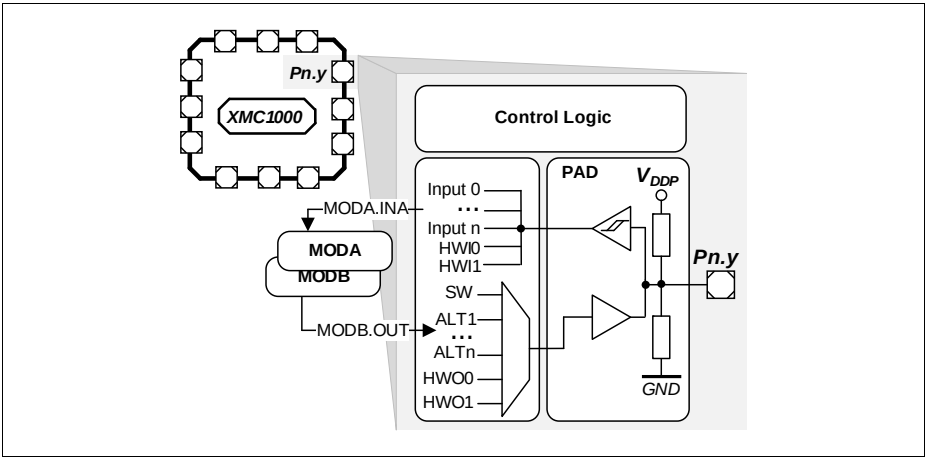

Figure 9 Simplified Port Structure

Pn.y is the port pin name, defining the control and data bits/registers associated with it. As GPIO, the port is under software control. Its input value is read via Pn_IN.y, Pn_OUT defines the output value.

Up to seven alternate output functions (ALT1/2/3/4/5/6/7) can be mapped to a single port pin, selected by Pn_IOCR.PC. The output value is directly driven by the respective module, with the pin characteristics controlled by the port registers (within the limits of the connected pad).

The port pin input can be connected to multiple peripherals. Most peripherals have an input multiplexer to select between different possible input sources.

The input path is also active while the pin is configured as output. This allows to feedback an output to on-chip resources without wasting an additional external pin.

Please refer to the **Port I/O Functions** table for the complete Port I/O function mapping.

Table 9 Port I/O Functions

Function	Outputs							Inputs							
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	Input	Input	Input	Input	Input	Input	Input	Input
P0.0	ERU0.PDOUT0	LEDTS0.LINE7	ERU0.GOUT0	CCU40.OUT0		USIC0_CH0.SELO0	USIC0_CH1.SELO0	BCCU0.TRAPINB	CCU40.IN0C			USIC0_CH0.DX2A	USIC0_CH1.DX2A		
P0.1	ERU0.PDOUT1	LEDTS0.LINE6	ERU0.GOUT1	CCU40.OUT1		BCCU0.OUT8	SCU.VDROP		CCU40.IN1C						
P0.2	ERU0.PDOUT2	LEDTS0.LINE5	ERU0.GOUT2	CCU40.OUT2		VADC0.EMUX02			CCU40.IN2C						
P0.3	ERU0.PDOUT3	LEDTS0.LINE4	ERU0.GOUT3	CCU40.OUT3		VADC0.EMUX01			CCU40.IN3C						
P0.4	BCCU0.OUT0	LEDTS0.LINE3	LEDTS0.COL3	CCU40.OUT1		VADC0.EMUX00	WWDT.SERVICE_OUT								
P0.5	BCCU0.OUT1	LEDTS0.LINE2	LEDTS0.COL2	CCU40.OUT0		ACMP2.OUT									
P0.6	BCCU0.OUT2	LEDTS0.LINE1	LEDTS0.COL1	CCU40.OUT0		USIC0_CH1.MCLKOUT	USIC0_CH1.DOUT0		CCU40.IN0B			USIC0_CH1.DX0C			
P0.7	BCCU0.OUT3	LEDTS0.LINE0	LEDTS0.COL0	CCU40.OUT1		USIC0_CH0.SCLKOUT	USIC0_CH1.DOUT0		CCU40.IN1B			USIC0_CH0.DX1C	USIC0_CH1.DX0D	USIC0_CH1.DX1C	
P0.8	BCCU0.OUT4	LEDTS1.LINE0	LEDTS0.COLA	CCU40.OUT2		USIC0_CH0.SCLKOUT	USIC0_CH1.SCLKOUT		CCU40.IN2B			USIC0_CH0.DX1B	USIC0_CH1.DX1B		
P0.9	BCCU0.OUT5	LEDTS1.LINE1	LEDTS0.COL6	CCU40.OUT3		USIC0_CH0.SELO0	USIC0_CH1.SELO0		CCU40.IN3B			USIC0_CH0.DX2B	USIC0_CH1.DX2B		
P0.10	BCCU0.OUT6	LEDTS1.LINE2	LEDTS0.COL5	ACMP0.OUT		USIC0_CH0.SELO1	USIC0_CH1.SELO1					USIC0_CH0.DX2C	USIC0_CH1.DX2C		
P0.11	BCCU0.OUT7	LEDTS1.LINE3	LEDTS0.COL4	USIC0_CH0.MCLKOUT		USIC0_CH0.SELO2	USIC0_CH1.SELO2					USIC0_CH0.DX2D	USIC0_CH1.DX2D		
P0.12	BCCU0.OUT6	LEDTS1.LINE4	LEDTS0.COL3	LEDTS1.COL3		USIC0_CH0.SELO3		BCCU0.TRAPINA	CCU40.IN0A	CCU40.IN1A	CCU40.IN2A	CCU40.IN3A	USIC0_CH0.DX2E		
P0.13	WWDT.SERVICE_OUT	LEDTS1.LINE5	LEDTS0.COL2	LEDTS1.COL2		USIC0_CH0.SELO4						USIC0_CH0.DX2F			
P0.14	BCCU0.OUT7	LEDTS1.LINE6	LEDTS0.COL1	LEDTS1.COL1		USIC0_CH0.DOUT0	USIC0_CH0.SCLKOUT					USIC0_CH0.DX0A	USIC0_CH0.DX1A		

Table 10 Hardware Controlled I/O Functions

Function	Outputs		Inputs		Pull Control			
	HWO0	HWO1	HWI0	HWI1	HW0_PD	HW0_PU	HW1_PD	HW1_PU
P1.3		USIC0_CH0.DOUT3		USIC0_CH0.HWIN3	BCCU0.OUT5	BCCU0.OUT5		
P1.4					BCCU0.OUT6	BCCU0.OUT6		
P1.5					BCCU0.OUT7	BCCU0.OUT7		
P1.6					BCCU0.OUT8	BCCU0.OUT8		
P2.0					BCCU0.OUT1	BCCU0.OUT1		
P2.1					BCCU0.OUT6	BCCU0.OUT6		
P2.2					BCCU0.OUT0	BCCU0.OUT0	CCU40.OUT3	CCU40.OUT3
P2.3					ACMP2.OUT	ACMP2.OUT		
P2.4					BCCU0.OUT8	BCCU0.OUT8		
P2.5					ACMP1.OUT	ACMP1.OUT		
P2.6					BCCU0.OUT2	BCCU0.OUT2	CCU40.OUT3	CCU40.OUT3
P2.7					BCCU0.OUT8	BCCU0.OUT8	CCU40.OUT3	CCU40.OUT3
P2.8					BCCU0.OUT1	BCCU0.OUT1	CCU40.OUT2	CCU40.OUT2
P2.9					BCCU0.OUT7	BCCU0.OUT7	CCU40.OUT2	CCU40.OUT2
P2.10					BCCU0.OUT4	BCCU0.OUT4		
P2.11					BCCU0.OUT5	BCCU0.OUT5		

If a pin current is outside of the **Operating Conditions** but within the overload conditions, then the parameters of this pin as stated in the Operating Conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

Note: An overload condition on one or more pins does not require a reset.

Note: A series resistor at the pin to limit the current to the maximum permitted overload current is sufficient to handle failure situations like short to battery.

Table 12 Overload Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input current on any port pin during overload condition	I_{OV} SR	-5	–	5	mA	
Absolute sum of all input circuit currents during overload condition	I_{OVS} SR	–	–	25	mA	

Figure 10 shows the path of the input currents during overload via the ESD protection structures. The diodes against V_{DDP} and ground are a simplified representation of these ESD protection structures.

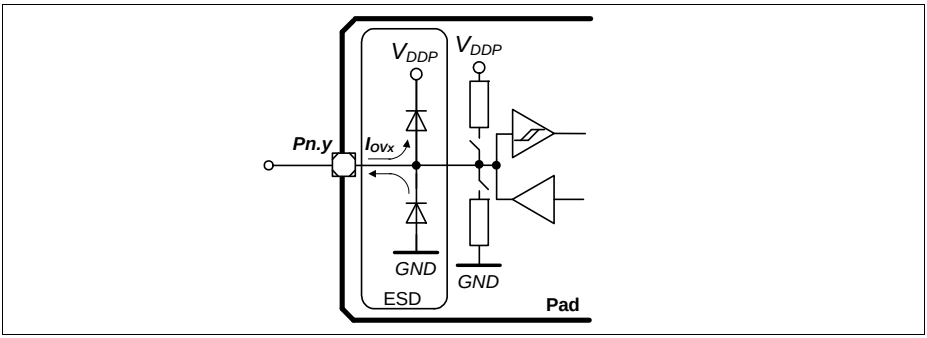

Figure 10 Input Overload Current via ESD structures

Table 13 and **Table 14** list input voltages that can be reached under overload conditions. Note that the absolute maximum input voltages as defined in the **Absolute Maximum Ratings** must not be exceeded during overload.

Table 13 PN-Junction Characterisitics for positive Overload

Pad Type	I_{OV} = 5 mA, T_J = -40 °C	I_{OV} = 5 mA, T_J = 115 °C
Standard, High-current, AN/DIG_IN	$V_{IN} = V_{DDP} + 0.5$ V	$V_{IN} = V_{DDP} + 0.5$ V

Table 14 PN-Junction Characterisitics for negative Overload

Pad Type	I_{OV} = 5 mA, T_J = -40 °C	I_{OV} = 5 mA, T_J = 115 °C
Standard, High-current, AN/DIG_IN	$V_{IN} = V_{SS} - 0.5$ V	$V_{IN} = V_{SS} - 0.5$ V

Table 22 provides the active current consumption of some modules operating at 5 V power supply at 25 °C. The typical values shown are used as a reference guide on the current consumption when these modules are enabled.

Table 22 Typical Active Current Consumption

Active Current Consumption	Symbol	Limit Values	Unit	Test Condition
		Typ.		
Baseload current	I_{CPUDDC}	5.04	mA	Modules including Core, SCU, PORT, memories, ANATOP[1)]
VADC and SHS	I_{ADCDDC}	3.4	mA	Set CGATCLR0.VADC to 1[2)]
USIC0	$I_{USIC0DDC}$	0.87	mA	Set CGATCLR0.USIC0 to 1[3)]
CCU40	$I_{CCU40DDC}$	0.94	mA	Set CGATCLR0.CCU40 to 1[4)]
LEDTSx	$I_{LTSxDDC}$	0.76	mA	Set CGATCLR0.LEDTSx to 1[5)]
BCCU0	$I_{BCCU0DDC}$	0.24	mA	Set CGATCLR0.BCCU0 to 1[6)]
WDT	I_{WDTDDC}	0.03	mA	Set CGATCLR0.WDT to 1[7)]
RTC	I_{RTCDDC}	0.01	mA	Set CGATCLR0.RTC to 1[8)]

1) Baseload current is measured with device running in user mode, MCLK=PCLK=32 MHz, with an endless loop in the flash memory. The clock to the modules stated in CGATSTAT0 are gated.

2) Active current is measured with: module enabled, MCLK=32 MHz, running in auto-scan conversion mode

3) Active current is measured with: module enabled, alternating messages sent to PC at 57.6kbaud every 200ms

4) Active current is measured with: module enabled, MCLK=PCLK=32 MHz, 1 CCU4 slice for PWM switching from 1500Hz and 1000Hz at regular intervals, 1 CCU4 slice in capture mode for reading period and duty cycle

5) Active current is measured with: module enabled, MCLK=32 MHz, 1 LED column, 6 LED/TS lines, Pad Scheme A with large pad hysteresis config, time slice duration = 1.048 ms

6) Active current is measured with: module enabled, MCLK=32 MHz, PCLK=64MHz, FCLK=0.8MHz, Normal mode (BCCU Clk = FCLK/4), 3 BCCU Channels and 1 Dimming Engine, change color or dim every 1s

7) Active current is measured with: module enabled, MCLK=32 MHz, time-out mode; WLB = 0, WUB = 0x00008000; WDT serviced every 1s

8) Active current is measured with: module enabled, MCLK=32 MHz, Periodic interrupt enabled

3.3 AC Parameters

3.3.1 Testing Waveforms

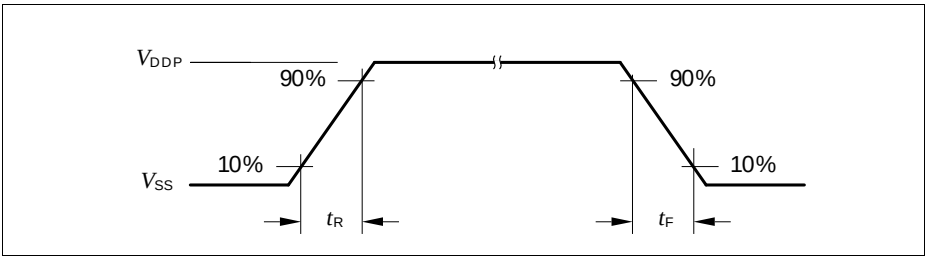

Figure 16 Rise/Fall Time Parameters

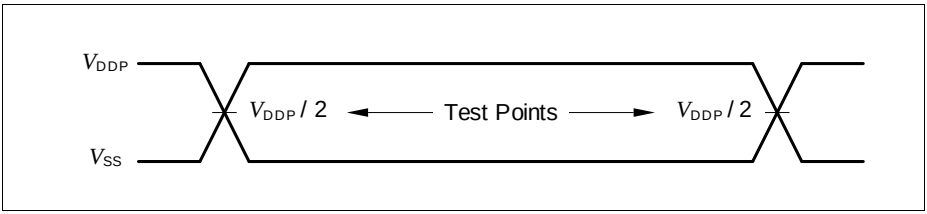

Figure 17 Testing Waveform, Output Delay

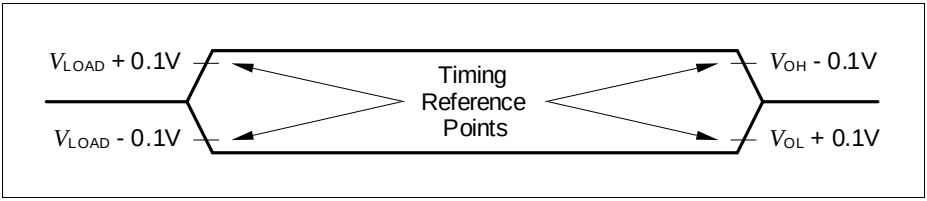

Figure 18 Testing Waveform, Output High Impedance

3.3.2 Power-Up and Supply Monitoring Characteristics

Table 24 provides the characteristics of the power-up and supply monitoring in XMC1200.

The guard band between the lowest valid operating voltage and the brownout reset threshold provides a margin for noise immunity and hysteresis. The electrical parameters may be violated while V_{DDP} is outside its operating range.

The brownout detection triggers a reset within the defined range. The prewarning detection can be used to trigger an early warning and issue corrective and/or fail-safe actions in case of a critical supply voltage drop.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 24 Power-Up and Supply Monitoring Parameters (Operating Conditions apply)[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
V_{DDP} ramp-up time	t_{RAMPUP} SR	V_{DDP}/ $S_{VDDPrise}$	–	10^7	µs	
V_{DDP} slew rate	S_{VDDPOP} SR	0	–	0.1	V/µs	Slope during normal operation
	S_{VDDP10} SR	0	–	10	V/µs	Slope during fast transient within +/- 10% of V_{DDP}
	$S_{VDDPrise}$ SR	0	–	10	V/µs	Slope during power-on or restart after brownout event
	$S_{VDDPfall}$[2)] SR	0	–	0.25	V/µs	Slope during supply falling out of the +/-10% limits[3)]
V_{DDP} prewarning voltage	V_{DDPPW} CC	2.1	2.25	2.4	V	ANAVDEL.VDEL_SELECT = 00_B
		2.85	3	3.15	V	ANAVDEL.VDEL_SELECT = 01_B
		4.2	4.4	4.6	V	ANAVDEL.VDEL_SELECT = 10_B

3.3.3 On-Chip Oscillator Characteristics

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 25 provides the characteristics of the 64 MHz clock output from the digital controlled oscillator, DCO1 in XMC1200.

Table 25 64 MHz DCO1 Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Nominal frequency	f_{NOM}	CC	–	64	–	MHz	under nominal conditions[1] after trimming
Accuracy[2]	Δf_{LT}	CC	-1.7	–	3.4	%	with respect to f_{NOM}(typ), over temperature (0 °C to 85 °C)
			-3.9	–	4.0	%	with respect to f_{NOM}(typ), over temperature (-40 °C to 105 °C)

1) The deviation is relative to the factory trimmed frequency at nominal V_{DDC} and T_A = + 25 °C.

2) The accuracy of the DCO1 oscillator can be further improved through alternative methods, refer to XMC1000 Oscillator Handling Application Note.

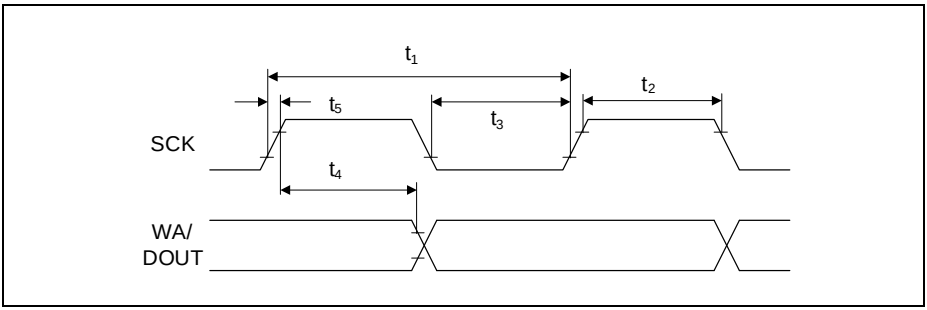

Figure 24 USIC IIS Master Transmitter Timing

Table 34 USIC IIS Slave Receiver Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	t_6 SR	$4/f_{MCLK}$	-	-	ns	
Clock HIGH	t_7 SR	0.35 x t_{6min}	-	-	ns	
Clock Low	t_8 SR	0.35 x t_{6min}	-	-	ns	
Set-up time	t_9 SR	0.2 x t_{6min}	-	-	ns	
Hold time	t_{10} SR	10	-	-	ns	

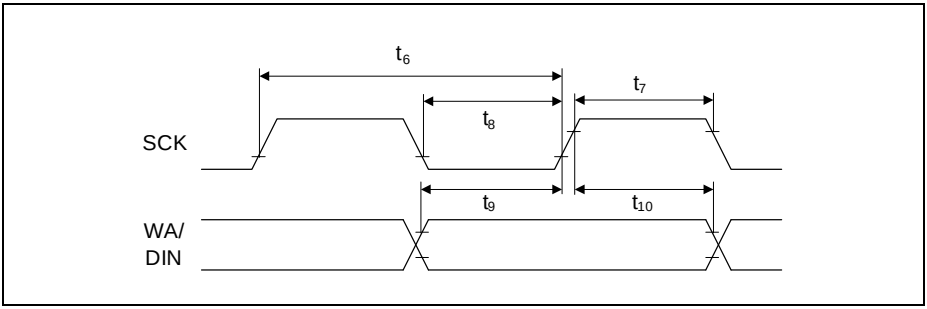

Figure 25 USIC IIS Slave Receiver Timing

4.2 Package Outlines

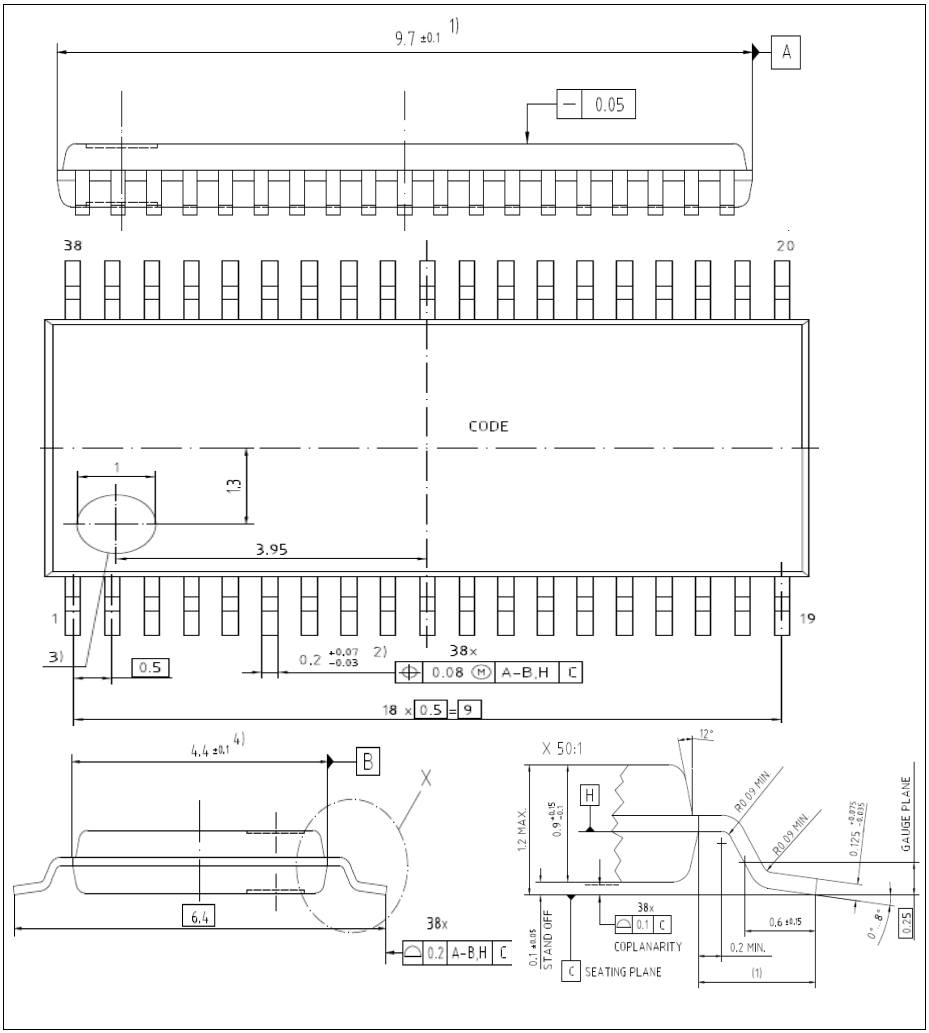

Figure 26 PG-TSSOP-38-9

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