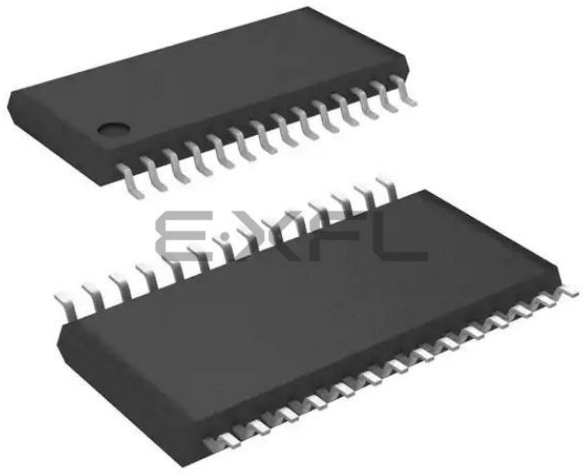
Infineon Technologies - XMC1202T028X0016ABXUMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, I²S, POR, PWM, WDT
Number of I/O	20
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 14x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	28-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	PG-TSSOP-28-16
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc1202t028x0016abxuma1

XMC1200 Data Sheet

Revision History: V1.7 2016-08

Previous Version: V1.6	
Page	Subjects
many	Added XMC™ trademark
10, **11**, **12**	Added new marking variants XMC1201-T028F0016, XMC1201-T028F0032 and XMC1202-T016X0064
53	Flash Memory Parameters Table: • Erase time per page parameter is renamed to Erase time per page / sector. • Erase cycles parameter is renamed to include test condition of sum of page and sector erase cycles. • Added parameter for fixed wait states configuration.

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1 Summary of Features

The XMC1200 devices are members of the XMC™1000 Family of microcontrollers based on the ARM Cortex-M0 processor core. The XMC1200 series devices are optimized for LED Lighting and Human-Machine interface (HMI) applications.

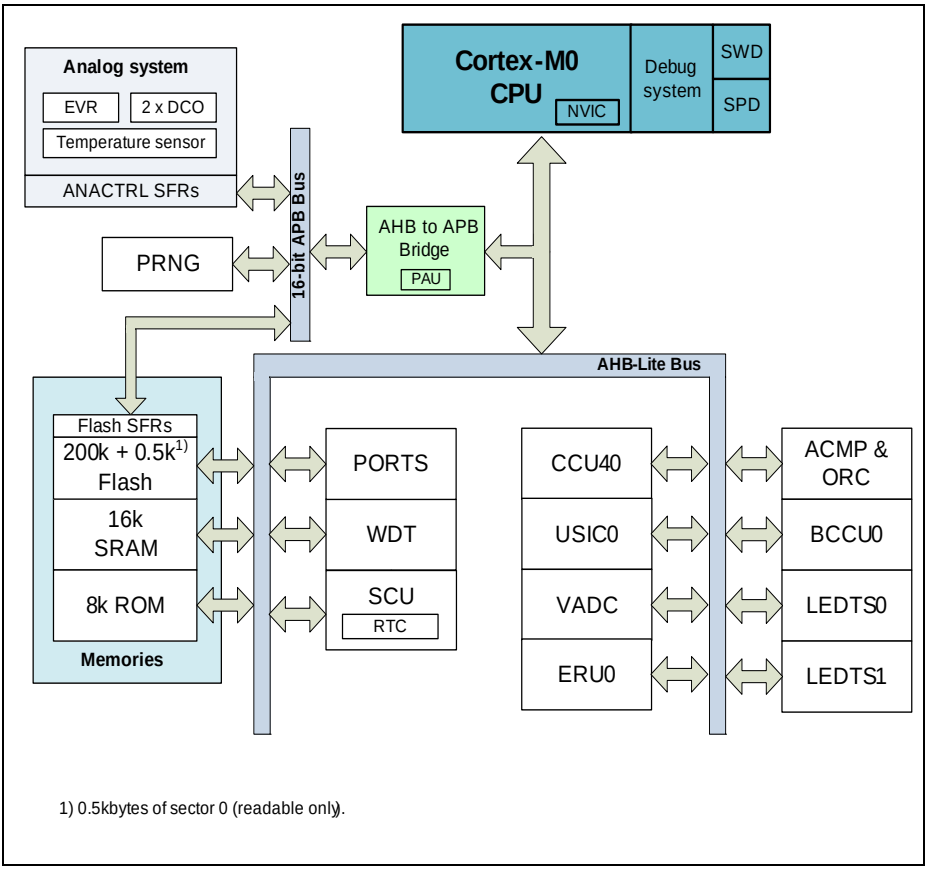


Figure 1 System Block Diagram

CPU Subsystem

- CPU Core
  - High-performance 32-bit ARM Cortex-M0 CPU
  - Most 16-bit Thumb and subset of 32-bit Thumb2 instruction set
  - Single cycle 32-bit hardware multiplier

Table 3 ADC Channels [1)]

Package	VADC0 G0	VADC0 G1
PG-TSSOP-16	CH0..CH5	CH0..CH4
PG-TSSOP-28	CH0..CH7	CH0 .. CH4, CH7
PG-TSSOP-38	CH0..CH7	CH0..CH7
PG-VQFN-24	CH0..CH7	CH0..CH4
PG-VQFN-40	CH0..CH7	CH1, CH5 .. CH7

1) Some pins in a package may be connected to more than one channel. For the detailed mapping see the Port I/O Function table.

1.4 Chip Identification Number

The Chip Identification Number allows software to identify the marking. It is a 8 words value with the most significant 7 words stored in Flash configuration sector 0 (CS0) at address location : 1000 0F00$_H$ (MSB) - 1000 0F1B$_H$ (LSB). The least significant word and most significant word of the Chip Identification Number are the value of registers DBGROMID and IDCHIP, respectively.

Table 4 XMC1200 Chip Identification Number

Derivative	Value	Marking
XMC1201-T028F0016	00012022 01CF00FF 00001FF7 00006000 00000C00 00001000 00005000 201ED083$_H$	AB
XMC1201-T028F0032	00012022 01CF00FF 00001FF7 00006000 00000C00 00001000 00009000 201ED083$_H$	AB
XMC1201-T038F0016	00012012 01CF00FF 00001FF7 00006000 00000C00 00001000 00005000 201ED083$_H$	AB
XMC1201-T038F0032	00012012 01CF00FF 00001FF7 00006000 00000C00 00001000 00009000 201ED083$_H$	AB
XMC1201-T038F0064	00012012 01CF00FF 00001FF7 00006000 00000C00 00001000 00011000 201ED083$_H$	AB
XMC1201-T038F0128	00012012 01CF00FF 00001FF7 00006000 00000C00 00001000 00021000 201ED083$_H$	AB
XMC1201-T038F0200	00012012 01CF00FF 00001FF7 00006000 00000C00 00001000 00033000 201ED083$_H$	AB
XMC1200-T038F0200	00012012 01CF00FF 00001FF7 0000E000 00000C00 00001000 00033000 201ED083$_H$	AB

Table 4 XMC1200 Chip Identification Number (cont'd)

Derivative	Value	Marking
XMC1202-T028X0016	00012023 01CF00FF 00001FF7 00008000 00000C00 00001000 00005000 201ED083$_H$	AB
XMC1202-T028X0032	00012023 01CF00FF 00001FF7 00008000 00000C00 00001000 00009000 201ED083$_H$	AB
XMC1202-T028X0064	00012023 01CF00FF 00001FF7 00008000 00000C00 00001000 00011000 201ED083$_H$	AB
XMC1202-T016X0016	00012033 01CF00FF 00001FF7 00008000 00000C00 00001000 00005000 201ED083$_H$	AB
XMC1202-T016X0032	00012033 01CF00FF 00001FF7 00008000 00000C00 00001000 00009000 201ED083$_H$	AB
XMC1202-T016X0064	00012033 01CF00FF 00001FF7 00008000 00000C00 00001000 00011000 201ED083$_H$	AB
XMC1202-Q024X0016	00012063 01CF00FF 00001FF7 00008000 00000C00 00001000 00005000 201ED083$_H$	AB
XMC1202-Q024X0032	00012063 01CF00FF 00001FF7 00008000 00000C00 00001000 00009000 201ED083$_H$	AB
XMC1201-Q040F0016	00012042 01CF00FF 00001FF7 00006000 00000C00 00001000 00005000 201ED083$_H$	AB
XMC1201-Q040F0032	00012042 01CF00FF 00001FF7 00006000 00000C00 00001000 00009000 201ED083$_H$	AB
XMC1201-Q040F0064	00012042 01CF00FF 00001FF7 00006000 00000C00 00001000 00011000 201ED083$_H$	AB
XMC1201-Q040F0128	00012042 01CF00FF 00001FF7 00006000 00000C00 00001000 00021000 201ED083$_H$	AB
XMC1201-Q040F0200	00012042 01CF00FF 00001FF7 00006000 00000C00 00001000 00033000 201ED083$_H$	AB
XMC1202-Q040X0016	00012043 01CF00FF 00001FF7 00008000 00000C00 00001000 00005000 201ED083$_H$	AB
XMC1202-Q040X0032	00012043 01CF00FF 00001FF7 00008000 00000C00 00001000 00009000 201ED083$_H$	AB

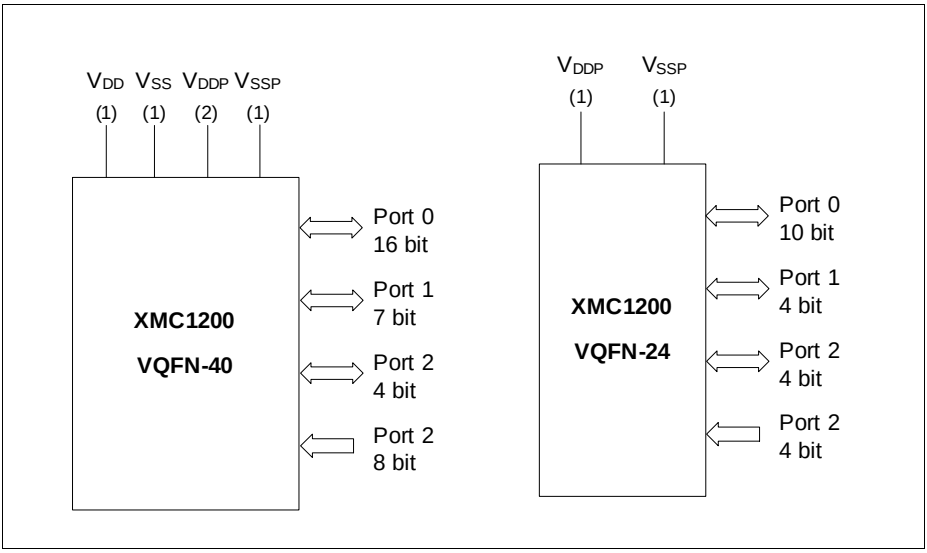


Figure 3 XMC1200 Logic Symbol for VQFN-24 and VQFN-40

Table 6 Package Pin Mapping (cont'd)

Function	VQFN 40	TSSOP 38	TSSOP 28	VQFN 24	TSSOP 16	Pad Type	Notes
VSSP	31	25	-	-	-	Power	I/O port ground
VDDP	32	26	-	-	-	Power	I/O port supply
VSSP	Exp. Pad	-	-	Exp. Pad	-	Power	**Exposed Die Pad** The exposed die pad is connected internally to VSSP. For proper operation, it is mandatory to connect the exposed pad to the board ground. For thermal aspects, please refer to the Package and Reliability chapter.

2.2.3 Hardware Controlled I/O Function Description

The following general building block is used to describe the hardware I/O and pull control functions of each PORT pin:

Table 8 Hardware Controlled I/O Function Description

Function	Outputs	Inputs	Pull Control	
	HWO0	**HWI0**	**HW0_PD**	**HW0_PU**
P0.0	MODB.OUT	MODB.INA		
Pn.y			$\overline{\text{MODC.OUT}}$	MODC.OUT

By Pn_HWSEL, it is possible to select between different hardware “masters” (HWO0/HWI0, HWO1/HWI1). The selected peripheral can take control of the pin(s). Hardware control overrules settings in the respective port pin registers. Additional hardware signals HW0_PD/HW1_PD and HW0_PU/HW1_PU controlled by the peripherals can be used to control the pull devices of the pin.

Please refer to the **Hardware Controlled I/O Functions** table for the complete hardware I/O and pull control function mapping.

Table 10 Hardware Controlled I/O Functions

Function	Outputs		Inputs		Pull Control			
	HWO0	HWO1	HWI0	HWI1	HW0_PD	HW0_PU	HW1_PD	HW1_PU
P1.3		USIC0_CH0.DOUT3		USIC0_CH0.HWIN3	BCCU0.OUT5	BCCU0.OUT5		
P1.4					BCCU0.OUT6	BCCU0.OUT6		
P1.5					BCCU0.OUT7	BCCU0.OUT7		
P1.6					BCCU0.OUT8	BCCU0.OUT8		
P2.0					BCCU0.OUT1	BCCU0.OUT1		
P2.1					BCCU0.OUT6	BCCU0.OUT6		
P2.2					BCCU0.OUT0	BCCU0.OUT0	CCU40.OUT3	CCU40.OUT3
P2.3					ACMP2.OUT	ACMP2.OUT		
P2.4					BCCU0.OUT8	BCCU0.OUT8		
P2.5					ACMP1.OUT	ACMP1.OUT		
P2.6					BCCU0.OUT2	BCCU0.OUT2	CCU40.OUT3	CCU40.OUT3
P2.7					BCCU0.OUT8	BCCU0.OUT8	CCU40.OUT3	CCU40.OUT3
P2.8					BCCU0.OUT1	BCCU0.OUT1	CCU40.OUT2	CCU40.OUT2
P2.9					BCCU0.OUT7	BCCU0.OUT7	CCU40.OUT2	CCU40.OUT2
P2.10					BCCU0.OUT4	BCCU0.OUT4		
P2.11					BCCU0.OUT5	BCCU0.OUT5		

3 Electrical Parameter

This section provides the electrical parameter which are implementation-specific for the XMC1200.

3.1 General Parameters

3.1.1 Parameter Interpretation

The parameters listed in this section represent partly the characteristics of the XMC1200 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are indicated by the abbreviations in the “Symbol” column:

- **CC**
  Such parameters indicate **C**ontroller **C**haracteristics, which are distinctive feature of the XMC1200 and must be regarded for a system design.
- **SR**
  Such parameters indicate **S**ystem **R**equirements, which must be provided by the application system in which the XMC1200 is designed in.

Table 17 ADC Characteristics (Operating Conditions apply)[1] (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Maximum sample rate in 8-bit mode [3]	f_{C8} CC	–	–	f_{ADC} / 38.5	–	1 sample pending
		–	–	f_{ADC} / 54.5	–	2 samples pending
RMS noise [4]	EN_{RMS} CC	–	1.5	–	LSB 12	DC input, V_{DD} = 5.0 V, V_{AIN} = 2.5 V, 25°C
DNL error	EA_{DNL} CC	–	±2.0	–	LSB 12	
INL error	EA_{INL} CC	–	±4.0	–	LSB 12	
Gain error with external reference	EA_{GAIN} CC	–	±0.5	–	%	SHSCFG.AREF = 00_B (calibrated)
Gain error with internal reference [5]	EA_{GAIN} CC	–	±3.6	–	%	SHSCFG.AREF = $1X_B$ (calibrated), -40°C - 105°C
		–	±2.0	–	%	SHSCFG.AREF = $1X_B$ (calibrated), 0°C - 85°C
Offset error	EA_{OFF} CC	–	±8.0	–	mV	Calibrated, V_{DD} = 5.0 V

1) The parameters are defined for ADC clock frequency f_{SH} = 32MHz, SHSCFG.DIVS = 0000_B. Usage of any other frequencies may affect the ADC performance.

2) No pending samples assumed, excluding sampling time and calibration.

3) Includes synchronization and calibration (average of gain and offset calibration).

4) This parameter can also be defined as an SNR value: SNR[dB] = 20 × log(A_{MAXeff} / N_{RMS}).
With $A_{MAXeff} = 2^N / 2$, SNR[dB] = 20 × log (2048 / N_{RMS}) [N = 12].
N_{RMS} = 1.5 LSB12, therefore, equals SNR = 20 × log (2048 / 1.5) = 62.7 dB.

5) Includes error from the reference voltage.

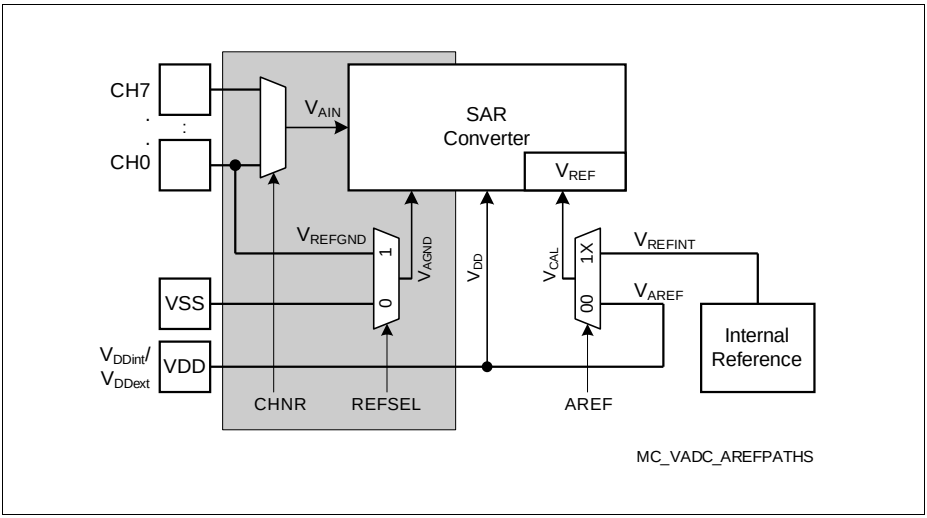


Figure 11 ADC Voltage Supply

3.2.3 Out of Range Comparator (ORC) Characteristics

The Out-of-Range Comparator (ORC) triggers on analog input voltages (V_{AIN}) above the V_{DDP} on selected input pins (ORCx.AIN) and generates a service request trigger (ORCx.OUT).

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 18 Out of Range Comparator (ORC) Characteristics (Operating Conditions apply; V_{DDP} = 3.0 V - 5.5 V; C_L = 0.25 pF)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
DC Switching Level	V_{ODC} C C		54	–	183	mV	$V_{AIN} \geq V_{DDP} + V_{ODC}$
Hysteresis	V_{OHYS}	CC	15	–	54	mV	
Always detected Overvoltage Pulse	t_{OPDD}	CC	103	–	–	ns	$V_{AIN} \geq V_{DDP}$ + 150 mV
			88	–	–	ns	$V_{AIN} \geq V_{DDP}$ + 350 mV
Never detected Overvoltage Pulse	t_{OPDN}	CC	–	–	21	ns	$V_{AIN} \geq V_{DDP}$ + 150 mV
			–	–	11	ns	$V_{AIN} \geq V_{DDP}$ + 350 mV
Detection Delay of a persistent Overvoltage	t_{ODD}	CC	39	–	132	ns	$V_{AIN} \geq V_{DDP}$ + 150 mV
			31	–	121	ns	$V_{AIN} \geq V_{DDP}$ + 350 mV
Release Delay	t_{ORD}	CC	44	–	240	ns	$V_{AIN} \leq V_{DDP}$; V_{DDP} = 5 V
			57	–	340	ns	$V_{AIN} \leq V_{DDP}$; V_{DDP} = 3.3 V
Enable Delay	t_{OED}	CC	–	–	300	ns	ORCCTRL.ENORCx = 1

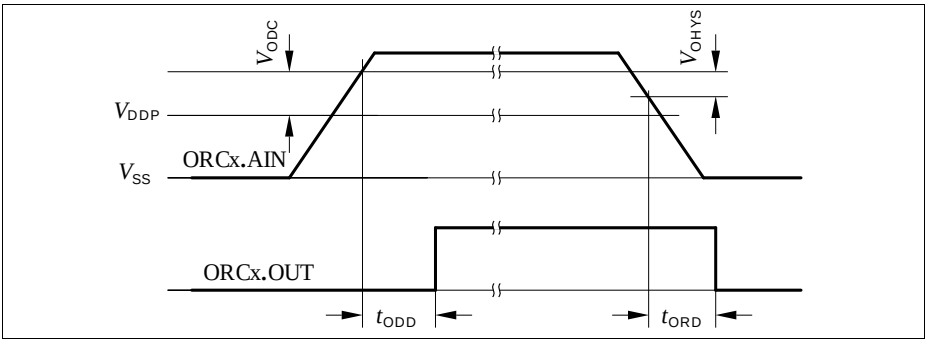


Figure 12 ORCx.OUT Trigger Generation

3.2.4 Analog Comparator Characteristics

Table 19 below shows the Analog Comparator characteristics.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 19 Analog Comparator Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Notes/ Test Conditions
			Min.	Typ.	Max.		
Input Voltage	V_{CMP}	SR	-0.05	–	V_{DDP} + 0.05	V	
Input Offset	V_{CMPOFF}	CC	–	+/-3	–	mV	High power mode ΔV_{CMP} < 200 mV
			–	+/-20	–	mV	Low power mode ΔV_{CMP} < 200 mV
Propagation Delay[1)]	t_{PDELAY}	CC	–	25	–	ns	High power mode, ΔV_{CMP} = 100 mV
			–	80	–	ns	High power mode, ΔV_{CMP} = 25 mV
			–	250	–	ns	Low power mode, ΔV_{CMP} = 100 mV
			–	700	–	ns	Low power mode, ΔV_{CMP} = 25 mV
Current Consumption	I_{ACMP}	CC	–	100	–	µA	First active ACMP in high power mode, ΔV_{CMP} > 30 mV
			–	66	–	µA	Each additional ACMP in high power mode, ΔV_{CMP} > 30 mV
			–	10	–	µA	First active ACMP in low power mode
			–	6	–	µA	Each additional ACMP in low power mode
Input Hysteresis	V_{HYS}	CC	–	+/-15	–	mV	
Filter Delay[1)]	t_{FDELAY}	CC	–	5	–	ns	

1) Total Analog Comparator Delay is the sum of Propagation Delay and Filter Delay.

3.2.6 Power Supply Current

The total power supply current defined below consists of a leakage and a switching component.

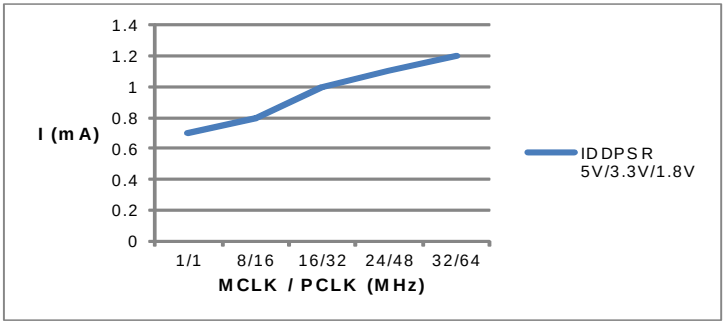
Application relevant values are typically lower than those given in the following tables, and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 21 Power Supply Parameters; V_{DDP} = 5V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.[1]	Max.		
Active mode current Peripherals enabled f_{MCLK} / f_{PCLK} in MHz[2]	I_{DDPAE} CC	–	8.8	11.5	mA	32 / 64
		–	7.7	–	mA	24 / 48
		–	6.4	–	mA	16 / 32
		–	5.3	–	mA	8 / 16
		–	3.9	–	mA	1 / 1
Active mode current Peripherals disabled f_{MCLK} / f_{PCLK} in MHz[3]	I_{DDPAD} CC	–	4.8	–	mA	32 / 64
		–	4.1	–	mA	24 / 48
		–	3.3	–	mA	16 / 32
		–	2.6	–	mA	8 / 16
		–	1.5	–	mA	1 / 1
Active mode current Code execution from RAM Flash is powered down f_{MCLK} / f_{PCLK} in MHz	I_{DDPAR} CC	–	6.7	–	mA	32 / 64
		–	5.8	–	mA	24 / 48
		–	4.9	–	mA	16 / 32
		–	4.0	–	mA	8 / 16
		–	3.1	–	mA	1 / 1
Sleep mode current Peripherals clock enabled f_{MCLK} / f_{PCLK} in MHz[4]	I_{DDPSE} CC	–	6.2	–	mA	32 / 64
			5.6	–	mA	24 / 48
			5.0	–	mA	16 / 32
			4.4	–	mA	8 / 16
			3.7	–	mA	1 / 1

Figure 15 shows typical graphs for sleep mode current for V_{DDP} = 5V, V_{DDP} = 3.3V, V_{DDP} = 1.8V across different clock frequencies.



Condition:
1. TA = +25° C

Figure 15 Sleep mode, peripherals clocks disabled, Flash powered down: Supply current I_{DDPSR} over supply voltage V_{DDP} for different clock frequencies

3.3.3 On-Chip Oscillator Characteristics

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 25 provides the characteristics of the 64 MHz clock output from the digital controlled oscillator, DCO1 in XMC1200.

Table 25 64 MHz DCO1 Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Nominal frequency	f_{NOM}	CC	–	64	–	MHz	under nominal conditions[1] after trimming
Accuracy[2]	Δf_{LT}	CC	-1.7	–	3.4	%	with respect to f_{NOM}(typ), over temperature (0 °C to 85 °C)
			-3.9	–	4.0	%	with respect to f_{NOM}(typ), over temperature (-40 °C to 105 °C)

1) The deviation is relative to the factory trimmed frequency at nominal V_{DDC} and T_A = + 25 °C.

2) The accuracy of the DCO1 oscillator can be further improved through alternative methods, refer to XMC1000 Oscillator Handling Application Note.

Figure 20 shows the typical curves for the accuracy of DCO1, with and without calibration based on temperature sensor, respectively.

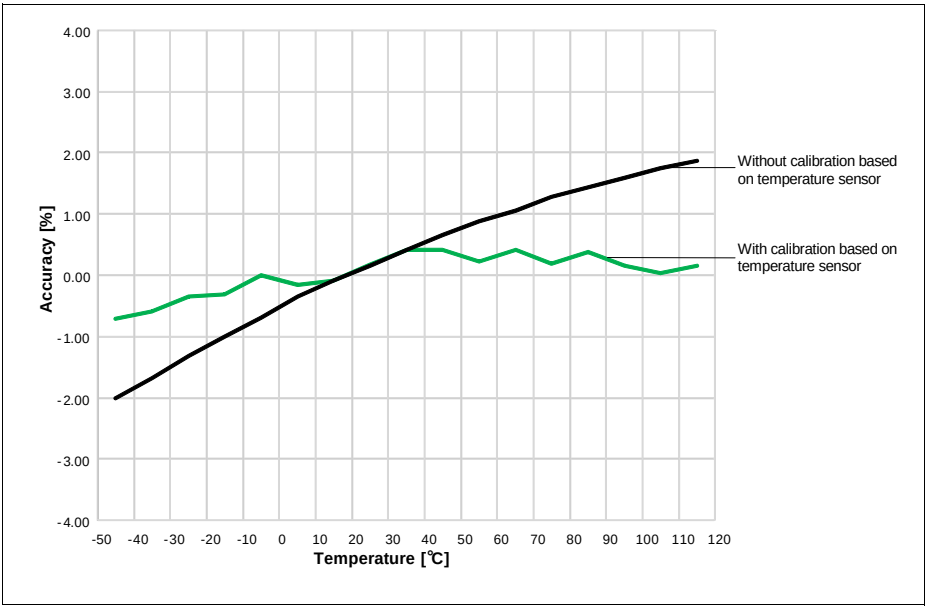


Figure 20 Typical DCO1 accuracy over temperature

Table 26 provides the characteristics of the 32 kHz clock output from digital controlled oscillators, DCO2 in XMC1200.

Table 26 32 kHz DCO2 Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Nominal frequency	f_{NOM}	CC	–	32.75	–	kHz	under nominal conditions[1] after trimming
Accuracy	Δf_{LT}	CC	-1.7	–	3.4	%	with respect to f_{NOM}(typ), over temperature (0 °C to 85 °C)
			-3.9	–	4.0	%	with respect to f_{NOM}(typ), over temperature (-40 °C to 105 °C)

1) The deviation is relative to the factory trimmed frequency at nominal V_{DDC} and T_A = + 25 °C.

3.3.6 Peripheral Timings

Note: These parameters are not subject to production test, but verified by design and/or characterization.

3.3.6.1 Synchronous Serial Interface (USIC SSC) Timing

The following parameters are applicable for a USIC channel operated in SSC mode.

Note: Operating Conditions apply.

Table 29 USIC SSC Master Mode Timing

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
SCLKOUT master clock period	t_{CLK}	CC	62.5	–	–	ns	
Slave select output SELO active to first SCLKOUT transmit edge	t_1	CC	80	–	–	ns	
Slave select output SELO inactive after last SCLKOUT receive edge	t_2	CC	0	–	–	ns	
Data output DOUT[3:0] valid time	t_3	CC	-10	–	10	ns	
Receive data input DX0/DX[5:3] setup time to SCLKOUT receive edge	t_4	SR	80	–	–	ns	
Data input DX0/DX[5:3] hold time from SCLKOUT receive edge	t_5	SR	0	–	–	ns	

3.3.6.2 Inter-IC (IIC) Interface Timing

The following parameters are applicable for a USIC channel operated in IIC mode.

Note: Operating Conditions apply.

Table 31 USIC IIC Standard Mode Timing[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	-	-	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	-	-	1000	ns	
Data hold time	t_3 CC/SR	0	-	-	µs	
Data set-up time	t_4 CC/SR	250	-	-	ns	
LOW period of SCL clock	t_5 CC/SR	4.7	-	-	µs	
HIGH period of SCL clock	t_6 CC/SR	4.0	-	-	µs	
Hold time for (repeated) START condition	t_7 CC/SR	4.0	-	-	µs	
Set-up time for repeated START condition	t_8 CC/SR	4.7	-	-	µs	
Set-up time for STOP condition	t_9 CC/SR	4.0	-	-	µs	
Bus free time between a STOP and START condition	t_{10} CC/SR	4.7	-	-	µs	
Capacitive load for each bus line	C_b SR	-	-	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximalely 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

The difference between junction temperature and ambient temperature is determined by $\Delta T = (P_{INT} + P_{IOSTAT} + P_{IODYN}) \times R_{\Theta JA}$

The internal power consumption is defined as
$P_{INT} = V_{DDP} \times I_{DDP}$ (switching current and leakage current).

The static external power consumption caused by the output drivers is defined as
$P_{IOSTAT} = \Sigma((V_{DDP}-V_{OH}) \times I_{OH}) + \Sigma(V_{OL} \times I_{OL})$

The dynamic external power consumption caused by the output drivers (P_{IODYN}) depends on the capacitive load connected to the respective pins and their switching frequencies.

If the total power dissipation for a given system configuration exceeds the defined limit, countermeasures must be taken to ensure proper system operation:

- Reduce V_{DDP}, if possible in the system
- Reduce the system frequency
- Reduce the number of output pins
- Reduce the load on active output drivers