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### Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

### Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

#### Details

Product Status	Obsolete
Core Processor	Z80
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	8MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/zilog/z84c0008fec">https://www.e-xfl.com/product-detail/zilog/z84c0008fec</a>

address. This flexibility in selecting the interrupt service routine address allows the peripheral device to use several different types of service routines. These routines may be located at any available location in memory. Since the interrupting device supplies the low-order byte of the 2-byte vector, bit 0 ( $A_0$ ) must be a zero.

**Interrupt Enable/Disable Operation.** Two flip-flops, IFF<sub>1</sub> and IFF<sub>2</sub>, referred to in the register description, are used to signal the CPU interrupt status. Operation of the two flip-flops is described in Table 2. For more details, refer to the *Z80 CPU Technical Manual* (03-0029-01) and *Z80 Assembly Language Programming Manual* (03-0002-01).

Table 2. State of Flip-Flops

Action	IFF <sub>1</sub>	IFF <sub>2</sub>	Comments
CPU Reset	0	0	Maskable interrupt INT disabled
DI instruction execution	0	0	Maskable interrupt INT disabled
EI instruction execution	1	1	Maskable interrupt INT enabled
LD A,I instruction execution	•	•	IFF <sub>2</sub> → Parity flag
LD A,R instruction execution	•	•	IFF <sub>2</sub> → Parity flag
Accept NMI	0	•	Maskable interrupt INT disabled
RETN instruction execution	IFF <sub>2</sub>	•	IFF <sub>2</sub> → IFF <sub>1</sub> at completion of an NMI service routine.

## INSTRUCTION SET

The microprocessor has one of the most powerful and versatile instruction sets available in any 8-bit microprocessor. It includes such unique operations as a block move for fast, efficient data transfers within memory, or between memory and I/O. It also allows operations on any bit in any location in memory.

The following is a summary of the instruction set which shows the assembly language mnemonic, the operation, the flag status, and gives comments on each instruction. For an explanation of flag notations and symbols for mnemonic tables, see the Symbolic Notations section which follows these tables. The *Z80 CPU Technical Manual* (03-0029-01), the *Programmer's Reference Guide* (03-0012-03), and *Assembly Language Programming Manual* (03-0002-01) contain significantly more details for programming use.

The instructions are divided into the following categories:

- ☐ 8-bit loads
- ☐ 16-bit loads
- ☐ Exchanges, block transfers, and searches
- ☐ 8-bit arithmetic and logic operations
- ☐ General-purpose arithmetic and CPU control
- ☐ 16-bit arithmetic operations
- ☐ Rotates and shifts

- ☐ Bit set, reset, and test operations
- ☐ Jumps
- ☐ Calls, returns, and restarts
- ☐ Input and output operations

A variety of addressing modes are implemented to permit efficient and fast data transfer between various registers, memory locations, and input/output devices. These addressing modes include:

- ☐ Immediate
- ☐ Immediate extended
- ☐ Modified page zero
- ☐ Relative
- ☐ Extended
- ☐ Indexed
- ☐ Register
- ☐ Register indirect
- ☐ Implied
- ☐ Bit

## 8-BIT LOAD GROUP

Mnemonic	Symbolic Operation	S	Z	Flags H	P/V	N	C	76	543	210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments	
LD r, r'	$r \leftarrow r'$	•	•	X	•	X	•	•	01	r	r'	1	1	4	r, r' Reg.	
LD r, n	$r \leftarrow n$	•	•	X	•	X	•	•	00	r	110	2	2	7	000 B	
										$\leftarrow n \rightarrow$					001 C	
LD r, (HL)	$r \leftarrow (HL)$	•	•	X	•	X	•	•	01	r	110	1	2	7	010 D	
LD r, (IX+d)	$r \leftarrow (IX+d)$	•	•	X	•	X	•	•	11	011	101	DD	3	5	19	011 E
										01	r	110				100 H
										$\leftarrow d \rightarrow$						101 L
LD r, (IY+d)	$r \leftarrow (IY+d)$	•	•	X	•	X	•	•	11	111	101	FD	3	5	19	111 A
										01	r	110				
										$\leftarrow d \rightarrow$						
LD (HL), r	$(HL) \leftarrow r$	•	•	X	•	X	•	•	01	110	r	1	2	7		
LD (IX+d), r	$(IX+d) \leftarrow r$	•	•	X	•	X	•	•	11	011	101	DD	3	5	19	
										01	110	r				
										$\leftarrow d \rightarrow$						
LD (IY+d), r	$(IY+d) \leftarrow r$	•	•	X	•	X	•	•	11	111	101	FD	3	5	19	
										01	110	r				
										$\leftarrow d \rightarrow$						
LD (HL), n	$(HL) \leftarrow n$	•	•	X	•	X	•	•	00	110	110	36	2	3	10	
										$\leftarrow n \rightarrow$						
LD (IX+d), n	$(IX+d) \leftarrow n$	•	•	X	•	X	•	•	11	011	101	DD	4	5	19	
										00	110	110	36			
										$\leftarrow d \rightarrow$						
										$\leftarrow n \rightarrow$						

# 16-BIT LOAD GROUP (Continued)

Mnemonic	Symbolic Operation	S	Z	Flags H	P/V	N	C	76	543	210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
LD IX, (nn)	$IX_H \leftarrow (nn+1)$ $IX_L \leftarrow (nn)$	•	•	X	•	X	•	•	11	011 101	DD	4	6	20	
									00	101 010	2A				
									$\leftarrow n \rightarrow$						
									$\leftarrow n \rightarrow$						
LD IY, (nn)	$IY_H \leftarrow (nn+1)$ $IY_L \leftarrow (nn)$	•	•	X	•	X	•	•	11	111 101	FD	4	6	20	
									00	101 010	2A				
									$\leftarrow n \rightarrow$						
									$\leftarrow n \rightarrow$						
LD (nn), HL	$(nn+1) \leftarrow H$ $(nn) \leftarrow L$	•	•	X	•	X	•	•	00	100 010	22	3	5	16	
									$\leftarrow n \rightarrow$						
									$\leftarrow n \rightarrow$						
LD (nn), dd	$(nn+1) \leftarrow dd_H$ $(nn) \leftarrow dd_L$	•	•	X	•	X	•	•	11	101 101	ED	4	6	20	
									01	dd0 011					
									$\leftarrow n \rightarrow$						
									$\leftarrow n \rightarrow$						
LD (nn), IX	$(nn+1) \leftarrow IX_H$ $(nn) \leftarrow IX_L$	•	•	X	•	X	•	•	11	011 101	DD	4	6	20	
									00	100 010	22				
									$\leftarrow n \rightarrow$						
									$\leftarrow n \rightarrow$						
LD (nn), IY	$(nn+1) \leftarrow IY_H$ $(nn) \leftarrow IY_L$	•	•	X	•	X	•	•	11	111 101	FD	4	6	20	
									00	100 010	22				
									$\leftarrow n \rightarrow$						
									$\leftarrow n \rightarrow$						
LD SP, HL	$SP \leftarrow HL$	•	•	X	•	X	•	•	11	111 001	F9	1	1	6	
LD SP, IX	$SP \leftarrow IX$	•	•	X	•	X	•	•	11	011 101	DD	2	2	10	
									11	111 001	F9				
LD SP, IY	$SP \leftarrow IY$	•	•	X	•	X	•	•	11	111 101	FD	2	2	10	
									11	111 001	F9				
PUSH qq	$(SP-2) \leftarrow qq_L$ $(SP-1) \leftarrow qq_H$ $SP \rightarrow SP-2$	•	•	X	•	X	•	•	11	qq0 101		1	3	11	qq BC
															01 DE
															10 HL
PUSH IX	$(SP-2) \leftarrow IX_L$ $(SP-1) \leftarrow IX_H$ $SP \rightarrow SP-2$	•	•	X	•	X	•	•	11	011 101	DD	2	4	15	11 AF
									11	100 101	E5				
PUSH IY	$(SP-2) \leftarrow IY_L$ $(SP-1) \leftarrow IY_H$ $SP \rightarrow SP-2$	•	•	X	•	X	•	•	11	111 101	FD	2	4	15	
									11	100 101	E5				
POP qq	$qq_H \leftarrow (SP+1)$ $qq_L \leftarrow (SP)$ $SP \rightarrow SP+2$	•	•	X	•	X	•	•	11	qq0 001		1	3	10	
POP IX	$IX_H \leftarrow (SP+1)$ $IX_L \leftarrow (SP)$ $SP \rightarrow SP+2$	•	•	X	•	X	•	•	11	011 101	DD	2	4	14	
									11	100 001	E1				
POP IY	$IY_H \leftarrow (SP+1)$ $IY_L \leftarrow (SP)$ $SP \rightarrow SP+2$	•	•	X	•	X	•	•	11	111 101	FD	2	4	14	
									11	100 001	E1				

NOTE: (PAIR)<sub>H</sub>, (PAIR)<sub>L</sub> refer to high order and low order eight bits of the register pair respectively, e.g., BC<sub>L</sub> = C, AF<sub>H</sub> = A.

## EXCHANGE, BLOCK TRANSFER, BLOCK SEARCH GROUPS (Continued)

Mnemonic	Symbolic Operation	S	Z	Flags H	P/V	N	C	76	543	210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
CPIR	A ← (HL)	†	†	X	†	X	†	1	•	11 101 101	ED	2	5	21	If BC ≠ 0 and A ≠ (HL)
	HL ← HL + 1									10 110 001	B1	2	4	16	If BC = 0 or A = (HL)
	BC ← BC - 1														
	Repeat until A = (HL) or BC = 0														
CPD	A ← (HL)	†	†	X	†	X	†	1	•	11 101 101	ED	2	4	16	
	HL ← HL - 1									10 101 001	A9				
	BC ← BC - 1														
CPDR	A ← (HL)	†	†	X	†	X	†	1	•	11 101 101	ED	2	5	21	If BC ≠ 0 and A ≠ (HL)
	HL ← HL - 1									10 111 001	B9	2	4	16	If BC = 0 or A = (HL)
	BC ← BC - 1														
	Repeat until A = (HL) or BC = 0														

NOTE: ① P/V flag is 0 if the result of BC - 1 = 0, otherwise P/V = 1.  
 ② P/V flag is 0 only at completion of instruction.  
 ③ Z flag is 1 if A = (HL), otherwise Z = 0.

## 8-BIT ARITHMETIC AND LOGICAL GROUP

Mnemonic	Symbolic Operation	S	Z	Flags H	P/V	N	C	76	Opcode 543	210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
ADD A, r	A ← A + r	†	†	X	†	X	V	0	†	10 [000] r		1	1	4	r Reg.
ADD A, n	A ← A + n	†	†	X	†	X	V	0	†	11 [000]	110	2	2	7	000 B
										← n →					001 C
															010 D
ADD A, (HL)	A ← A + (HL)	†	†	X	†	X	V	0	†	10 [000]	110	1	2	7	011 E
ADD A, (IX + d)	A ← A + (IX + d)	†	†	X	†	X	V	0	†	11 011 101	DD	3	5	19	100 H
										10 [000]	110				101 L
										← d →					111 A
ADD A, (IY + d)	A ← A + (IY + d)	†	†	X	†	X	V	0	†	11 111 101	FD	3	5	19	
										10 [000]	110				
										← d →					
ADC A, s	A ← A + s + CY	†	†	X	†	X	V	0	†	[001]					s is any of r, n, (HL), (IX + d), (IY + d) as shown for ADD instruction. The indicated bits replace the [000] in the ADD set above.
SUB s	A ← A - s	†	†	X	†	X	V	1	†	[010]					
SBC A, s	A ← A - s - CY	†	†	X	†	X	V	1	†	[011]					
AND s	A ← A > s	†	†	X	1	X	P	0	0	[100]					
OR s	A ← A > s	†	†	X	0	X	P	0	0	[110]					
XOR s	A ← A ⊕ s	†	†	X	0	X	P	0	0	[101]					
CP s	A ← s	†	†	X	†	X	V	1	†	[111]					

## 8-BIT ARITHMETIC AND LOGICAL GROUP (Continued)

Mnemonic	Symbolic Operation	S	Z	Flags H	P/V	N	C	Opcode 76 543 210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
INC r	$r \leftarrow r + 1$	†	†	X	†	X	V 0 •	00 r 100		1	1	4	
INC (HL)	(HL) $\leftarrow$ (HL) + 1	†	†	X	†	X	V 0 •	00 110 100		1	3	11	
INC (IX+d)	(IX+d) $\leftarrow$ (IX+d) + 1	†	†	X	†	X	V 0 •	11 011 101 DD 00 110 100		3	6	23	
								$\leftarrow d \rightarrow$					
INC (IY+d)	(IY+d) $\leftarrow$ (IY+d) + 1	†	†	X	†	X	V 0 •	11 111 101 FD 00 110 100		3	6	23	
								$\leftarrow d \rightarrow$					
DEC m	$m \leftarrow m - 1$	†	†	X	†	X	V 1 •	101					

NOTE: m is any of r, (HL), (IX+d), (IY+d) as shown for INC. DEC same format and states as INC. Replace 100 with 101 in opcode.

## GENERAL-PURPOSE ARITHMETIC AND CPU CONTROL GROUPS

Mnemonic	Symbolic Operation	S	Z	Flags H	P/V	N	C	Opcode 76 543 210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
DAA	@	†	†	X	†	X	P • †	00 100 111 27		1	1	4	Decimal adjust accumulator
CPL	$A \leftarrow A$	•	•	X	1	X	• 1 •	00 101 111 2F		1	1	4	Complement accumulator (one's complement)
NEG	$A \leftarrow 0 - A$	†	†	X	†	X	V 1 †	11 101 101 ED 01 000 100 44		2	2	8	Negate acc. (two's complement)
CCF	$CY \leftarrow CY$	•	•	X	X	X	• 0 †	00 111 111 3F		1	1	4	Complement carry flag
SCF	$CY \leftarrow 1$	•	•	X	0	X	• 0 1	00 110 111 37		1	1	4	Set carry flag
NOP	No operation	•	•	X	•	X	• • •	00 000 000 00		1	1	4	
HALT	CPU halted	•	•	X	•	X	• • •	01 110 110 76		1	1	4	
DI ★	$IFF \leftarrow 0$	•	•	X	•	X	• • •	11 110 011 F3		1	1	4	
EI ★	$IFF \leftarrow 1$	•	•	X	•	X	• • •	11 111 011 FB		1	1	4	
IM 0	Set interrupt mode 0	•	•	X	•	X	• • •	11 101 101 ED 01 000 110 46		2	2	8	
IM 1	Set interrupt mode 1	•	•	X	•	X	• • •	11 101 101 ED 01 010 110 56		2	2	8	
IM 2	Set interrupt mode 2	•	•	X	•	X	• • •	11 101 101 ED 01 011 110 5E		2	2	8	

NOTES: @ converts accumulator content into packed BCD following add or subtract with packed BCD operands.

IFF indicates the interrupt enable flip-flop.


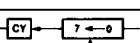
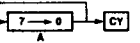
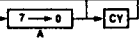
CY indicates the carry flip-flop.

★ indicates interrupts are not sampled at the end of EI or DI.

## 16-BIT ARITHMETIC GROUP

Mnemonic	Symbolic Operation	S	Z	Flags				Opcode				No. of		No. of M		No. of T		Comments		
				H	P/V	N	C	76	543	210	Hex	Bytes	Cycles	States						
ADD HL, ss	HL ← HL + ss	•	•	X	X	X	•	0	‡	00	ssl	001	1	3	11	ss	Reg.			
																00	BC			
ADC HL, ss	HL ←															01	DE			
	HL + ss + CY	‡	‡	X	X	X	V	0	‡	11	101	101	ED	2	4	15	10	HL		
										01	ss1	010				11	SP			
SBC HL, ss	HL ←																			
	HL - ss - CY	‡	‡	X	X	X	V	1	‡	11	101	101	ED	2	4	15				
										01	ss0	010								
ADD IX, pp	IX ← IX + pp	•	•	X	X	X	•	0	‡	11	011	101	DD	2	4	15	pp	Reg.		
										01	pp1	001				00	BC			
																01	DE			
																10	IX			
																11	SP			
ADD IY, rr	IY ← IY + rr	•	•	X	X	X	•	0	‡	11	111	101	FD	2	4	15	rr	Reg.		
										00	rr1	001				00	BC			
INC ss	ss ← ss + 1	•	•	X	•	X	•	•	•	00	ss0	011	1	1	6	01	DE			
INC IX	IX ← IX + 1	•	•	X	•	X	•	•	•	11	011	101	DD	2	2	10	10	IY		
										00	100	011	23			11	SP			
INC IY	IY ← IY + 1	•	•	X	•	X	•	•	•	11	111	101	FD	2	2	10				
										00	100	011	23							
DEC ss	ss ← ss - 1	•	•	X	•	X	•	•	•	00	ss1	011	1	1	6					
DEC IX	IX ← IX - 1	•	•	X	•	X	•	•	•	11	011	101	DD	2	2	10				
										00	101	011	2B							
DEC IY	IY ← IY - 1	•	•	X	•	X	•	•	•	11	111	101	FD	2	2	10				
										00	101	011	2B							

## ROTATE AND SHIFT GROUP

Mnemonic	Symbolic Operation	Flags						Opcode				No. of Bytes	No. of M Cycles	No. of T States	Comments		
		S	Z	H	P/V	N	C	76	543	210	Hex						
RLCA		•	•	X	0	X	•	0	†	00	000	111	07	1	1	4	Rotate left circular accumulator.
RLA		•	•	X	0	X	•	0	†	00	010	111	17	1	1	4	Rotate left accumulator.
RRCA		•	•	X	0	X	•	0	†	00	001	111	0F	1	1	4	Rotate right circular accumulator.
RRA		•	•	X	0	X	•	0	†	00	011	111	1F	1	1	4	Rotate right accumulator.

## BIT SET, RESET AND TEST GROUP

Mnemonic	Symbolic Operation	S	Z	Flags				Opcode			Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
				H	P/V	N	C	76	543	210					
BIT b, r	$Z \leftarrow r_b$	X	†	X	1	X	X	0	•	11 001 011	CB	2	2	8	r Reg.
								01	b r						000 B
BIT b, (HL)	$Z \leftarrow (HL)_b$	X	†	X	1	X	X	0	•	11 001 011	CB	2	3	12	001 C
								01	b 110						010 D
BIT b, (IX+d) <sub>b</sub>	$Z \leftarrow (IX+d)_b$	X	†	X	1	X	X	0	•	11 011 101	DD	4	5	20	011 E
								11	001 011	CB					100 H
								$\leftarrow d \rightarrow$							101 L
								01	b 110						111 A
								b Bit Tested							
BIT b, (IY+d) <sub>b</sub>	$Z \leftarrow (IY+d)_b$	X	†	X	1	X	X	0	•	11 111 101	FD	4	5	20	000 0
								11	001 011	CB					001 1
								$\leftarrow d \rightarrow$							010 2
								01	b 110						011 3
SET b, r	$r_b \leftarrow 1$	•	•	X	•	X	•	•	•	11 001 011	CB	2	2	8	100 4
								11	b r						101 5
SET b, (HL)	$(HL)_b \leftarrow 1$	•	•	X	•	X	•	•	•	11 001 011	CB	2	4	15	110 6
								11	b 110						111 7
SET b, (IX+d)	$(IX+d)_b \leftarrow 1$	•	•	X	•	X	•	•	•	11 011 101	DD	4	6	23	
								11	001 011	CB					
								$\leftarrow d \rightarrow$							
								11	b 110						
SET b, (IY+d)	$(IY+d)_b \leftarrow 1$	•	•	X	•	X	•	•	•	11 111 101	FD	4	6	23	
								11	001 011	CB					
								$\leftarrow d \rightarrow$							
								11	b 110						
RES b, m	$m_b \leftarrow 0$	•	•	X	•	X	•	•	•	11 101 101	FD	4	6	23	
	$m \leftarrow r, (HL),$							11	b 110						
	$(IX+d), (IY+d)$							10							

To form new opcode replace 11 of SET b, s with 10. Flags and time states for SET instruction.

To form new opcode replace **11** of SET b, s with **10**. Flags and time states for SET instruction.

NOTE: The notation  $m_b$  indicates location m, bit b (0 to 7).

## JUMP GROUP

Mnemonic	Symbolic Operation	Flags					Opcode			Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments	
		S	Z	H	P/V/N	C	76	543	210						
JP nn	PC ← nn	•	•	X	•	X	•	•	•	11 000 011	C3	3	3	10	cc Condition 000 NZ (non-zero) 001 Z (zero)
JP cc, nn	If condition cc is true PC←nn, otherwise continue	•	•	X	•	X	•	•	•	11 cc 010		3	3	10	010 NC (non-carry)
										011 C (carry)					
										100 PO (parity odd)					
										101 PE (parity even)					
JR e	PC ← PC+e	•	•	X	•	X	•	•	•	00 011 000	18	2	3	12	110 P (sign positive) 111 M (sign negative)
JR C, e	If C=0, continue If C=1, PC←PC+e	•	•	X	•	X	•	•	•	00 111 000	38	2	2	7	If condition not met.
										←e-2→					
JR NC, e	If C=1, continue If C=0, PC←PC+e	•	•	X	•	X	•	•	•	00 110 000	30	2	2	7	If condition not met.
										←e-2→					
JP Z, e	If Z=0, continue If Z=1, PC←PC+e	•	•	X	•	X	•	•	•	00 101 000	28	2	2	7	If condition not met.
										←e-2→					
JR NZ, e	If Z=1, continue If Z=0, PC←PC+e	•	•	X	•	X	•	•	•	00 100 000	20	2	2	7	If condition not met.
										←e-2→					
JP (HL)	PC ← HL	•	•	X	•	X	•	•	•	11 101 001	E9	1	1	4	
JP (IX)	PC ← IX	•	•	X	•	X	•	•	•	11 011 101	DD	2	2	8	
										11 101 001					
JP (IY)	PC ← IY	•	•	X	•	X	•	•	•	11 111 101	FD	2	2	8	
										11 101 001					
DJNZ, e	B ← B - 1 If B=0, continue If B≠0, PC ← PC+e	•	•	X	•	X	•	•	•	00 010 000	10	2	2	8	If B=0
										←e-2→					
												2	3	13	If B≠0.

NOTES: e represents the extension in the relative addressing mode.

e is a signed two's complement number in the range < -126, 129 >.

e - 2 in the opcode provides an effective address of pc + e as PC is incremented by 2 prior to the addition of e.

## SUMMARY OF FLAG OPERATION

Instructions	D <sub>7</sub> S	Z	H	P/V	N	D <sub>0</sub> C	Comments
ADD A, s; ADC A, s	†	†	X	†	X	V 0	8-bit add or add with carry.
SUB s; SBC A, s; CP s; NEG	†	†	X	†	X	V 1	8-bit subtract, subtract with carry, compare and negate accumulator.
AND s	†	†	X	1	X	P 0 0	Logical operation.
OR s, XOR s	†	†	X	0	X	P 0 0	Logical operation.
INC s	†	†	X	†	X	V 0 •	8-bit increment.
DEC s	†	†	X	†	X	V 1 •	8-bit decrement.
ADD DD, ss	•	•	X	X	X	• 0 †	16-bit add.
ADC HL, ss	†	†	X	X	X	V 0 †	16-bit add with carry.
SBC HL, ss	†	†	X	X	X	V 1 †	16-bit subtract with carry.
RLA; RLCA; RRA; RRCA	•	•	X	0	X	• 0 †	Rotate accumulator.
RL m; RLC m; RR m; RRC m; SLA m; SRA m; SRL m	†	†	X	0	X	P 0 †	Rotate and shift locations.
RLD; RRD	†	†	X	0	X	P 0 •	Rotate digit left and right.
DAA	†	†	X	†	X	P • †	Decimal adjust accumulator.
CPL	•	•	X	1	X	• 1 •	Complement accumulator.
SCF	•	•	X	0	X	• 0 1	Set carry.
CCF	•	•	X	X	X	• 0 †	Complement carry.
IN r (C)	†	†	X	0	X	P 0 •	Input register indirect.
INI; IND; OUTI; OUTD	X	†	X	X	X	X 1 •	Block input and output. Z = 1 if B ≠ 0, otherwise Z = 0.
INIR; INDR; OTIR; OTDR	X	1	X	X	X	X 1 •	Block input and output. Z = 1 if B ≠ 0, otherwise Z = 0.
LDI; LDD	X	X	X	0	X	† 0 •	Block transfer instructions. P/V = 1 if BC ≠ 0, otherwise P/V = 0.
LDIR; LDDR	X	X	X	0	X	0 0 •	Block transfer instructions. P/V = 1 if BC ≠ 0, otherwise P/V = 0.
CPI; CPIR; CPD; CPDR	X	†	X	X	X	† 1 •	Block search instructions. Z = 1 if A = (HL), otherwise Z = 0. P/V = 1 if BC ≠ 0, otherwise P/V = 0.
LD A, I; LD A, R	†	†	X	0	X	IFF 0 •	IFF, the content of the interrupt enable flip-flop, (IFF <sub>2</sub> ), is copied into the P/V flag.
BIT b, s	X	†	X	1	X	X 0 •	The state of bit b of location s is copied into the Z flag.

## SYMBOLIC NOTATION

Symbol	Operation	Symbol	Operation
S	Sign flag. S = 1 if the MSB of the result is 1.	†	The flag is affected according to the result of the operation.
Z	Zero flag. Z = 1 if the result of the operation is 0.	•	The flag is unchanged by the operation.
P/V	Parity or overflow flag. Parity (P) and overflow (V) share the same flag. Logical operations affect this flag with the parity of the result while arithmetic operations affect this flag with the overflow of the result. If P/V holds parity: P/V = 1 if the result of the operation is even; P/V = 0 if result is odd. If P/V holds overflow, P/V = 1 if the result of the operation produced an overflow. If P/V does not hold overflow, P/V = 0.	0	The flag is reset by the operation.
H*	Half-carry flag. H = 1 if the add or subtract operation produced a carry into, or borrow from, bit 4 of the accumulator.	1	The flag is set by the operation.
N*	Add/Subtract flag. N = 1 if the previous operation was a subtract.	X	The flag is indeterminate.
C	Carry/Link flag. C = 1 if the operation produced a carry from the MSB of the operand or result.	V	P/V flag affected according to the overflow result of the operation.
		P	P/V flag affected according to the parity result of the operation.
		r	Any one of the CPU registers A, B, C, D, E, H, L.
		s	Any 8-bit location for all the addressing modes allowed for the particular instruction.
		ss	Any 16-bit location for all the addressing modes allowed for that instruction.
		ii	Any one of the two index registers IX or IY.
		R	Refresh counter.
		n	8-bit value in range < 0, 255 >.
		nn	16-bit value in range < 0, 65535 >.

\* H and N flags are used in conjunction with the decimal adjust instruction (DAA) to properly correct the result into packed BCD format following addition or subtraction using operands with packed BCD format.

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## PIN DESCRIPTIONS

**A<sub>0</sub>-A<sub>15</sub>.** *Address Bus* (output, active High, 3-state). A<sub>0</sub>-A<sub>15</sub> form a 16-bit address bus. The Address Bus provides the address for memory data bus exchanges (up to 64K bytes) and for I/O device exchanges.

**BUSACK.** *Bus Acknowledge* (output, active Low). Bus Acknowledge indicates to the requesting device that the CPU address bus, data bus, and control signals  $\overline{\text{MREQ}}$ ,  $\overline{\text{IORQ}}$ ,  $\overline{\text{RD}}$ , and  $\overline{\text{WR}}$  have entered their high-impedance states. The external circuitry can now control these lines.

**BUSREQ.** *Bus Request* (input, active Low). Bus Request has a higher priority than  $\overline{\text{NMI}}$  and is always recognized at the end of the current machine cycle.  $\overline{\text{BUSREQ}}$  forces the CPU address bus, data bus, and control signals  $\overline{\text{MREQ}}$ ,  $\overline{\text{IORQ}}$ ,  $\overline{\text{RD}}$ , and  $\overline{\text{WR}}$  to go to a high-impedance state so that other devices can control these lines.  $\overline{\text{BUSREQ}}$  is normally wired-OR and requires an external pullup for these applications. Extended  $\overline{\text{BUSREQ}}$  periods due to extensive DMA operations can prevent the CPU from properly refreshing dynamic RAMs.

**D<sub>0</sub>-D<sub>7</sub>.** *Data Bus* (input/output, active High, 3-state). D<sub>0</sub>-D<sub>7</sub> constitute an 8-bit bidirectional data bus, used for data exchanges with memory and I/O.

**HALT.** *Halt State* (output, active Low).  $\overline{\text{HALT}}$  indicates that the CPU has executed a Halt instruction and is awaiting either a nonmaskable or a maskable interrupt (with the mask enabled) before operation can resume. While halted, the CPU executes NOPs to maintain memory refresh.

**INT.** *Interrupt Request* (input, active Low). Interrupt Request is generated by I/O devices. The CPU honors a request at the end of the current instruction if the internal software-controlled interrupt enable flip-flop (IFF) is enabled.  $\overline{\text{INT}}$  is normally wired-OR and requires an external pullup for these applications.

**IORQ.** *Input/Output Request* (output, active Low, 3-state).  $\overline{\text{IORQ}}$  indicates that the lower half of the address bus holds a valid I/O address for an I/O read or write operation.  $\overline{\text{IORQ}}$  is also generated concurrently with  $\overline{\text{M1}}$  during an interrupt acknowledge cycle to indicate that an interrupt response vector can be placed on the data bus.

**M1.** *Machine Cycle One* (output, active Low).  $\overline{\text{M1}}$ , together with  $\overline{\text{MREQ}}$ , indicates that the current machine cycle is the opcode fetch cycle of an instruction execution.  $\overline{\text{M1}}$ , together with  $\overline{\text{IORQ}}$ , indicates an interrupt acknowledge cycle.

**MREQ.** *Memory Request* (output, active Low, 3-state).  $\overline{\text{MREQ}}$  indicates that the address bus holds a valid address for a memory read or memory write operation.

**NMI.** *Non-Maskable Interrupt* (input, negative edge-triggered).  $\overline{\text{NMI}}$  has a higher priority than  $\overline{\text{INT}}$ .  $\overline{\text{NMI}}$  is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop, and automatically forces the CPU to restart at location 0066H.

**RD.** *Read* (output, active Low, 3-state).  $\overline{\text{RD}}$  indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.

**RESET.** *Reset* (input, active Low).  $\overline{\text{RESET}}$  initializes the CPU as follows: it resets the interrupt enable flip-flop, clears the PC and Registers I and R, and sets the interrupt status to Mode 0. During reset time, the address and data bus go to a high-impedance state, and all control output signals go to the inactive state. Note that  $\overline{\text{RESET}}$  must be active for a minimum of three full clock cycles before the reset operation is complete.

**RFSH.** *Refresh* (output, active Low).  $\overline{\text{RFSH}}$ , together with  $\overline{\text{MREQ}}$ , indicates that the lower seven bits of the system's address bus can be used as a refresh address to the system's dynamic memories.

**WAIT.** *Wait* (input, active Low).  $\overline{\text{WAIT}}$  indicates to the CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter a Wait state as long as this signal is active. Extended  $\overline{\text{WAIT}}$  periods can prevent the CPU from properly refreshing dynamic memory.

**WR.** *Write* (output, active Low, 3-state).  $\overline{\text{WR}}$  indicates that the CPU data bus holds valid data to be stored at the addressed memory or I/O location.

## CPU TIMING

The Z80 CPU executes instructions by proceeding through a specific sequence of operations:

- Memory read or write
- I/O device read or write
- Interrupt acknowledge

The basic clock period is referred to as a T time or cycle, and three or more T cycles make up a machine cycle (M1, M2 or M3 for instance). Machine cycles can be extended either by the CPU automatically inserting one or more Wait states or by the insertion of one or more Wait states by the user.

**Instruction Opcode Fetch.** The CPU places the contents of the Program Counter (PC) on the address bus at the start of the cycle (Figure 5). Approximately one-half clock cycle later,  $\overline{\text{MREQ}}$  goes active. When active,  $\overline{\text{RD}}$  indicates that the memory data can be enabled onto the CPU data bus.

The CPU samples the  $\overline{\text{WAIT}}$  input with the falling edge of clock state T<sub>2</sub>. During clock states T<sub>3</sub> and T<sub>4</sub> of an M1 cycle, dynamic RAM refresh can occur while the CPU starts decoding and executing the instruction. When the Refresh Control signal becomes active, refreshing of dynamic memory can take place.

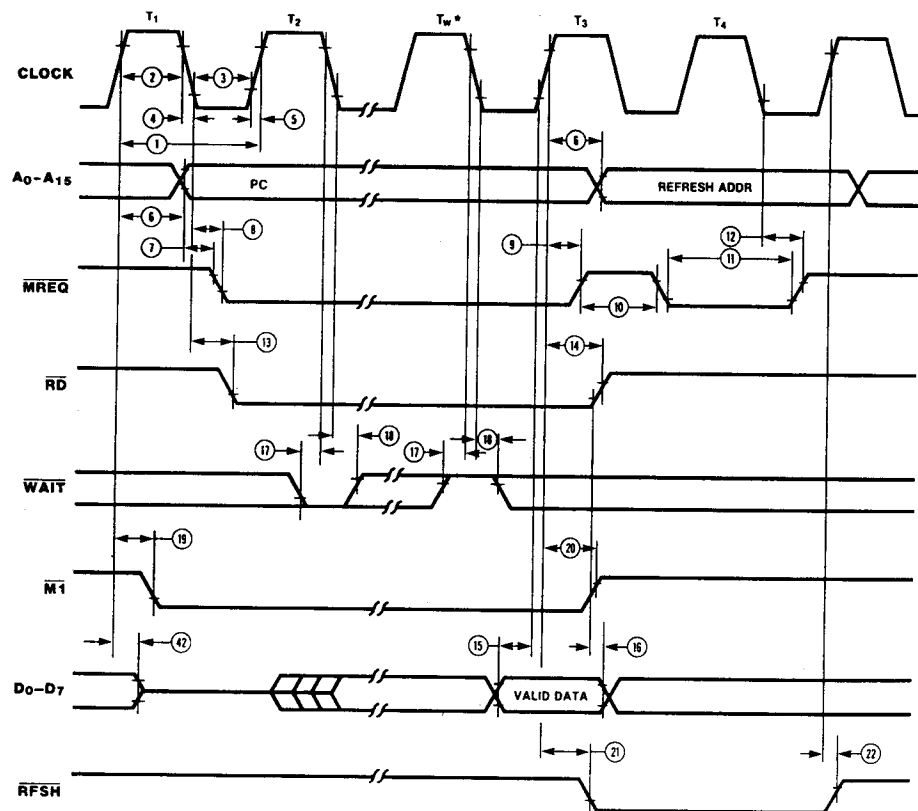


Figure 5. Instruction Opcode Fetch

**Memory Read or Write Cycles.** Figure 6 shows the timing of memory read or write cycles other than an opcode fetch (M1) cycle. The  $\overline{\text{MREQ}}$  and  $\overline{\text{RD}}$  signals function exactly as in the fetch cycle. In a memory write cycle,  $\overline{\text{MREQ}}$  also

becomes active when the address bus is stable. The  $\overline{\text{WR}}$  line is active when the data bus is stable, so that it can be used directly as an R/W pulse to most semiconductor memories.

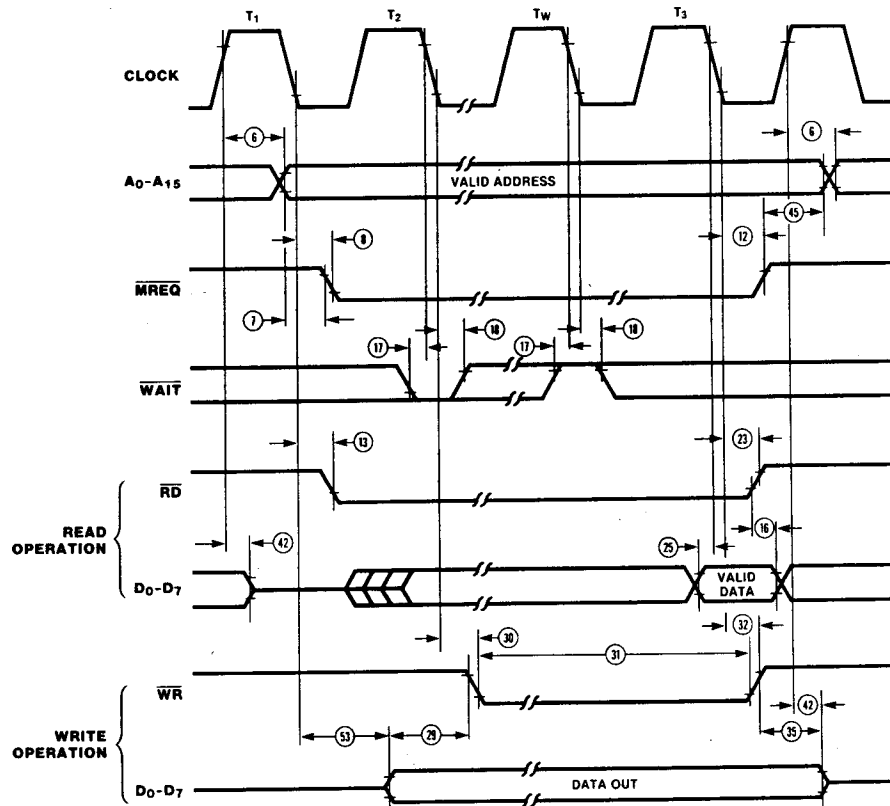
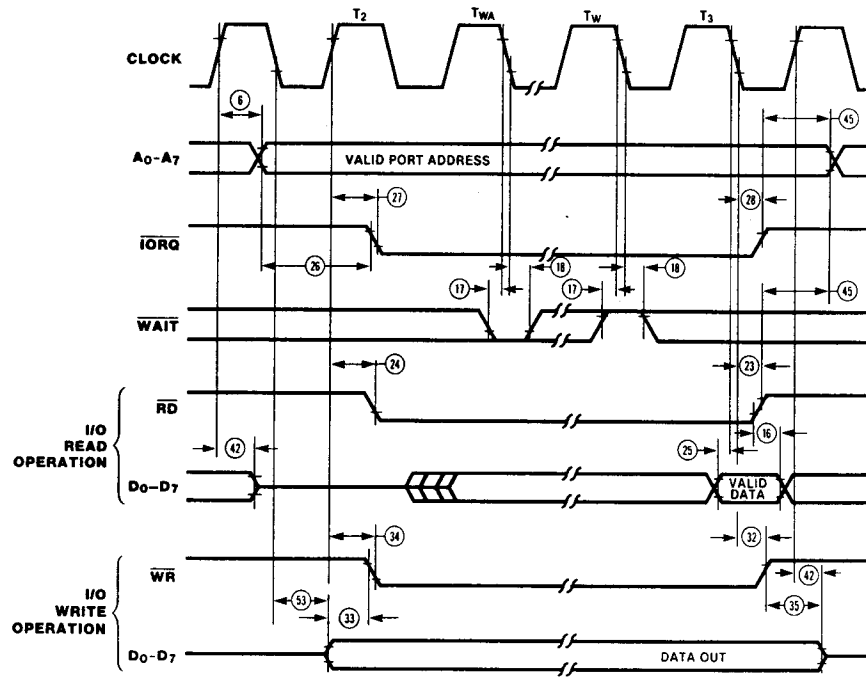


Figure 6. Memory Read or Write Cycles

**Input or Output Cycles.** Figure 7 shows the timing for an I/O read or I/O write operation. During I/O operations, the CPU automatically inserts a single Wait state ( $T_{WA}$ ). This

extra Wait state allows sufficient time for an I/O port to decode the address from the port address lines.

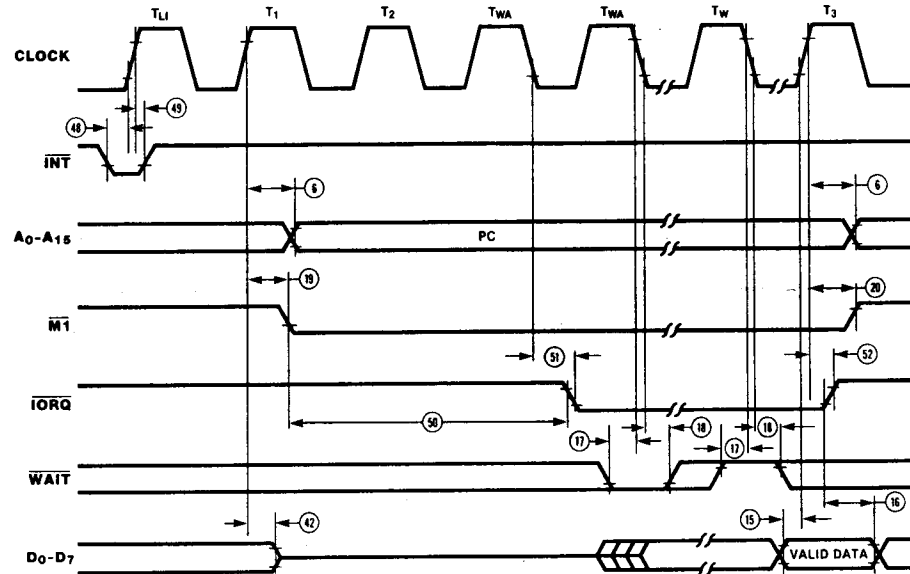


$T_{WA}$  = One wait cycle automatically inserted by CPU.

**Figure 7. Input or Output Cycles**

**Interrupt Request/Acknowledge Cycle.** The CPU samples the interrupt signal with the rising edge of the last clock cycle at the end of any instruction (Figure 8). When an interrupt is accepted, a special M1 cycle is generated.

During this  $\overline{M1}$  cycle,  $\overline{IORQ}$  becomes active (instead of  $\overline{MREQ}$ ) to indicate that the interrupting device can place an 8-bit vector on the data bus. The CPU automatically adds two Wait states to this cycle.



**Power-Down Release Cycle.** The system clock must be supplied to the CPU to release the power-down state. When the system clock is supplied to the CLK input, the CPU restarts operations from the point at which the power-down state was implemented. The timing diagrams for the release from power-down mode are shown in Figure 14.

**NOTES:**

- 1) When the external oscillator has been stopped to enter the power-down state, some warm-up time may be required to obtain a stable clock for the release.
- 2) When the HALT instruction is executed to enter the power-down state, the CPU will also enter the Halt state. An interrupt signal (either  $\overline{\text{NMI}}$  or  $\overline{\text{INT}}$ ) or a RESET signal must be applied to the CPU after the system clock is supplied in order to release the power-down state.

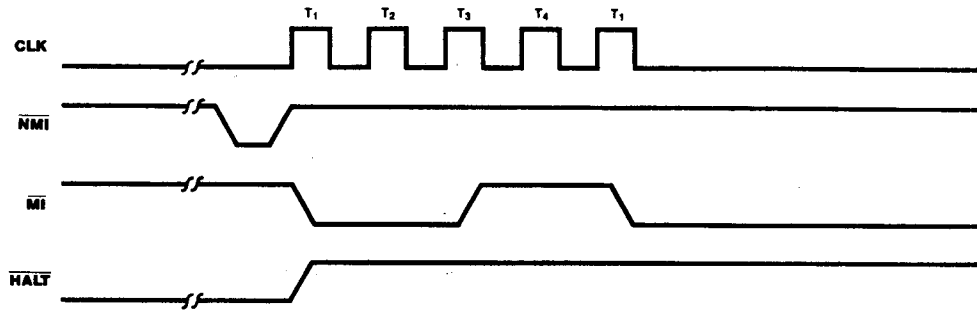


Figure 14a.

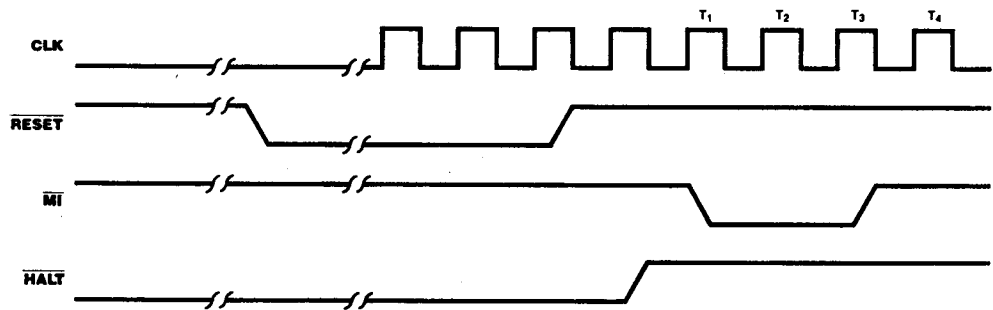


Figure 14b.

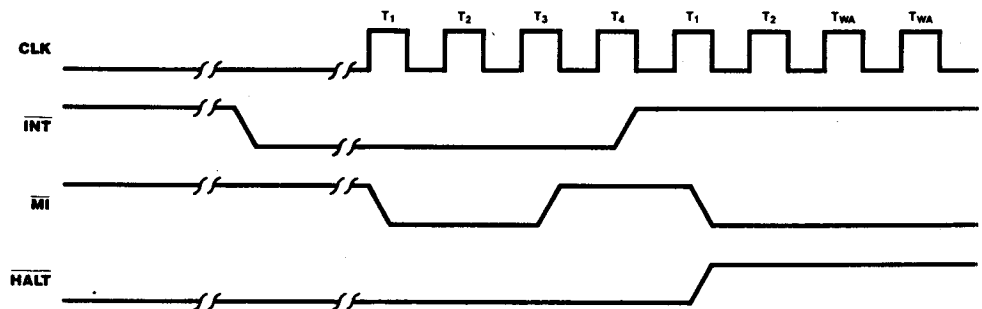


Figure 14c.

Figure 13. Power-Down Release

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## ABSOLUTE MAXIMUM RATINGS

Voltage on  $V_{CC}$  with respect to  $V_{SS}$  . . . . .  $-0.3V$  to  $+7V$   
Voltages on all inputs with respect  
to  $V_{SS}$  . . . . .  $-0.3V$  to  $V_{CC} + 0.3V$   
Operating Ambient  
Temperature . . . . . See Ordering Information  
Storage Temperature . . . . .  $-65^{\circ}C$  to  $+150^{\circ}C$

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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## STANDARD TEST CONDITIONS

The DC Characteristics and capacitance sections below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND (0V). Positive current flows into the referenced pin.

The Ordering Information section lists temperature ranges and product numbers. Package drawings are in the Package Information section. Refer to the Literature List for additional documentation.

Available operating temperature ranges are:

■ **S =  $0^{\circ}C$  to  $+70^{\circ}C$**

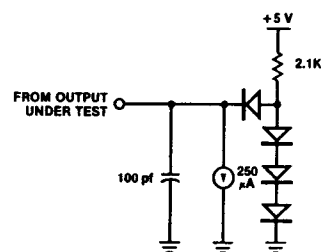
**Voltage Supply Range:**

NMOS:  $+4.75V \leq V_{CC} \leq +5.25V$

CMOS:  $+4.50V \leq V_{CC} \leq +5.50V$

■ **E =  $-40^{\circ}C$  to  $100^{\circ}C$ ,  $+4.50V \leq V_{CC} \leq +5.50V$**

All ac parameters assume a load capacitance of 100 pf. Add 10 ns delay for each 50 pf increase in load up to a maximum of 200 pf for the data bus and 100 pf for address and control lines. AC timing measurements are referenced to 1.5 volts (except for clock, which is referenced to the 10% and 90% points).



## DC CHARACTERISTICS (Z84C00/CMOS Z80 CPU)

Symbol	Parameter	Min	Max	Unit	Condition
$V_{ILC}$	Clock Input Low Voltage	-0.3	0.45	V	
$V_{IHC}$	Clock Input High Voltage	$V_{CC} - .6$	$V_{CC} + .3$	V	
$V_{IL}$	Input Low Voltage	-0.3	0.8	V	
$V_{IH}$	Input High Voltage	2.2	$V_{CC}$	V	
$V_{OL}$	Output Low Voltage		0.4	V	$I_{OL} = 2.0 \text{ mA}$
$V_{OH1}$	Output High Voltage	2.4		V	$I_{OH} = -1.6 \text{ mA}$
$V_{OH2}$	Output High Voltage	$V_{CC} - 0.8$		V	$I_{OH} = -250 \mu\text{A}$
$I_{CC1}$	Power Supply Current	4 MHz	20	mA	$V_{CC} = 5\text{V}$
			30	mA	$V_{IH} = V_{CC} - 0.2\text{V}$
			40	mA	$V_{IL} = 0.2\text{V}$
			50	mA	$V_{CC} = 5\text{V}$
			100	mA	$V_{CC} = 5\text{V}$
$I_{CC2}$	Standby Supply Current		10	$\mu\text{A}$	CLK = (0) $V_{IH} = V_{CC} - 0.2\text{V}$ $V_{IL} = 0.2\text{V}$
$I_{LI}$	Input Leakage Current	-10	10	$\mu\text{A}$	$V_{IN} = 0.4 \text{ to } V_{CC}$
$I_{LO}$	3-State Output Leakage Current in Float	-10	$10^2$	$\mu\text{A}$	$V_{OUT} = 0.4 \text{ to } V_{CC}$

1. Measurements made with outputs floating.

2. A<sub>15</sub>-A<sub>0</sub>, D<sub>7</sub>-D<sub>0</sub>, MREQ, IORQ, RD, and WR.

3.  $I_{CC2}$  standby supply current is guaranteed only when the supplied clock is stopped at a low level during T<sub>4</sub> of the machine cycle immediately following the execution of a HALT instruction.

## CAPACITANCE

Symbol	Parameter	Min	Max	Unit
$C_{CLOCK}$	Clock Capacitance		10	pf
$C_{IN}$	Input Capacitance		5	pf
$C_{OUT}$	Output Capacitance		15	pf

T<sub>A</sub> = 25°C, f = 1 MHz.

Unmeasured pins returned to ground.

# AC CHARACTERISTICS† (Z84C00/CMOS Z80 CPU; Continued)

V<sub>CC</sub>=5.0V ± 10%, unless otherwise specified

No	Symbol	Parameter	Z84C0004**		Z84C0006		Z84C0008		Z84C0010		Z84C0020[1]		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
39	ThBUSREQ (Cr)	/BUSREQ hold time after Clock Rise	10		10		10		10		10		nS	
40	TdCr (BUSACKf)	Clock Rise to /BASACK Fall delay		100		90		80		75		40	nS	
41	TdCf (BUSACKr)	Clock Fall to /BASACK Rise delay		100		90		80		75		40	nS	
42	TdCr(Dz)	Clock Rise to Data float delay		90		80		70		65		40	nS	
43	TdCr(CTz)	Clock Rise to Control Outputs Float Delay (/MREQ, /IORQ, /RD and /WR)		80		70		60		65		40	nS	
44	TdCr(Az)	Clock Rise to Address float delay		90		80		70		75		40	nS	
45	TdCTr(A)	Address Hold time from /MREQ, /IORQ, /RD or /WR	80*		35*		20*		20*		0*		nS	
46	TsRESET(Cr)	/RESET to Clock Rise setup time	60		60		45		40		15		nS	
47	ThRESET(Cr)	/RESET to Clock Rise Hold time	10		10		10		10		10		nS	
48	TsINTf(Cr)	/INT Fall to Clock Rise Setup Time	80		70		55		50		15		nS	
49	ThINTr(Cr)	/INT Rise to Clock Rise Hold Time	10		10		10		10		10		nS	
50	TdM1f (IORQf)	/M1 Fall to /IORQ Fall delay	565*		359*		270*		220*		100*		nS	
51	TdCf(IORQf)	/Clock Fall to /IORQ Fall delay		85		70		60		55		45	nS	
52	TdCf(IORQr)	Clock Rise to /IORQ Rise delay		85		70		60		55		45	nS	
53	TdCf(D)	Clock Fall to Data Valid delay		150		130		115		110		75	nS	

## Notes:

\* For Clock periods other than the minimum shown, calculate parameters using the following table.

Calculated values above assumed TrC = TtC = maximum.

\*\* 4 MHz CMOS Z80 is obsoleted and replaced by 6 MHz

[1] Z84C0020 parameters are guaranteed with 50pF load Capacitance.

[2] If Capacitive Load is other than 50pF, please use Figure 1. to calculate the value.

[3] Increasing delay by 10nS for each 50pF increase in loading, 200pF max for data lines, and 100pF for control lines.

## FOOTNOTES TO AC CHARACTERISTICS

No	Symbol	Parameter	Z84C0004**	Z84C0006	Z84C0008	Z84C0010	Z84C0020
1	TcC	TwCh + TwCl + TrC + TtC					
7	TdA(MREQf)	TwCh + TtC	-65	-50	-45	-45	-45
10	TwMREQh	TwCh + TtC	-20	-20	-20	-20	-20
11	TwMREQf	TcC	-30	-30	-25	-25	-25
26	TdA(IORQf)	TcC	-70	-55	-50	-50	-50
29	TdD(WRf)	TcC	-170	-140	-120	-60	-60
31	TwWR	TcC	-30	-30	-25	-25	-25
33	TdD(WRf)	TwCl + TrC	-140	-140	-120	-60	-60
35	TdWRr(D)	TwCl + TrC	-70	-55	-50	-40	-25
45	TdCTr(A)	TwCl + TrC	-50	-50	-45	-30	-30
50	TdM1f(IORQf)	2TcC + TwCh + TtC	-65	-50	-45	-30	-30

AC Test Conditions: V<sub>IH</sub> = 2.0 V  
V<sub>IL</sub> = 0.8 V

V<sub>OH</sub> = 1.5 V  
V<sub>OL</sub> = 1.5 V

V<sub>IHC</sub> = V<sub>CC</sub> - 0.6 V  
V<sub>ILC</sub> = 0.45 V

FLOAT = ±0.5 V

# AC CHARACTERISTICS† (Z8400/NMOS Z80 CPU; Continued)

Number	Symbol	Parameter	Z0840004		Z0840006		Z0840008	
			Min	Max	Min	Max	Min	Max
39	ThBUSREQ(Cr)	BUSREQ Hold Time after Clock ↑	0		0		0	
40	TdCr(BUSACKf)	Clock ↑ to BUSACK ↓ Delay		100		90		80
41	TdCl(BUSACKr)	Clock ↓ to BUSACK ↑ Delay		100		90		80
42	TdCr(Dz)	Clock ↑ to Data Float Delay		90		80		70
43	TdCr(CTz)	Clock ↑ to Control Outputs Float Delay (MREQ, IORQ, RD, and WR)		80		70		60
44	TdCr(Az)	Clock ↑ to Address Float Delay		90		80		70
45	TdCTr(A)	MREQ ↑, IORQ ↑, RD ↑, and WR ↑ to Address Hold Time	80*		35*		20*	
46	TsRESET(Cr)	RESET to Clock ↑ Setup Time	60		60		45	
47	ThRESET(Cr)	RESET to Clock ↑ Hold Time		0		0		0
48	TsINTf(Cr)	INT to Clock ↑ Setup Time	80		70		55	
49	ThINTr(Cr)	INT to Clock ↑ Hold Time		0		0		0
50	TdM1f(IORQf)	M1 ↓ to IORQ ↓ Delay	565*		365*		270*	
51	TdCf(IORQf)	Clock ↓ to IORQ ↓ Delay		85		70		60
52	TdCf(IORQr)	Clock ↑ to IORQ ↑ Delay		85		70		60
53	TdCf(D)	Clock ↓ to Data Valid Delay		150		130		115

\*For clock periods other than the minimums shown, calculate parameters using the following table. Calculated values above assumed TrC = TrC = 20 ns.

†Units in nanoseconds (ns).

## FOOTNOTES TO AC CHARACTERISTICS

Number	Symbol	General Parameter	Z0840004	Z0840006	Z0840008
1	TcC	TwCh + TwCl + TrC + TrC			
7	TdA(MREQf)	TwCh + TrC	- 65	- 50	- 45
10	TwMREQh	TwCh + TrC	- 20	- 20	- 20
11	TwMREQl	TcC	- 30	- 30	- 25
26	TdA(IORQf)	TcC	- 70	- 55	- 50
29	TdD(WRf)	TcC	- 170	- 140	- 120
31	TwWR	TcC	- 30	- 30	- 25
33	TdD(WRf)	TwCl + TrC	- 140	- 140	- 120
35	TdWRr(D)	TwCl + TrC	- 70	- 55	- 50
45	TdCTr(A)	TwCl + TrC	- 50	- 50	- 45
50	TdM1f(IORQf)	2TcC + TwCh + TrC	- 65	- 50	- 45

AC Test Conditions:

V<sub>IH</sub> = 2.0 V

V<sub>IL</sub> = 0.8 V

V<sub>IHC</sub> = V<sub>CC</sub> - 0.6 V

V<sub>ILC</sub> = 0.45 V

V<sub>OH</sub> = 1.5 V

V<sub>OL</sub> = 1.5 V

FLOAT = ±0.5 V

# Customer Support

For answers to technical questions about the product, documentation, or any other issues with Zilog's offerings, please visit Zilog's Knowledge Base at <http://www.zilog.com/kb>.

For any comments, detail technical questions, or reporting problems, please visit Zilog's Technical Support at <http://support.zilog.com>.