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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	Z80
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	10MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z84c0010feg

Table 1. Z80C CPU Registers

Register	Size (Bits)	Remarks	
A, A'	Accumulator	8	Stores an operand or the results of an operation.
F, F'	Flags	8	See Instruction Set.
B, B'	General Purpose	8	Can be used separately or as a 16-bit register with C.
C, C'	General Purpose	8	Can be used separately or as a 16-bit register with B.
D, D'	General Purpose	8	Can be used separately or as a 16-bit register with E.
E, E'	General Purpose	8	Can be used separately or as a 16-bit register with D.
H, H'	General Purpose	8	Can be used separately or as a 16-bit register with L.
L, L'	General Purpose	8	Can be used separately or as a 16-bit register with H.
Note: The (B,C), (D,E), and (H,L) sets are combined as follows:			
B — High byte C — Low byte			
D — High byte E — Low byte			
H — High byte L — Low byte			
I	Interrupt Register	8	Stores upper eight bits of memory address for vectored interrupt processing.
R	Refresh Register	8	Provides user-transparent dynamic memory refresh. Automatically incremented and placed on the address bus during each instruction fetch cycle.
IX	Index Register	16	Used for indexed addressing.
IY	Index Register	16	Used for indexed addressing.
SP	Stack Pointer	16	Holds address of the top of the stack. See Push or Pop in instruction set.
PC	Program Counter	16	Holds address of next instruction.
IFF ₁ -IFF ₂	Interrupt Enable	Flip-Flops	Set or reset to indicate interrupt status (see Figure 4).
IMFa-IMFb	Interrupt Mode	Flip-Flops	Reflect Interrupt mode (see Figure 4).

failure has been detected. After recognition of the $\overline{\text{NMI}}$ signal (providing $\overline{\text{BUSREQ}}$ is not active), the CPU jumps to restart location 0066H. Normally, software starting at this address contains the interrupt service routine.

Maskable Interrupt ($\overline{\text{INT}}$). Regardless of the interrupt mode set by the user, the CPU response to a maskable interrupt input follows a common timing cycle. After the interrupt has been detected by the CPU (provided that interrupts are enabled and $\overline{\text{BUSREQ}}$ is not active) a special interrupt processing cycle begins. This is a special fetch ($\overline{\text{M1}}$) cycle in which $\overline{\text{IORQ}}$ becomes active rather than $\overline{\text{MREQ}}$, as in a normal $\overline{\text{M1}}$ cycle. In addition, this special $\overline{\text{M1}}$ cycle is automatically extended by two $\overline{\text{WAIT}}$ states, to allow for the time required to acknowledge the interrupt request.

Mode 0 Interrupt Operation. This mode is similar to the 8080 microprocessor interrupt service procedures. The interrupting device places an instruction on the data bus. This is normally a Restart instruction, which will initiate a call

to the selected one of eight restart locations in page zero of memory. Unlike the 8080, the Z80 CPU responds to the Call instruction with only one interrupt acknowledge cycle followed by two memory read cycles.

Mode 1 Interrupt Operation. Mode 1 operation is very similar to that for the NMI. The principal difference is that the Mode 1 interrupt has only one restart location, 003BH.

Mode 2 Interrupt Operation. This interrupt mode has been designed to most effectively utilize the capabilities of the Z80 microprocessor and its associated peripheral family. The interrupting peripheral device selects the starting address of the interrupt service routine. It does this by placing an 8-bit vector on the data bus during the interrupt acknowledge cycle. The CPU forms a pointer using this byte as the lower 8 bits and the contents of the I register as the upper 8 bits. This points to an entry in a table of addresses for interrupt service routines. The CPU then jumps to the routine at that

8-BIT LOAD GROUP (Continued)

Mnemonic	Symbolic Operation	S	Z	Flags			Opcode				No. of Bytes	No. of M Cycles	No. of T States	Comments			
				H	P/V	N	C	76	543	210					Hex		
LD (Y+d), n	(Y+d) ← n	•	•	X	•	X	•	•	•	11 00	111 110	101 110	FD 36	4	5	19	
LDA, (BC)	A ← (BC)	•	•	X	•	X	•	•	•	00	001 010	010 0A	0A	1	2	7	
LDA, (DE)	A ← (DE)	•	•	X	•	X	•	•	•	00	011 010	010 1A	1A	1	2	7	
LDA, (nn)	A ← (nn)	•	•	X	•	X	•	•	•	00	111 010	010 3A	3A	3	4	13	
LD (BC), A	(BC) ← A	•	•	X	•	X	•	•	•	00	000 010	010 02	02	1	2	7	
LD (DE), A	(DE) ← A	•	•	X	•	X	•	•	•	00	010 010	010 12	12	1	2	7	
LD (nn), A	(nn) ← A	•	•	X	•	X	•	•	•	00	110 010	010 32	32	3	4	13	
LDA, I	A ← I	‡	‡	X	0	X	IFF	0	•	11 01	101 101	101 ED	ED	2	2	9	
LDA, R	A ← R	‡	‡	X	0	X	IFF	0	•	11 01	101 101	101 ED	ED	2	2	9	
LD I, A	I ← A	•	•	X	•	X	•	•	•	11 01	101 101	101 ED	ED	2	2	9	
LDR, A	R ← A	•	•	X	•	X	•	•	•	11 01	101 101	101 ED	ED	2	2	9	

NOTE: IFF, the content of the interrupt enable flip-flop, (IFF₂), is copied into the P/V flag.

16-BIT LOAD GROUP

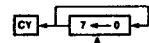
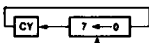
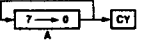
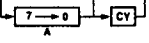
Mnemonic	Symbolic Operation	S	Z	Flags			Opcode				No. of Bytes	No. of M Cycles	No. of T States	Comments			
				H	P/V	N	C	76	543	210					Hex		
LD dd, nn	dd ← nn	•	•	X	•	X	•	•	•	00 dd0	001		3	3	10	dd Pair	
LD IX, nn	IX ← nn	•	•	X	•	X	•	•	•	11 00	011 101	DD 21	DD	4	4	14	10 HL 11 SP
LD IY, nn	IY ← nn	•	•	X	•	X	•	•	•	11 00	111 101	FD 21	FD	4	4	14	
LD HL, (nn)	H ← (nn+1) L ← (nn)	•	•	X	•	X	•	•	•	00 101	010 2A	2A	3	5	16		
LD dd, (nn)	dd _H ← (nn+1) dd _L ← (nn)	•	•	X	•	X	•	•	•	11 01	101 011	ED	ED	4	6	20	

NOTE: (PAIR)_H, (PAIR)_L refer to high order and low order eight bits of the register pair respectively. e.g., BC_L = C, AF_H = A.

16-BIT ARITHMETIC GROUP

Mnemonic	Symbolic Operation	S	Z	Flags			Opcode			Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments			
				H	P/V	N	C	76	543					210	ss	Reg.	
ADD HL, ss	HL ← HL + ss	•	•	X	X	X	•	0	‡	00	ssl	001		1	3	11	ss Reg. 00 BC
ADC HL, ss	HL ← HL + ss + CY	‡	‡	X	X	X	V	0	‡	11	101	101	ED	2	4	15	01 DE 10 HL 11 SP
SBC HL, ss	HL ← HL - ss - CY	‡	‡	X	X	X	V	1	‡	11	101	101	ED	2	4	15	01 ss0 010
ADD IX, pp	IX ← IX + pp	•	•	X	X	X	•	0	‡	11	011	101	DD	2	4	15	pp Reg. 00 BC 01 DE 10 IX 11 SP
ADD IY, rr	IY ← IY + rr	•	•	X	X	X	•	0	‡	11	111	101	FD	2	4	15	rr Reg. 00 BC
INC ss	ss ← ss + 1	•	•	X	•	X	•	•	•	00	ss0	011		1	1	6	01 DE
INC IX	IX ← IX + 1	•	•	X	•	X	•	•	•	11	011	101	DD	2	2	10	10 IY 11 SP
INC IY	IY ← IY + 1	•	•	X	•	X	•	•	•	11	111	101	FD	2	2	10	00 100 011 23
DEC ss	ss ← ss - 1	•	•	X	•	X	•	•	•	00	ss1	011		1	1	6	
DEC IX	IX ← IX - 1	•	•	X	•	X	•	•	•	11	011	101	DD	2	2	10	00 101 011 2B
DEC IY	IY ← IY - 1	•	•	X	•	X	•	•	•	11	111	101	FD	2	2	10	00 101 011 2B

ROTATE AND SHIFT GROUP

Mnemonic	Symbolic Operation	S	Z	Flags			Opcode			Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments			
				H	P/V	N	C	76	543						210		
RLCA		•	•	X	0	X	•	0	‡	00	000	111	07	1	1	4	Rotate left circular accumulator.
RLA		•	•	X	0	X	•	0	‡	00	010	111	17	1	1	4	Rotate left accumulator.
RRCA		•	•	X	0	X	•	0	‡	00	001	111	0F	1	1	4	Rotate right circular accumulator.
RRA		•	•	X	0	X	•	0	‡	00	011	111	1F	1	1	4	Rotate right accumulator.

ROTATE AND SHIFT GROUP (Continued)

Symbolic Mnemonic Operation	Flags		Flags				Opcode			No. of Bytes	No. of M Cycles	No. of T States	Comments		
	S	Z	H	P/V	N	C	76	543	210					Hex	
RLC r	†	†	X	0	X	P	0	†	11 001 011	CB	2	2	8	Rotate left circular register r.	
									00 000 r						
RLC (HL)	†	†	X	0	X	P	0	†	11 001 011	CB	2	4	15	r Reg.	
									00 000 110					000 B	
RLC (IX+d)	†	†	X	0	X	P	0	†	11 011 101	DD	4	6	23	001 C	
									11 001 011	CB				010 D	
									00 000 110					011 E	
									00 000 110					001 H	
									00 000 110					101 L	
									00 000 110					111 A	
RLC (IY+d)	†	†	X	0	X	P	0	†	11 111 101	FD	4	6	23		
									11 001 011	CB					
									00 000 110						
RL m	†	†	X	0	X	P	0	†	00 000 110					Instruction format and states are as shown for RLCs. To form new opcode replace 000 or RLCs with shown code.	
									00 010						
RRC m	†	†	X	0	X	P	0	†	001						
RR m	†	†	X	0	X	P	0	†	011						
SLA m	†	†	X	0	X	P	0	†	100						
SRA m	†	†	X	0	X	P	0	†	101						
SRL m	†	†	X	0	X	P	0	†	111						
RLD	†	†	X	0	X	P	0	•	11 101 101	ED	2	5	18		Rotate digit left and right between the accumulator and location (HL).
									01 101 111	6F					
RRD	†	†	X	0	X	P	0	•	11 101 101	ED	2	5	18		The content of the upper half of the accumulator is unaffected.
									01 100 111	67					

BIT SET, RESET AND TEST GROUP

Mnemonic	Symbolic Operation	Flags						Opcode			Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments											
		S	Z	H	P/V	N	C	76	543	210																
BIT b, r	$Z \leftarrow r_b$	X	†	X	1	X	X	0	•	11	001	011	CB	2	2	8	r Reg. 000 B									
BIT b, (HL)	$Z \leftarrow (HL)_b$	X	†	X	1	X	X	0	•	11	001	011	CB	2	3	12	001 C 010 D									
BIT b, (IX+d) _b	$Z \leftarrow (IX+d)_b$	X	†	X	1	X	X	0	•	11	011	101	DD	4	5	20	011 E									
										11	001	011	CB								100 H					
										←d→																101 L
										01	b	110														111 A
BIT b, (IY+d) _b	$Z \leftarrow (IY+d)_b$	X	†	X	1	X	X	0	•	11	111	101	FD	4	5	20	000 0									
										11	001	011	CB											001 1		
										←d→																010 2
										01	b	110														011 3
SET b, r	$r_b \leftarrow 1$	•	•	X	•	X	•	•	•	11	001	011	CB	2	2	8	100 4									
SET b, (HL)	$(HL)_b \leftarrow 1$	•	•	X	•	X	•	•	•	11	b	r					101 5									
										11	b	110													110 6	
SET b, (IX+d)	$(IX+d)_b \leftarrow 1$	•	•	X	•	X	•	•	•	11	011	101	DD	4	6	23										
										11	001	011	CB													
										←d→																
SET b, (IY+d)	$(IY+d)_b \leftarrow 1$	•	•	X	•	X	•	•	•	11	b	110														
										11	111	101	FD	4	6	23										
										11	001	011	CB													
RES b, m	$m_b \leftarrow 0$ $m = r, (HL),$ $(IX+d), (IY+d)$	•	•	X	•	X	•	•	•	11	b	110														
										10																

To form new opcode replace **11** of SET b, s with **10**. Flags and time states for SET instruction.

NOTE: The notation m_b indicates location m, bit b (0 to 7).

JUMP GROUP

Mnemonic	Symbolic Operation	Flags					Opcode			No. of Bytes	No. of M Cycles	No. of T States	Comments				
		S	Z	H	P/V/N	C	76	543	210					Hex			
JP nn	PC ← nn	•	•	X	•	X	•	•	•	11	000	011	C3	3	3	10	cc Condition 000 NZ (non-zero) 001 Z (zero)
JP cc, nn	If condition cc is true PC ← nn, otherwise continue	•	•	X	•	X	•	•	•	11	cc	010		3	3	10	010 NC (non-carry) 011 C (carry) 100 PO (parity odd) 101 PE (parity even)
JR e	PC ← PC + e	•	•	X	•	X	•	•	•	00	011	000	18	2	3	12	110 P (sign positive) 111 M (sign negative)
JR C, e	If C = 0, continue If C = 1, PC ← PC + e	•	•	X	•	X	•	•	•	00	111	000	38	2	2	7	If condition not met.
														2	3	12	If condition is met.
JR NC, e	If C = 1, continue If C = 0, PC ← PC + e	•	•	X	•	X	•	•	•	00	110	000	30	2	2	7	If condition not met.
														2	3	12	If condition is met.
JP Z, e	If Z = 0, continue If Z = 1, PC ← PC + e	•	•	X	•	X	•	•	•	00	101	000	28	2	2	7	If condition not met.
														2	3	12	If condition is met.
JR NZ, e	If Z = 1, continue If Z = 0, PC ← PC + e	•	•	X	•	X	•	•	•	00	100	000	20	2	2	7	If condition not met.
														2	3	12	If condition is met.
JP (HL)	PC ← HL	•	•	X	•	X	•	•	•	11	101	001	E9	1	1	4	
JP (IX)	PC ← IX	•	•	X	•	X	•	•	•	11	011	101	DD	2	2	8	
										11	101	001	E9				
JP (IY)	PC ← IY	•	•	X	•	X	•	•	•	11	111	101	FD	2	2	8	
										11	101	001	E9				
DJNZ, e	B ← B - 1 If B = 0, continue If B ≠ 0, PC ← PC + e	•	•	X	•	X	•	•	•	00	010	000	10	2	2	8	If B = 0
														2	3	13	If B ≠ 0.

NOTES: e represents the extension in the relative addressing mode.
e is a signal two's complement number in the range < -126, 129 >.
e - 2 in the opcode provides an effective address of pc + e as PC is incremented by 2 prior to the addition of e.

INPUT AND OUTPUT GROUP

Mnemonic	Symbolic Operation	Flags					Opcode				No. of Bytes	No. of M Cycles	No. of T States	Comments					
		S	Z	H	P/V/N	C	76	543	210	Hex									
INA, (n)	A ← (n)	•	•	X	•	X	•	•	•	•	11	011	01	DB	2	3	11	n to A ₀ ~ A ₇ Acc. to A ₈ ~ A ₁₅	
IN r, (C)	r ← (C) if r=110 only the flags will be affected	‡	‡	X	‡	X	P	0	•	•	11	101	101	ED	2	3	12	C to A ₀ ~ A ₇ B to A ₈ ~ A ₁₅	
INI	(HL) ← (C)			X	‡	X	X	X	X	1	X	11	101	101	ED	2	4	16	C to A ₀ ~ A ₇ B to A ₈ ~ A ₁₅
	B ← B-1 HL ← HL+1											10	100	010	A2				
INIR	(HL) ← (C)			X	1	X	X	X	X	1	X	11	101	101	ED	2	5 (if B≠0)	21	C to A ₀ ~ A ₇ B to A ₈ ~ A ₁₅
	B ← B-1 HL ← HL+1											10	110	010	B2				
	Repeat until B=0																		
IND	(HL) ← (C)			X	‡	X	X	X	X	1	X	11	101	101	ED	2	4	16	C to A ₀ ~ A ₇ B to A ₈ ~ A ₁₅
	B ← B-1 HL ← HL-1											10	101	010	AA				
INDR	(HL) ← (C)			X	1	X	X	X	X	1	X	11	101	101	ED	2	5 (if B≠0)	21	C to A ₀ ~ A ₇ B to A ₈ ~ A ₁₅
	B ← B-1 HL ← HL-1											10	111	010	BA				
	Repeat until B=0																		
OUT (n), A	(n) → A	•	•	X	•	X	•	•	•	•	•	11	010	011	D3	2	3	11	n to A ₀ ~ A ₇ Acc. to A ₈ ~ A ₁₅
OUT (C), r	(C) → r	•	•	X	•	X	•	•	•	•	•	11	101	101	ED	2	3	12	C to A ₀ ~ A ₇ B to A ₈ ~ A ₁₅
OUTI	(C) ← (HL)			X	‡	X	X	X	X	1	X	11	101	101	ED	2	4	16	C to A ₀ ~ A ₇ B to A ₈ ~ A ₁₅
	B ← B-1 HL ← HL+1											10	100	011	A3				
OTIR	(C) ← (HL)			X	1	X	X	X	X	1	X	11	101	101	ED	2	5 (if B≠0)	21	C to A ₀ ~ A ₇ B to A ₈ ~ A ₁₅
	B ← B-1 HL ← HL+1											10	110	011	B3				
	Repeat until B=0																		
OUTD	(C) ← (HL)			X	‡	X	X	X	X	1	X	11	101	101	ED	2	4	16	C to A ₀ ~ A ₇ B to A ₈ ~ A ₁₅
	B ← B-1 HL ← HL-1											10	101	011	AB				
OTDR	(C) ← (HL)			X	1	X	X	X	X	1	X	11	101	101	ED	2	5 (if B≠0)	21	C to A ₀ ~ A ₇ B to A ₈ ~ A ₁₅
	B ← B-1 HL ← HL-1											10	111	011					
	Repeat until B=0																		

NOTES: ① If the result of B-1 is zero, the Z flag is set; otherwise it is reset.
 ② Z flag is set upon instruction completion only.

SUMMARY OF FLAG OPERATION

Instructions	D ₇				D ₀			Comments	
	S	Z	H	P/V	N	C			
ADD A, s; ADC A, s	†	†	X	†	X	V	0	†	8-bit add or add with carry.
SUB s; SBC A, s; CP s; NEG	†	†	X	†	X	V	1	†	8-bit subtract, subtract with carry, compare and negate accumulator.
AND s	†	†	X	1	X	P	0	0	Logical operation.
OR s, XOR s	†	†	X	0	X	P	0	0	Logical operation.
INC s	†	†	X	†	X	V	0	•	8-bit increment.
DEC s	†	†	X	†	X	V	1	•	8-bit decrement.
ADD DD, ss	•	•	X	X	X	•	0	†	16-bit add.
ADC HL, ss	†	†	X	X	X	V	0	†	16-bit add with carry.
SBC HL, ss	†	†	X	X	X	V	1	†	16-bit subtract with carry.
RLA; RLCA; RRA; RRCA	•	•	X	0	X	•	0	†	Rotate accumulator.
RL m; RLC m; RR m; RRC m; SLA m; SRA m; SRL m	†	†	X	0	X	P	0	†	Rotate and shift locations.
RLD; RRD	†	†	X	0	X	P	0	•	Rotate digit left and right.
DAA	†	†	X	†	X	P	•	†	Decimal adjust accumulator.
CPL	•	•	X	1	X	•	1	•	Complement accumulator.
SCF	•	•	X	0	X	•	0	1	Set carry.
CCF	•	•	X	X	X	•	0	†	Complement carry.
IN r (C)	†	†	X	0	X	P	0	•	Input register indirect.
INI; IND; OUTI; OUTD	X	†	X	X	X	X	1	•	Block input and output. Z = 1 if B ≠ 0, otherwise Z = 0.
INIR; INDR; OTIR; OTDR	X	1	X	X	X	X	1	•	Block input and output. Z = 1 if B ≠ 0, otherwise Z = 0.
LDI; LDD	X	X	X	0	X	†	0	•	Block transfer instructions. P/V = 1 if BC ≠ 0, otherwise P/V = 0.
LDIR; LDDR	X	X	X	0	X	0	0	•	Block transfer instructions. P/V = 1 if BC ≠ 0, otherwise P/V = 0.
CPI; CPIR; CPD; CPDR	X	†	X	X	X	†	1	•	Block search instructions. Z = 1 if A = (HL), otherwise Z = 0. P/V = 1 if BC ≠ 0, otherwise P/V = 0.
LDA; I, LD A, R	†	†	X	0	X	IFF	0	•	IFF, the content of the interrupt enable flip-flop, (IFF ₂), is copied into the P/V flag.
BIT b, s	X	†	X	1	X	X	0	•	The state of bit b of location s is copied into the Z flag.

SYMBOLIC NOTATION

Symbol	Operation	Symbol	Operation
S	Sign flag. S = 1 if the MSB of the result is 1.	†	The flag is affected according to the result of the operation.
Z	Zero flag. Z = 1 if the result of the operation is 0.	•	The flag is unchanged by the operation.
P/V	Parity or overflow flag. Parity (P) and overflow (V) share the same flag. Logical operations affect this flag with the parity of the result while arithmetic operations affect this flag with the overflow of the result. If P/V holds parity: P/V = 1 if the result of the operation is even; P/V = 0 if result is odd. If P/V holds overflow, P/V = 1 if the result of the operation produced an overflow. If P/V does not hold overflow, P/V = 0.	0	The flag is reset by the operation.
H*	Half-carry flag. H = 1 if the add or subtract operation produced a carry into, or borrow from, bit 4 of the accumulator.	1	The flag is set by the operation.
N*	Add/Subtract flag. N = 1 if the previous operation was a subtract.	X	The flag is indeterminate.
C	Carry/Link flag. C = 1 if the operation produced a carry from the MSB of the operand or result.	V	P/V flag affected according to the overflow result of the operation.
		P	P/V flag affected according to the parity result of the operation.
		r	Any one of the CPU registers A, B, C, D, E, H, L.
		s	Any 8-bit location for all the addressing modes allowed for the particular instruction.
		ss	Any 16-bit location for all the addressing modes allowed for that instruction.
		ii	Any one of the two index registers IX or IY.
		R	Refresh counter.
		n	8-bit value in range <0, 255>.
		nn	16-bit value in range <0, 65535>.

* H and N flags are used in conjunction with the decimal adjust instruction (DAA) to properly correct the result into packed BCD format following addition or subtraction using operands with packed BCD format.

CPU REGISTERS

Figure 4 shows three groups of registers within the CPU. The first group consists of duplicate sets of 8-bit registers: a principal set and an alternate set [designated by ' (prime), e.g., A']. Both sets consist of the Accumulator register, the Flag register, and six general-purpose registers. Transfer of data between these duplicate sets of registers is accomplished by use of "Exchange" instructions. The result is faster response to interrupts and easy, efficient implementation of such versatile programming techniques

as background-foreground data processing. The second set of registers consists of six registers with assigned functions. These are the I (Interrupt register), the R (Refresh register), the IX and IY (Index registers), the SP (Stack Pointer), and the PC (Program Counter). The third group consists of two interrupt status flip-flops, plus an additional pair of flip-flops which assists in identifying the interrupt mode at any particular time. Table 1 provides further information on these registers.

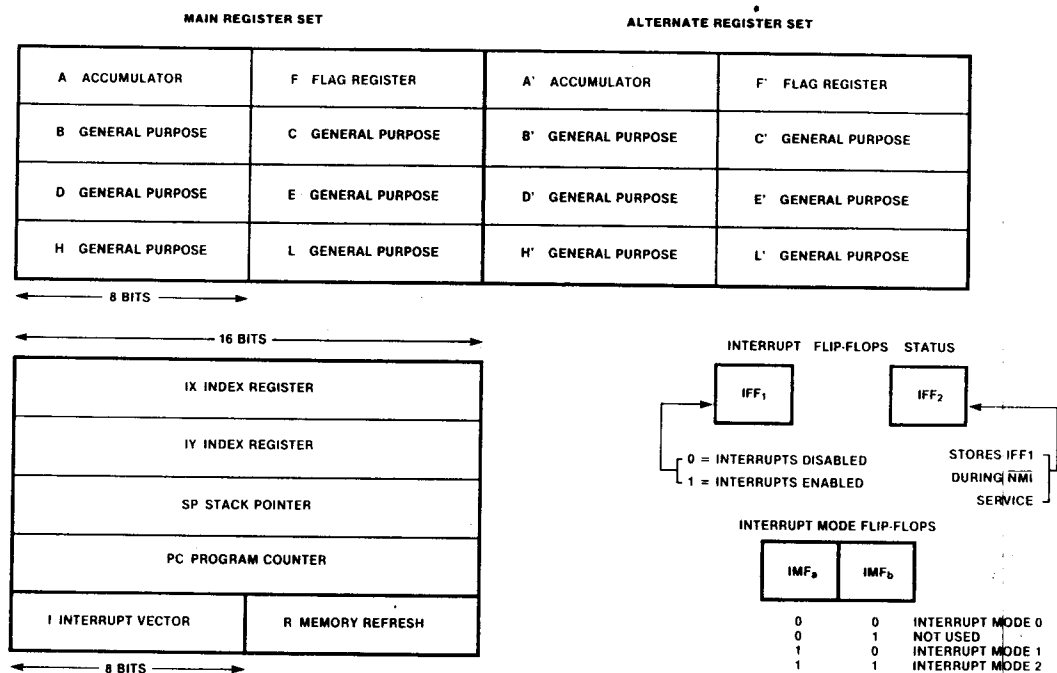


Figure 4. CPU Registers

INTERRUPTS: GENERAL OPERATION

The CPU accepts two interrupt input signals: $\overline{\text{NMI}}$ and $\overline{\text{INT}}$. The $\overline{\text{NMI}}$ is a non-maskable interrupt and has the highest priority. $\overline{\text{INT}}$ is a lower priority interrupt and it requires that interrupts be enabled in software in order to operate. $\overline{\text{INT}}$ can be connected to multiple peripheral devices in a wired-OR configuration.

The Z80 has a single response mode for interrupt service on the non-maskable interrupt. The maskable interrupt, $\overline{\text{INT}}$, has three programmable response modes available. These are:

- Mode 0 — similar to the 8080 microprocessor.
- Mode 1 — Peripheral Interrupt service, for use with non-8080/Z80 systems.

- Mode 2 - a vectored interrupt scheme, usually daisy-chained, for use with the Z80 Family and compatible peripheral devices.

The CPU services interrupts by sampling the $\overline{\text{NMI}}$ and $\overline{\text{INT}}$ signals at the rising edge of the last clock of an instruction. Further interrupt service processing depends upon the type of interrupt that was detected. Details on interrupt responses are shown in the CPU Timing Section.

Non-Maskable Interrupt ($\overline{\text{NMI}}$). The nonmaskable interrupt cannot be disabled by program control and therefore will be accepted at all times by the CPU. $\overline{\text{NMI}}$ is usually reserved for servicing only the highest priority type interrupts, such as that for orderly shutdown after power

CPU TIMING

The Z80 CPU executes instructions by proceeding through a specific sequence of operations:

- Memory read or write
- I/O device read or write
- Interrupt acknowledge

The basic clock period is referred to as a T time or cycle, and three or more T cycles make up a machine cycle (M1, M2 or M3 for instance). Machine cycles can be extended either by the CPU automatically inserting one or more Wait states or by the insertion of one or more Wait states by the user.

Instruction Opcode Fetch. The CPU places the contents of the Program Counter (PC) on the address bus at the start of the cycle (Figure 5). Approximately one-half clock cycle later, \overline{MREQ} goes active. When active, \overline{RD} indicates that the memory data can be enabled onto the CPU data bus.

The CPU samples the \overline{WAIT} input with the falling edge of clock state T_2 . During clock states T_3 and T_4 of an $\overline{M1}$ cycle, dynamic RAM refresh can occur while the CPU starts decoding and executing the instruction. When the Refresh Control signal becomes active, refreshing of dynamic memory can take place.

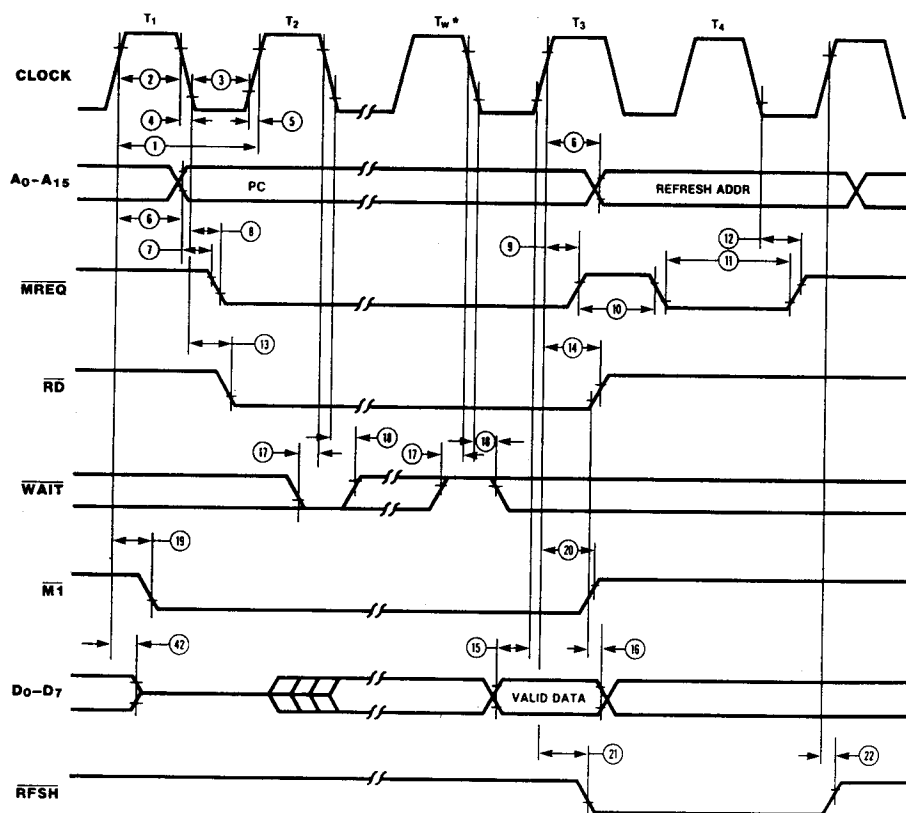
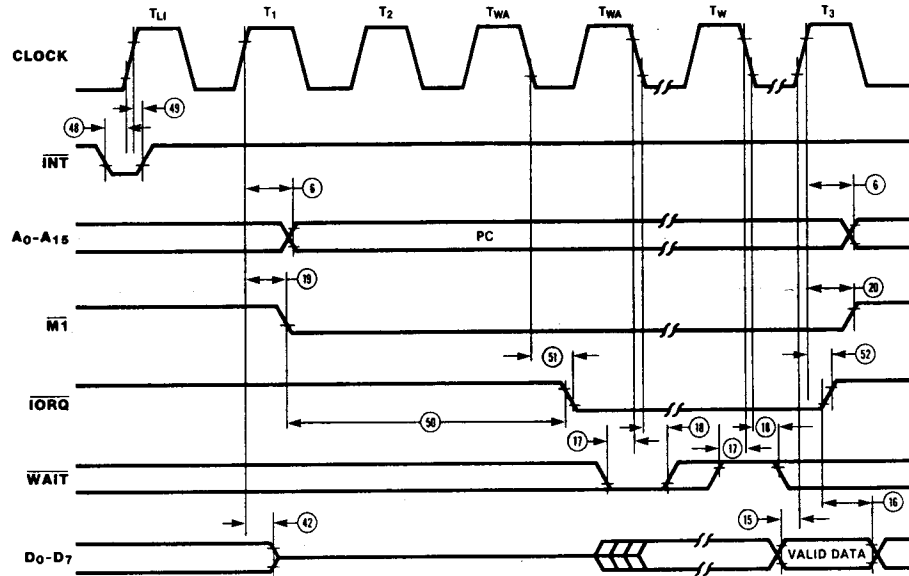


Figure 5. Instruction Opcode Fetch

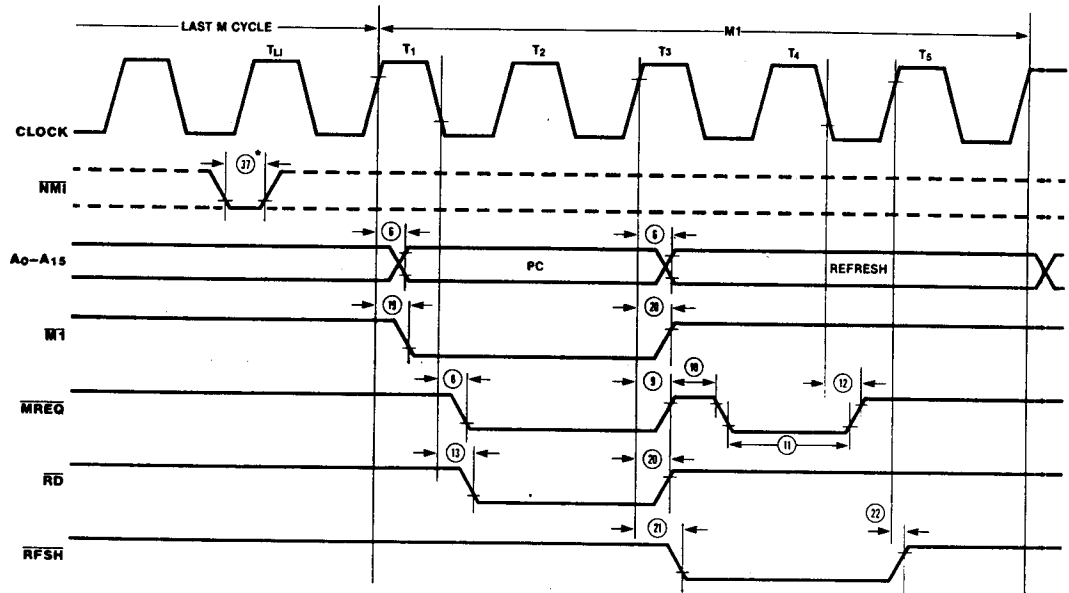
Interrupt Request/Acknowledge Cycle. The CPU samples the interrupt signal with the rising edge of the last clock cycle at the end of any instruction (Figure 8). When an interrupt is accepted, a special M1 cycle is generated.

During this $\overline{M1}$ cycle, \overline{IORQ} becomes active (instead of \overline{MREQ}) to indicate that the interrupting device can place an 8-bit vector on the data bus. The CPU automatically adds two Wait states to this cycle.



Non-Maskable Interrupt Request Cycle. \overline{NMI} is sampled at the same time as the maskable interrupt input \overline{INT} but has higher priority and cannot be disabled under software control. The subsequent timing is similar to that of a normal

memory read operation except that data put on the bus by the memory is ignored. The CPU instead executes a restart (RST) operation and jumps to the \overline{NMI} service routine located at address 0066H (Figure 9).



*Although \overline{NMI} is an asynchronous input, to guarantee its being recognized on the following machine cycle, \overline{NMI} 's falling edge must occur no later than the rising edge of the clock cycle preceding the last state of any instruction cycle (T_{L1}).

Figure 9. Non-Maskable Interrupt Request Operation

Power-Down mode of operation (Only applies to CMOS Z80 CPU).

CMOS Z80 CPU supports Power-Down mode of operation.

This mode is also referred to as the "standby mode", and supply current for the CPU goes down as low as 10 uA (Where specified as I_{cc2}).

Power-Down Acknowledge Cycle. When the clock input to the CPU is stopped at either a High or Low level, the CPU stops its operation and maintains all registers and control signals. However, I_{cc2} (standby supply current) is guaranteed only when the system clock is stopped at a Low

level during T_4 of the machine cycle following the execution of the HALT instruction. The timing diagram for the power-down function, when implemented with the HALT instruction, is shown in Figure 13.

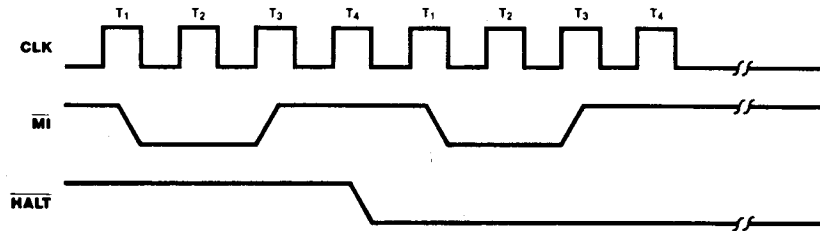


Figure 13. Power-Down Acknowledge

Power-Down Release Cycle. The system clock must be supplied to the CPU to release the power-down state. When the system clock is supplied to the CLK input, the CPU restarts operations from the point at which the power-down state was implemented. The timing diagrams for the release from power-down mode are shown in Figure 14.

NOTES:

- 1) When the external oscillator has been stopped to enter the power-down state, some warm-up time may be required to obtain a stable clock for the release.
- 2) When the HALT instruction is executed to enter the power-down state, the CPU will also enter the Halt state. An interrupt signal (either $\overline{\text{NMI}}$ or $\overline{\text{INT}}$) or a RESET signal must be applied to the CPU after the system clock is supplied in order to release the power-down state.

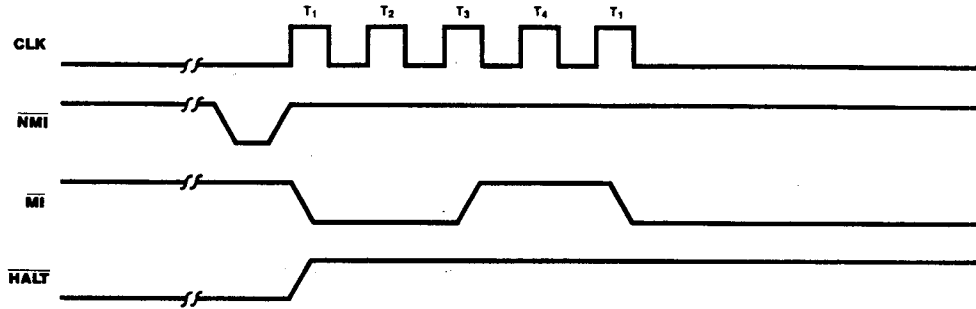


Figure 14a.

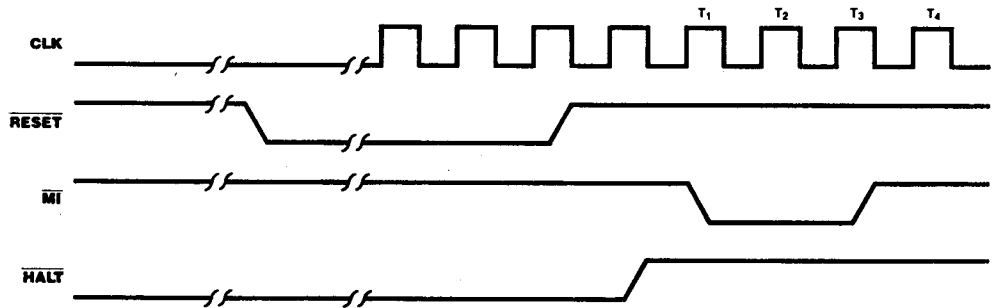


Figure 14b.

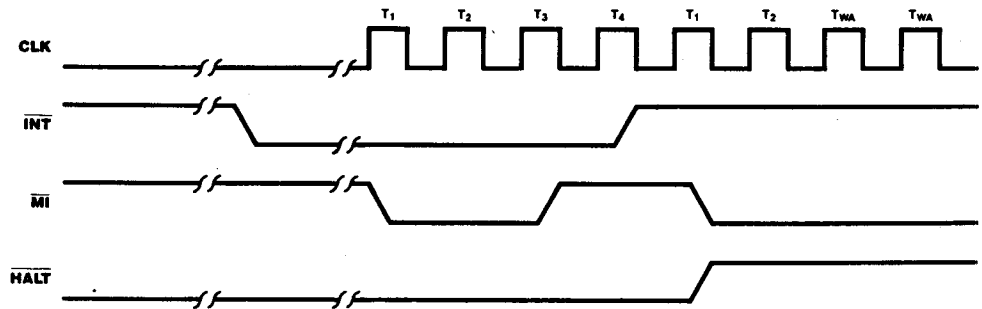


Figure 14c.

Figure 13. Power-Down Release

ABSOLUTE MAXIMUM RATINGS

Voltage on V_{CC} with respect to V_{SS}	-0.3V to +7V
Voltages on all inputs with respect to V_{SS}	-0.3V to $V_{CC} + 0.3V$
Operating Ambient Temperature	See Ordering Information
Storage Temperature	-65°C to +150°C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

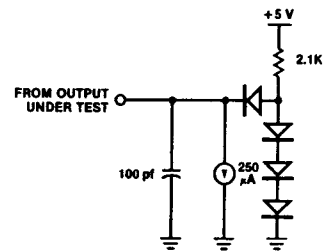
The DC Characteristics and capacitance sections below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND (0V). Positive current flows into the referenced pin.

The Ordering Information section lists temperature ranges and product numbers. Package drawings are in the Package Information section. Refer to the Literature List for additional documentation.

Available operating temperature ranges are:

- **S = 0°C to +70°C**
Voltage Supply Range:
 NMOS: $+4.75V \leq V_{CC} \leq +5.25V$
 CMOS: $+4.50V \leq V_{CC} \leq +5.50V$
- **E = -40°C to 100°C, $+4.50V \leq V_{CC} \leq +5.50V$**

All ac parameters assume a load capacitance of 100 pf. Add 10 ns delay for each 50 pf increase in load up to a maximum of 200 pf for the data bus and 100 pf for address and control lines. AC timing measurements are referenced to 1.5 volts (except for clock, which is referenced to the 10% and 90% points).



DC CHARACTERISTICS (Z84C00/CMOS Z80 CPU)

Symbol	Parameter	Min	Max	Unit	Condition
V _{ILC}	Clock Input Low Voltage	-0.3	0.45	V	
V _{IHC}	Clock Input High Voltage	V _{CC} - .6	V _{CC} + .3	V	
V _{IL}	Input Low Voltage	-0.3	0.8	V	
V _{IH}	Input High Voltage	2.2	V _{CC}	V	
V _{OL}	Output Low Voltage		0.4	V	I _{OL} = 2.0 mA
V _{OH1}	Output High Voltage	2.4		V	I _{OH} = -1.6 mA
V _{OH2}	Output High Voltage	V _{CC} - 0.8		V	I _{OH} = -250 μA
I _{CC1}	Power Supply Current	4 MHz	20	mA	V _{CC} = 5V
		6 MHz	30	mA	V _{IH} = V _{CC} - 0.2V
		8 MHz	40	mA	V _{IL} = 0.2V
		10 MHz	50	mA	
I _{CC2}	Standby Supply Current	20 MHz	100	mA	V _{CC} = 5V
			10	μA	V _{CC} = 5V
					CLK = (0)
					V _{IH} = V _{CC} - 0.2V
					V _{IL} = 0.2V
I _{LI}	Input Leakage Current	-10	10	μA	V _{IN} = 0.4 to V _{CC}
I _{LO}	3-State Output Leakage Current in Float	-10	10 ²	μA	V _{OUT} = 0.4 to V _{CC}

1. Measurements made with outputs floating.
2. A₁₅-A₀, D₇-D₀, MREQ, IORQ, RD, and WR.
3. I_{CC2} standby supply current is guaranteed only when the supplied clock is stopped at a low level during T₄ of the machine cycle immediately following the execution of a HALT instruction.

CAPACITANCE

Symbol	Parameter	Min	Max	Unit
C _{CLOCK}	Clock Capacitance		10	pf
C _{IN}	Input Capacitance		5	pf
C _{OUT}	Output Capacitance		15	pf

T_A = 25°C, f = 1 MHz.
Unmeasured pins returned to ground.

AC CHARACTERISTICS† (Z84C00/CMOS Z80 CPU)

V_{cc}=5.0V ± 10%, unless otherwise specified

No	Symbol	Parameter	Z84C0004**		Z84C0006		Z84C0008		Z84C0010		Z84C0020[1]		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
1	TcC	Clock Cycle time	250*	DC	162*	DC	125*	DC	100*	DC	50*	DC	nS	
2	TwCh	Clock Pulse width (high)	110	DC	65	DC	55	DC	40	DC	20	DC	nS	
3	TwCl	Clock Pulse width (low)	110	DC	65	DC	55	DC	40	DC	20	DC	nS	
4	TfC	Clock Fall time		30		20		10		10		10	nS	
5	TrC	Clock Rise time		30		20		10		10		10	nS	
6	TdCr(A)	Address valid from Clock Rise		110		90		80		65		57	nS	[2]
7	TdA(MREQf)	Address valid to /MREQ Fall	65*		35*		20*		5*		-15*		nS	
8	TdCf(MREQf)	Clock Fall to /MREQ Fall delay		85		70		60		55		40	nS	
9	TdCr(MREQr)	Clock Rise to /MREQ Rise delay		85		70		60		55		40	nS	
10	TwMREQh	/MREQ pulse width (High)	110*		65*		45**		30*		10*		nS	[3]
11	TwMREQl	/MREQ pulse width (low)	220*		132*		100*		75*		25*		nS	[3]
12	TdCf(MERQr)	Clock Fall to /MREQ Rise delay		85		70		60		55		40	nS	
13	TdCf(RDf)	Clock Fall to /RD Fall delay		95		80		70		65		40	nS	
14	TdCr(RDr)	Clock Rise to /RD Rise delay		85		70		60		55		40	nS	
15	TsD(Cr)	Data setup time to Clock Rise	35		30		30		25		12		nS	
16	ThD(RDr)	Data hold time after /RD Rise	0		0		0		0		0		nS	
17	TsWAIT(Cf)	/WAIT setup time to Clock Fall	70		60		50		20		7.5		nS	
18	ThWAIT(Cf)	/WAIT hold time after Clock Fall	10		10		10		10		10		nS	
19	TdCr(M1f)	Clock Rise to /M1 Fall delay		100		80		70		65		45	nS	
20	TdCr(M1r)	Clock Rise to /M1 Rise delay		100		80		70		65		45	nS	
21	TdCr(RFSHf)	Clock Rise to /RFSH Fall delay		130		110		95		80		60	nS	
22	TdCr(RFSHr)	Clock Rise to /RFSH Rise delay		120		100		85		80		60	nS	
23	TdCf(RDr)	Clock Fall to /RD Rise delay		85		70		60		55		40	nS	
24	TdCr(RDf)	Clock Rise to /RD Fall delay		85		70		60		55		40	nS	
25	TsD(Cf)	Data setup to Clock Fall during M2, M3, M4 or M5 cycles		50		40		30		25		12	nS	
26	TdA(IORQf)	Address stable prior to /IORQ Fall	180*		107*		75*		50*		0*		nS	
27	TdCr(IORQf)	Clock Rise to /IORQ Fall delay		75		65		55		50		40	nS	
28	TdCf(IORQr)	Clock Fall to /IORQ Rise delay		85		70		60		55		40	nS	
29	TdD(WRf)Mw	Data stable prior to /WR Fall	80*		22*		5*		40*		-10*		nS	
30	TdCf(WRf)	Clock Fall to /WR Fall delay		80		70		60		55		40	nS	
31	TwWR	/WR pulse width	220*		132*		100*		75*		25*		nS	
32	TdCf(WRr)	Clock Fall to /WR Rise delay		80		70		60		55		40	nS	
33	TdD(WRf)IO	Data stable prior to /WR Fall	-10*		-55*		-55*		-10*		-30*		nS	
34	TdCr(WRf)	Clock Rise to /WR Fall delay		65		60		60		50		40	nS	
35	TdWRr(D)	Data stable from /WR Rise	60*		30*		15*		10*		0*		nS	
36	TdCf(HALT)	Clock Fall to /HALT 'L' or 'H'		300		260		225		90		70	nS	
37	TwNMI	/NMI pulse width	80		60		60		60		60		nS	
38	TsBUSREQ (Cr)	/BUSREQ setup time to Clock Rise	50		50		40		30		15		nS	

*For clock periods other than the minimums shown, calculate parameters using the table on the following page.
Calculated values above assumed TrC = TtC = 20 ns.

†Units in nanoseconds (ns).

†† For loading ≥ 50 pf. Decrease width by 10 ns for each additional 50 pf.

**4 MHz CMOS Z80 is obsoleted and replaced by 6 MHz

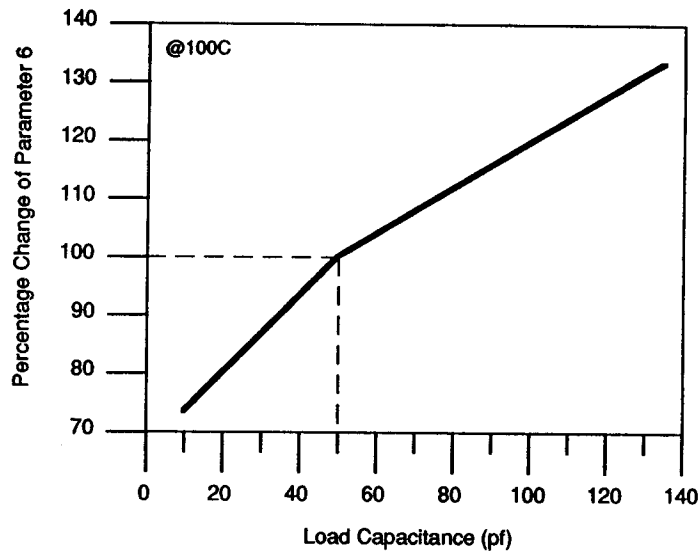


Figure 1. Address Delay Characteristics (Parameter 6)

DC CHARACTERISTICS (Z8400/NMOS Z80 CPU)

All parameters are tested unless otherwise noted.

Symbol	Parameter	Min	Max	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	-0.3	0.45	V	
V_{IHC}	Clock Input High Voltage	$V_{CC} - .6$	$V_{CC} + .3$	V	
V_{IL}	Input Low Voltage	-0.3	0.8	V	
V_{IH}	Input High Voltage	2.0^1	V_{CC}	V	
V_{OL}	Output Low Voltage		0.4	V	$I_{OL} = 2.0 \text{ mA}$
V_{OH}	Output High Voltage	2.4^1		V	$I_{OH} = -250 \mu\text{A}$
I_{CC}	Power Supply Current		200	mA	Note 3
I_{LI}	Input Leakage Current		10	μA	$V_{IN} = 0 \text{ to } V_{CC}$
I_{LO}	3-State Output Leakage Current in Float	-10	10^2	μA	$V_{OUT} = 0.4 \text{ to } V_{CC}$

1. For military grade parts, refer to the Z80 Military Electrical Specification.

2. A_{15} - A_0 , D_7 - D_0 , $MREQ$, $IORD$, RD , and WR .

3. Measurements made with outputs floating.

CAPACITANCE

Guaranteed by design and characterization.

Symbol	Parameter	Min	Max	Unit
C_{CLOCK}	Clock Capacitance		35	pf
C_{IN}	Input Capacitance		5	pf
C_{OUT}	Output Capacitance		15	pf

NOTES:

$T_A = 25^\circ\text{C}$, $f = 1 \text{ MHz}$.

Unmeasured pins returned to ground.

AC CHARACTERISTICS† (Z8400/NMOS Z80 CPU)

Number	Symbol	Parameter	Z0840004		Z0840006		Z0840008	
			Min	Max	Min	Max	Min	Max
1	TcC	Clock Cycle Time	250*		162*		125*	
2	TwCh	Clock Pulse Width (High)	110	2000	65	2000	55	2000
3	TwCl	Clock Pulse Width (Low)	110	2000	65	2000	55	2000
4	TfC	Clock Fall Time		30		20		10
5	TrC	Clock Rise Time		30		20		10
6	TdCr(A)	Clock ↑ to Address Valid Delay		110		90		80
7	TdA(MREQf)	Address Valid to $\overline{\text{MREQ}}$ ↓ Delay	65*		35*		20*	
8	TdCf(MREQf)	Clock ↓ to $\overline{\text{MREQ}}$ ↓ Delay		85		70		60
9	TdCr(MREQr)	Clock ↑ to $\overline{\text{MREQ}}$ ↑ Delay		85		70		60
10	TwMREQh	$\overline{\text{MREQ}}$ Pulse Width (High)	110*††		65*††		45*††	
11	TwMREQl	$\overline{\text{MREQ}}$ Pulse Width (Low)	220*††		135*††		100*††	
12	TdCf(MREQr)	Clock ↓ to $\overline{\text{MREQ}}$ ↑ Delay		85		70		60
13	TdCf(RDf)	Clock ↓ to $\overline{\text{RD}}$ ↓ Delay		95		80		70
14	TdCr(RDr)	Clock ↑ to $\overline{\text{RD}}$ ↑ Delay		85		70		60
15	TsD(Cr)	Data Setup Time to Clock ↑	35		30		30	
16	ThD(RDr)	Data Hold Time to $\overline{\text{RD}}$ ↑		0		0		0
17	TsWAIT(Cf)	$\overline{\text{WAIT}}$ Setup Time to Clock ↓	70		60		50	
18	ThWAIT(Cf)	$\overline{\text{WAIT}}$ Hold Time after Clock ↓		0		0		0
19	TdCr(M1f)	Clock ↑ to $\overline{\text{M1}}$ ↓ Delay		100		80		70
20	TdCr(M1r)	Clock ↑ to $\overline{\text{M1}}$ ↑ Delay		100		80		70
21	TdCr(RFSHf)	Clock ↑ to $\overline{\text{RFSH}}$ ↓ Delay		130		110		95
22	TdCr(RFSHr)	Clock ↑ to $\overline{\text{RFSH}}$ ↑ Delay		120		100		85
23	TdCf(RDr)	Clock ↓ to $\overline{\text{RD}}$ ↑ Delay		85		70		60
24	TdCr(RDf)	Clock ↑ to $\overline{\text{RD}}$ ↓ Delay		85		70		60
25	TsD(Cf)	Data Setup to Clock ↓ during M ₂ , M ₃ , M ₄ , or M ₅ Cycles	50		40		30	
26	TdA(IORQf)	Address Stable prior to $\overline{\text{IORQ}}$ ↓	180*		110*		75*	
27	TdCr(IORQf)	Clock ↑ to $\overline{\text{IORQ}}$ ↓ Delay		75		65		55
28	TdCf(IORQr)	Clock ↓ to $\overline{\text{IORQ}}$ ↑ Delay		85		70		60
29	TdD(WRf)	Data Stable prior to $\overline{\text{WR}}$ ↓	80*		25*		5*	
30	TdCf(WRf)	Clock ↓ to $\overline{\text{WR}}$ ↓ Delay		80		70		60
31	TwWR	$\overline{\text{WR}}$ Pulse Width	220*		135*		100*	
32	TdCf(WRr)	Clock ↓ to $\overline{\text{WR}}$ ↑ Delay		80		70		60
33	TdD(WRf)	Data Stable prior to $\overline{\text{WR}}$ ↓	-10*		-55*		55*	
34	TdCr(WRf)	Clock ↑ to $\overline{\text{WR}}$ ↓ Delay		65		60		55
35	TdWRr(D)	Data Stable from $\overline{\text{WR}}$ ↑	60*		30*		15*	
36	TdCf(HALT)	Clock ↓ to $\overline{\text{HALT}}$ ↑ or ↓		300		260		225
37	TwNMI	$\overline{\text{NMI}}$ Pulse Width	80		70		60*	
38	TsBUSREQ(Cr)	$\overline{\text{BUSREQ}}$ Setup Time to Clock ↑	50		50		40	

*For clock periods other than the minimums shown, calculate parameters using the table on the following page. Calculated values above assumed TrC = TfC = 20 ns.

†Units in nanoseconds (ns).

†† For loading ≥ 50 pf., Decrease width by 10 ns for each additional 50 pf.

Customer Support

For answers to technical questions about the product, documentation, or any other issues with Zilog's offerings, please visit Zilog's Knowledge Base at <http://www.zilog.com/kb>.

For any comments, detail technical questions, or reporting problems, please visit Zilog's Technical Support at <http://support.zilog.com>.