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Details

Table 1. Z80C CPU Registers

Register		Size (Bits)	Remarks
A, A'	Accumulator	8	Stores an operand or the results of an operation.
F, F'	Flags	8	See Instruction Set.
B, B'	General Purpose	8	Can be used separately or as a 16-bit register with C.
C, C'	General Purpose	8	Can be used separately or as a 16-bit register with B.
D, D'	General Purpose	8	Can be used separately or as a 16-bit register with E.
E, E'	General Purpose	8	Can be used separately or as a 16-bit register with D.
H, H'	General Purpose	8	Can be used separately or as a 16-bit register with L.
L, L'	General Purpose	8	Can be used separately or as a 16-bit register with H.
Note: The (B,C), (D,E), and (H,L) sets are combined as follows:			
B — High byte C — Low byte			
D — High byte E — Low byte			
H — High byte L — Low byte			
I	Interrupt Register	8	Stores upper eight bits of memory address for vectored interrupt processing.
R	Refresh Register	8	Provides user-transparent dynamic memory refresh. Automatically incremented and placed on the address bus during each instruction fetch cycle.
IX	Index Register	16	Used for indexed addressing.
IY	Index Register	16	Used for indexed addressing.
SP	Stack Pointer	16	Holds address of the top of the stack. See Push or Pop in instruction set.
PC	Program Counter	16	Holds address of next instruction.
IFF ₁ -IFF ₂	Interrupt Enable	Flip-Flops	Set or reset to indicate interrupt status (see Figure 4).
IMFa-IMFb	Interrupt Mode	Flip-Flops	Reflect Interrupt mode (see Figure 4).

failure has been detected. After recognition of the $\overline{\text{NMI}}$ signal (providing $\overline{\text{BUSREQ}}$ is not active), the CPU jumps to restart location 0066H. Normally, software starting at this address contains the interrupt service routine.

Maskable Interrupt ($\overline{\text{INT}}$). Regardless of the interrupt mode set by the user, the CPU response to a maskable interrupt input follows a common timing cycle. After the interrupt has been detected by the CPU (provided that interrupts are enabled and $\overline{\text{BUSREQ}}$ is not active) a special interrupt processing cycle begins. This is a special fetch ($\overline{\text{M1}}$) cycle in which $\overline{\text{IORQ}}$ becomes active rather than $\overline{\text{MREQ}}$, as in a normal $\overline{\text{M1}}$ cycle. In addition, this special $\overline{\text{M1}}$ cycle is automatically extended by two $\overline{\text{WAIT}}$ states, to allow for the time required to acknowledge the interrupt request.

Mode 0 Interrupt Operation. This mode is similar to the 8080 microprocessor interrupt service procedures. The interrupting device places an instruction on the data bus. This is normally a Restart instruction, which will initiate a call

to the selected one of eight restart locations in page zero of memory. Unlike the 8080, the Z80 CPU responds to the Call instruction with only one interrupt acknowledge cycle followed by two memory read cycles.

Mode 1 Interrupt Operation. Mode 1 operation is very similar to that for the NMI. The principal difference is that the Mode 1 interrupt has only one restart location, 003BH.

Mode 2 Interrupt Operation. This interrupt mode has been designed to most effectively utilize the capabilities of the Z80 microprocessor and its associated peripheral family. The interrupting peripheral device selects the starting address of the interrupt service routine. It does this by placing an 8-bit vector on the data bus during the interrupt acknowledge cycle. The CPU forms a pointer using this byte as the lower 8 bits and the contents of the I register as the upper 8 bits. This points to an entry in a table of addresses for interrupt service routines. The CPU then jumps to the routine at that

address. This flexibility in selecting the interrupt service routine address allows the peripheral device to use several different types of service routines. These routines may be located at any available location in memory. Since the interrupting device supplies the low-order byte of the 2-byte vector, bit 0 (A_0) must be a zero.

Interrupt Enable/Disable Operation. Two flip-flops, IFF₁ and IFF₂, referred to in the register description, are used to signal the CPU interrupt status. Operation of the two flip-flops is described in Table 2. For more details, refer to the *Z80 CPU Technical Manual* (03-0029-01) and *Z80 Assembly Language Programming Manual* (03-0002-01).

Table 2. State of Flip-Flops

Action	IFF ₁	IFF ₂	Comments
CPU Reset	0	0	Maskable interrupt INT disabled
DI instruction execution	0	0	Maskable interrupt INT disabled
EI instruction execution	1	1	Maskable interrupt INT enabled
LD A,I instruction execution	•	•	IFF ₂ → Parity flag
LD A,R instruction execution	•	•	IFF ₂ → Parity flag
Accept NMI	0	•	Maskable interrupt INT disabled
RETN instruction execution	IFF ₂	•	IFF ₂ → IFF ₁ at completion of an NMI service routine.

INSTRUCTION SET

The microprocessor has one of the most powerful and versatile instruction sets available in any 8-bit microprocessor. It includes such unique operations as a block move for fast, efficient data transfers within memory, or between memory and I/O. It also allows operations on any bit in any location in memory.

The following is a summary of the instruction set which shows the assembly language mnemonic, the operation, the flag status, and gives comments on each instruction. For an explanation of flag notations and symbols for mnemonic tables, see the Symbolic Notations section which follows these tables. The *Z80 CPU Technical Manual* (03-0029-01), the *Programmer's Reference Guide* (03-0012-03), and *Assembly Language Programming Manual* (03-0002-01) contain significantly more details for programming use.

The instructions are divided into the following categories:

- ☐ 8-bit loads
- ☐ 16-bit loads
- ☐ Exchanges, block transfers, and searches
- ☐ 8-bit arithmetic and logic operations
- ☐ General-purpose arithmetic and CPU control
- ☐ 16-bit arithmetic operations
- ☐ Rotates and shifts

- ☐ Bit set, reset, and test operations
- ☐ Jumps
- ☐ Calls, returns, and restarts
- ☐ Input and output operations

A variety of addressing modes are implemented to permit efficient and fast data transfer between various registers, memory locations, and input/output devices. These addressing modes include:

- ☐ Immediate
- ☐ Immediate extended
- ☐ Modified page zero
- ☐ Relative
- ☐ Extended
- ☐ Indexed
- ☐ Register
- ☐ Register indirect
- ☐ Implied
- ☐ Bit

8-BIT LOAD GROUP (Continued)

Mnemonic	Symbolic Operation	S	Z	Flags H	P/V	N	C	Opcode 76 543 210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
LD (IY+d), n	(IY+d) ← n	•	•	X	•	X	•	•	11 111 101 FD 00 110 110 36	4	5	19	
									← d → ← n →				
LD A, (BC)	A ← (BC)	•	•	X	•	X	•	•	00 001 010 0A	1	2	7	
LD A, (DE)	A ← (DE)	•	•	X	•	X	•	•	00 011 010 1A	1	2	7	
LD A, (nn)	A ← (nn)	•	•	X	•	X	•	•	00 111 010 3A	3	4	13	
									← n → ← n →				
LD (BC), A	(BC) ← A	•	•	X	•	X	•	•	00 000 010 02	1	2	7	
LD (DE), A	(DE) ← A	•	•	X	•	X	•	•	00 010 010 12	1	2	7	
LD (nn), A	(nn) ← A	•	•	X	•	X	•	•	00 110 010 32	3	4	13	
									← n → ← n →				
LDA, I	A ← I	‡	‡	X	0	X	IFF	0	• 11 101 101 ED 01 010 111 57	2	2	9	
LDA, R	A ← R	‡	‡	X	0	X	IFF	0	• 11 101 101 ED 01 011 111 5F	2	2	9	
LD I, A	I ← A	•	•	X	•	X	•	•	11 101 101 ED 01 000 111 47	2	2	9	
LDR, A	R ← A	•	•	X	•	X	•	•	11 101 101 ED 01 001 111 4F	2	2	9	

NOTE: IFF, the content of the interrupt enable flip-flop, (IFF₂), is copied into the P/V flag.

16-BIT LOAD GROUP

Mnemonic	Symbolic Operation	S	Z	Flags H	P/V	N	C	Opcode 76 543 210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
LD dd, nn	dd ← nn	•	•	X	•	X	•	•	00 dd0 001	3	3	10	dd Pair 00 BC 01 DE
									← n → ← n →				
LD IX, nn	IX ← nn	•	•	X	•	X	•	•	11 011 101 DD 00 100 001 21	4	4	14	10 HL 11 SP
									← n → ← n →				
LD IY, nn	IY ← nn	•	•	X	•	X	•	•	11 111 101 FD 00 100 001 21	4	4	14	
									← n → ← n →				
LD HL, (nn)	H ← (nn+1) L ← (nn)	•	•	X	•	X	•	•	00 101 010 2A	3	5	16	
									← n → ← n →				
LD dd, (nn)	dd _H ← (nn+1) dd _L ← (nn)	•	•	X	•	X	•	•	11 101 101 ED 01 dd1 011	4	6	20	
									← n → ← n →				

NOTE: (PAIR)_H, (PAIR)_L refer to high order and low order eight bits of the register pair respectively. e.g., BC_L = C, AF_H = A.

16-BIT LOAD GROUP (Continued)

Mnemonic	Symbolic Operation	S	Z	Flags H	P/V	N	C	76	543	210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
LD IX, (nn)	$IX_H \leftarrow (nn+1)$ $IX_L \leftarrow (nn)$	•	•	X	•	X	•	•	11	011 101	DD	4	6	20	
									00	101 010	2A				
									$\leftarrow n \rightarrow$						
									$\leftarrow n \rightarrow$						
LD IY, (nn)	$IY_H \leftarrow (nn+1)$ $IY_L \leftarrow (nn)$	•	•	X	•	X	•	•	11	111 101	FD	4	6	20	
									00	101 010	2A				
									$\leftarrow n \rightarrow$						
									$\leftarrow n \rightarrow$						
LD (nn), HL	$(nn+1) \leftarrow H$ $(nn) \leftarrow L$	•	•	X	•	X	•	•	00	100 010	22	3	5	16	
									$\leftarrow n \rightarrow$						
									$\leftarrow n \rightarrow$						
LD (nn), dd	$(nn+1) \leftarrow dd_H$ $(nn) \leftarrow dd_L$	•	•	X	•	X	•	•	11	101 101	ED	4	6	20	
									01	dd0 011					
									$\leftarrow n \rightarrow$						
									$\leftarrow n \rightarrow$						
LD (nn), IX	$(nn+1) \leftarrow IX_H$ $(nn) \leftarrow IX_L$	•	•	X	•	X	•	•	11	011 101	DD	4	6	20	
									00	100 010	22				
									$\leftarrow n \rightarrow$						
									$\leftarrow n \rightarrow$						
LD (nn), IY	$(nn+1) \leftarrow IY_H$ $(nn) \leftarrow IY_L$	•	•	X	•	X	•	•	11	111 101	FD	4	6	20	
									00	100 010	22				
									$\leftarrow n \rightarrow$						
									$\leftarrow n \rightarrow$						
LD SP, HL	$SP \leftarrow HL$	•	•	X	•	X	•	•	11	111 001	F9	1	1	6	
LD SP, IX	$SP \leftarrow IX$	•	•	X	•	X	•	•	11	011 101	DD	2	2	10	
									11	111 001	F9				
LD SP, IY	$SP \leftarrow IY$	•	•	X	•	X	•	•	11	111 101	FD	2	2	10	
									11	111 001	F9				
PUSH qq	$(SP-2) \leftarrow qq_L$ $(SP-1) \leftarrow qq_H$ $SP \rightarrow SP-2$	•	•	X	•	X	•	•	11	qq0 101		1	3	11	qq BC
															01 DE
															10 HL
PUSH IX	$(SP-2) \leftarrow IX_L$ $(SP-1) \leftarrow IX_H$ $SP \rightarrow SP-2$	•	•	X	•	X	•	•	11	011 101	DD	2	4	15	11 AF
									11	100 101	E5				
PUSH IY	$(SP-2) \leftarrow IY_L$ $(SP-1) \leftarrow IY_H$ $SP \rightarrow SP-2$	•	•	X	•	X	•	•	11	111 101	FD	2	4	15	
									11	100 101	E5				
POP qq	$qq_H \leftarrow (SP+1)$ $qq_L \leftarrow (SP)$ $SP \rightarrow SP+2$	•	•	X	•	X	•	•	11	qq0 001		1	3	10	
POP IX	$IX_H \leftarrow (SP+1)$ $IX_L \leftarrow (SP)$ $SP \rightarrow SP+2$	•	•	X	•	X	•	•	11	011 101	DD	2	4	14	
									11	100 001	E1				
POP IY	$IY_H \leftarrow (SP+1)$ $IY_L \leftarrow (SP)$ $SP \rightarrow SP+2$	•	•	X	•	X	•	•	11	111 101	FD	2	4	14	
									11	100 001	E1				

NOTE: (PAIR)_H, (PAIR)_L refer to high order and low order eight bits of the register pair respectively, e.g., BC_L = C, AF_H = A.

8-BIT ARITHMETIC AND LOGICAL GROUP (Continued)

Mnemonic	Symbolic Operation	Flags			P/V/N/C			Opcode			Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
		S	Z	H				76	543	210					
INC r	$r \leftarrow r + 1$	†	†	X	†	X	V	0	•	00 r	100	1	1	4	
INC (HL)	(HL) $\leftarrow$ (HL) + 1	†	†	X	†	X	V	0	•	00 110	100	1	3	11	
INC (IX+d)	(IX+d) $\leftarrow$ (IX+d) + 1	†	†	X	†	X	V	0	•	11 011 101	DD	3	6	23	
										00 110	100				
										$\leftarrow d \rightarrow$					
INC (IY+d)	(IY+d) $\leftarrow$ (IY+d) + 1	†	†	X	†	X	V	0	•	11 111 101	FD	3	6	23	
										00 110	100				
										$\leftarrow d \rightarrow$					
DEC m	$m \leftarrow m - 1$	†	†	X	†	X	V	1	•		101				

NOTE: m is any of r, (HL), (IX+d), (IY+d) as shown for INC. DEC same format and states as INC. Replace 100 with 101 in opcode.

GENERAL-PURPOSE ARITHMETIC AND CPU CONTROL GROUPS

Mnemonic	Symbolic Operation	Flags			P/V/N/C			Opcode			Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
		S	Z	H				76	543	210					
DAA	@	†	†	X	†	X	P	•	†	00 100 111	27	1	1	4	Decimal adjust accumulator
CPL	$A \leftarrow A$	•	•	X	1	X	•	1	•	00 101 111	2F	1	1	4	Complement accumulator (one's complement)
NEG	$A \leftarrow 0 - A$	†	†	X	†	X	V	1	†	11 101 101	ED	2	2	8	Negate acc. (two's complement)
								01	000	100	44				
CCF	$CY \leftarrow CY$	•	•	X	X	X	•	0	†	00 111 111	3F	1	1	4	Complement carry flag
SCF	$CY \leftarrow 1$	•	•	X	0	X	•	0	1	00 110 111	37	1	1	4	Set carry flag
NOP	No operation	•	•	X	•	X	•	•	•	00 000 000	00	1	1	4	
HALT	CPU halted	•	•	X	•	X	•	•	•	01 110 110	76	1	1	4	
DI *	$IFF \leftarrow 0$	•	•	X	•	X	•	•	•	11 110 011	F3	1	1	4	
EI *	$IFF \leftarrow 1$	•	•	X	•	X	•	•	•	11 111 011	FB	1	1	4	
IM 0	Set interrupt mode 0	•	•	X	•	X	•	•	•	11 101 101	ED	2	2	8	
								01	000	110	46				
IM 1	Set interrupt mode 1	•	•	X	•	X	•	•	•	11 101 101	ED	2	2	8	
								01	010	110	56				
IM 2	Set interrupt mode 2	•	•	X	•	X	•	•	•	11 101 101	ED	2	2	8	
								01	011	110	5E				

NOTES: @ converts accumulator content into packed BCD following add or subtract with packed BCD operands.

IFF indicates the interrupt enable flip-flop.

CY indicates the carry flip-flop.

* indicates interrupts are not sampled at the end of EI or DI.

ROTATE AND SHIFT GROUP (Continued)

Symbolic Mnemonic Operation	S	Z	Flags H P/V N C	Opcode 76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
RLC r	†	†	X 0 X P 0 *	11 001 011 CB 00 000 r	2	2	8	Rotate left circular register r.
RLC (HL)	†	†	X 0 X P 0 †	11 001 011 CB 00 000 110	2	4	15	r Reg. 000 B 001 C 010 D 011 E 001 H 101 L 111 A
RLC (IX+d)	†	†	X 0 X P 0 †	11 011 101 DD 11 001 011 CB 00 000 110	4	6	23	
RLC (IY+d)	†	†	X 0 X P 0 †	11 111 101 FD 11 001 011 CB 00 000 110	4	6	23	
RL m	†	†	X 0 X P 0 †	00 000 010				Instruction format and states are as shown for RLCs. To form new opcode, replace 000 or RLCs with shown code.
RRC m	†	†	X 0 X P 0 †	001				
RR m	†	†	X 0 X P 0 †	011				
SLA m	†	†	X 0 X P 0 †	100				
SRA m	†	†	X 0 X P 0 †	101				
SRL m	†	†	X 0 X P 0 †	111				
RLD	†	†	X 0 X P 0 *	11 101 101 ED 01 101 111 6F	2	5	18	Rotate digit left and right between the accumulator and location (HL).
RRD	†	†	X 0 X P 0 *	11 101 101 ED 01 100 111 67	2	5	18	The content of the upper half of the accumulator is unaffected.

JUMP GROUP

Mnemonic	Symbolic Operation	Flags					Opcode			Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments	
		S	Z	H	P/V/N	C	76	543	210						
JP nn	PC ← nn	•	•	X	•	X	•	•	•	11 000 011	C3	3	3	10	cc Condition 000 NZ (non-zero) 001 Z (zero)
JP cc, nn	If condition cc is true PC←nn, otherwise continue	•	•	X	•	X	•	•	•	11 cc 010		3	3	10	010 NC (non-carry)
										011 C (carry)					
										100 PO (parity odd)					
										101 PE (parity even)					
JR e	PC ← PC+e	•	•	X	•	X	•	•	•	00 011 000	18	2	3	12	110 P (sign positive) 111 M (sign negative)
JR C, e	If C=0, continue If C=1, PC←PC+e	•	•	X	•	X	•	•	•	00 111 000	38	2	2	7	If condition not met.
JR NC, e	If C=1, continue If C=0, PC←PC+e	•	•	X	•	X	•	•	•	00 110 000	30	2	2	7	If condition not met.
JP Z, e	If Z=0 continue If Z=1, PC←PC+e	•	•	X	•	X	•	•	•	00 101 000	28	2	2	7	If condition not met.
JR NZ, e	If Z=1, continue If Z=0, PC←PC+e	•	•	X	•	X	•	•	•	00 100 000	20	2	2	7	If condition not met.
JP (HL)	PC ← HL	•	•	X	•	X	•	•	•	11 101 001	E9	1	1	4	
JP (IX)	PC ← IX	•	•	X	•	X	•	•	•	11 011 101	DD	2	2	8	
										11 101 001					
JP (IY)	PC ← IY	•	•	X	•	X	•	•	•	11 111 101	FD	2	2	8	
										11 101 001					
DJNZ, e	B ← B - 1 If B=0, continue If B≠0, PC ← PC+e	•	•	X	•	X	•	•	•	00 010 000	10	2	2	8	If B=0
												2	3	13	If B≠0.

NOTES: e represents the extension in the relative addressing mode.

e is a signed two's complement number in the range < -126, 129 >.

e - 2 in the opcode provides an effective address of pc + e as PC is incremented by 2 prior to the addition of e.

CPU TIMING

The Z80 CPU executes instructions by proceeding through a specific sequence of operations:

- Memory read or write
- I/O device read or write
- Interrupt acknowledge

The basic clock period is referred to as a T time or cycle, and three or more T cycles make up a machine cycle (M1, M2 or M3 for instance). Machine cycles can be extended either by the CPU automatically inserting one or more Wait states or by the insertion of one or more Wait states by the user.

Instruction Opcode Fetch. The CPU places the contents of the Program Counter (PC) on the address bus at the start of the cycle (Figure 5). Approximately one-half clock cycle later, $\overline{\text{MREQ}}$ goes active. When active, $\overline{\text{RD}}$ indicates that the memory data can be enabled onto the CPU data bus.

The CPU samples the $\overline{\text{WAIT}}$ input with the falling edge of clock state T₂. During clock states T₃ and T₄ of an M1 cycle, dynamic RAM refresh can occur while the CPU starts decoding and executing the instruction. When the Refresh Control signal becomes active, refreshing of dynamic memory can take place.

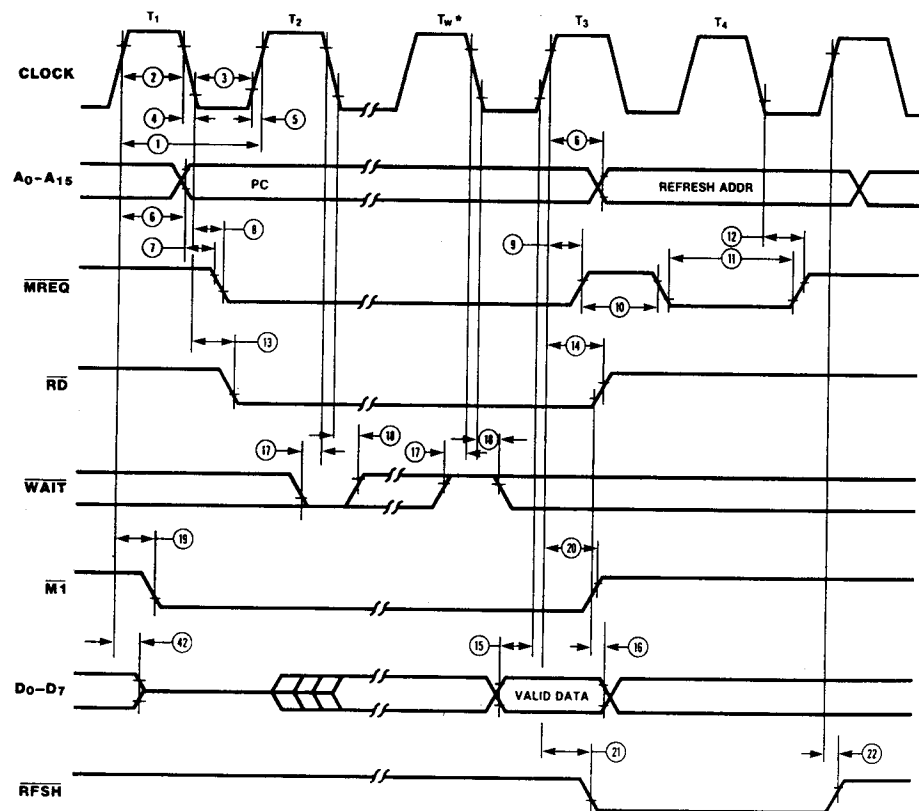


Figure 5. Instruction Opcode Fetch

Memory Read or Write Cycles. Figure 6 shows the timing of memory read or write cycles other than an opcode fetch (M1) cycle. The $\overline{\text{MREQ}}$ and $\overline{\text{RD}}$ signals function exactly as in the fetch cycle. In a memory write cycle, $\overline{\text{MREQ}}$ also

becomes active when the address bus is stable. The $\overline{\text{WR}}$ line is active when the data bus is stable, so that it can be used directly as an R/W pulse to most semiconductor memories.

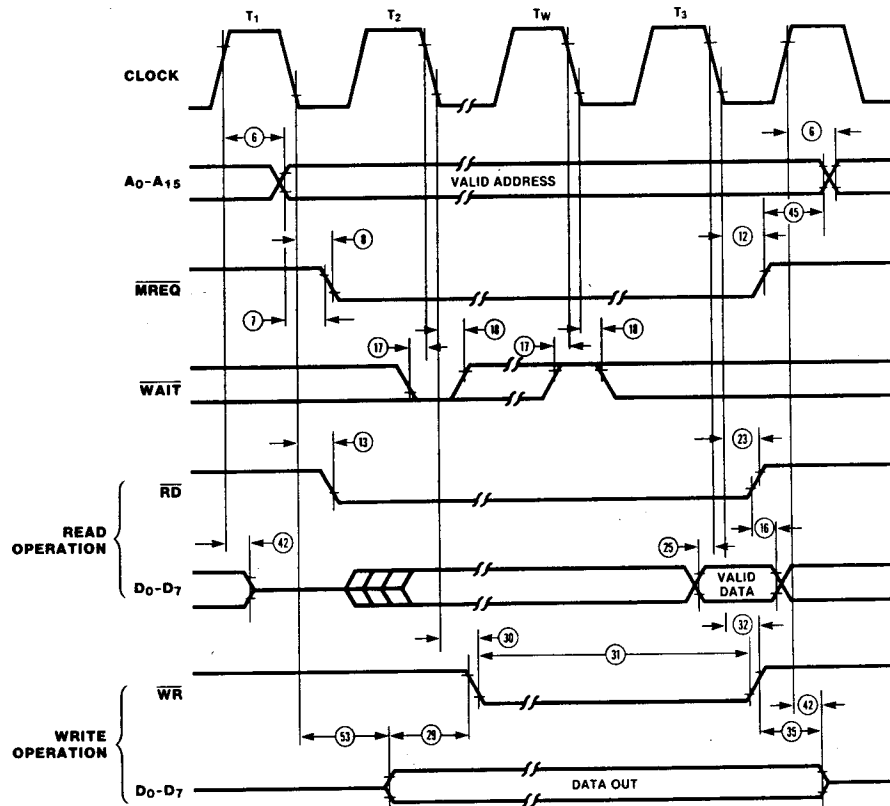
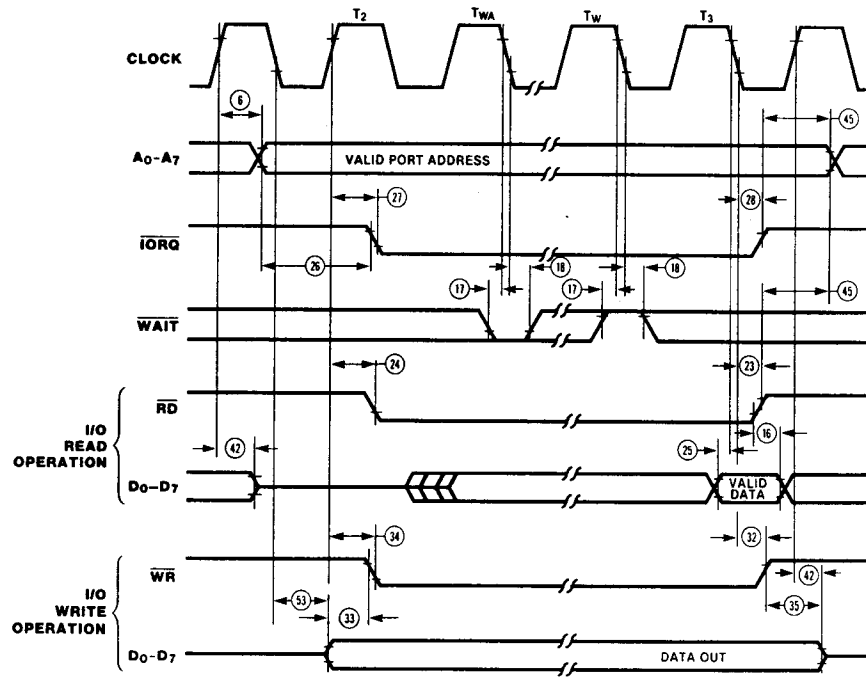


Figure 6. Memory Read or Write Cycles

Input or Output Cycles. Figure 7 shows the timing for an I/O read or I/O write operation. During I/O operations, the CPU automatically inserts a single Wait state (T_{WA}). This

extra Wait state allows sufficient time for an I/O port to decode the address from the port address lines.

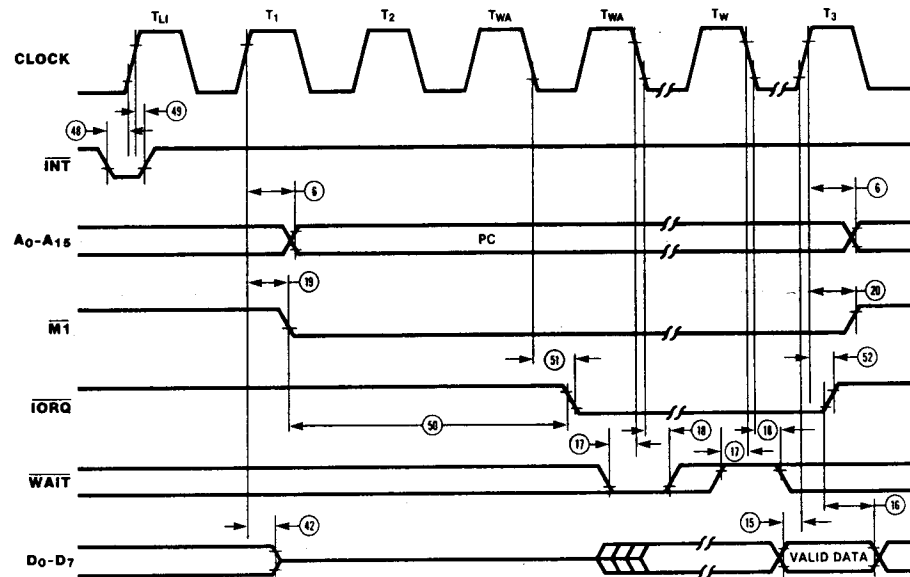


T_{WA} = One wait cycle automatically inserted by CPU.

Figure 7. Input or Output Cycles

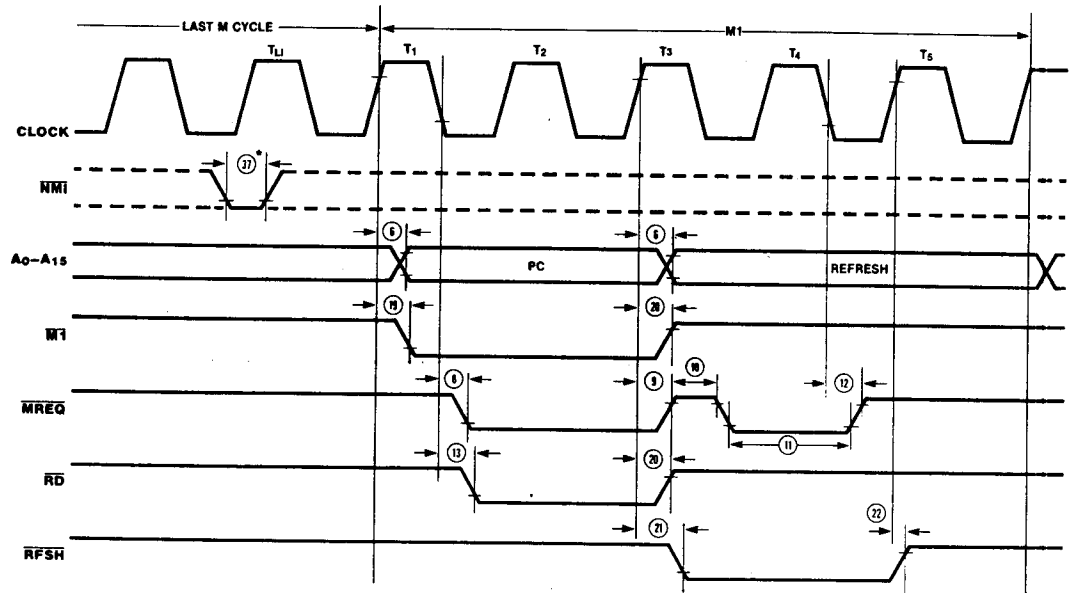
Interrupt Request/Acknowledge Cycle. The CPU samples the interrupt signal with the rising edge of the last clock cycle at the end of any instruction (Figure 8). When an interrupt is accepted, a special M1 cycle is generated.

During this $\overline{M1}$ cycle, $\overline{IORQ}$ becomes active (instead of $\overline{MREQ}$) to indicate that the interrupting device can place an 8-bit vector on the data bus. The CPU automatically adds two Wait states to this cycle.



Non-Maskable Interrupt Request Cycle. $\overline{\text{NMI}}$ is sampled at the same time as the maskable interrupt input $\overline{\text{INT}}$ but has higher priority and cannot be disabled under software control. The subsequent timing is similar to that of a normal

memory read operation except that data put on the bus by the memory is ignored. The CPU instead executes a restart (RST) operation and jumps to the $\overline{\text{NMI}}$ service routine located at address 0066H (Figure 9).

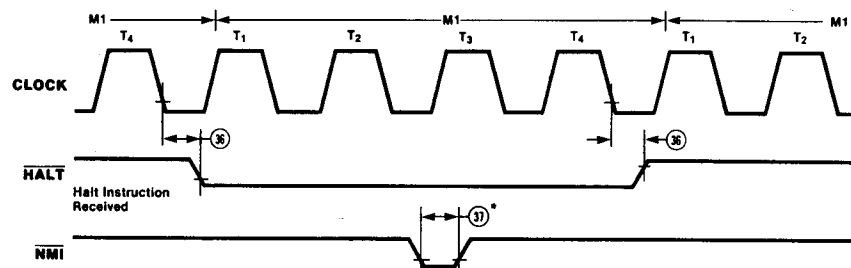


*Although $\overline{\text{NMI}}$ is an asynchronous input, to guarantee its being recognized on the following machine cycle, $\overline{\text{NMI}}$'s falling edge must occur no later than the rising edge of the clock cycle preceding the last state of any instruction cycle (T_{L1}).

Figure 9. Non-Maskable Interrupt Request Operation

Halt Acknowledge Cycle. When the CPU receives a $\overline{\text{HALT}}$ instruction, it executes NOP states until either an $\overline{\text{INT}}$ or $\overline{\text{NMI}}$ input is received. When in the Halt state, the $\overline{\text{HALT}}$ output is

active and remains so until an interrupt is received (Figure 11). $\overline{\text{INT}}$ will also force a Halt exit.



*Although $\overline{\text{NMI}}$ is an asynchronous input, to guarantee its being recognized on the following machine cycle, $\overline{\text{NMI}}$'s falling edge must occur no later than the rising edge of the clock cycle preceding the last state of any instruction cycle (T_{LJ}).

Figure 11. Halt Acknowledge

Reset Cycle. $\overline{\text{RESET}}$ must be active for at least three clock cycles for the CPU to properly accept it. As long as $\overline{\text{RESET}}$ remains active, the address and data buses float, and the control outputs are inactive. Once $\overline{\text{RESET}}$ goes inactive, two

internal T cycles are consumed before the CPU resumes normal processing operation. $\overline{\text{RESET}}$ clears the PC register, so the first opcode fetch will be to location 0000H (Figure 12).

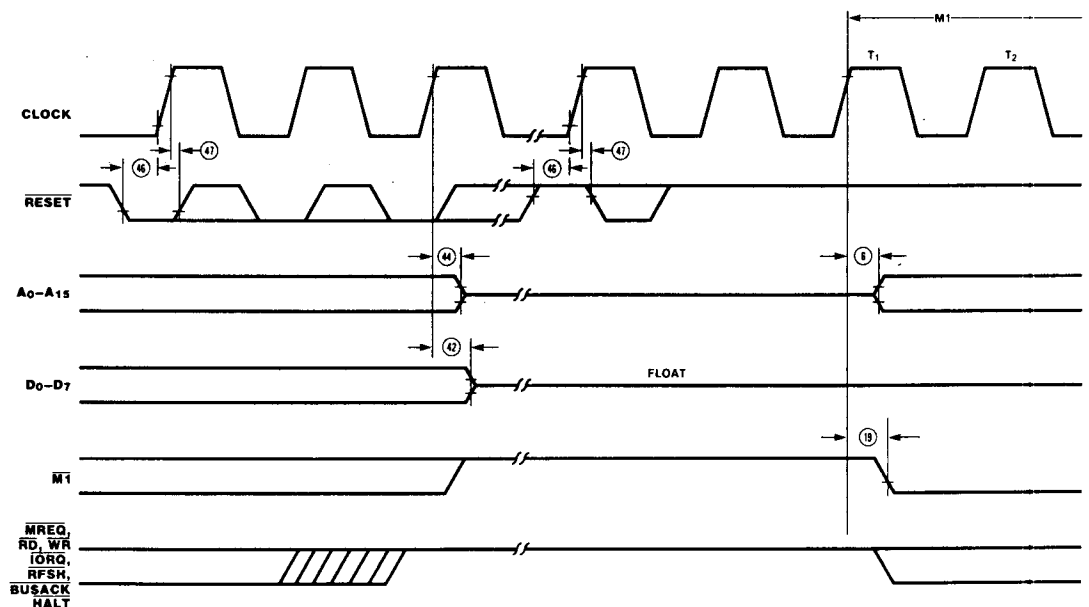


Figure 12. Reset Cycle

Power-Down mode of operation (Only applies to CMOS Z80 CPU).

CMOS Z80 CPU supports Power-Down mode of operation.

This mode is also referred to as the "standby mode", and supply current for the CPU goes down as low as 10 μA (Where specified as I_{CC2}).

Power-Down Acknowledge Cycle. When the clock input to the CPU is stopped at either a High or Low level, the CPU stops its operation and maintains all registers and control signals. However, I_{CC2} (standby supply current) is guaranteed only when the system clock is stopped at a Low

level during T_4 of the machine cycle following the execution of the HALT instruction. The timing diagram for the power-down function, when implemented with the HALT instruction, is shown in Figure 13.

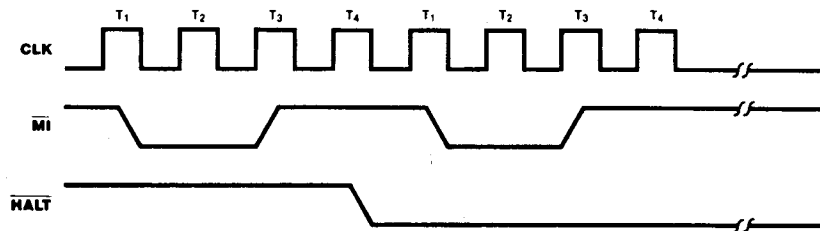


Figure 13. Power-Down Acknowledge

ABSOLUTE MAXIMUM RATINGS

Voltage on V_{CC} with respect to V_{SS} $-0.3V$ to $+7V$
Voltages on all inputs with respect
to V_{SS} $-0.3V$ to $V_{CC} + 0.3V$
Operating Ambient
Temperature See Ordering Information
Storage Temperature $-65^{\circ}C$ to $+150^{\circ}C$

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

The DC Characteristics and capacitance sections below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND (0V). Positive current flows into the referenced pin.

The Ordering Information section lists temperature ranges and product numbers. Package drawings are in the Package Information section. Refer to the Literature List for additional documentation.

Available operating temperature ranges are:

■ **S = $0^{\circ}C$ to $+70^{\circ}C$**

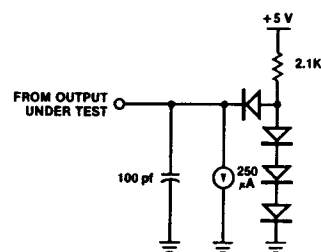
Voltage Supply Range:

NMOS: $+4.75V \leq V_{CC} \leq +5.25V$

CMOS: $+4.50V \leq V_{CC} \leq +5.50V$

■ **E = $-40^{\circ}C$ to $100^{\circ}C$, $+4.50V \leq V_{CC} \leq +5.50V$**

All ac parameters assume a load capacitance of 100 pf. Add 10 ns delay for each 50 pf increase in load up to a maximum of 200 pf for the data bus and 100 pf for address and control lines. AC timing measurements are referenced to 1.5 volts (except for clock, which is referenced to the 10% and 90% points).



DC CHARACTERISTICS (Z84C00/CMOS Z80 CPU)

Symbol	Parameter	Min	Max	Unit	Condition
V_{ILC}	Clock Input Low Voltage	-0.3	0.45	V	
V_{IHC}	Clock Input High Voltage	$V_{CC} - .6$	$V_{CC} + .3$	V	
V_{IL}	Input Low Voltage	-0.3	0.8	V	
V_{IH}	Input High Voltage	2.2	V_{CC}	V	
V_{OL}	Output Low Voltage		0.4	V	$I_{OL} = 2.0 \text{ mA}$
V_{OH1}	Output High Voltage	2.4		V	$I_{OH} = -1.6 \text{ mA}$
V_{OH2}	Output High Voltage	$V_{CC} - 0.8$		V	$I_{OH} = -250 \mu\text{A}$
I_{CC1}	Power Supply Current	4 MHz	20	mA	$V_{CC} = 5\text{V}$
			30	mA	$V_{IH} = V_{CC} - 0.2\text{V}$
			40	mA	$V_{IL} = 0.2\text{V}$
			50	mA	$V_{CC} = 5\text{V}$
			100	mA	$V_{CC} = 5\text{V}$
I_{CC2}	Standby Supply Current		10	μA	$V_{CC} = 5\text{V}$ CLK = (0) $V_{IH} = V_{CC} - 0.2\text{V}$ $V_{IL} = 0.2\text{V}$
I_{LI}	Input Leakage Current	-10	10	μA	$V_{IN} = 0.4 \text{ to } V_{CC}$
I_{LO}	3-State Output Leakage Current in Float	-10	10^2	μA	$V_{OUT} = 0.4 \text{ to } V_{CC}$

1. Measurements made with outputs floating.

2. A₁₅-A₀, D₇-D₀, MREQ, IORQ, RD, and WR.

3. I_{CC2} standby supply current is guaranteed only when the supplied clock is stopped at a low level during T₄ of the machine cycle immediately following the execution of a HALT instruction.

CAPACITANCE

Symbol	Parameter	Min	Max	Unit
C_{CLOCK}	Clock Capacitance		10	pf
C_{IN}	Input Capacitance		5	pf
C_{OUT}	Output Capacitance		15	pf

T_A = 25°C, f = 1 MHz.

Unmeasured pins returned to ground.

AC CHARACTERISTICS† (Z84C00/CMOS Z80 CPU; Continued)

V_{CC} = 5.0V ± 10%, unless otherwise specified

No	Symbol	Parameter	Z84C0004**		Z84C0006		Z84C0008		Z84C0010		Z84C0020[1]		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
39	ThBUSREQ (Cr)	/BUSREQ hold time after Clock Rise	10		10		10		10		10		nS	
40	TdCr (BUSACKf)	Clock Rise to /BASACK Fall delay		100		90		80		75		40	nS	
41	TdCf (BUSACKr)	Clock Fall to /BASACK Rise delay		100		90		80		75		40	nS	
42	TdCr(Dz)	Clock Rise to Data float delay		90		80		70		65		40	nS	
43	TdCr(CTz)	Clock Rise to Control Outputs Float Delay (/MREQ, /IORQ, /RD and /WR)		80		70		60		65		40	nS	
44	TdCr(Az)	Clock Rise to Address float delay		90		80		70		75		40	nS	
45	TdCTr(A)	Address Hold time from /MREQ, /IORQ, /RD or /WR	80*		35*		20*		20*		0*		nS	
46	TsRESET(Cr)	/RESET to Clock Rise setup time	60		60		45		40		15		nS	
47	ThRESET(Cr)	/RESET to Clock Rise Hold time	10		10		10		10		10		nS	
48	TsINTf(Cr)	/INT Fall to Clock Rise Setup Time	80		70		55		50		15		nS	
49	ThINTr(Cr)	/INT Rise to Clock Rise Hold Time	10		10		10		10		10		nS	
50	TdM1f (IORQf)	/M1 Fall to /IORQ Fall delay	565*		359*		270*		220*		100*		nS	
51	TdCf(IORQf)	/Clock Fall to /IORQ Fall delay		85		70		60		55		45	nS	
52	TdCf(IORQr)	Clock Rise to /IORQ Rise delay		85		70		60		55		45	nS	
53	TdCf(D)	Clock Fall to Data Valid delay		150		130		115		110		75	nS	

Notes:

* For Clock periods other than the minimum shown, calculate parameters using the following table.

Calculated values above assumed TrC = TtC = maximum.

** 4 MHz CMOS Z80 is obsoleted and replaced by 6 MHz

[1] Z84C0020 parameters are guaranteed with 50pF load Capacitance.

[2] If Capacitive Load is other than 50pF, please use Figure 1. to calculate the value.

[3] Increasing delay by 10nS for each 50pF increase in loading, 200pF max for data lines, and 100pF for control lines.

FOOTNOTES TO AC CHARACTERISTICS

No	Symbol	Parameter	Z84C0004**	Z84C0006	Z84C0008	Z84C0010	Z84C0020
1	TcC	TwCh + TwCl + TrC + TtC					
7	TdA(MREQf)	TwCh + TtC	-65	-50	-45	-45	-45
10	TwMREQh	TwCh + TtC	-20	-20	-20	-20	-20
11	TwMREQf	TcC	-30	-30	-25	-25	-25
26	TdA(IORQf)	TcC	-70	-55	-50	-50	-50
29	TdD(WRf)	TcC	-170	-140	-120	-60	-60
31	TwWR	TcC	-30	-30	-25	-25	-25
33	TdD(WRf)	TwCl + TrC	-140	-140	-120	-60	-60
35	TdWRr(D)	TwCl + TrC	-70	-55	-50	-40	-25
45	TdCTr(A)	TwCl + TrC	-50	-50	-45	-30	-30
50	TdM1f(IORQf)	2TcC + TwCh + TtC	-65	-50	-45	-30	-30

AC Test Conditions: V_{IH} = 2.0 V
V_{IL} = 0.8 V

V_{OH} = 1.5 V
V_{OL} = 1.5 V

V_{IHC} = V_{CC} - 0.6 V
V_{ILC} = 0.45 V

FLOAT = ±0.5 V

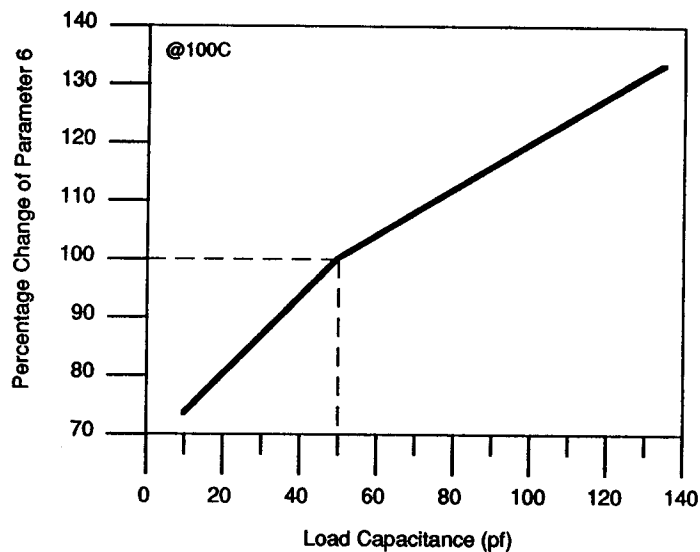


Figure 1. Address Delay Characteristics
(Parameter 6)

DC CHARACTERISTICS (Z8400/NMOS Z80 CPU)

All parameters are tested unless otherwise noted.

Symbol	Parameter	Min	Max	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	-0.3	0.45	V	
V_{IHC}	Clock Input High Voltage	$V_{CC} - .6$	$V_{CC} + .3$	V	
V_{IL}	Input Low Voltage	-0.3	0.8	V	
V_{IH}	Input High Voltage	2.0 ¹	V_{CC}	V	
V_{OL}	Output Low Voltage		0.4	V	$I_{OL} = 2.0 \text{ mA}$
V_{OH}	Output High Voltage	2.4 ¹		V	$I_{OH} = -250 \mu\text{A}$
I_{CC}	Power Supply Current		200	mA	Note 3
I_{LI}	Input Leakage Current		10	μA	$V_{IN} = 0 \text{ to } V_{CC}$
I_{LO}	3-State Output Leakage Current in Float	-10	10 ²	μA	$V_{OUT} = 0.4 \text{ to } V_{CC}$

1. For military grade parts, refer to the Z80 Military Electrical Specification.

2. A_{15} - A_0 , D_7 - D_0 , $MREQ$, $IORD$, RD , and WR .

3. Measurements made with outputs floating.

CAPACITANCE

Guaranteed by design and characterization.

Symbol	Parameter	Min	Max	Unit
C_{CLOCK}	Clock Capacitance		35	pf
C_{IN}	Input Capacitance		5	pf
C_{OUT}	Output Capacitance		15	pf

NOTES:

$T_A = 25^\circ\text{C}$, $f = 1 \text{ MHz}$.

Unmeasured pins returned to ground.

AC CHARACTERISTICS† (Z8400/NMOS Z80 CPU; Continued)

Number	Symbol	Parameter	Z0840004		Z0840006		Z0840008	
			Min	Max	Min	Max	Min	Max
39	ThBUSREQ(Cr)	BUSREQ Hold Time after Clock ↑	0		0		0	
40	TdCr(BUSACKf)	Clock ↑ to BUSACK ↓ Delay		100		90		80
41	TdCl(BUSACKr)	Clock ↓ to BUSACK ↑ Delay		100		90		80
42	TdCr(Dz)	Clock ↑ to Data Float Delay		90		80		70
43	TdCr(CTz)	Clock ↑ to Control Outputs Float Delay (MREQ, IORQ, RD, and WR)		80		70		60
44	TdCr(Az)	Clock ↑ to Address Float Delay		90		80		70
45	TdCTr(A)	MREQ ↑, IORQ ↑, RD ↑, and WR ↑ to Address Hold Time	80*		35*		20*	
46	TsRESET(Cr)	RESET to Clock ↑ Setup Time	60		60		45	
47	ThRESET(Cr)	RESET to Clock ↑ Hold Time		0		0		0
48	TsINTf(Cr)	INT to Clock ↑ Setup Time	80		70		55	
49	ThINTr(Cr)	INT to Clock ↑ Hold Time		0		0		0
50	TdM1f(IORQf)	M1 ↓ to IORQ ↓ Delay	565*		365*		270*	
51	TdCf(IORQf)	Clock ↓ to IORQ ↓ Delay		85		70		60
52	TdCf(IORQr)	Clock ↑ to IORQ ↑ Delay		85		70		60
53	TdCf(D)	Clock ↓ to Data Valid Delay		150		130		115

*For clock periods other than the minimums shown, calculate parameters using the following table. Calculated values above assumed TrC = TrC = 20 ns.

†Units in nanoseconds (ns).

FOOTNOTES TO AC CHARACTERISTICS

Number	Symbol	General Parameter	Z0840004	Z0840006	Z0840008
1	TcC	TwCh + TwCl + TrC + TrC			
7	TdA(MREQf)	TwCh + TrC	- 65	- 50	- 45
10	TwMREQh	TwCh + TrC	- 20	- 20	- 20
11	TwMREQl	TcC	- 30	- 30	- 25
26	TdA(IORQf)	TcC	- 70	- 55	- 50
29	TdD(WRf)	TcC	- 170	- 140	- 120
31	TwWR	TcC	- 30	- 30	- 25
33	TdD(WRf)	TwCl + TrC	- 140	- 140	- 120
35	TdWRr(D)	TwCl + TrC	- 70	- 55	- 50
45	TdCTr(A)	TwCl + TrC	- 50	- 50	- 45
50	TdM1f(IORQf)	2TcC + TwCh + TrC	- 65	- 50	- 45

AC Test Conditions:

V_{IH} = 2.0 V

V_{IL} = 0.8 V

V_{IHC} = V_{CC} - 0.6 V

V_{ILC} = 0.45 V

V_{OH} = 1.5 V

V_{OL} = 1.5 V

FLOAT = ±0.5 V