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Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	Z80
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	20MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	40-DIP (0.620", 15.75mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z84c0020pec



Figure 2a. 44-Pin LQFP, Pin Assignments
(Only available for 84C00)



Figure 2b. 44-Pin Chip Carrier Pin Assignments

GENERAL DESCRIPTION

The CPUs are fourth-generation enhanced microprocessors with exceptional computational power. They offer higher system throughput and more efficient memory utilization than comparable second- and third-generation microprocessors. The internal registers contain 208 bits of read/write memory that are accessible to the programmer. These registers include two sets of six general-purpose registers which may be used individually as either 8-bit registers or as 16-bit register pairs. In addition, there are two sets of accumulator and flag registers. A group of "Exchange" instructions makes either set of main or alternate registers accessible to the programmer. The alternate set allows operation in foreground-background mode or it may be reserved for very fast interrupt response.

The CPU also contains a Stack Pointer, Program Counter, two index registers, a Refresh register (counter), and an Interrupt register. The CPU is easy to incorporate into a system since it requires only a single +5V power source. All output signals are fully decoded and timed to control standard memory or peripheral circuits; the CPU is supported by an extensive family of peripheral controllers. The internal block diagram (Figure 3) shows the primary functions of the processors. Subsequent text provides more detail on the I/O controller family, registers, instruction set, interrupts and daisy chaining, and CPU timing.

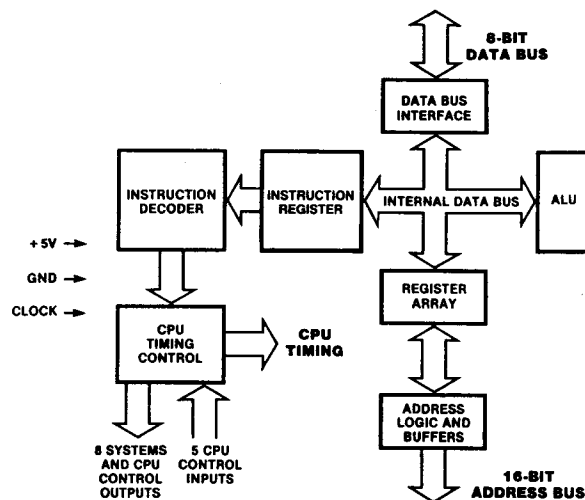


Figure 3. Z80C CPU Block Diagram

Table 1. Z80C CPU Registers

Register	Size (Bits)	Remarks	
A, A'	Accumulator	8	Stores an operand or the results of an operation.
F, F'	Flags	8	See Instruction Set.
B, B'	General Purpose	8	Can be used separately or as a 16-bit register with C.
C, C'	General Purpose	8	Can be used separately or as a 16-bit register with B.
D, D'	General Purpose	8	Can be used separately or as a 16-bit register with E.
E, E'	General Purpose	8	Can be used separately or as a 16-bit register with D.
H, H'	General Purpose	8	Can be used separately or as a 16-bit register with L.
L, L'	General Purpose	8	Can be used separately or as a 16-bit register with H.
Note: The (B,C), (D,E), and (H,L) sets are combined as follows:			
B — High byte C — Low byte			
D — High byte E — Low byte			
H — High byte L — Low byte			
I	Interrupt Register	8	Stores upper eight bits of memory address for vectored interrupt processing.
R	Refresh Register	8	Provides user-transparent dynamic memory refresh. Automatically incremented and placed on the address bus during each instruction fetch cycle.
IX	Index Register	16	Used for indexed addressing.
IY	Index Register	16	Used for indexed addressing.
SP	Stack Pointer	16	Holds address of the top of the stack. See Push or Pop in instruction set.
PC	Program Counter	16	Holds address of next instruction.
IFF ₁ -IFF ₂	Interrupt Enable	Flip-Flops	Set or reset to indicate interrupt status (see Figure 4).
IMFa-IMFb	Interrupt Mode	Flip-Flops	Reflect Interrupt mode (see Figure 4).

failure has been detected. After recognition of the $\overline{\text{NMI}}$ signal (providing $\overline{\text{BUSREQ}}$ is not active), the CPU jumps to restart location 0066H. Normally, software starting at this address contains the interrupt service routine.

Maskable Interrupt ($\overline{\text{INT}}$). Regardless of the interrupt mode set by the user, the CPU response to a maskable interrupt input follows a common timing cycle. After the interrupt has been detected by the CPU (provided that interrupts are enabled and $\overline{\text{BUSREQ}}$ is not active) a special interrupt processing cycle begins. This is a special fetch ($\overline{\text{M1}}$) cycle in which $\overline{\text{IORQ}}$ becomes active rather than $\overline{\text{MREQ}}$, as in a normal $\overline{\text{M1}}$ cycle. In addition, this special $\overline{\text{M1}}$ cycle is automatically extended by two $\overline{\text{WAIT}}$ states, to allow for the time required to acknowledge the interrupt request.

Mode 0 Interrupt Operation. This mode is similar to the 8080 microprocessor interrupt service procedures. The interrupting device places an instruction on the data bus. This is normally a Restart instruction, which will initiate a call

to the selected one of eight restart locations in page zero of memory. Unlike the 8080, the Z80 CPU responds to the Call instruction with only one interrupt acknowledge cycle followed by two memory read cycles.

Mode 1 Interrupt Operation. Mode 1 operation is very similar to that for the NMI. The principal difference is that the Mode 1 interrupt has only one restart location, 003BH.

Mode 2 Interrupt Operation. This interrupt mode has been designed to most effectively utilize the capabilities of the Z80 microprocessor and its associated peripheral family. The interrupting peripheral device selects the starting address of the interrupt service routine. It does this by placing an 8-bit vector on the data bus during the interrupt acknowledge cycle. The CPU forms a pointer using this byte as the lower 8 bits and the contents of the I register as the upper 8 bits. This points to an entry in a table of addresses for interrupt service routines. The CPU then jumps to the routine at that

address. This flexibility in selecting the interrupt service routine address allows the peripheral device to use several different types of service routines. These routines may be located at any available location in memory. Since the interrupting device supplies the low-order byte of the 2-byte vector, bit 0 (A_0) must be a zero.

Interrupt Enable/Disable Operation. Two flip-flops, IFF₁ and IFF₂, referred to in the register description, are used to signal the CPU interrupt status. Operation of the two flip-flops is described in Table 2. For more details, refer to the *Z80 CPU Technical Manual* (03-0029-01) and *Z80 Assembly Language Programming Manual* (03-0002-01).

Table 2. State of Flip-Flops

Action	IFF ₁	IFF ₂	Comments
CPU Reset	0	0	Maskable interrupt INT disabled
DI instruction execution	0	0	Maskable interrupt INT disabled
EI instruction execution	1	1	Maskable interrupt INT enabled
LD A,I instruction execution	•	•	IFF ₂ → Parity flag
LD A,R instruction execution	•	•	IFF ₂ → Parity flag
Accept NMI	0	•	Maskable interrupt INT disabled
RETN instruction execution	IFF ₂	•	IFF ₂ → IFF ₁ at completion of an NMI service routine.

INSTRUCTION SET

The microprocessor has one of the most powerful and versatile instruction sets available in any 8-bit microprocessor. It includes such unique operations as a block move for fast, efficient data transfers within memory, or between memory and I/O. It also allows operations on any bit in any location in memory.

The following is a summary of the instruction set which shows the assembly language mnemonic, the operation, the flag status, and gives comments on each instruction. For an explanation of flag notations and symbols for mnemonic tables, see the Symbolic Notations section which follows these tables. The *Z80 CPU Technical Manual* (03-0029-01), the *Programmer's Reference Guide* (03-0012-03), and *Assembly Language Programming Manual* (03-0002-01) contain significantly more details for programming use.

The instructions are divided into the following categories:

- 8-bit loads
- 16-bit loads
- Exchanges, block transfers, and searches
- 8-bit arithmetic and logic operations
- General-purpose arithmetic and CPU control
- 16-bit arithmetic operations
- Rotates and shifts

- Bit set, reset, and test operations
- Jumps
- Calls, returns, and restarts
- Input and output operations

A variety of addressing modes are implemented to permit efficient and fast data transfer between various registers, memory locations, and input/output devices. These addressing modes include:

- Immediate
- Immediate extended
- Modified page zero
- Relative
- Extended
- Indexed
- Register
- Register indirect
- Implied
- Bit

8-BIT LOAD GROUP (Continued)

Mnemonic	Symbolic Operation	S	Z	Flags				Opcode				No. of Bytes	No. of M Cycles	No. of T States	Comments		
				H	P/V	N	C	76	543	210	Hex						
LD (Y+d), n	(Y+d) ← n	•	•	X	•	X	•	•	•	11	111	101	FD	4	5	19	
										00	110	110	36				
LDA, (BC)	A ← (BC)	•	•	X	•	X	•	•	•	00	001	010	0A	1	2	7	
LDA, (DE)	A ← (DE)	•	•	X	•	X	•	•	•	00	011	010	1A	1	2	7	
LDA, (nn)	A ← (nn)	•	•	X	•	X	•	•	•	00	111	010	3A	3	4	13	
LD (BC), A	(BC) ← A	•	•	X	•	X	•	•	•	00	000	010	02	1	2	7	
LD (DE), A	(DE) ← A	•	•	X	•	X	•	•	•	00	010	010	12	1	2	7	
LD (nn), A	(nn) ← A	•	•	X	•	X	•	•	•	00	110	010	32	3	4	13	
LDA, I	A ← I	‡	‡	X	0	X	IFF	0	•	11	101	101	ED	2	2	9	
										01	010	111	57				
LDA, R	A ← R	‡	‡	X	0	X	IFF	0	•	11	101	101	ED	2	2	9	
										01	011	111	5F				
LD I, A	I ← A	•	•	X	•	X	•	•	•	11	101	101	ED	2	2	9	
										01	000	111	47				
LDR, A	R ← A	•	•	X	•	X	•	•	•	11	101	101	ED	2	2	9	
										01	001	111	4F				

NOTE: IFF, the content of the interrupt enable flip-flop, (IFF₂), is copied into the P/V flag.

16-BIT LOAD GROUP

Mnemonic	Symbolic Operation	S	Z	Flags				Opcode				No. of Bytes	No. of M Cycles	No. of T States	Comments		
				H	P/V	N	C	76	543	210	Hex						
LD dd, nn	dd ← nn	•	•	X	•	X	•	•	•	00	dd0	001		3	3	10	dd Pair
																	00 BC
																	01 DE
LD IX, nn	IX ← nn	•	•	X	•	X	•	•	•	11	011	101	DD	4	4	14	10 HL
										00	100	001	21				11 SP
LD IY, nn	IY ← nn	•	•	X	•	X	•	•	•	11	111	101	FD	4	4	14	
										00	100	001	21				
LD HL, (nn)	H ← (nn+1) L ← (nn)	•	•	X	•	X	•	•	•	00	101	010	2A	3	5	16	
LD dd, (nn)	dd _H ← (nn+1) dd _L ← (nn)	•	•	X	•	X	•	•	•	11	101	101	ED	4	6	20	
										01	dd1	011					

NOTE: (PAIR)_H, (PAIR)_L refer to high order and low order eight bits of the register pair respectively. e.g., BC_L = C, AF_H = A.

EXCHANGE, BLOCK TRANSFER, BLOCK SEARCH GROUPS

Mnemonic	Symbolic Operation	Flags						Opcode			Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments				
		S	Z	H	P/V	N	C	76	543	210									
EX DE, HL	DE ↔ HL	•	•	X	•	X	•	•	•	•	11	101	011	EB	1	1	4		
EX AF, AF'	AF ↔ AF'	•	•	X	•	X	•	•	•	•	00	001	000	08	1	1	4		
EXX	BC ↔ BC'	•	•	X	•	X	•	•	•	•	11	011	001	D9	1	1	4	Register bank and auxiliary register bank exchange	
	DE ↔ DE'																		
	HL ↔ HL'																		
EX (SP), HL	H ↔ (SP + 1) L ↔ (SP)	•	•	X	•	X	•	•	•	•	11	100	011	E3	1	5	19		
EX (SP), IX	IX _H ↔ (SP + 1)	•	•	X	•	X	•	•	•	•	11	011	101	DD	2	6	23		
	IX _L ↔ (SP)										11	100	011	E3					
EX (SP), IY	IY _H ↔ (SP + 1)	•	•	X	•	X	•	•	•	•	11	111	101	FD	2	6	23		
	IY _L ↔ (SP)										11	100	011	E3					
LDI	(DE) ← (HL)	•	•	X	0	X	†	0	•	•	11	101	101	ED	2	4	16	Load (HL) into (DE), increment the pointers and decrement the byte counter (BC)	
	DE ← DE + 1										10	100	000	A0					
	HL ← HL + 1																		
	BC ← BC - 1																		
LDIR	(DE) ← (HL)	•	•	X	0	X	0	0	•	•	11	101	101	ED	2	5	21	If BC ≠ 0	
	DE ← DE + 1										10	110	000	B0	2	4	16	If BC = 0	
	HL ← HL + 1																		
	BC ← BC - 1																		
	Repeat until BC = 0																		
LDD	(DE) ← (HL)	•	•	X	0	X	†	0	•	•	11	101	101	ED	2	4	16		
	DE ← DE - 1										10	101	000	A8					
	HL ← HL - 1																		
	BC ← BC - 1																		
LDDR	(DE) ← (HL)	•	•	X	0	X	0	0	•	•	11	101	101	ED	2	5	21	If BC ≠ 0	
	DE ← DE - 1										10	111	000	B8	2	4	16	If BC = 0	
	HL ← HL - 1																		
	BC ← BC - 1																		
	Repeat until BC = 0																		
CPI	A - (HL)	†	†	X	†	X	†	1	•	•	11	101	101	ED	2	4	16		
	HL ← HL + 1										10	100	001	A1					
	BC ← BC - 1																		

NOTE: ① P/V flag is 0 if the result of BC - 1 = 0, otherwise P/V = 1.
 ② P/V flag is 0 only at completion of instruction.
 ③ Z flag is 1 if A = HL, otherwise Z = 0.

EXCHANGE, BLOCK TRANSFER, BLOCK SEARCH GROUPS (Continued)

Mnemonic	Symbolic Operation	S Z		Flags				Opcode				No. of Bytes	No. of M Cycles	No. of T States	Comments		
		S	Z	H	P/V	N	C	76	543	210	Hex						
CPIR	A ← (HL)	‡	‡	X	‡	X	‡	1	•	11	101	101	ED	2	5	21	If BC ≠ 0 and A ≠ (HL)
	HL ← HL + 1									10	110	001	B1	2	4	16	If BC = 0 or A = (HL)
	BC ← BC - 1 Repeat until A = (HL) or BC = 0																
CPD	A ← (HL)	‡	‡	X	‡	X	‡	1	•	11	101	101	ED	2	4	16	
	HL ← HL - 1									10	101	001	A9				
	BC ← BC - 1																
CPDR	A ← (HL)	‡	‡	X	‡	X	‡	1	•	11	101	101	ED	2	5	21	If BC ≠ 0 and A ≠ (HL)
	HL ← HL - 1									10	111	001	B9	2	4	16	If BC = 0 or A = (HL)
	BC ← BC - 1 Repeat until A = (HL) or BC = 0																

NOTE: ① P/V flag is 0 if the result of BC - 1 = 0, otherwise P/V = 1.
 ② P/V flag is 0 only at completion of instruction.
 ③ Z flag is 1 if A = (HL), otherwise Z = 0.

8-BIT ARITHMETIC AND LOGICAL GROUP

Mnemonic	Symbolic Operation	S Z		Flags				Opcode				No. of Bytes	No. of M Cycles	No. of T States	Comments										
		S	Z	H	P/V	N	C	76	543	210	Hex														
ADD A, r	A ← A + r	‡	‡	X	‡	X	V	0	‡	10	000	r		1	1	4	r Reg.								
ADD A, n	A ← A + n	‡	‡	X	‡	X	V	0	‡	11	000	110		2	2	7	000 B								
																					001 C				
																									010 D
ADD A, (HL)	A ← A + (HL)	‡	‡	X	‡	X	V	0	‡	10	000	110		1	2	7	100 H								
ADD A, (IX + d)	A ← A + (IX + d)	‡	‡	X	‡	X	V	0	‡	11	011	101	DD	3	5	19	101 L								
																								111 A	
ADD A, (IY + d)	A ← A + (IY + d)	‡	‡	X	‡	X	V	0	‡	11	111	101	FD	3	5	19									
ADC A, s	A ← A + s + CY	‡	‡	X	‡	X	V	0	‡		001						s is any of r, n, (HL), (IX + d), (IY + d) as shown for ADD instruction. The indicated bits replace the 000 in the ADD set above.								
SUB s	A ← A - s	‡	‡	X	‡	X	V	1	‡		010														
SBC A, s	A ← A - s - CY	‡	‡	X	‡	X	V	1	‡		011														
AND s	A ← A > s	‡	‡	X	1	X	P	0	0		100														
OR s	A ← A > s	‡	‡	X	0	X	P	0	0		110														
XOR s	A ← A ⊕ s	‡	‡	X	0	X	P	0	0		101														
CP s	A ← s	‡	‡	X	‡	X	V	1	‡		111														

8-BIT ARITHMETIC AND LOGICAL GROUP (Continued)

Mnemonic	Symbolic Operation	Flags					Opcode				No. of Bytes	No. of M Cycles	No. of T States	Comments			
		S	Z	H	P/V	N	C	76	543	210					Hex		
INC r	r ← r+1	†	†	X	†	X	V	0	•	00	r	100	1	1	4		
INC (HL)	(HL) ← (HL)+1	†	†	X	†	X	V	0	•	00	110	100	1	3	11		
INC (IX+d)	(IX+d) ← (IX+d)+1	†	†	X	†	X	V	0	•	11	011	101	DD	3	6	23	
										00	110	100					
INC (IY+d)	(IY+d) ← (IY+d)+1	†	†	X	†	X	V	0	•	11	111	101	FD	3	6	23	
										00	110	100					
DEC m	m ← m-1	†	†	X	†	X	V	1	•			101					

NOTE: m is any of r, (HL), (IX+d), (IY+d) as shown for INC. DEC same format and states as INC. Replace 100 with 101 in opcode.

GENERAL-PURPOSE ARITHMETIC AND CPU CONTROL GROUPS

Mnemonic	Symbolic Operation	Flags					Opcode				No. of Bytes	No. of M Cycles	No. of T States	Comments			
		S	Z	H	P/V	N	C	76	543	210					Hex		
DAA	@	†	†	X	†	X	P	•	†	00	100	111	27	1	1	4	Decimal adjust accumulator
CPL	A ← A	•	•	X	1	X	•	1	•	00	101	111	2F	1	1	4	Complement accumulator (one's complement)
NEG	A ← 0 - A	†	†	X	†	X	V	1	†	11	101	101	ED	2	2	8	Negate acc. (two's complement)
										01	000	100	44				
CCF	CY ← CY	•	•	X	X	X	•	0	†	00	111	111	3F	1	1	4	Complement carry flag.
SCF	CY ← 1	•	•	X	0	X	•	0	1	00	110	111	37	1	1	4	Set carry flag.
NOP	No operation	•	•	X	•	X	•	•	•	00	000	000	00	1	1	4	
HALT	CPU halted	•	•	X	•	X	•	•	•	01	110	110	76	1	1	4	
DI ★	IFF ← 0	•	•	X	•	X	•	•	•	11	110	011	F3	1	1	4	
EI ★	IFF ← 1	•	•	X	•	X	•	•	•	11	111	011	FB	1	1	4	
IM 0	Set interrupt mode 0	•	•	X	•	X	•	•	•	11	101	101	ED	2	2	8	
										01	000	110	46				
IM 1	Set interrupt mode 1	•	•	X	•	X	•	•	•	11	101	101	ED	2	2	8	
										01	010	110	56				
IM 2	Set interrupt mode 2	•	•	X	•	X	•	•	•	11	101	101	ED	2	2	8	
										01	011	110	5E				

NOTES: @ converts accumulator content into packed BCD following add or subtract with packed BCD operands.
 IFF indicates the interrupt enable flip-flop.
 CY indicates the carry flip-flop.
 ★ indicates interrupts are not sampled at the end of EI or DI.

BIT SET, RESET AND TEST GROUP

Mnemonic	Symbolic Operation	S	Z	Flags			P/V	N	C	Opcode			Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments									
				H						76	543	210														
BIT b, r	$Z \leftarrow r_b$	X	†	X	1	X	X	0	•	11	001	011	CB	2	2	8	r Reg. 000 B									
BIT b, (HL)	$Z \leftarrow (HL)_b$	X	†	X	1	X	X	0	•	11	001	011	CB	2	3	12	001 C 010 D									
BIT b, (IX+d) _b	$Z \leftarrow (IX+d)_b$	X	†	X	1	X	X	0	•	11	011	101	DD	4	5	20	011 E									
										11	001	011	CB								100 H					
										←d→																101 L
										01	b	110														111 A
BIT b, (IY+d) _b	$Z \leftarrow (IY+d)_b$	X	†	X	1	X	X	0	•	11	111	101	FD	4	5	20	000 0									
										11	001	011	CB											001 1		
										←d→																010 2
										01	b	110														011 3
SET b, r	$r_b \leftarrow 1$	•	•	X	•	X	•	•	•	11	001	011	CB	2	2	8	100 4									
SET b, (HL)	$(HL)_b \leftarrow 1$	•	•	X	•	X	•	•	•	11	b	r					101 5									
										11	001	011	CB	2	4	15	110 6									
SET b, (IX+d)	$(IX+d)_b \leftarrow 1$	•	•	X	•	X	•	•	•	11	011	101	DD	4	6	23										
										11	001	011	CB													
										←d→																
SET b, (IY+d)	$(IY+d)_b \leftarrow 1$	•	•	X	•	X	•	•	•	11	b	110														
										11	111	101	FD	4	6	23										
										11	001	011	CB													
RES b, m	$m_b \leftarrow 0$ $m=r, (HL),$ $(IX+d), (IY+d)$	•	•	X	•	X	•	•	•	11	b	110														
										10																

To form new opcode replace **11** of SET b, s with **10**. Flags and time states for SET instruction.

NOTE: The notation m_b indicates location m, bit b (0 to 7).

JUMP GROUP

Mnemonic	Symbolic Operation	Flags					Opcode				No. of Bytes	No. of M Cycles	No. of T States	Comments				
		S	Z	H	P/V/N	C	76	543	210	Hex								
JP nn	PC ← nn	•	•	X	•	X	•	•	•	•	11	000	011	C3	3	3	10	cc Condition 000 NZ (non-zero) 001 Z (zero)
JP cc, nn	If condition cc is true PC ← nn, otherwise continue	•	•	X	•	X	•	•	•	•	11	cc	010		3	3	10	010 NC (non-carry) 011 C (carry) 100 PO (parity odd) 101 PE (parity even)
JR e	PC ← PC + e	•	•	X	•	X	•	•	•	•	00	011	000	18	2	3	12	110 P (sign positive) 111 M (sign negative)
JR C, e	If C = 0, continue If C = 1, PC ← PC + e	•	•	X	•	X	•	•	•	•	00	111	000	38	2	2	7	If condition not met.
															2	3	12	If condition is met.
JR NC, e	If C = 1, continue If C = 0, PC ← PC + e	•	•	X	•	X	•	•	•	•	00	110	000	30	2	2	7	If condition not met.
															2	3	12	If condition is met.
JP Z, e	If Z = 0, continue If Z = 1, PC ← PC + e	•	•	X	•	X	•	•	•	•	00	101	000	28	2	2	7	If condition not met.
															2	3	12	If condition is met.
JR NZ, e	If Z = 1, continue If Z = 0, PC ← PC + e	•	•	X	•	X	•	•	•	•	00	100	000	20	2	2	7	If condition not met.
															2	3	12	If condition is met.
JP (HL)	PC ← HL	•	•	X	•	X	•	•	•	•	11	101	001	E9	1	1	4	
JP (IX)	PC ← IX	•	•	X	•	X	•	•	•	•	11	011	101	DD	2	2	8	
											11	101	001	E9				
JP (IY)	PC ← IY	•	•	X	•	X	•	•	•	•	11	111	101	FD	2	2	8	
											11	101	001	E9				
DJNZ, e	B ← B - 1 If B = 0, continue If B ≠ 0, PC ← PC + e	•	•	X	•	X	•	•	•	•	00	010	000	10	2	2	8	If B = 0
															2	3	13	If B ≠ 0.

NOTES: e represents the extension in the relative addressing mode.
e is a signed two's complement number in the range < -126, 129 >.
e - 2 in the opcode provides an effective address of pc + e as PC is incremented by 2 prior to the addition of e.

CALL AND RETURN GROUP

Mnemonic	Symbolic Operation	Flags					Opcode				No. of Bytes	No. of M Cycles	No. of T States	Comments				
		S	Z	H	P/VN	C	76	543	210	Hex								
CALL nn	(SP-1) \leftarrow PC _H (SP-2) \leftarrow PC _L PC \leftarrow nn,	•	•	X	•	X	•	•	•	•	11	001	101	CD	3	5	17	
CALL cc,nn	If condition cc is false continue, otherwise same as CALL nn	•	•	X	•	X	•	•	•	•	11	cc	100		3	3	10	If cc is false.
															3	5	17	If cc is true.
RET	PC _L \leftarrow (SP) PC _H \leftarrow (SP+1)	•	•	X	•	X	•	•	•	•	11	001	001	C9	1	3	10	
RET cc	If condition cc is false continue, otherwise same as RET	•	•	X	•	X	•	•	•	•	11	cc	000		1	1	5	If cc is false.
															1	3	11	If cc is true.
																		cc Condition
																		000 NZ (non-zero)
																		001 Z (zero)
																		010 NC (non-carry)
RETI	Return from interrupt	•	•	X	•	X	•	•	•	•	11	101	101	ED	2	4	14	011 C (carry)
												01	001	101	4D			100 PO (parity odd)
RETN ¹	Return from non-maskable interrupt	•	•	X	•	X	•	•	•	•	11	101	101	ED	2	4	14	101 PE (parity even)
												01	000	101	45			110 P (sign positive)
																		111 M (sign negative)
RST p	(SP-1) \leftarrow PC _H (SP-2) \leftarrow PC _L PC _H \leftarrow 0 PC _L \leftarrow p	•	•	X	•	X	•	•	•	•	11	t	111		1	3	11	t p
																		000 00H
																		001 08H
																		010 10H
																		011 18H
																		100 20H
																		101 28H
																		110 30H
																		111 38H

NOTE: ¹RETN loads IFF₂ \rightarrow IFF₁

PIN DESCRIPTIONS

A₀-A₁₅. *Address Bus* (output, active High, 3-state). A₀-A₁₅ form a 16-bit address bus. The Address Bus provides the address for memory data bus exchanges (up to 64K bytes) and for I/O device exchanges.

BUSACK. *Bus Acknowledge* (output, active Low). Bus Acknowledge indicates to the requesting device that the CPU address bus, data bus, and control signals \overline{MREQ} , \overline{IORQ} , \overline{RD} , and \overline{WR} have entered their high-impedance states. The external circuitry can now control these lines.

BUSREQ. *Bus Request* (input, active Low). Bus Request has a higher priority than NMI and is always recognized at the end of the current machine cycle. \overline{BUSREQ} forces the CPU address bus, data bus, and control signals \overline{MREQ} , \overline{IORQ} , \overline{RD} , and \overline{WR} to go to a high-impedance state so that other devices can control these lines. \overline{BUSREQ} is normally wired-OR and requires an external pullup for these applications. Extended \overline{BUSREQ} periods due to extensive DMA operations can prevent the CPU from properly refreshing dynamic RAMs.

D₀-D₇. *Data Bus* (input/output, active High, 3-state). D₀-D₇ constitute an 8-bit bidirectional data bus, used for data exchanges with memory and I/O.

HALT. *Halt State* (output, active Low). \overline{HALT} indicates that the CPU has executed a Halt instruction and is awaiting either a nonmaskable or a maskable interrupt (with the mask enabled) before operation can resume. While halted, the CPU executes NOPs to maintain memory refresh.

INT. *Interrupt Request* (input, active Low). Interrupt Request is generated by I/O devices. The CPU honors a request at the end of the current instruction if the internal software-controlled interrupt enable flip-flop (IFF) is enabled. \overline{INT} is normally wired-OR and requires an external pullup for these applications.

IORQ. *Input/Output Request* (output, active Low, 3-state). \overline{IORQ} indicates that the lower half of the address bus holds a valid I/O address for an I/O read or write operation. \overline{IORQ} is also generated concurrently with $\overline{M1}$ during an interrupt acknowledge cycle to indicate that an interrupt response vector can be placed on the data bus.

M1. *Machine Cycle One* (output, active Low). $\overline{M1}$, together with \overline{MREQ} , indicates that the current machine cycle is the opcode fetch cycle of an instruction execution. $\overline{M1}$, together with \overline{IORQ} , indicates an interrupt acknowledge cycle.

MREQ. *Memory Request* (output, active Low, 3-state). \overline{MREQ} indicates that the address bus holds a valid address for a memory read or memory write operation.

NMI. *Non-Maskable Interrupt* (input, negative edge-triggered). \overline{NMI} has a higher priority than \overline{INT} . \overline{NMI} is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop, and automatically forces the CPU to restart at location 0066H.

RD. *Read* (output, active Low, 3-state). \overline{RD} indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.

RESET. *Reset* (input, active Low). \overline{RESET} initializes the CPU as follows: it resets the interrupt enable flip-flop, clears the PC and Registers I and R, and sets the interrupt status to Mode 0. During reset time, the address and data bus go to a high-impedance state, and all control output signals go to the inactive state. Note that \overline{RESET} must be active for a minimum of three full clock cycles before the reset operation is complete.

RFSH. *Refresh* (output, active Low). \overline{RFSH} , together with \overline{MREQ} , indicates that the lower seven bits of the system's address bus can be used as a refresh address to the system's dynamic memories.

WAIT. *Wait* (input, active Low). \overline{WAIT} indicates to the CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter a Wait state as long as this signal is active. Extended \overline{WAIT} periods can prevent the CPU from properly refreshing dynamic memory.

WR. *Write* (output, active Low, 3-state). \overline{WR} indicates that the CPU data bus holds valid data to be stored at the addressed memory or I/O location.

CPU TIMING

The Z80 CPU executes instructions by proceeding through a specific sequence of operations:

- Memory read or write
- I/O device read or write
- Interrupt acknowledge

The basic clock period is referred to as a T time or cycle, and three or more T cycles make up a machine cycle (M1, M2 or M3 for instance). Machine cycles can be extended either by the CPU automatically inserting one or more Wait states or by the insertion of one or more Wait states by the user.

Instruction Opcode Fetch. The CPU places the contents of the Program Counter (PC) on the address bus at the start of the cycle (Figure 5). Approximately one-half clock cycle later, \overline{MREQ} goes active. When active, \overline{RD} indicates that the memory data can be enabled onto the CPU data bus.

The CPU samples the \overline{WAIT} input with the falling edge of clock state T_2 . During clock states T_3 and T_4 of an $\overline{M1}$ cycle, dynamic RAM refresh can occur while the CPU starts decoding and executing the instruction. When the Refresh Control signal becomes active, refreshing of dynamic memory can take place.

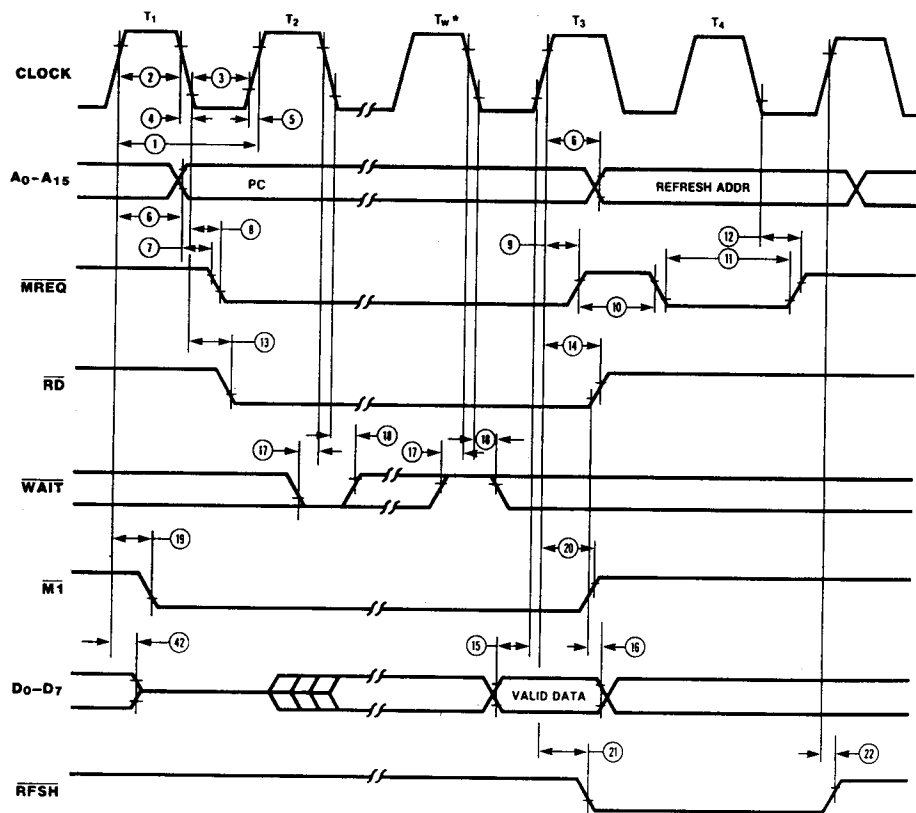


Figure 5. Instruction Opcode Fetch

Memory Read or Write Cycles. Figure 6 shows the timing of memory read or write cycles other than an opcode fetch ($\overline{M1}$) cycle. The \overline{MREQ} and \overline{RD} signals function exactly as in the fetch cycle. In a memory write cycle, \overline{MREQ} also

becomes active when the address bus is stable. The \overline{WR} line is active when the data bus is stable, so that it can be used directly as an R/W pulse to most semiconductor memories.

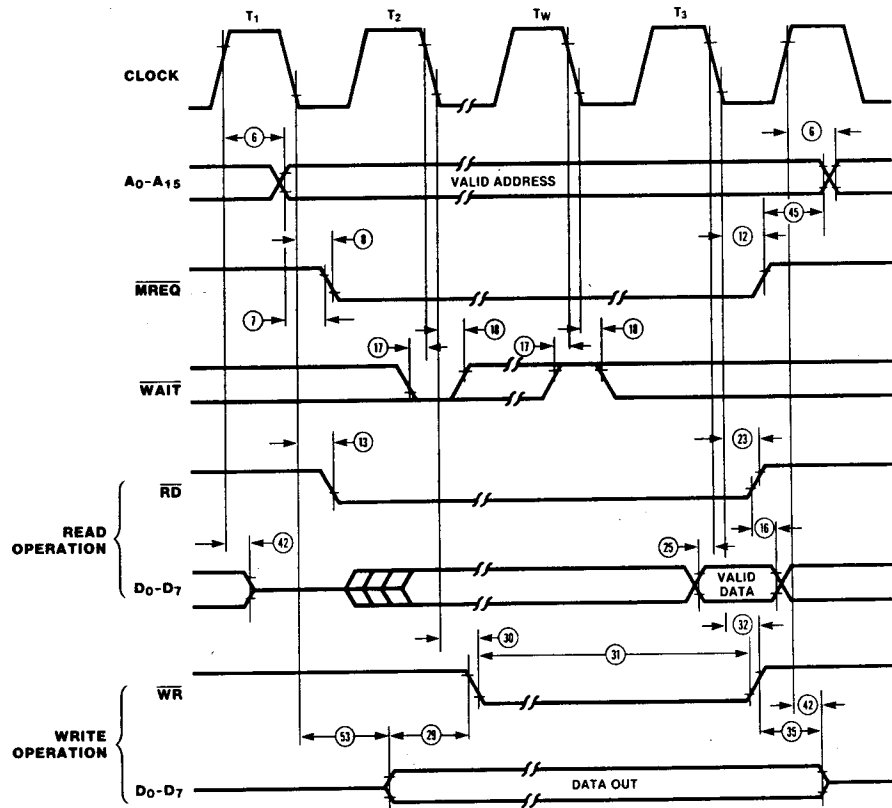
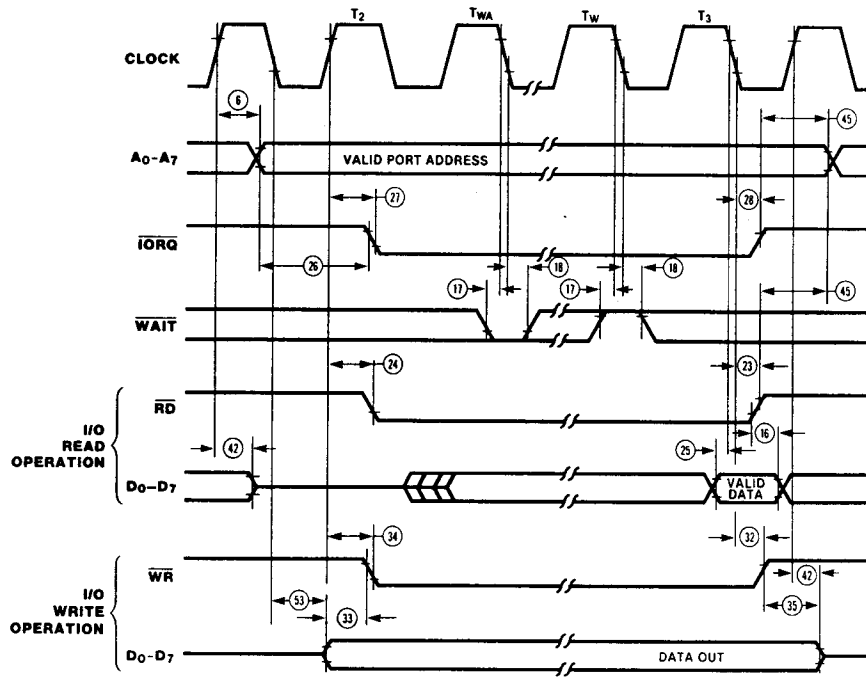


Figure 6. Memory Read or Write Cycles

Input or Output Cycles. Figure 7 shows the timing for an I/O read or I/O write operation. During I/O operations, the CPU automatically inserts a single Wait state (T_{WA}). This

extra Wait state allows sufficient time for an I/O port to decode the address from the port address lines.

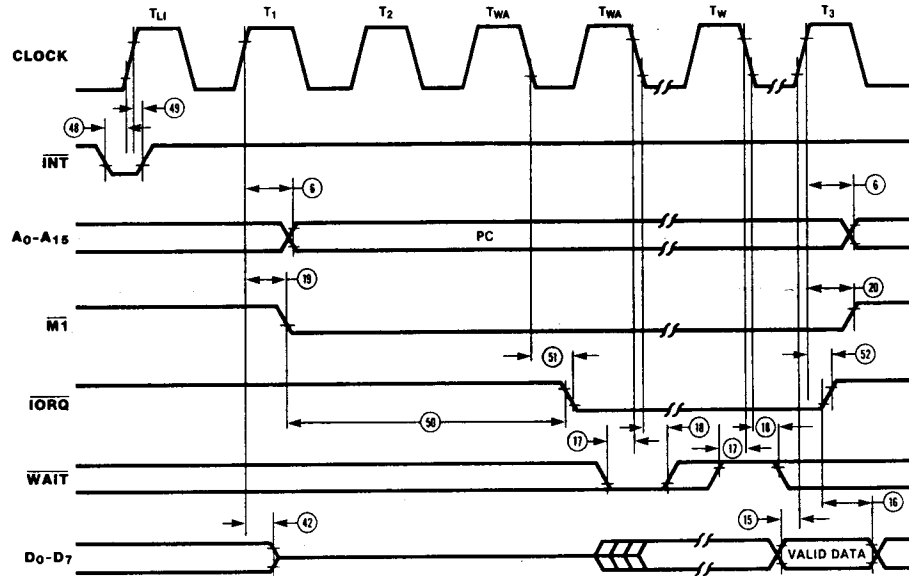


T_{WA} = One wait cycle automatically inserted by CPU.

Figure 7. Input or Output Cycles

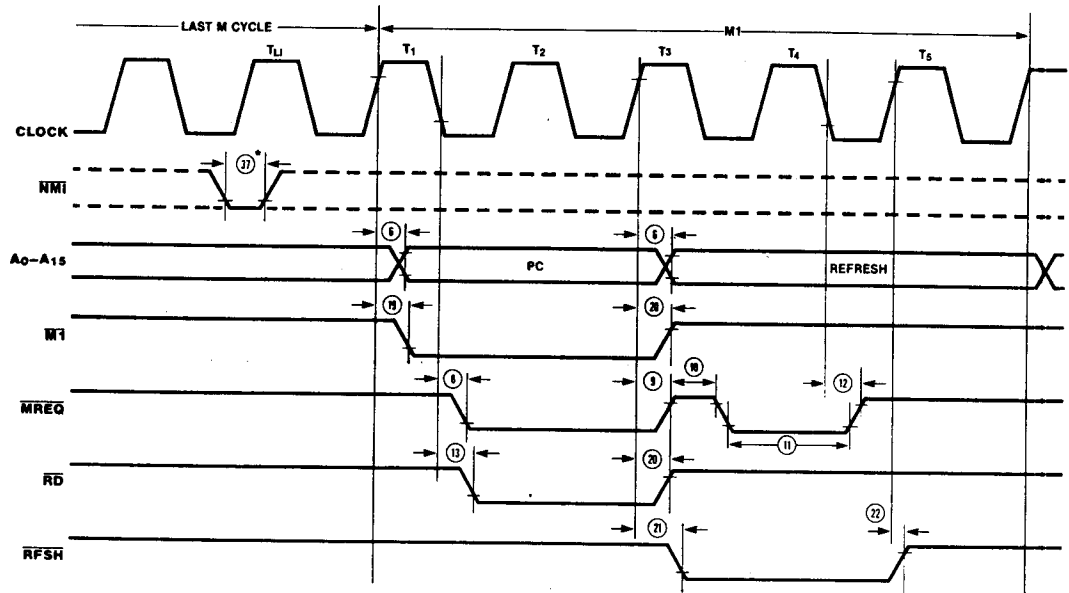
Interrupt Request/Acknowledge Cycle. The CPU samples the interrupt signal with the rising edge of the last clock cycle at the end of any instruction (Figure 8). When an interrupt is accepted, a special M1 cycle is generated.

During this $\overline{M1}$ cycle, \overline{IORQ} becomes active (instead of \overline{MREQ}) to indicate that the interrupting device can place an 8-bit vector on the data bus. The CPU automatically adds two Wait states to this cycle.



Non-Maskable Interrupt Request Cycle. $\overline{\text{NMI}}$ is sampled at the same time as the maskable interrupt input $\overline{\text{INT}}$ but has higher priority and cannot be disabled under software control. The subsequent timing is similar to that of a normal

memory read operation except that data put on the bus by the memory is ignored. The CPU instead executes a restart (RST) operation and jumps to the $\overline{\text{NMI}}$ service routine located at address 0066H (Figure 9).



*Although $\overline{\text{NMI}}$ is an asynchronous input, to guarantee its being recognized on the following machine cycle, $\overline{\text{NMI}}$'s falling edge must occur no later than the rising edge of the clock cycle preceding the last state of any instruction cycle (T_{L1}).

Figure 9. Non-Maskable Interrupt Request Operation

ABSOLUTE MAXIMUM RATINGS

Voltage on V_{CC} with respect to V_{SS} $-0.3V$ to $+7V$
Voltages on all inputs with respect
to V_{SS} $-0.3V$ to $V_{CC} + 0.3V$
Operating Ambient
Temperature See Ordering Information
Storage Temperature $-65^{\circ}C$ to $+150^{\circ}C$

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

The DC Characteristics and capacitance sections below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND (0V). Positive current flows into the referenced pin.

The Ordering Information section lists temperature ranges and product numbers. Package drawings are in the Package Information section. Refer to the Literature List for additional documentation.

Available operating temperature ranges are:

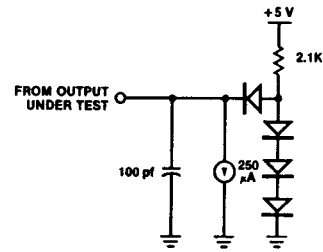
■ **S = $0^{\circ}C$ to $+70^{\circ}C$**

Voltage Supply Range:

NMOS: $+4.75V \leq V_{CC} \leq +5.25V$
CMOS: $+4.50V \leq V_{CC} \leq +5.50V$

■ **E = $-40^{\circ}C$ to $100^{\circ}C$, $+4.50V \leq V_{CC} \leq +5.50V$**

All ac parameters assume a load capacitance of 100 pf. Add 10 ns delay for each 50 pf increase in load up to a maximum of 200 pf for the data bus and 100 pf for address and control lines. AC timing measurements are referenced to 1.5 volts (except for clock, which is referenced to the 10% and 90% points).



AC CHARACTERISTICS† (Z84C00/CMOS Z80 CPU)

V_{cc}=5.0V ± 10%, unless otherwise specified

No	Symbol	Parameter	Z84C0004**		Z84C0006		Z84C0008		Z84C0010		Z84C0020[1]		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
1	TcC	Clock Cycle time	250*	DC	162*	DC	125*	DC	100*	DC	50*	DC	nS	
2	TwCh	Clock Pulse width (high)	110	DC	65	DC	55	DC	40	DC	20	DC	nS	
3	TwCl	Clock Pulse width (low)	110	DC	65	DC	55	DC	40	DC	20	DC	nS	
4	TfC	Clock Fall time		30		20		10		10		10	nS	
5	TrC	Clock Rise time		30		20		10		10		10	nS	
6	TdCr(A)	Address valid from Clock Rise		110		90		80		65		57	nS	[2]
7	TdA(MREQf)	Address valid to /MREQ Fall	65*		35*		20*		5*		-15*		nS	
8	TdCf(MREQf)	Clock Fall to /MREQ Fall delay		85		70		60		55		40	nS	
9	TdCr(MREQr)	Clock Rise to /MREQ Rise delay		85		70		60		55		40	nS	
10	TwMREQh	/MREQ pulse width (High)	110*		65*		45**		30*		10*		nS	[3]
11	TwMREQl	/MREQ pulse width (low)	220*		132*		100*		75*		25*		nS	[3]
12	TdCf(MERQr)	Clock Fall to /MREQ Rise delay		85		70		60		55		40	nS	
13	TdCf(RDf)	Clock Fall to /RD Fall delay		95		80		70		65		40	nS	
14	TdCr(RDr)	Clock Rise to /RD Rise delay		85		70		60		55		40	nS	
15	TsD(Cr)	Data setup time to Clock Rise	35		30		30		25		12		nS	
16	ThD(RDr)	Data hold time after /RD Rise	0		0		0		0		0		nS	
17	TsWAIT(Cf)	/WAIT setup time to Clock Fall	70		60		50		20		7.5		nS	
18	ThWAIT(Cf)	/WAIT hold time after Clock Fall	10		10		10		10		10		nS	
19	TdCr(M1f)	Clock Rise to /M1 Fall delay		100		80		70		65		45	nS	
20	TdCr(M1r)	Clock Rise to /M1 Rise delay		100		80		70		65		45	nS	
21	TdCr(RFSHf)	Clock Rise to /RFSH Fall delay		130		110		95		80		60	nS	
22	TdCr(RFSHr)	Clock Rise to /RFSH Rise delay		120		100		85		80		60	nS	
23	TdCf(RDr)	Clock Fall to /RD Rise delay		85		70		60		55		40	nS	
24	TdCr(RDf)	Clock Rise to /RD Fall delay		85		70		60		55		40	nS	
25	TsD(Cf)	Data setup to Clock Fall during M2, M3, M4 or M5 cycles	50		40		30		25		12		nS	
26	TdA(IORQf)	Address stable prior to /IORQ Fall	180*		107*		75*		50*		0*		nS	
27	TdCr(IORQf)	Clock Rise to /IORQ Fall delay		75		65		55		50		40	nS	
28	TdCf(IORQr)	Clock Fall to /IORQ Rise delay		85		70		60		55		40	nS	
29	TdD(WRf)Mw	Data stable prior to /WR Fall	80*		22*		5*		40*		-10*		nS	
30	TdCf(WRf)	Clock Fall to /WR Fall delay		80		70		60		55		40	nS	
31	TwWR	/WR pulse width	220*		132*		100*		75*		25*		nS	
32	TdCf(WRr)	Clock Fall to /WR Rise delay		80		70		60		55		40	nS	
33	TdD(WRf)IO	Data stable prior to /WR Fall	-10*		-55*		-55*		-10*		-30*		nS	
34	TdCr(WRf)	Clock Rise to /WR Fall delay		65		60		60		50		40	nS	
35	TdWRr(D)	Data stable from /WR Rise	60*		30*		15*		10*		0*		nS	
36	TdCf(HALT)	Clock Fall to /HALT 'L' or 'H'		300		260		225		90		70	nS	
37	TwNMI	/NMI pulse width	80		60		60		60		60		nS	
38	TsBUSREQ (Cr)	/BUSREQ setup time to Clock Rise	50		50		40		30		15		nS	

*For clock periods other than the minimums shown, calculate parameters using the table on the following page.
Calculated values above assumed TrC = TtC = 20 ns.

†Units in nanoseconds (ns).

†† For loading ≥ 50 pf. Decrease width by 10 ns for each additional 50 pf.

**4 MHz CMOS Z80 is obsoleted and replaced by 6 MHz

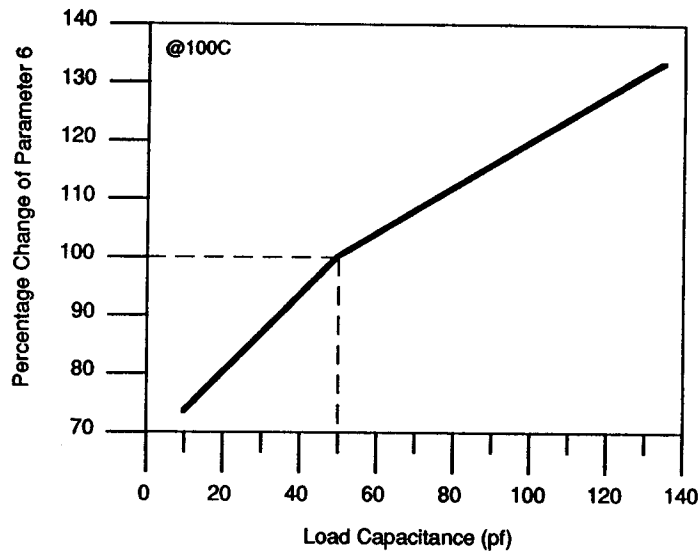


Figure 1. Address Delay Characteristics
(Parameter 6)

DC CHARACTERISTICS (Z8400/NMOS Z80 CPU)

All parameters are tested unless otherwise noted.

Symbol	Parameter	Min	Max	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	-0.3	0.45	V	
V_{IHC}	Clock Input High Voltage	$V_{CC} - .6$	$V_{CC} + .3$	V	
V_{IL}	Input Low Voltage	-0.3	0.8	V	
V_{IH}	Input High Voltage	2.0^1	V_{CC}	V	
V_{OL}	Output Low Voltage		0.4	V	$I_{OL} = 2.0 \text{ mA}$
V_{OH}	Output High Voltage	2.4^1		V	$I_{OH} = -250 \mu\text{A}$
I_{CC}	Power Supply Current		200	mA	Note 3
I_{LI}	Input Leakage Current		10	μA	$V_{IN} = 0 \text{ to } V_{CC}$
I_{LO}	3-State Output Leakage Current in Float	-10	10^2	μA	$V_{OUT} = 0.4 \text{ to } V_{CC}$

1. For military grade parts, refer to the Z80 Military Electrical Specification.

2. A_{15} - A_0 , D_7 - D_0 , $MREQ$, $IORD$, RD , and WR .

3. Measurements made with outputs floating.

CAPACITANCE

Guaranteed by design and characterization.

Symbol	Parameter	Min	Max	Unit
C_{CLOCK}	Clock Capacitance		35	pf
C_{IN}	Input Capacitance		5	pf
C_{OUT}	Output Capacitance		15	pf

NOTES:

$T_A = 25^\circ\text{C}$, $f = 1 \text{ MHz}$.

Unmeasured pins returned to ground.

Customer Support

For answers to technical questions about the product, documentation, or any other issues with Zilog's offerings, please visit Zilog's Knowledge Base at <http://www.zilog.com/kb>.

For any comments, detail technical questions, or reporting problems, please visit Zilog's Technical Support at <http://support.zilog.com>.