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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | Z80 |
| Number of Cores/Bus Width | 1 Core, 8-Bit |
| Speed | 20MHz |
| Co-Processors/DSP | - |
| RAM Controllers | - |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | - |
| SATA | - |
| USB | - |
| Voltage - I/O | 5.0V |
| Operating Temperature | -40°C ~ 100°C (TA) |
| Security Features | - |
| Package / Case | 44-LCC (J-Lead) |
| Supplier Device Package | 44-PLCC |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/z84c0020veg |

**address. This flexibility in selecting the interrupt service routine address allows the peripheral device to use several different types of service routines. These routines may be located at any available location in memory. Since the interrupting device supplies the low-order byte of the 2-byte vector, bit 0 ($A_0$) must be a zero.**

**Interrupt Enable/Disable Operation.** Two flip-flops, $IFF_1$ and $IFF_2$, referred to in the register description, are used to signal the CPU interrupt status. Operation of the two flip-flops is described in Table 2. For more details, refer to the *Z80 CPU Technical Manual* (03-0029-01) and *Z80 Assembly Language Programming Manual* (03-0002-01).

**Table 2. State of Flip-Flops**

| Action | $IFF_1$ | $IFF_2$ | Comments |
|---|---|---|---|
| CPU Reset | 0 | 0 | Maskable interrupt $\overline{INT}$ disabled |
| DI instruction execution | 0 | 0 | Maskable interrupt $\overline{INT}$ disabled |
| EI instruction execution | 1 | 1 | Maskable interrupt $\overline{INT}$ enabled |
| LD A,I instruction execution | • | • | $IFF_2 \rightarrow$ Parity flag |
| LD A,R instruction execution | • | • | $IFF_2 \rightarrow$ Parity flag |
| Accept $\overline{NMI}$ | 0 | • | Maskable interrupt $\overline{INT}$ disabled |
| RETN instruction execution | $IFF_2$ | • | $IFF_2 \rightarrow IFF_1$ at completion of an $\overline{NMI}$ service routine. |

## INSTRUCTION SET

The microprocessor has one of the most powerful and versatile instruction sets available in any 8-bit microprocessor. It includes such unique operations as a block move for fast, efficient data transfers within memory, or between memory and I/O. It also allows operations on any bit in any location in memory.

The following is a summary of the instruction set which shows the assembly language mnemonic, the operation, the flag status, and gives comments on each instruction. For an explanation of flag notations and symbols for mnemonic tables, see the Symbolic Notations section which follows these tables. The *Z80 CPU Technical Manual* (03-0029-01), the *Programmer's Reference Guide* (03-0012-03), and *Assembly Language Programming Manual* (03-0002-01) contain significantly more details for programming use.

The instructions are divided into the following categories:

- 8-bit loads
- 16-bit loads
- Exchanges, block transfers, and searches
- 8-bit arithmetic and logic operations
- General-purpose arithmetic and CPU control
- 16-bit arithmetic operations
- Rotates and shifts
- Bit set, reset, and test operations
- Jumps
- Calls, returns, and restarts
- Input and output operations

A variety of addressing modes are implemented to permit efficient and fast data transfer between various registers, memory locations, and input/output devices. These addressing modes include:

- Immediate
- Immediate extended
- Modified page zero
- Relative
- Extended
- Indexed
- Register
- Register indirect
- Implied
- Bit

## 8-BIT LOAD GROUP

| Mnemonic | Symbolic Operation | S | Z | H | P/V | N | C | 76 | 543 | 210 | Hex | No. of Bytes | No. of M Cycles | No. of T States | Comments |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LD r, r' | r ← r' | • | • | X | • | X | • | • | • | 01 | r | r' | | 1 | 1 | 4 | r, r' Reg. |
| LD r, n | r ← n | • | • | X | • | X | • | • | • | 00 | r | 110 | | 2 | 2 | 7 | 000 B |
| | | | | | | | | | | | ← n → | | | | | | 001 C |
| LD r, (HL) | r ← (HL) | • | • | X | • | X | • | • | • | 01 | r | 110 | | 1 | 2 | 7 | 010 D |
| LD r, (IX + d) | r ← (IX + d) | • | • | X | • | X | • | • | • | 11 | 011 | 101 | DD | 3 | 5 | 19 | 011 E |
| | | | | | | | | | | 01 | r | 110 | | | | | 100 H |
| | | | | | | | | | | | ← d → | | | | | | 101 L |
| LD r, (IY + d) | r ← (IY + d) | • | • | X | • | X | • | • | • | 11 | 111 | 101 | FD | 3 | 5 | 19 | 111 A |
| | | | | | | | | | | 01 | r | 110 | | | | | |
| | | | | | | | | | | | ← d → | | | | | | |
| LD (HL), r | (HL) ← r | • | • | X | • | X | • | • | • | 01 | 110 | r | | 1 | 2 | 7 | |
| LD (IX + d), r | (IX + d) ← r | • | • | X | • | X | • | • | • | 11 | 011 | 101 | DD | 3 | 5 | 19 | |
| | | | | | | | | | | 01 | 110 | r | | | | | |
| | | | | | | | | | | | ← d → | | | | | | |
| LD (IY + d), r | (IY + d) ← r | • | • | X | • | X | • | • | • | 11 | 111 | 101 | FD | 3 | 5 | 19 | |
| | | | | | | | | | | 01 | 110 | r | | | | | |
| | | | | | | | | | | | ← d → | | | | | | |
| LD (HL), n | (HL) ← n | • | • | X | • | X | • | • | • | 00 | 110 | 110 | 36 | 2 | 3 | 10 | |
| | | | | | | | | | | | ← n → | | | | | | |
| LD (IX + d), n | (IX + d) ← n | • | • | X | • | X | • | • | • | 11 | 011 | 101 | DD | 4 | 5 | 19 | |
| | | | | | | | | | | 00 | 110 | 110 | 36 | | | | |
| | | | | | | | | | | | ← d → | | | | | | |
| | | | | | | | | | | | ← n → | | | | | | |

## 16-BIT LOAD GROUP (Continued)

| Mnemonic | Symbolic Operation | S | Z | H | P/V | N | C | 76 | 543 | 210 | Hex | No. of Bytes | No. of M Cycles | No. of T States | Comments |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LD IX, (nn) | $IX_H \leftarrow (nn+1)$ | • | • | X | X | • | • | 11 | 011 | 101 | DD | 4 | 6 | 20 | |
| | $IX_L \leftarrow (nn)$ | | | | | | | 00 | 101 | 010 | 2A | | | | |
| | | | | | | | | | ←n→ | | | | | | |
| | | | | | | | | | ←n→ | | | | | | |
| LD IY, (nn) | $IY_H \leftarrow (nn+1)$ | • | • | X | X | • | • | 11 | 111 | 101 | FD | 4 | 6 | 20 | |
| | $IY_L \leftarrow (nn)$ | | | | | | | 00 | 101 | 010 | 2A | | | | |
| | | | | | | | | | ←n→ | | | | | | |
| | | | | | | | | | ←n→ | | | | | | |
| LD (nn), HL | $(nn+1) \leftarrow H$ | • | • | X | X | • | • | 00 | 100 | 010 | 22 | 3 | 5 | 16 | |
| | $(nn) \leftarrow L$ | | | | | | | | ←n→ | | | | | | |
| | | | | | | | | | ←n→ | | | | | | |
| LD (nn), dd | $(nn+1) \leftarrow dd_H$ | • | • | X | X | • | • | 11 | 101 | 101 | ED | 4 | 6 | 20 | |
| | $(nn) \leftarrow dd_L$ | | | | | | | 01 | dd0 | 011 | | | | | |
| | | | | | | | | | ←n→ | | | | | | |
| | | | | | | | | | ←n→ | | | | | | |
| LD (nn), IX | $(nn+1) \leftarrow IX_H$ | • | • | X | X | • | • | 11 | 011 | 101 | DD | 4 | 6 | 20 | |
| | $(nn) \leftarrow IX_L$ | | | | | | | 00 | 100 | 010 | 22 | | | | |
| | | | | | | | | | ←n→ | | | | | | |
| | | | | | | | | | ←n→ | | | | | | |
| LD (nn), IY | $(nn+1) \leftarrow IY_H$ | • | • | X | X | • | • | 11 | 111 | 101 | FD | 4 | 6 | 20 | |
| | $(nn) \leftarrow IY_L$ | | | | | | | 00 | 100 | 010 | 22 | | | | |
| | | | | | | | | | ←n→ | | | | | | |
| | | | | | | | | | ←n→ | | | | | | |
| LD SP, HL | $SP \leftarrow HL$ | • | • | X | X | • | • | 11 | 111 | 001 | F9 | 1 | 1 | 6 | |
| LD SP, IX | $SP \leftarrow IX$ | • | • | X | X | • | • | 11 | 011 | 101 | DD | 2 | 2 | 10 | |
| | | | | | | | | 11 | 111 | 001 | F9 | | | | |
| LD SP, IY | $SP \leftarrow IY$ | • | • | X | X | • | • | 11 | 111 | 101 | FD | 2 | 2 | 10 | |
| | | | | | | | | 11 | 111 | 001 | F9 | | | | |
| PUSH qq | $(SP-2) \leftarrow qq_L$ | • | • | X | X | • | • | 11 | qq0 | 101 | | 1 | 3 | 11 | |
| | $(SP-1) \leftarrow qq_H$ | | | | | | | | | | | | | | |
| | $SP \rightarrow SP-2$ | | | | | | | | | | | | | | |
| PUSH IX | $(SP-2) \leftarrow IX_L$ | • | • | X | X | • | • | 11 | 011 | 101 | DD | 2 | 4 | 15 | |
| | $(SP-1) \leftarrow IX_H$ | | | | | | | 11 | 100 | 101 | E5 | | | | |
| | $SP \rightarrow SP-2$ | | | | | | | | | | | | | | |
| PUSH IY | $(SP-2) \leftarrow IY_L$ | • | • | X | X | • | • | 11 | 111 | 101 | FD | 2 | 4 | 15 | |
| | $(SP-1) \leftarrow IY_H$ | | | | | | | 11 | 100 | 101 | E5 | | | | |
| | $SP \rightarrow SP-2$ | | | | | | | | | | | | | | |
| POP qq | $qq_H \leftarrow (SP+1)$ | • | • | X | X | • | • | 11 | qq0 | 001 | | 1 | 3 | 10 | |
| | $qqL \leftarrow (SP)$ | | | | | | | | | | | | | | |
| | $SP \rightarrow SP+2$ | | | | | | | | | | | | | | |
| POP IX | $IX_H \leftarrow (SP+1)$ | • | • | X | X | • | • | 11 | 011 | 101 | DD | 2 | 4 | 14 | |
| | $IX_L \leftarrow (SP)$ | | | | | | | 11 | 100 | 001 | E1 | | | | |
| | $SP \rightarrow SP+2$ | | | | | | | | | | | | | | |
| POP IY | $IY_H \leftarrow (SP+1)$ | • | • | X | X | • | • | 11 | 111 | 101 | FD | 2 | 4 | 14 | |
| | $IY_L \leftarrow (SP)$ | | | | | | | 11 | 100 | 001 | E1 | | | | |
| | $SP \rightarrow SP+2$ | | | | | | | | | | | | | | |

| qq | Pair |
|---|---|
| 00 | BC |
| 01 | DE |
| 10 | HL |
| 11 | AF |

NOTE: $(PAIR)_H$, $(PAIR)_L$ refer to high order and low order eight bits of the register pair respectively, e.g., $BC_L$ = C, $AF_H$ = A.

## 8-BIT ARITHMETIC AND LOGICAL GROUP (Continued)

| Mnemonic | Symbolic Operation | S | Z | | H | | P/V | N | C | 76 | 543 | 210 | Hex | No. of Bytes | No. of M Cycles | No. of T States | Comments |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| INC r | r ← r + 1 | ‡ | ‡ | X | ‡ | X | V | 0 | • | 00 | r | 100 | | 1 | 1 | 4 | |
| INC (HL) | (HL) ← | | | | | | | | | | | | | | | | |
| | (HL) + 1 | ‡ | ‡ | X | ‡ | X | V | 0 | • | 00 | 110 | 100 | | 1 | 3 | 11 | |
| INC (IX + d) | (IX + d) ← | ‡ | ‡ | X | ‡ | X | V | 0 | • | 11 | 011 | 101 | DD | 3 | 6 | 23 | |
| | (IX + d) + 1 | | | | | | | | | 00 | 110 | 100 | | | | | |
| | | | | | | | | | | ← d → | | | | | | | |
| INC (IY + d) | (IY + d) ← | ‡ | ‡ | X | ‡ | X | V | 0 | • | 11 | 111 | 101 | FD | 3 | 6 | 23 | |
| | (IY + d) + 1 | | | | | | | | | 00 | 110 | 100 | | | | | |
| | | | | | | | | | | ← d → | | | | | | | |
| DEC m | m ← m − 1 | ‡ | ‡ | X | ‡ | X | V | 1 | • | | | 101 | | | | | |

NOTE: m is any of r, (HL), (IX + d), (IY + d) as shown for INC. DEC same format and states as INC. Replace 100 with 101 in opcode.

## GENERAL-PURPOSE ARITHMETIC AND CPU CONTROL GROUPS

| Mnemonic | Symbolic Operation | S | Z | | H | | P/V | N | C | 76 | 543 | 210 | Hex | No. of Bytes | No. of M Cycles | No. of T States | Comments |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DAA | @ | ‡ | ‡ | X | ‡ | X | P | • | ‡ | 00 | 100 | 111 | 27 | 1 | 1 | 4 | Decimal adjust accumulator. |
| CPL | A ← Ā | • | • | X | 1 | X | • | 1 | • | 00 | 101 | 111 | 2F | 1 | 1 | 4 | Complement accumulator (one's complement). |
| NEG | A ← 0 − A | ‡ | ‡ | X | ‡ | X | V | 1 | ‡ | 11 | 101 | 101 | ED | 2 | 2 | 8 | Negate acc. (two's complement). |
| | | | | | | | | | | 01 | 000 | 100 | 44 | | | | |
| CCF | CY ← C̄Y | • | • | X | X | X | • | 0 | ‡ | 00 | 111 | 111 | 3F | 1 | 1 | 4 | Complement carry flag. |
| SCF | CY ← 1 | • | • | X | 0 | X | • | 0 | 1 | 00 | 110 | 111 | 37 | 1 | 1 | 4 | Set carry flag. |
| NOP | No operation | • | • | X | • | X | • | • | • | 00 | 000 | 000 | 00 | 1 | 1 | 4 | |
| HALT | CPU halted | • | • | X | • | X | • | • | • | 01 | 110 | 110 | 76 | 1 | 1 | 4 | |
| DI ★ | IFF ← 0 | • | • | X | • | X | • | • | • | 11 | 110 | 011 | F3 | 1 | 1 | 4 | |
| EI ★ | IFF ← 1 | • | • | X | • | X | • | • | • | 11 | 111 | 011 | FB | 1 | 1 | 4 | |
| IM 0 | Set interrupt | • | • | X | • | X | • | • | • | 11 | 101 | 101 | ED | 2 | 2 | 8 | |
| | mode 0 | | | | | | | | | 01 | 000 | 110 | 46 | | | | |
| IM 1 | Set interrupt | • | • | X | • | X | • | • | • | 11 | 101 | 101 | ED | 2 | 2 | 8 | |
| | mode 1 | | | | | | | | | 01 | 010 | 110 | 56 | | | | |
| IM 2 | Set interrupt | • | • | X | • | X | • | • | • | 11 | 101 | 101 | ED | 2 | 2 | 8 | |
| | mode 2 | | | | | | | | | 01 | 011 | 110 | 5E | | | | |

NOTES: @ converts accumulator content into packed BCD following add or subtract with packed BCD operands.
IFF indicates the interrupt enable flip-flop.
CY indicates the carry flip-flop.
★ indicates interrupts are not sampled at the end of EI or DI.

## BIT SET, RESET AND TEST GROUP

| Mnemonic | Symbolic Operation | S | Z | H | P/V | N | C | 76 | 543 | 210 | Hex | No. of Bytes | No. of M Cycles | No. of T States | Comments |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| BIT b, r | $Z \leftarrow r_b$ | X | ‡ | X | X | 0 | • | 11 | 001 | 011 | CB | 2 | 2 | 8 | r Reg. |
| | | | | | | | | 01 | b | r | | | | | 000 B |
| BIT b, (HL) | $Z \leftarrow (HL)_b$ | X | ‡ | X | X | 0 | • | 11 | 001 | 011 | CB | 2 | 3 | 12 | 001 C |
| | | | | | | | | 01 | b | 110 | | | | | 010 D |
| BIT b,(IX+d) | $Z \leftarrow (IX+d)_b$ | X | ‡ | X | X | 0 | • | 11 | 011 | 101 | DD | 4 | 5 | 20 | 011 E |
| | | | | | | | | 11 | 001 | 011 | CB | | | | 100 H |
| | | | | | | | | | ←d→ | | | | | | 101 L |
| | | | | | | | | 01 | b | 110 | | | | | 111 A |
| BIT b, (IY+d) | $Z \leftarrow (IY+d)_b$ | X | ‡ | X | X | 0 | • | 11 | 111 | 101 | FD | 4 | 5 | 20 | b Bit Tested |
| | | | | | | | | 11 | 001 | 011 | CB | | | | 000 0 |
| | | | | | | | | | ←d→ | | | | | | 001 1 |
| | | | | | | | | 01 | b | 110 | | | | | 010 2 |
| SET b, r | $r_b \leftarrow 1$ | • | • | X | X | • | • | 11 | 001 | 011 | CB | 2 | 2 | 8 | 011 3 |
| | | | | | | | | [11] | b | r | | | | | 100 4 |
| SET b, (HL) | $(HL)_b \leftarrow 1$ | • | • | X | X | • | • | 11 | 001 | 011 | CB | 2 | 4 | 15 | 101 5 |
| | | | | | | | | [11] | b | 110 | | | | | 110 6 |
| SET b, (IX+d) | $(IX+d)_b \leftarrow 1$ | • | • | X | X | • | • | 11 | 011 | 101 | DD | 4 | 6 | 23 | 111 7 |
| | | | | | | | | 11 | 001 | 011 | CB | | | | |
| | | | | | | | | | ←d→ | | | | | | |
| | | | | | | | | [11] | b | 110 | | | | | |
| SET b, (IY+d) | $(IY+d)_b \leftarrow 1$ | • | • | X | X | • | • | 11 | 111 | 101 | FD | 4 | 6 | 23 | |
| | | | | | | | | 11 | 001 | 011 | CB | | | | |
| | | | | | | | | | ←d→ | | | | | | |
| | | | | | | | | [11] | b | 110 | | | | | |
| RES b, m | $m_b \leftarrow 0$ m≡r, (HL), (IX+d), (IY+d) | • | • | X | X | • | • | [10] | | | | | | | To form new opcode replace [11] of SET b, s with [10]. Flags and time states for SET instruction. |

NOTE: The notation $m_b$ indicates location m, bit b (0 to 7).

## PIN DESCRIPTIONS

**$A_0$-$A_{15}$.** *Address Bus* (output, active High, 3-state). $A_0$-$A_{15}$ form a 16-bit address bus. The Address Bus provides the address for memory data bus exchanges (up to 64K bytes) and for I/O device exchanges.

**$\overline{\text{BUSACK}}$.** *Bus Acknowledge* (output, active Low). Bus Acknowledge indicates to the requesting device that the CPU address bus, data bus, and control signals $\overline{\text{MREQ}}$, $\overline{\text{IORQ}}$, $\overline{\text{RD}}$, and $\overline{\text{WR}}$ have entered their high-impedance states. The external circuitry can now control these lines.

**$\overline{\text{BUSREQ}}$.** *Bus Request* (input, active Low). Bus Request has a higher priority than $\overline{\text{NMI}}$ and is always recognized at the end of the current machine cycle. $\overline{\text{BUSREQ}}$ forces the CPU address bus, data bus, and control signals $\overline{\text{MREQ}}$, $\overline{\text{IORQ}}$, RD, and WR to go to a high-impedance state so that other devices can control these lines. $\overline{\text{BUSREQ}}$ is normally wired-OR and requires an external pullup for these applications. Extended $\overline{\text{BUSREQ}}$ periods due to extensive DMA operations can prevent the CPU from properly refreshing dynamic RAMs.

**$D_0$-$D_7$.** *Data Bus* (input/output, active High, 3-state). $D_0$-$D_7$ constitute an 8-bit bidirectional data bus, used for data exchanges with memory and I/O.

**$\overline{\text{HALT}}$.** *Halt State* (output, active Low). $\overline{\text{HALT}}$ indicates that the CPU has executed a Halt instruction and is awaiting either a nonmaskable or a maskable interrupt (with the mask enabled) before operation can resume. While halted, the CPU executes NOPs to maintain memory refresh.

**$\overline{\text{INT}}$.** *Interrupt Request* (input, active Low). Interrupt Request is generated by I/O devices. The CPU honors a request at the end of the current instruction if the internal software-controlled interrupt enable flip-flop (IFF) is enabled. $\overline{\text{INT}}$ is normally wired-OR and requires an external pullup for these applications.

**$\overline{\text{IORQ}}$.** *Input/Output Request* (output, active Low, 3-state). $\overline{\text{IORQ}}$ indicates that the lower half of the address bus holds a valid I/O address for an I/O read or write operation. $\overline{\text{IORQ}}$ is also generated concurrently with $\overline{\text{M1}}$ during an interrupt acknowledge cycle to indicate that an interrupt response vector can be placed on the data bus.

**$\overline{\text{M1}}$.** *Machine Cycle One* (output, active Low). $\overline{\text{M1}}$, together with $\overline{\text{MREQ}}$, indicates that the current machine cycle is the opcode fetch cycle of an instruction execution. $\overline{\text{M1}}$, together with $\overline{\text{IORQ}}$, indicates an interrupt acknowledge cycle.

**$\overline{\text{MREQ}}$.** *Memory Request* (output, active Low, 3-state). $\overline{\text{MREQ}}$ indicates that the address bus holds a valid address for a memory read or memory write operation.

**$\overline{\text{NMI}}$.** *Non-Maskable Interrupt* (input, negative edge-triggered). $\overline{\text{NMI}}$ has a higher priority than $\overline{\text{INT}}$. $\overline{\text{NMI}}$ is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop, and automatically forces the CPU to restart at location 0066H.

**$\overline{\text{RD}}$.** *Read* (output, active Low, 3-state). $\overline{\text{RD}}$ indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.

**$\overline{\text{RESET}}$.** *Reset* (input, active Low). $\overline{\text{RESET}}$ initializes the CPU as follows: it resets the interrupt enable flip-flop, clears the PC and Registers I and R, and sets the interrupt status to Mode 0. During reset time, the address and data bus go to a high-impedance state, and all control output signals go to the inactive state. Note that $\overline{\text{RESET}}$ must be active for a minimum of three full clock cycles before the reset operation is complete.

**$\overline{\text{RFSH}}$.** *Refresh* (output, active Low). $\overline{\text{RFSH}}$, together with $\overline{\text{MREQ}}$, indicates that the lower seven bits of the system's address bus can be used as a refresh address to the system's dynamic memories.

**$\overline{\text{WAIT}}$.** *Wait* (input, active Low). $\overline{\text{WAIT}}$ indicates to the CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter a Wait state as long as this signal is active. Extended $\overline{\text{WAIT}}$ periods can prevent the CPU from properly refreshing dynamic memory.

**$\overline{\text{WR}}$.** *Write* (output, active Low, 3-state). $\overline{\text{WR}}$ indicates that the CPU data bus holds valid data to be stored at the addressed memory or I/O location.

**Memory Read or Write Cycles.** Figure 6 shows the timing of memory read or write cycles other than an opcode fetch ($\overline{M1}$) cycle. The $\overline{MREQ}$ and $\overline{RD}$ signals function exactly as in the fetch cycle. In a memory write cycle, $\overline{MREQ}$ also becomes active when the address bus is stable. The $\overline{WR}$ line is active when the data bus is stable, so that it can be used directly as an R/$\overline{W}$ pulse to most semiconductor memories.

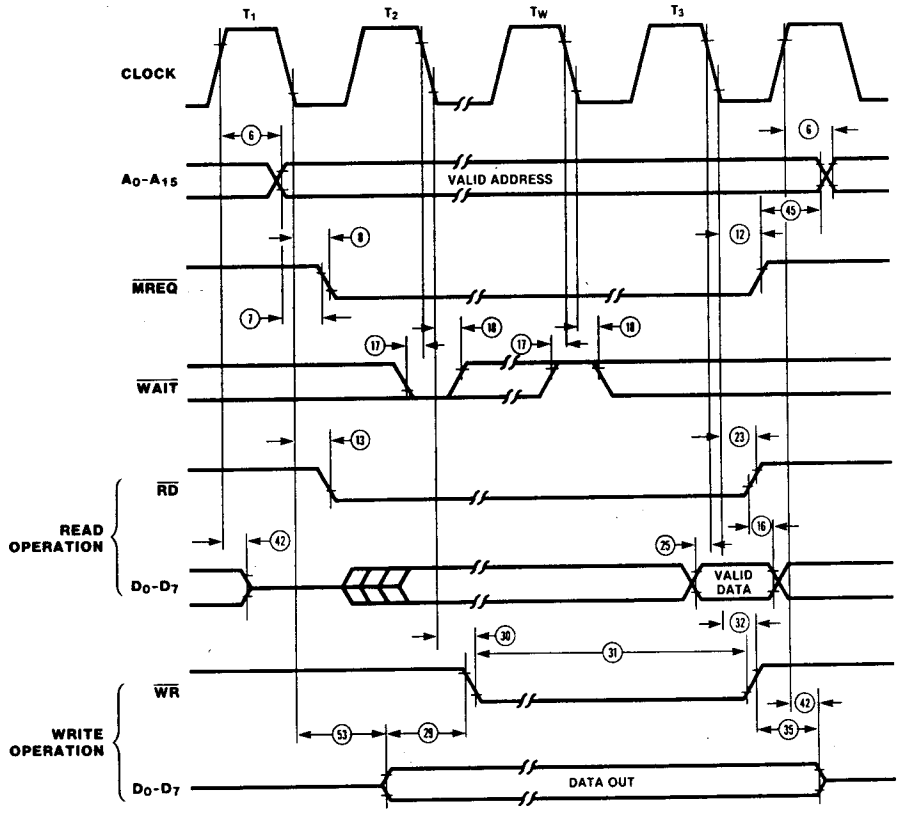
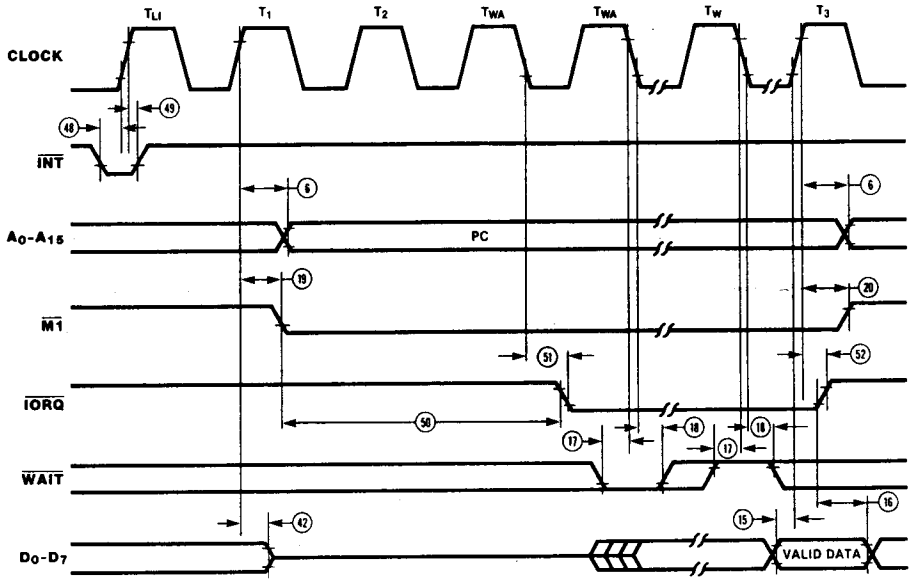
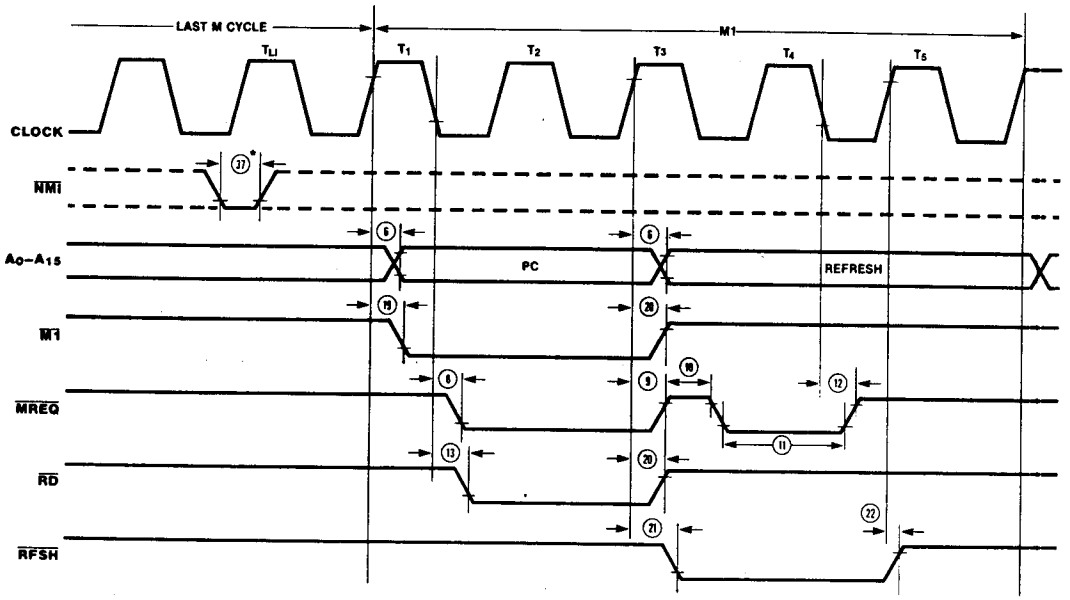



**Figure 6. Memory Read or Write Cycles**

**Interrupt Request/Acknowledge Cycle.** The CPU samples the interrupt signal with the rising edge of the last clock cycle at the end of any instruction (Figure 8). When an interrupt is accepted, a special $\overline{M1}$ cycle is generated. During this $\overline{M1}$ cycle, $\overline{IORQ}$ becomes active (instead of $\overline{MREQ}$) to indicate that the interrupting device can place an 8-bit vector on the data bus. The CPU automatically adds two Wait states to this cycle.



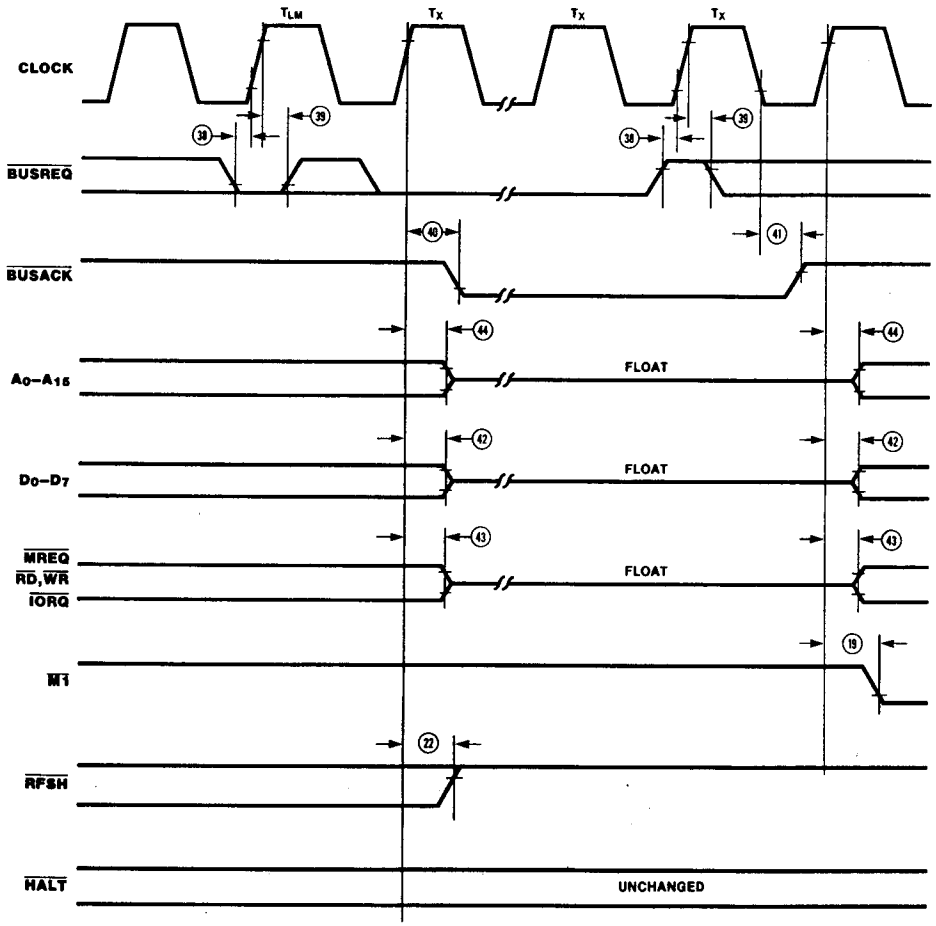
**Non-Maskable Interrupt Request Cycle.** $\overline{NMI}$ is sampled at the same time as the maskable interrupt input $\overline{INT}$ but has higher priority and cannot be disabled under software control. The subsequent timing is similar to that of a normal memory read operation except that data put on the bus by the memory is ignored. The CPU instead executes a restart (RST) operation and jumps to the $\overline{NMI}$ service routine located at address 0066H (Figure 9).




*Although $\overline{NMI}$ is an asynchronous input, to guarantee its being recognized on the following machine cycle, $\overline{NMI}$'s falling edge must occur no later than the rising edge of the clock cycle preceding the last state of any instruction cycle ($T_{LI}$).

**Figure 9. Non-Maskable Interrupt Request Operation**

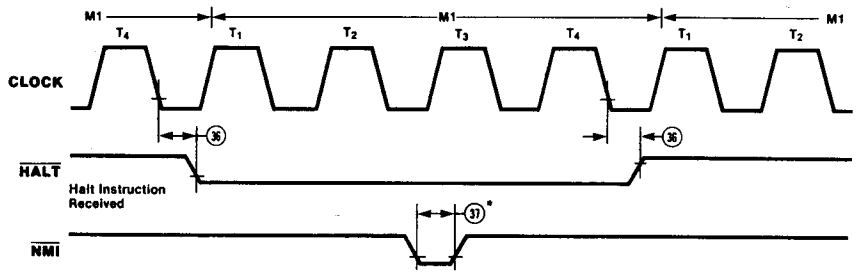
**Bus Request/Acknowledge Cycle.** The CPU samples $\overline{BUSREQ}$ with the rising edge of the last clock period of any machine cycle (Figure 10). If $\overline{BUSREQ}$ is active, the CPU sets its address, data, and $\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, and $\overline{WR}$ lines to a high-impedance state with the rising edge of the next clock pulse. At that time, any external device can take control of these lines, usually to transfer data between memory and I/O devices.




NOTES: 1) $T_{LM}$ = Last state of any M cycle.
2) $T_X$ = An arbitrary clock cycle used by requesting device.

**Figure 10. BUS Request/Acknowledge Cycle**

**Halt Acknowledge Cycle.** When the CPU receives a HALT instruction, it executes NOP states until either an $\overline{INT}$ or $\overline{NMI}$ input is received. When in the Halt state, the $\overline{HALT}$ output is active and remains so until an interrupt is received (Figure 11). $\overline{INT}$ will also force a Halt exit.




*Although $\overline{NMI}$ is an asynchronous input, to guarantee its being recognized on the following machine cycle, $\overline{NMI}$'s falling edge must occur no later than the rising edge of the clock cycle preceding the last state of any instruction cycle ($T_{Li}$).

**Figure 11. Halt Acknowledge**

**Reset Cycle.** $\overline{RESET}$ must be active for at least three clock cycles for the CPU to properly accept it. As long as $\overline{RESET}$ remains active, the address and data buses float, and the control outputs are inactive. Once $\overline{RESET}$ goes inactive, two internal T cycles are consumed before the CPU resumes normal processing operation. $\overline{RESET}$ clears the PC register, so the first opcode fetch will be to location 0000H (Figure 12).

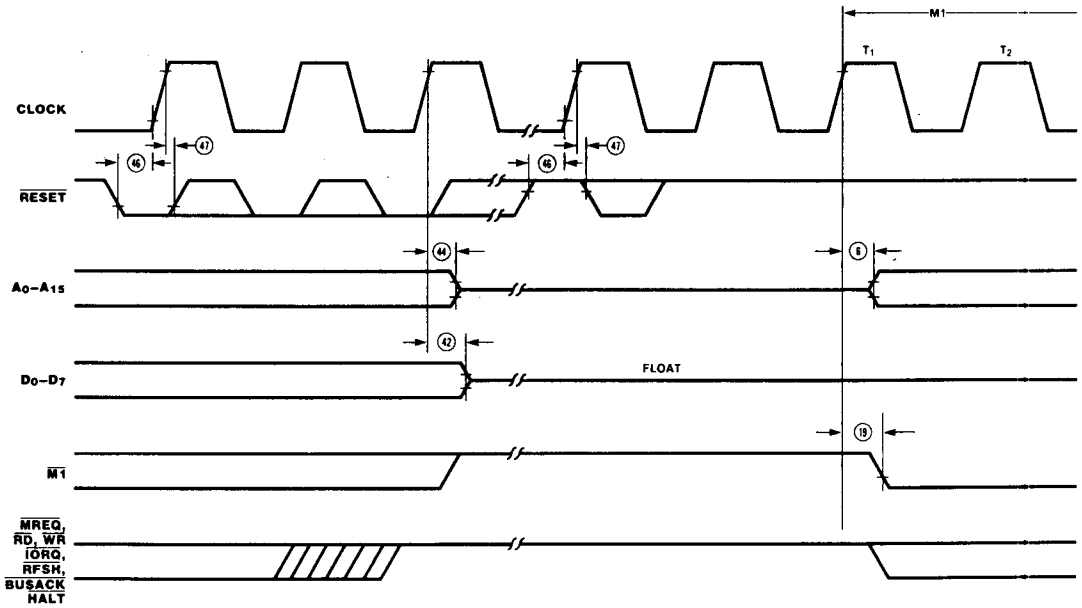



**Figure 12. Reset Cycle**

**Power-Down mode of operation (Only applies to CMOS Z80 CPU).**

**CMOS Z80 CPU supports Power-Down mode of operation. This mode is also referred to as the "standby mode", and supply current for the CPU goes down as low as 10 uA (Where specified as $Icc_2$).**

**Power-Down Acknowledge Cycle.** When the clock input to the CPU is stopped at either a High or Low level, the CPU stops its operation and maintains all registers and control signals. However, $I_{CC2}$ (standby supply current) is guaranteed only when the system clock is stopped at a Low level during $T_4$ of the machine cycle following the execution of the HALT instruction. The timing diagram for the power-down function, when implemented with the HALT instruction, is shown in Figure 13.

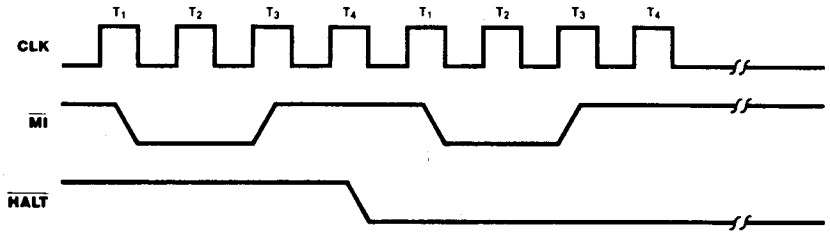



**Figure 13. Power-Down Acknowledge**

**Power-Down Release Cycle.** The system clock must be supplied to the CPU to release the power-down state. When the system clock is supplied to the CLK input, the CPU restarts operations from the point at which the power-down state was implemented.

The timing diagrams for the release from power-down mode are shown in Figure 14.

NOTES:

1) When the external oscillator has been stopped to enter the power-down state, some warm-up time may be required to obtain a stable clock for the release.
2) When the HALT instruction is executed to enter the power-down state, the CPU will also enter the Halt state. An interrupt signal (either $\overline{NMI}$ or $\overline{INT}$) or a $\overline{RESET}$ signal must be applied to the CPU after the system clock is supplied in order to release the power-down state.

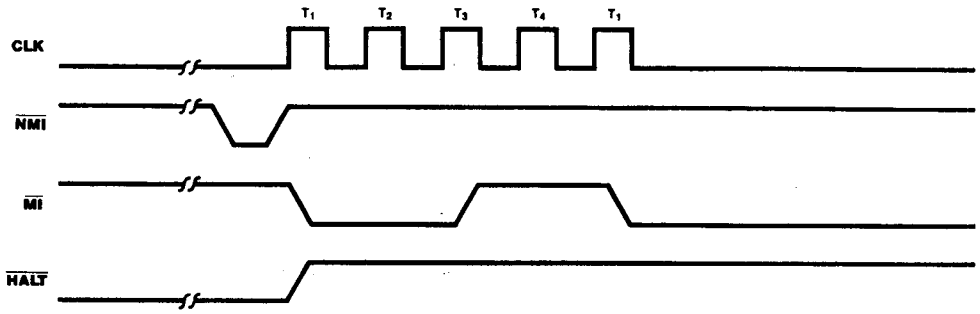



Figure 14a.

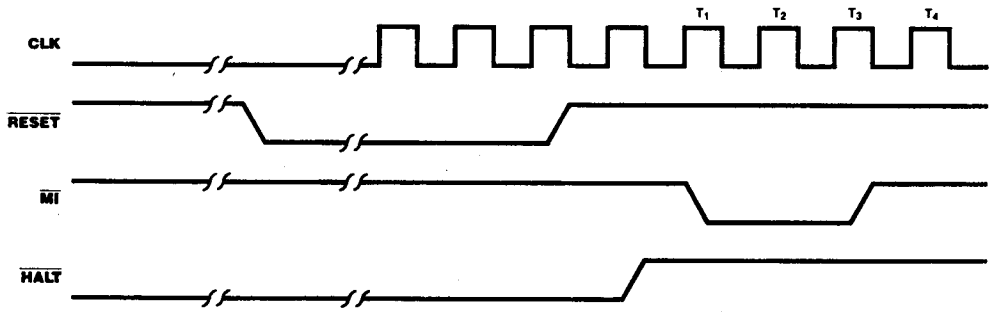



Figure 14b.

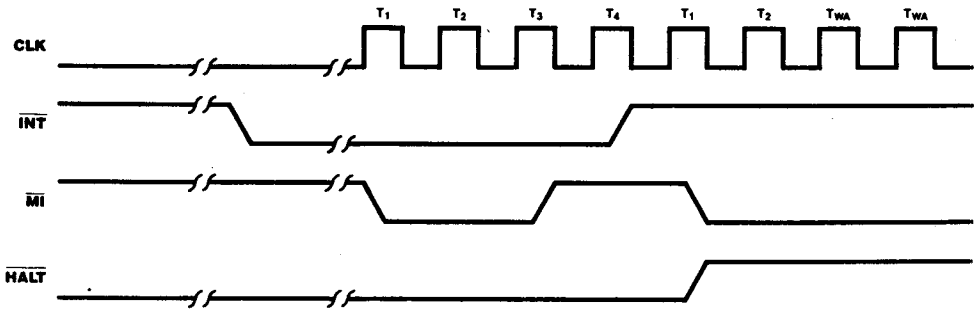



Figure 14c.

**Figure 13. Power-Down Release**

## ABSOLUTE MAXIMUM RATINGS

Voltage on $V_{CC}$ with respect to $V_{SS}$ . . . . . −0.3V to +7V
Voltages on all inputs with respect to $V_{SS}$ . . . . . −0.3V to $V_{CC}$ + 0.3V
Operating Ambient Temperature . . . . . See Ordering Information
Storage Temperature . . . . . −65°C to +150°C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## STANDARD TEST CONDITIONS

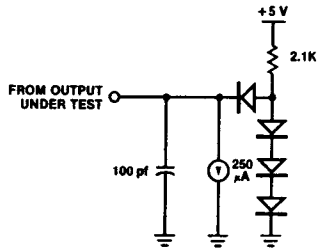
The DC Characteristics and capacitance sections below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND (0V). Positive current flows into the referenced pin.

Available operating temperature ranges are:

- **S = 0°C to +70°C**
  **Voltage Supply Range:**
  NMOS: +4.75V ≤ VCC ≤ +5.25V
  CMOS: +4.50V ≤ VCC ≤ +5.50V
- E= -40°C to 100°C, +4.50V ≤ VCC ≤ +5.50V

All ac parameters assume a load capacitance of 100 pf. Add 10 ns delay for each 50 pf increase in load up to a maximum of 200 pf for the data bus and 100 pf for address and control lines. AC timing measurements are referenced to 1.5 volts (except for clock, which is referenced to the 10% and 90% points).

The Ordering Information section lists temperature ranges and product numbers. Package drawings are in the Package Information section. Refer to the Literature List for additional documentation.



## DC CHARACTERISTICS (Z84C00/CMOS Z80 CPU)

| Symbol | Parameter | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $V_{ILC}$ | Clock Input Low Voltage | −0.3 | 0.45 | V | |
| $V_{IHC}$ | Clock Input High Voltage | $V_{CC}$ − .6 | $V_{CC}$ + .3 | V | |
| $V_{IL}$ | Input Low Voltage | −0.3 | 0.8 | V | |
| $V_{IH}$ | Input High Voltage | 2.2 | $V_{CC}$ | V | |
| $V_{OL}$ | Output Low Voltage | | 0.4 | V | $I_{OL}$ = 2.0 mA |
| $V_{OH_1}$ | Output High Voltage | 2.4 | | V | $I_{OH}$ = −1.6 mA |
| $V_{OH_2}$ | Output High Voltage | $V_{CC}$ − 0.8 | | V | $I_{OH}$ = −250 μA |
| $I_{CC_1}$ | Power Supply Current **4 MHz** | | **20** | **mA** | $V_{CC}$ = 5V |
| | **6 MHz** | | **30** | **mA** | $V_{IH}$ = $V_{CC}$ − 0.2V |
| | **8 MHz** | | **40** | **mA** | $V_{IL}$ = 0.2V |
| | **10 MHz** | | **50** | **mA** | |
| | 20 MHz | | 100 | mA | $V_{cc}$ = 5V |
| $I_{CC_2}$ | Standby Supply Current | | 10 | μA | $V_{CC}$ = 5V |
| | | | | | CLK = (0) |
| | | | | | $V_{IH}$ = $V_{CC}$ − 0.2V |
| | | | | | $V_{IL}$ = 0.2V |
| $I_{LI}$ | Input Leakage Current | −10 | 10 | μA | $V_{IN}$ = 0.4 to $V_{CC}$ |
| $I_{LO}$ | 3-State Output Leakage Current in Float | −10 | $10^2$ | μA | $V_{OUT}$ = 0.4 to $V_{CC}$ |

1. Measurements made with outputs floating.
2. $A_{15}$-$A_0$, $D_7$-$D_0$, $\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, and $\overline{WR}$.
3. $I_{CC_2}$ standby supply current is guaranteed only when the supplied clock is stopped at a low level during $T_4$ of the machine cycle immediately following the execution of a HALT instruction.

## CAPACITANCE

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $C_{CLOCK}$ | Clock Capacitance | | **10** | pf |
| $C_{IN}$ | Input Capacitance | | 5 | pf |
| $C_{OUT}$ | Output Capacitance | | 15 | pf |

$T_A$ = 25°C, f = 1 MHz.
Unmeasured pins returned to ground.

## AC CHARACTERISTICS† (Z84C00/CMOS Z80 CPU)

$V_{cc}$=5.0V ± 10%, unless otherwise specified

| No | Symbol | Parameter | Z84C0004** Min | Z84C0004** Max | Z84C0006 Min | Z84C0006 Max | Z84C0008 Min | Z84C0008 Max | Z84C0010 Min | Z84C0010 Max | Z84C0020[1] Min | Z84C0020[1] Max | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | TcC | Clock Cycle time | 250* | DC | 162* | DC | 125* | DC | 100* | DC | 50* | DC | nS | |
| 2 | TwCh | Clock Pulse width (high) | 110 | DC | 65 | DC | 55 | DC | 40 | DC | 20 | DC | nS | |
| 3 | TwCl | Clock Pulse width (low) | 110 | DC | 65 | DC | 55 | DC | 40 | DC | 20 | DC | nS | |
| 4 | TfC | Clock Fall time | | 30 | | 20 | | 10 | | 10 | | 10 | nS | |
| 5 | TrC | Clock Rise time | | 30 | | 20 | | 10 | | 10 | | 10 | nS | |
| 6 | TdCr(A) | Address vaild from Clock Rise | | 110 | | 90 | | 80 | | 65 | | 57 | nS | [2] |
| 7 | TdA(MREQf) | Address valid to /MREQ Fall | 65* | | 35* | | 20* | | 5* | | -15* | | nS | |
| 8 | TdCf(MREQf) | Clock Fall to /MREQ Fall delay | | 85 | | 70 | | 60 | | 55 | | 40 | nS | |
| 9 | TdCr(MREQr) | Clock Rise to /MREQ Rise delay | | 85 | | 70 | | 60 | | 55 | | 40 | nS | |
| 10 | TwMREQh | /MREQ pulse width (High) | 110* | | 65* | | 45** | | 30* | | 10* | | nS | [3] |
| 11 | TwMREQl | /MREQ pulse width (low) | 220* | | 132* | | 100* | | 75* | | 25* | | nS | [3] |
| 12 | TdCf(MERQr) | Clock Fall to /MREQ Rise delay | | 85 | | 70 | | 60 | | 55 | | 40 | nS | |
| 13 | TdCf(RDf) | Clock Fall to /RD Fall delay | | 95 | | 80 | | 70 | | 65 | | 40 | nS | |
| 14 | TdCr(RDr) | Clock Rise to /RD Rise delay | | 85 | | 70 | | 60 | | 55 | | 40 | nS | |
| 15 | TsD(Cr) | Data setup time to Clock Rise | 35 | | 30 | | 30 | | 25 | | 12 | | nS | |
| 16 | ThD(RDr) | Data hold time after /RD Rise | 0 | | 0 | | 0 | | 0 | | 0 | | nS | |
| 17 | TsWAIT(Cf) | /WAIT setup time to Clock Fall | 70 | | 60 | | 50 | | 20 | | 7.5 | | nS | |
| 18 | ThWAIT(Cf) | /WAIT hold time after Clock Fall | 10 | | 10 | | 10 | | 10 | | 10 | | nS | |
| 19 | TdCr(M1f) | Clock Rise to /M1 Fall delay | | 100 | | 80 | | 70 | | 65 | | 45 | nS | |
| 20 | TdCr(M1r) | Clock Rise to /M1 Rise delay | | 100 | | 80 | | 70 | | 65 | | 45 | nS | |
| 21 | TdCr(RFSHf) | Clock Rise to /RFSH Fall delay | | 130 | | 110 | | 95 | | 80 | | 60 | nS | |
| 22 | TdCr(RFSHr) | Clock Rise to /RFSH Rise delay | | 120 | | 100 | | 85 | | 80 | | 60 | nS | |
| 23 | TdCf(RDr) | Clock Fall to /RD Rise delay | | 85 | | 70 | | 60 | | 55 | | 40 | nS | |
| 24 | TdCr(RDf) | Clock Rise to /RD Fall delay | | 85 | | 70 | | 60 | | 55 | | 40 | nS | |
| 25 | TsD(Cf) | Data setup to Clock Fall during M2, M3, M4 or M5 cycles | 50 | | 40 | | 30 | | 25 | | 12 | | nS | |
| 26 | TdA(IORQf) | Address stable prior to /IORQ Fall | 180* | | 107* | | 75* | | 50* | | 0* | | nS | |
| 27 | TdCr(IORQf) | Clock Rise to /IORQ Fall delay | | 75 | | 65 | | 55 | | 50 | | 40 | nS | |
| 28 | TdCf(IORQr) | Clock Fall to /IORQ Rise delay | | 85 | | 70 | | 60 | | 55 | | 40 | nS | |
| 29 | TdD(WRf)Mw | Data stable prior to /WR Fall | 80* | | 22* | | 5* | | 40* | | -10* | | nS | |
| 30 | TdCf(WRf) | Clock Fall to /WR Fall delay | | 80 | | 70 | | 60 | | 55 | | 40 | nS | |
| 31 | TwWR | /WR pulse width | 220* | | 132* | | 100* | | 75* | | 25* | | nS | |
| 32 | TdCf(WRr) | Clock Fall to /WR Rise delay | | 80 | | 70 | | 60 | | 55 | | 40 | nS | |
| 33 | TdD(WRf)IO | Data stable prior to /WR Fall | -10* | | -55* | | -55* | | -10* | | -30* | | nS | |
| 34 | TdCr(WRf) | Clock Rise to /WR Fall delay | | 65 | | 60 | | 60 | | 50 | | 40 | nS | |
| 35 | TdWRr(D) | Data stable from /WR Rise | 60* | | 30* | | 15* | | 10* | | 0* | | nS | |
| 36 | TdCf(HALT) | Clock Fall to /HALT 'L' or 'H' | | 300 | | 260 | | 225 | | 90 | | 70 | nS | |
| 37 | TwNMI | /NMI pulse width | 80 | | 60 | | 60 | | 60 | | 60 | | nS | |
| 38 | TsBUSREQ (Cr) | /BUSREQ setup time to Clock Rise | 50 | | 50 | | 40 | | 30 | | 15 | | nS | |

*For clock periods other than the minimums shown, calculate parameters using the table on the following page. Calculated values above assumed TrC = TfC = 20 ns.

†Units in nanoseconds (ns).

†† **For loading ≥ 50 pf. Decrease width by 10 ns for each additional 50 pf.**

**4 MHz CMOS Z80 is obsoleted and replaced by 6 MHz

## AC CHARACTERISTICS† (Z84C00/CMOS Z80 CPU; Continued)

$V_{CC}$=5.0V ± 10%, unless otherwise specified

| No | Symbol | Parameter | Z84C0004** Min | Z84C0004** Max | Z84C0006 Min | Z84C0006 Max | Z84C0008 Min | Z84C0008 Max | Z84C0010 Min | Z84C0010 Max | Z84C0020[1] Min | Z84C0020[1] Max | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 39 | ThBUSREQ (Cr) | /BUSREQ hold time after Clock Rise | 10 | | 10 | | 10 | | 10 | | 10 | | nS | |
| 40 | TdCr (BUSACKf) | Clock Rise to /BASACK Fall delay | | 100 | | 90 | | 80 | | 75 | | 40 | nS | |
| 41 | TdCf (BUSACKr) | Clock Fall to /BASACK Rise delay | | 100 | | 90 | | 80 | | 75 | | 40 | nS | |
| 42 | TdCr(Dz) | Clock Rise to Data float delay | | 90 | | 80 | | 70 | | 65 | | 40 | nS | |
| 43 | TdCr(CTz) | Clock Rise to Control Outputs Float Delay (/MREQ, /IORQ, /RD and /WR) | | 80 | | 70 | | 60 | | 65 | | 40 | nS | |
| 44 | TdCr(Az) | Clock Rise to Address float delay | | 90 | | 80 | | 70 | | 75 | | 40 | nS | |
| 45 | TdCTr(A) | Address Hold time from /MREQ, /IORQ, /RD or /WR | 80* | | 35* | | 20* | | 20* | | 0* | | nS | |
| 46 | TsRESET(Cr) | /RESET to Clock Rise setup time | 60 | | 60 | | 45 | | 40 | | 15 | | nS | |
| 47 | ThRESET(Cr) | /RESET to Clock Rise Hold time | 10 | | 10 | | 10 | | 10 | | 10 | | nS | |
| 48 | TsINTf(Cr) | /INT Fall to Clock Rise Setup Time | 80 | | 70 | | 55 | | 50 | | 15 | | nS | |
| 49 | ThINTr(Cr) | /INT Rise to Clock Rise Hold Time | 10 | | 10 | | 10 | | 10 | | 10 | | nS | |
| 50 | TdM1f (IORQf) | /M1 Fall to /IORQ Fall delay | 565* | | 359* | | 270* | | 220* | | 100* | | nS | |
| 51 | TdCf(IORQf) | /Clock Fall to /IORQ Fall delay | | 85 | | 70 | | 60 | | 55 | | 45 | nS | |
| 52 | TdCf(IORQr) | Clock Rise to /IORQ Rise delay | | 85 | | 70 | | 60 | | 55 | | 45 | nS | |
| 53 | TdCf(D) | Clock Fall to Data Valid delay | | 150 | | 130 | | 115 | | 110 | | 75 | nS | |

**Notes:**

* For Clock periods other than the minimum shown, calculate parameters using the following table. Calculated values above assumed TrC = TfC = maximum.

** 4 MHz CMOS Z80 is obsoleted and replaced by 6 MHz

[1] Z84C0020 parameters are guuaranteed with 50pF load Capacitance.

[2] If Capacitive Load is other than 50pF, please use Figure 1. to calculate the value.

[3] Increasing delay by 10nS for each 50pF increase in loading, 200pF max for data lines, and 100pF for control lines.

## FOOTNOTES TO AC CHARACTERISTICS

| No | Symbol | Parameter | Z84C0004** | Z84C0006 | Z84C0008 | Z84C0010 | Z84C0020 |
|---|---|---|---|---|---|---|---|
| 1 | TcC | TwCh + TwCl + TrC + TfC | | | | | |
| 7 | TdA(MREQf) | TwCh + TfC | -65 | -50 | -45 | -45 | -45 |
| 10 | TwMREQh | TwCh + TfC | -20 | -20 | -20 | -20 | -20 |
| 11 | TwMREQl | TcC | -30 | -30 | -25 | -25 | -25 |
| 26 | TdA(IORQf) | TcC | -70 | -55 | -50 | -50 | -50 |
| 29 | TdD(WRf) | TcC | -170 | -140 | -120 | -60 | -60 |
| 31 | TwWR | TcC | -30 | -30 | -25 | -25 | -25 |
| 33 | TdD(WRf) | TwCl + TrC | -140 | -140 | -120 | -60 | -60 |
| 35 | TdWRr(D) | TwCl + TrC | -70 | -55 | -50 | -40 | -25 |
| 45 | TdCTr(A) | TwCl + TrC | -50 | -50 | -45 | -30 | -30 |
| 50 | TdM1f(IORQf) | 2TcC + TwCh + TfC | -65 | -50 | -45 | -30 | -30 |

AC Test Conditions: $V_{IH}$ = 2.0 V, $V_{IL}$ = 0.8 V; $V_{OH}$ = 1.5 V, $V_{OL}$ = 1.5 V; $V_{IHC}$ = $V_{CC}$ −0.6 V, $V_{ILC}$ = 0.45 V; FLOAT = ±0.5 V

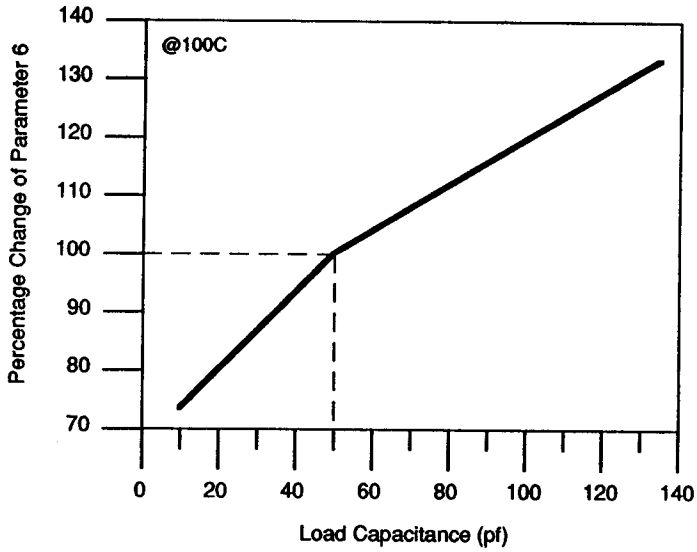



**Figure 1. Address Delay Characteristics**
(Parameter 6)

## DC CHARACTERISTICS (Z8400/NMOS Z80 CPU)

All parameters are tested unless otherwise noted.

| Symbol | Parameter | Min | Max | Unit | Test Condition |
|---|---|---|---|---|---|
| $V_{ILC}$ | Clock Input Low Voltage | −0.3 | 0.45 | V | |
| $V_{IHC}$ | Clock Input High Voltage | $V_{CC}$ −.6 | $V_{CC}$ +.3 | V | |
| $V_{IL}$ | Input Low Voltage | −0.3 | 0.8 | V | |
| $V_{IH}$ | Input High Voltage | 2.0[1] | $V_{CC}$ | V | |
| $V_{OL}$ | Output Low Voltage | | 0.4 | V | $I_{OL}$ = 2.0 mA |
| $V_{OH}$ | Output High Voltage | 2.4[1] | | V | $I_{OH}$ = −250 μA |
| $I_{CC}$ | Power Supply Current | | 200 | mA | Note 3 |
| $I_{LI}$ | Input Leakage Current | | 10 | μA | $V_{IN}$ = 0 to $V_{CC}$ |
| $I_{LO}$ | 3-State Output Leakage Current in Float | −10 | 10[2] | μA | $V_{OUT}$ = 0.4 to $V_{CC}$ |

1. For military grade parts, refer to the Z80 Military Electrical Specification.
2. $A_{15}$-$A_0$, $D_7$-$D_0$, $\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, and $\overline{WR}$.
3. Measurements made with outputs floating.

## CAPACITANCE

Guaranteed by design and characterization.

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $C_{CLOCK}$ | Clock Capacitance | | 35 | pf |
| $C_{IN}$ | Input Capacitance | | 5 | pf |
| $C_{OUT}$ | Output Capacitance | | 15 | pf |

NOTES:
$T_A$ = 25°C, f = 1 MHz.
Unmeasured pins returned to ground.

## AC CHARACTERISTICS† (Z8400/NMOS Z80 CPU; Continued)

| Number | Symbol | Parameter | Z0840004 Min | Z0840004 Max | Z0840006 Min | Z0840006 Max | Z0840008 Min | Z0840008 Max |
|---|---|---|---|---|---|---|---|---|
| 39 | ThBUSREQ(Cr) | $\overline{BUSREQ}$ Hold Time after Clock ↑ | 0 | | 0 | | 0 | |
| 40 | TdCr(BUSACKf) | Clock ↑ to $\overline{BUSACK}$ ↓ Delay | | 100 | | 90 | | 80 |
| 41 | TdCf(BUSACKr) | Clock ↓ to $\overline{BUSACK}$ ↑ Delay | | 100 | | 90 | | 80 |
| 42 | TdCr(Dz) | Clock ↑ to Data Float Delay | | 90 | | 80 | | 70 |
| 43 | TdCr(CTz) | Clock ↑ to Control Outputs Float Delay ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, and $\overline{WR}$) | | 80 | | 70 | | 60 |
| 44 | TdCr(Az) | Clock ↑ to Address Float Delay | | 90 | | 80 | | 70 |
| 45 | TdCTr(A) | $\overline{MREQ}$ ↑, $\overline{IORQ}$ ↑, $\overline{RD}$ ↑, and $\overline{WR}$ ↑ to Address Hold Time | 80* | | 35* | | 20* | |
| 46 | TsRESET(Cr) | $\overline{RESET}$ to Clock ↑ Setup Time | 60 | | 60 | | 45 | |
| 47 | ThRESET(Cr) | $\overline{RESET}$ to Clock ↑ Hold Time | | 0 | | 0 | | 0 |
| 48 | TsINTf(Cr) | $\overline{INT}$ to Clock ↑ Setup Time | 80 | | 70 | | 55 | |
| 49 | ThINTr(Cr) | $\overline{INT}$ to Clock ↑ Hold Time | | 0 | | 0 | | 0 |
| 50 | TdM1f(IORQf) | $\overline{M1}$ ↓ to $\overline{IORQ}$ ↓ Delay | 565* | | 365* | | 270* | |
| 51 | TdCf(IORQf) | Clock ↓ to $\overline{IORQ}$ ↓ Delay | | 85 | | 70 | | 60 |
| 52 | TdCf(IORQr) | Clock ↑ $\overline{IORQ}$ ↑ Delay | | 85 | | 70 | | 60 |
| 53 | TdCf(D) | Clock ↓ to Data Valid Delay | | 150 | | 130 | | 115 |

*For clock periods other than the minimums shown, calculate parameters using the following table. Calculated values above assumed TrC = TfC = 20 ns.
†Units in nanoseconds (ns).

## FOOTNOTES TO AC CHARACTERISTICS

| Number | Symbol | General Parameter | Z0840004 | Z0840006 | Z0840008 |
|---|---|---|---|---|---|
| 1 | TcC | TwCh + TwCl + TrC + TfC | | | |
| 7 | TdA(MREQf) | TwCh + TfC | −65 | −50 | −45 |
| 10 | TwMREQh | TwCh + TfC | −20 | −20 | −20 |
| 11 | TwMREQl | TcC | −30 | −30 | −25 |
| 26 | TdA(IORQf) | TcC | −70 | −55 | −50 |
| 29 | TdD(WRf) | TcC | −170 | −140 | −120 |
| 31 | TwWR | TcC | −30 | −30 | −25 |
| 33 | TdD(WRf) | TwCl + TrC | −140 | −140 | −120 |
| 35 | TdWRr(D) | TwCl + TrC | −70 | −55 | −50 |
| 45 | TdCTr(A) | TwCl + TrC | −50 | −50 | −45 |
| 50 | TdM1f(IORQf) | 2TcC + TwCh + TfC | −65 | −50 | −45 |

AC Test Conditions:
$V_{IH}$ = 2.0 V
$V_{IL}$ = 0.8 V
$V_{IHC} = V_{CC} - 0.6$ V
$V_{ILC}$ = 0.45 V
$V_{OH}$ = 1.5 V
$V_{OL}$ = 1.5 V
FLOAT = ±0.5 V

# Customer Support

For answers to technical questions about the product, documentation, or any other issues with Zilog's offerings, please visit Zilog's Knowledge Base at http://www.zilog.com/kb.

For any comments, detail technical questions, or reporting problems, please visit Zilog's Technical Support at http://support.zilog.com.