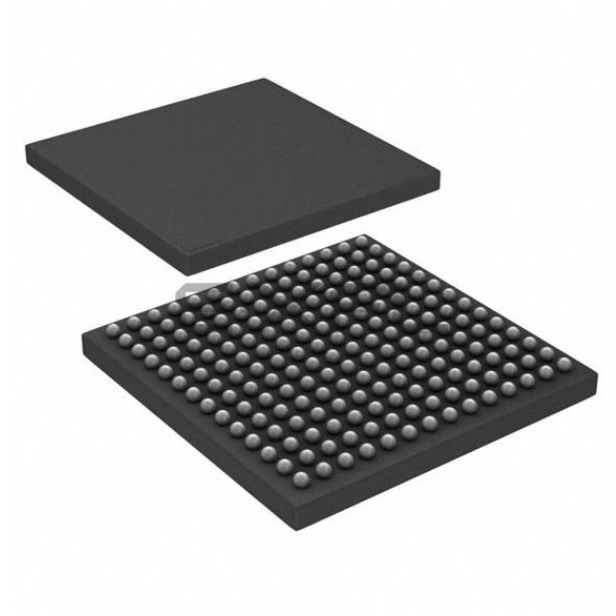

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Details	
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RAM Size	-
Interface	Ethernet, I²C, SPI
Number of I/O	48
Voltage - Supply	0.9V ~ 3.6V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	196-BGA
Supplier Device Package	196-BGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/mc-10105f1-821-fna-m1-a

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1. Pin Functions

1.1. List of Pin Functions

1.1.1. Host Interface –Parallel Interface

Table 1-1: Parallel host interface

Pin Name	I/O	Function	Remarks	Alternate Function
LBU_WR_EN_IN	I	Write Control	Active low (Intel mode) 0:write; 1:read (Motorola mode)	GPIO_0
LBU_READ_EN_IN	I	Read Control	Active low (Intel mode) No function (Motorola mode)	GPIO_1
LBU_CS_IN	I	Chip Select		GPIO_2
LBU_BE_1_IN	I	Byte Select 1		GPIO_3
LBU_BE_2_IN	I	Byte Select 2		GPIO_4
LBU_READY_OUT	O	Ready Signal	Polarity configurable	GPIO_5
LBU_DATA(15:0)	I/O	data line 0 – 15		GPIO_(21:6)
LBU_A(13:0)_IN	I	Address lines 0 - 13		GPIO_(35:22)
LBU_SEG0_IN	I	Low Bit of the segment select	Page selection	GPIO_36
LBU_SEG1_IN	I	High Bit of the segment select	Page selection	GPIO_37

1.1.2. Host Interface –SPI slave Interface

Table 1-2: SPI host interface

Pin Name	I/O	Function	Remarks	Alternate Function
HOST_RESET_IN	I	Serial Reset	The SPI Slave interface can be reset by using this signal. (signal is active high)	GPIO_38
HOST_SFRN_IN	I	Serial Frame	The start of a new SPI transfer is signaled.	GPIO_39
HOST_SRXD_IN	I	Serial Data Input	MOSI (Master out Slave in)	GPIO_40
HOST_SCLK_IN	I	Serial Clock Input	Serial Clock driven by the SPI Master	GPIO_41
HOST_STXD_OUT	O	Serial Data Output	MISO (Master in Slave out)	GPIO_42
HOST_SHDR_OUT	O	Serial Header Information	header information available	GPIO_43

Table 1-12: Interrupt signals

Pin Name	I/O	Function	Remark
INT_OUT	O	Interrupt output (to the Host)	Interrupt to host can be generated by a configurable set of internal TPS-1 events (active high).

Table 1-13: Watchdog signals

Pin Name	I/O	Function	Remark
WD_IN	I	Watchdog Input (from the Host)	This signal triggers the TPS-1 watchdog that monitors the Host CPU. A rising edge of this signal restarts the watchdog counter (active high).
WD_OUT	O	Watchdog Output (to the Host)	This signal is set when a watchdog trigger of the TPS-1 occurs (active low).

Table 1-14: JTAG interface pin definition

Pin Name	I/O	Function	Remark
TRSTN	I	Test Reset	JTAG Reset. Input: Reset signal of the target port. External pull-down (4.7KΩ to GND)
TMS	I	Test Mode Select	JTAG interface is activated from the debug unit. pull-up (4.7KΩ to V_{DD})
TDO	O	Test Data Output	can be left open
TCK	I	Test Clock	JTAG clock signal to the TPS-1. It is recommended that this pin is set to a defined state on the target board. External pull-up (4.7KΩ to V_{DD})
TDI	I	Test Data Input	External pull-up(4.7KΩ to V_{DD})

Table 1-15: Supply Voltage Circuitry

Pin Name	Function	Supply Voltage Generation
P(2:1)VDDARXTX	Analog port RX/TX power supply, 1.5 V (PHY port 2:1)	Must be generated from VDD15 via a filter.
VDDAPLL	Analog central power supply, 1.5 V (PHY)	
VDDACB	Analog central power supply, 3.3 V (PHY)	Must be generated from VDD33 via a filter.
VDD33ESD	Analog test power supply, 3.3 V (PHY)	
VSSAPLLCB	Analog central GND (PHY)	Must be generated from GND Core/IO via a filter or connected to GND Core/IO at the far end from TPS-1.
VDDQ_PECL_B(2:1)	PECL buffer power supply 3.3 V (port 1 and port 2)	
PLL_AGND	Analog Ground for the internal CPU clock generation	
PLL_AVDD	Power supply for the internal CPU clock generation (1.0V)	
GND	Digital GND	
AGND	Analog Ground for PHYs	
VDD33	Voltage Supply 3.3 V (external)	
VDD15	Voltage Supply 1.5 V from Switching Regulator or external	
VDD10	Voltage Supply 1.0 V (external)	
AGND_REG	Analog Ground for switching regulator.	

1.2. Pin Characteristics

Table 1-16: Signal characteristics

Pin Name	I/O	Input type	Output type	Pull up / down *internal*	Pull up / down *external*	Capacity load (pF)	Drive capability I_{OH}	Drive capability I_{OL}
SPI-Master for Flash ROM								
CS_FLASH_OUT	O	-	3.3V CMOS	-		30	6 mA	6 mA
SPI3_SCLK_OUT	O	-	3.3V CMOS	-		30	6 mA	6 mA
SPI3_SRXD_IN	I	Schmitt	3.3V CMOS	-		-	-	-
SPI3_STXD_OUT	O	-	3.3V CMOS	-		30	6 mA	6 mA
Synchronization signals								
TEST_SYNC	O	-	3.3V CMOS	-		30	6 mA	6 mA
T1	O	-	3.3V CMOS	-		30	6 mA	6 mA
T2	O	-	3.3V CMOS	-		30	6 mA	6 mA
T3	O	-	3.3V CMOS	-		30	6 mA	6 mA
T4	O	-	3.3V CMOS	-		30	6 mA	6 mA
T5	O	-	3.3V CMOS	-		30	6 mA	6 mA
T6	O	-	3.3V CMOS	-		30	6 mA	6 mA
LED signals for PROFINET IO status								
LED_BF_OUT	O	-	3.3V CMOS	-		30	6 mA	6 mA
LED_SF_OUT	O	-	3.3V CMOS	-		30	6 mA	6 mA
LED_READY_OUT	O	-	3.3V CMOS	-		30	6 mA	6 mA
LED_MT_OUT	O	-	3.3V CMOS			30	6 mA	6 mA
PHY Port 1								
I2C_1_D_INOUT	I/O	Schmitt	3.3V CMOS	-		30	6 mA	6 mA
SCLK_1_INOUT	I/O	Schmitt	3.3V CMOS	-		30	6 mA	6 mA
LINK_PHY1	O	-	3.3V CMOS	-		30	6 mA	6 mA
ACT_PHY1	O	-	3.3V CMOS	-		30	6 mA	6 mA
P1_TX_P	O	-	Analog	-		-	-	-
P1_TX_N	O	-	Analog	-		-	-	-
P1_RX_P	I	-	Analog	-		-	-	-
P1_RX_N	I	-	Analog	-		-	-	-
P1_SD_P	I	PECL	-	-		-	-	-
P1_SD_N	I	PECL	-	-		-	-	-
P1_RD_P	I	PECL	-	-		-	-	-
P1_RD_N	I	PECL	-	-		-	-	-
P1_TD_OUT_P	O	-	3.3V CMOS	-		-	12 mA	12 mA
P1_TD_OUT_N	O	-	3.3V CMOS	-		-	12 mA	12 mA
P1_FX_EN_OUT	O	-	3.3V CMOS	-		30	12 mA	12 mA
PHY Port 2								
I2C_2_D_INOUT	I/O	Schmitt	3.3V CMOS	-		30	6 mA	6 mA
SCLK_2_INOUT	I/O	Schmitt	3.3V CMOS	-		30	6 mA	6 mA
LINK_PHY2	O	-	3.3V CMOS	-		30	6 mA	6 mA
ACT_PHY2	O	-	3.3V CMOS	-		30	6 mA	6 mA
P2_TX_P	O	-	Analog	-		-	-	-
P2_TX_N	O	-	Analog	-		-	-	-
P2_RX_P	I	-	Analog	-		-	-	-
P2_RX_N	I	-	Analog	-		-	-	-
P2_SD_P	I	PECL	-	-		-	-	-
P2_SD_N	I	PECL	-	-		-	-	-
P2_RD_P	I	PECL	-	-		-	-	-
P2_RD_N	I	PECL	-	-		-	-	-
P2_TD_OUT_P	O	-	3.3V CMOS	-		-	12 mA	12 mA

Pin Name	I/O	Input type	Output type	Pull up / down *internal*	Pull up / down *external*	Capacity load (pF)	Drive capability I_{OH}	Drive capability I_{OL}
P2_TD_OUT_N	O	-	3.3V CMOS	-		-	12 mA	12 mA
P2_FX_EN_OUT	O	-	3.3V CMOS	-		30	12 mA	12 mA
Oscillator								
XCLK1	I	Osc. in	-	-		-	-	-
XCLK2	O	Osc. Out	-	-		25	6 mA	6 mA
JTAG – Interface								
TM0	I	Schmitt		Pull-up 50 kΩ	Pull-down 1 kΩ	-	-	-
TM1	I	Schmitt	-		Pull-down 1 kΩ	-	-	-
TRSTN	I	Schmitt	3.3V CMOS	-	Pull-down 4.7 kΩ	-	-	-
TMS	I	Schmitt	3.3V CMOS	-	Pull-up 4.7 kΩ	-	-	-
TDO	O	-	3.3V CMOS	-	-	30	6 mA	6 mA
TCK	I	Schmitt	3.3V CMOS	-	Pull-up 4.7 kΩ	-	-	-
TDI	I	Schmitt	3.3V CMOS		Pull-up 4.7 kΩ	-	-	-
Reset / Test								
RESETN	I	Schmitt	3.3V CMOS	-		-	-	-
ATP	IO		-	-		-	-	-
EXTRES	IO	Analog	-	-		-	-	-
TMC1	I		3.3V CMOS	pull-down (50 kΩ)		-	-	-
TMC2	I		3.3V CMOS	pull-down (l 50 kΩ)		-	-	-
TEST_1_IN	I	Schmitt	3.3V CMOS	pull-down (50 kΩ)		-	-	-
TEST_2_IN	I	Schmitt	3.3V CMOS	pull-down (50 kΩ)		-	-	-
TESTDOUT5	O		3.3V CMOS	-		-	12 mA	12 mA
TESTDOUT6	O		3.3V CMOS	-		-	12 mA	12 mA
TESTDOUT7	O		3.3V CMOS	-		-	12 mA	12 mA
Host interface								
WD_IN	I	Schmitt	3.3V CMOS	-		-	-	-
WD_OUT	O	-	3.3V CMOS	-		30	6 mA	6 mA
INT_OUT	O	-	3.3V CMOS	-		30	6 mA	6 mA
Boot interface (serial)								
UART6_TX	O	-	3.3V CMOS	-		30	6 mA	6 mA
UART6_RX	I	Schmitt	3.3V CMOS	-		-	6 mA	6 mA
BOOT_1	I	Schmitt	-	pull-down (50 kΩ)		-	-	-
Test signals – switching regulator								
TEST1	I	-	-	-	see note 1	-	-	-
TEST2	I	-	-	-	see note 1	-	-	-
TEST3	I	-	-	-	see note 1	-	-	-
Power Supplies								
GND	-	-	-	-		-	-	-
VDD33	-	-	-	-		-	-	-

Pin Name	I/O	Input type	Output type	Pull up / down *internal*	Pull up / down *external*	Capacity load (pF)	Drive capability I_{OH}	Drive capability I_{OL}
GPIO_30	I/O	Schmitt	3.3V CMOS	-	see note 2	30	6 mA	6 mA
GPIO_31	I/O	Schmitt	3.3V CMOS	-	see note 2	30	6 mA	6 mA
GPIO_32	I/O	Schmitt	3.3V CMOS	-	see note 2	30	6 mA	6 mA
GPIO_33	I/O	Schmitt	3.3V CMOS	-	see note 2	30	6 mA	6 mA
GPIO_34	I/O	Schmitt	3.3V CMOS	-	see note 2	30	6 mA	6 mA
GPIO_35	I/O	Schmitt	3.3V CMOS	-	see note 2	30	6 mA	6 mA
GPIO_36	I/O	Schmitt	3.3V CMOS	-	see note 2	30	6 mA	6 mA
GPIO_37	I/O	Schmitt	3.3V CMOS	-	see note 2	30	6 mA	6 mA
GPIO_38	I/O	Schmitt	3.3V CMOS	-	see note 2	30	6 mA	6 mA
GPIO_39	I/O	Schmitt	3.3V CMOS	-	see note 2	30	6 mA	6 mA
GPIO_40	I/O	Schmitt	3.3V CMOS	-	see note 2	30	6 mA	6 mA
GPIO_41	I/O	Schmitt	3.3V CMOS	-	see note 2	30	6 mA	6 mA
GPIO_42	I/O	Schmitt	3.3V CMOS	-	see note 2	30	6 mA	6 mA
GPIO_43	I/O	Schmitt	3.3V CMOS	-	see note 2	30	6 mA	6 mA
GPIO_44	I/O	Schmitt	3.3V CMOS	-	see note 2	30	6 mA	6 mA
GPIO_45	I/O	Schmitt	3.3V CMOS	-	see note 2	30	6 mA	6 mA
GPIO_46	I/O	Schmitt	3.3V CMOS	-	see note 2	30	6 mA	6 mA
GPIO_47	I/O	Schmitt	3.3V CMOS	-	see note 2	30	6 mA	6 mA

Note 1: These pins (TEST(3:1)) must not be left open. For the required connection please consult the TPS-1 User Manual.

Note 2: The GPIO pins GPIO_00 to GPIO_47 can be configured as diagnosis input lines (local IO mode). The GPIO pins are configured into groups of 8 bit. Unused diagnosis inputs must have a pull-down or pull-up resistor (depending on customer's design). A missing termination can cause undefined diagnosis.

Note 3: Generally unused GPIO pins should be pulled up (10 kΩ to VDD33). From PROFINET stack version V1.4 onwards all unused GPIOs should be left open, because the stack will configure them to outputs. This does not apply to pins handled in note 2.

Abbreviations:

I	Input
O	Output
I/O	Input/Output

2. Electrical Specifications

2.1. Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter		Symbol	Rating	Unit
Power supply for core		VDD10	-0.5 to +1.4	V
Power supply for IO		VDD33	-0.5 to +4.6	V
Power supply for PHYs		VDD15	-0.5 to +2.0	V
Analog power supply for PLL		PLL_AVDD	-0.5 to +1.4	V
Analog central 3.3V supply for PHYs		VDDACB	-0.5 to +4.6	V
Analog central 1.5V supply for PHYs		VDDAPLL	-0.5 to +2.0	V
Analog Rx/Tx port power supply		P(2:1)VDDARXTX	-0.5 to +2.0	V
PECL buffer power supply PHY 1		VDDQ_PECL_B1	-0.5 to +4.6	V
PECL buffer power supply PHY 2		VDDQ_PECL_B2	-0.5 to +4.6	V
Analog test supply		VDD33ESD	-0.5 to +4.6	V
Input voltage	3.3V CMOS V_I < VDD + 0.5V	V_I	-0.5 to +4.6	V
Operating temperature		T_J	-40 to + 125	^{0}C
Storage temperature		T_{STG}	-65 to + 150	^{0}C

Caution: Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

2.3. Thermal Characteristics

Table 2-5: Thermal Characteristics of the Package

Parameter	Symbol	Airflow (m/s)				Unit
		0	0.2	1	2	
Thermal resistance junction to ambient Note1	Θ_{ja}	21.99	20.91	18.86	17.80	K/W
Thermal resistance junction to top center of the package surface Note1	Ψ_{jt}	0.12	0.17	0.31	0.37	K/W
Thermal resistance junction to case Note2	Θ_{jc}	7.38				K/W

Note 1. The parameters are valid, if no heat sink is used and PCB with 4 layers and massive ground and power planes.

2. The parameter is valid, if a heat sink is used.

2.4. AC Characteristics

2.4.1. Clock Timing

Table 2-6: Clock AC Characteristics (using a crystal)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Oscillator clock frequency (XCLK1, Pin N11) XCLK2, Pin P11) Note 1	f_C	-	25	-	MHz
Frequency tolerance	f_{tol}	-50 ppm	-	+ 50 ppm	
EXTAL clock cycle time	T_{EXcyc}	-	40	-	ns
EXTAL clock rising time Note 2	t_{EXr}	0	-	4	ns
EXTAL clock falling time Note 2	t_{EXf}	0	-	4	ns
Input capacity (incl. package), XCLK1, N11	C_{IN}	-	4.2	-	pF
Output capacity (incl. package), XCLK2, P11	C_{OUT}	3	4	5	pF
High level input voltage	V_{IH}	2.0	-		V
Low level input voltage	V_{IL}	-	-	0.8	V
JTAG clock frequency	-	-	-	20	MHz

Notes: 1. See TPS-1 User's Manual: Hardware () for recommended XTAL
2. Input voltage rising from 10% to 90% or falling from 90% to 10% of its nominal value.

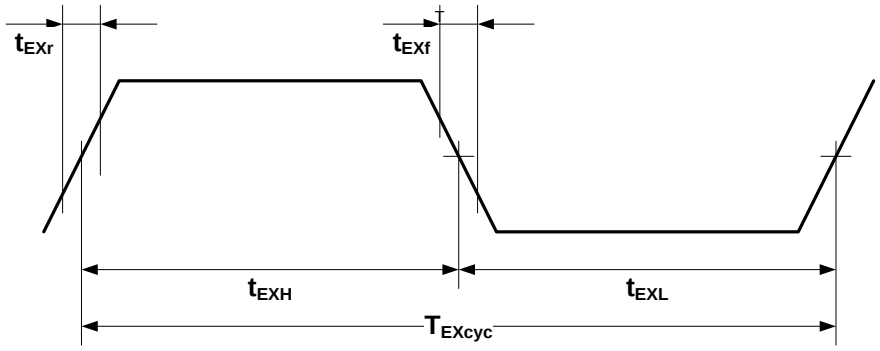


Figure 2-1: Clock Waveforms

Table 2-7: Clock AC Characteristics (using an external oscillator)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
External clock source frequency	f_{IN}	-	25	-	MHz
Frequency tolerance Note 1	f_{tol}	-50 ppm	-	+ 50 ppm	
XCLK1 high level voltage	V_{IH}	2	3.3	VDDACB	V
XCLK1 low level voltage	V_{IL}	0	-	0.8	V
XCLK1 rise or fall time	t_{RFC}	0	1	4	ns
XCLK1 high or low time Note 2	t_W	16	20	24	pF
XCLK1 jitter tolerance	t_{JIT}	-	20	-	ps (RMS)
XCLK1 duty cycle	DuCy	40	50	60	%

Notes: 1. The specified frequency tolerance must be maintained over all lifetime and temperature.
2. t_W was calculated at $f_{IN(TYP)}$=25 MHz, e.g. $t_{W(MIN)} = 10 * (DuCy_{(MIN)} / f_{IN(TYP)})$

2.4.2.1. JTAG interface timing

Table 2-8: Timing JTAG interface

Signal	Input		Output		Unit	Clock	Notes
	Setup time (T_{IS} min.)	Hold time (T_{IH} min.)	Valid delay (T_{OV} max.)	Hold time (T_{OH} min.)			
TRSTN	8	0			ns	TCK	
TMS	8	0			ns	TCK	
TDI	8	0			ns	TCK	
TCK	-	-	-	-	-	-	Note 2
TDO			10	2	ns	TCK	Note 1

Note 1: Minimum hold time is measured with 10 pF load and maximum valid Delay is measured with 30 pF load.
2: For TCK a maximum speed of 20 MHz is allowed.

2.4.2.2.2. Host write to TPS-1 with separate read/write line

(LBU_READY_OUT active low)

T_A = - 40 to +85^{O}C; V_{DD15} = 1.35 V ~ 1.65 V; V_{DD33} = 3.0 V ~ 3.6 V

Table 2-10: Host write with separate read/write line

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Chip select asserted to write pulse asserted delay	t_{CSWS}	-	0	-	ns
Address valid to write pulse asserted setup time	t_{AWS}	-	0	-	ns
Write pulse asserted to ready enabled delay	t_{WRE}	-	5	12	ns
Write pulse asserted to data valid delay	t_{WDV}	-	-	40	ns
Write pulse deasserted to chip select deasserted delay	t_{WCSH}	-	0	-	ns
Address hold time after write strobe deasserted	t_{WAH}	-	0	-	ns
Ready asserted to write pulse deasserted delay	t_{RTW}	-	0	-	ns
Data hold time after write pulse deasserted	t_{WDH}	-	0	-	ns
Write recovery time	t_{WR}	-	25	-	ns

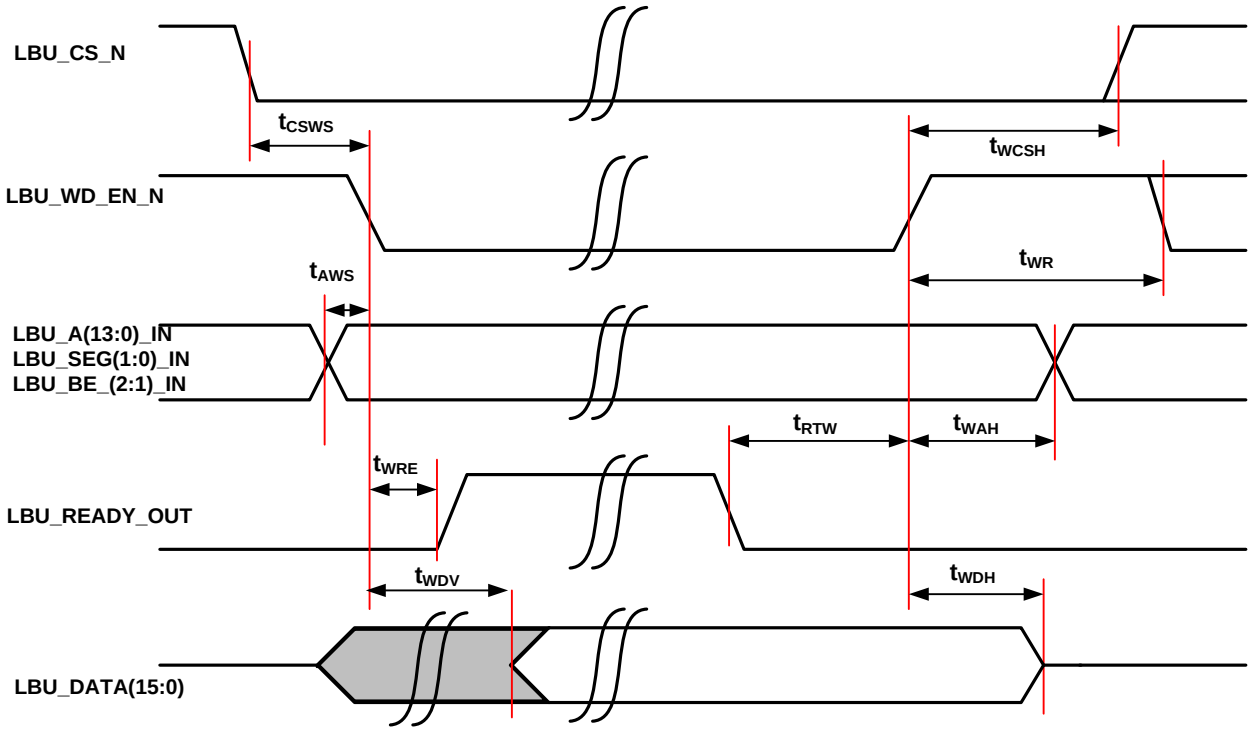


Figure 2-5: Host write with separate read/write line

2.4.2.2.4. Host write to TPS-1 with common read/write line

(LBU_READY_OUT active low)

T_A = - 40 to +85^{O}C; V_{DD15} = 1.35 V ~ 1.65 V; V_{DD33} = 3.0 V ~ 3.6 V

Table 2-12: Host write with common read/write line

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Write signal deasserted to chip select asserted setup time	t_{WCS}	-	2	-	ns
Address valid to chip select asserted setup time	t_{ACS}	-	0	-	ns
Chip select asserted to ready enabled delay	t_{CRE}	-	5	12	ns
Chip select asserted to data valid delay	t_{CDV}	-	-	40	ns
Write signal deasserted to chip select deasserted hold time	t_{CWH}	-	0	-	ns
Address hold time after chip select deasserted	t_{CAH}	-	0	-	ns
Ready asserted to chip select deasserted delay	t_{RTC}	-	0	-	ns
Chip select deasserted to data invalid hold time	t_{CDH}	-	0	-	ns
Read recovery time	t_{WR}	-	25	-	ns

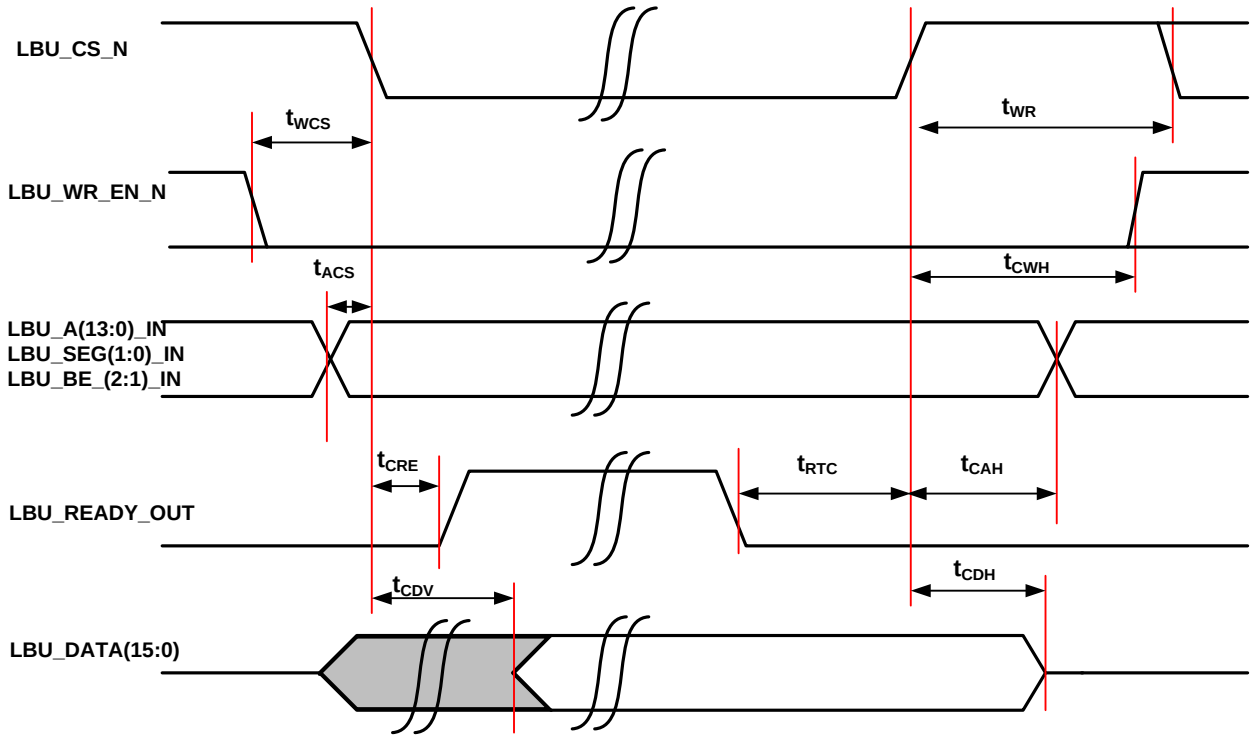


Figure 2-7: Host write with common read/write line

2.4.2.3 SPI Slave Timing

T_A = - 40 to +85^{O}C; V_{DD15} = 1.35 V ~ 1.65 V; V_{DD33} = 3.0 V ~ 3.6 V

Table 2-13: SPI Slave Timing

Parameter	Symbol	Condition	Min.	Max.	Unit
SPI clock	t_{cl}	-	40	-	ns
Setup time	t_{su}	-	13	-	ns
Hold time	t_h	-	13	-	ns

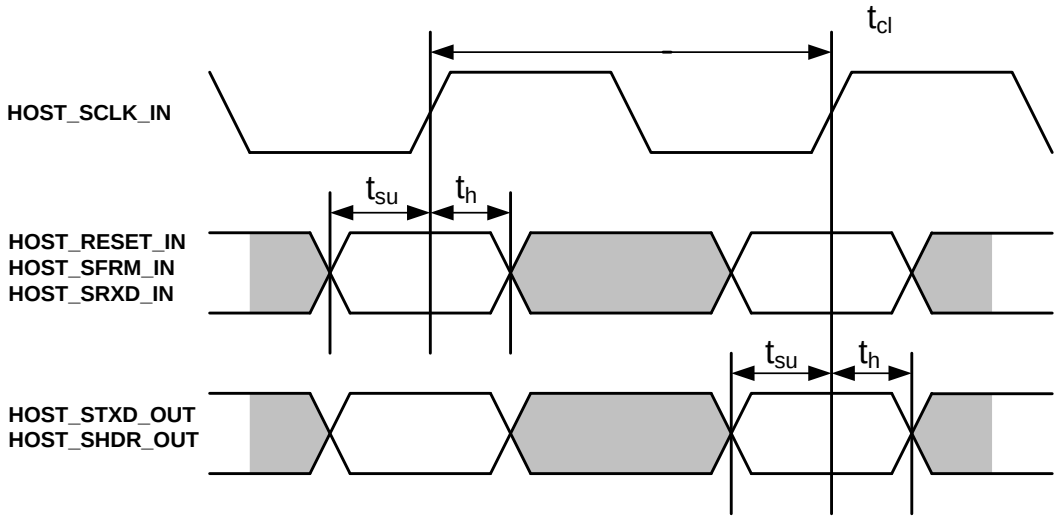


Figure 2-8: SPI Slave Timing

2.4.3.1. PHY DC Specifications(100 BASE-TX)

T_A = -40 to +85 ^{O}C, AVDD33 = 3.0 to 3.6V, AVDD15 = 1.35 to 1.65V, DVDD = 1.35 to 1.65V

Table 2-15: PHY DC Specification

Parameter	Symbol	Min.	Typ.	Max.	Unit
TX Output, High Level Differential Signal, TXP/TXN	V_{OUTH}	0.95		1.05	V
TX Output, Low Level Differential Signal, TXP/TXN	V_{OUTL}	-0.95		-1.05	V
TX Output, Mid. Level Differential Signal, TXP/TXN	V_{OUTM}	-0.05		+0.05	V
TX Output, Overshoot Differential Signal, TXP/TXN	V_{0VS}	0		5	%

These specifications are complying with ANSI/IEEE 802.3 Std.

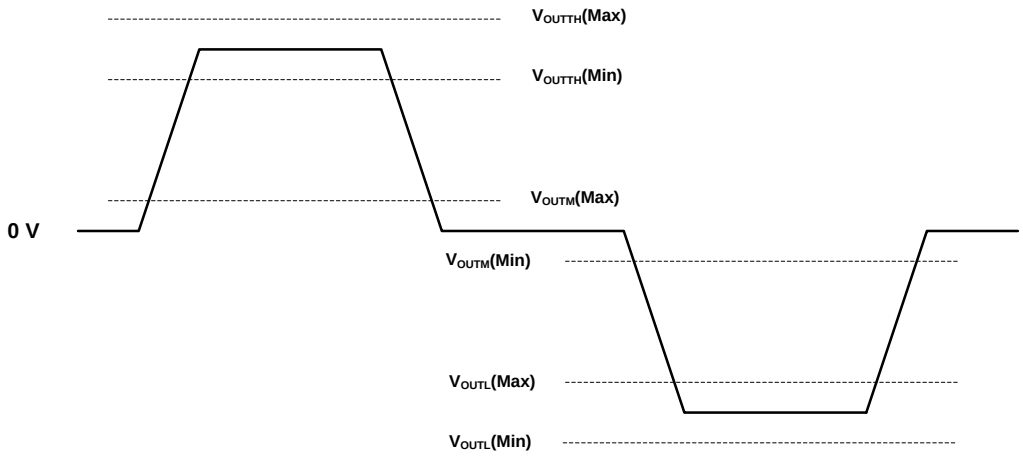


Figure 2-10: PHY DC Specification

2.4.3.2. PHY AC Specifications (100BASE-TX)

T_A = -40 to +85 ^{O}C, AVDD33 = 3.0 to 3.6V, AVDD15 = 1.35 to 1.65V, DVDD = 1.35 to 1.65V

Table 2-16: PHY AC Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
Rise time and fall time, TXP/TXN	t_r, t_f	3		5	ns
Duty cycle distortion, TXP/TXN				0.5	ns
Transmit Jitter, TXP/TXN				1.4	ns

These specifications are complying with ANSI/IEEE 802.3 Std.

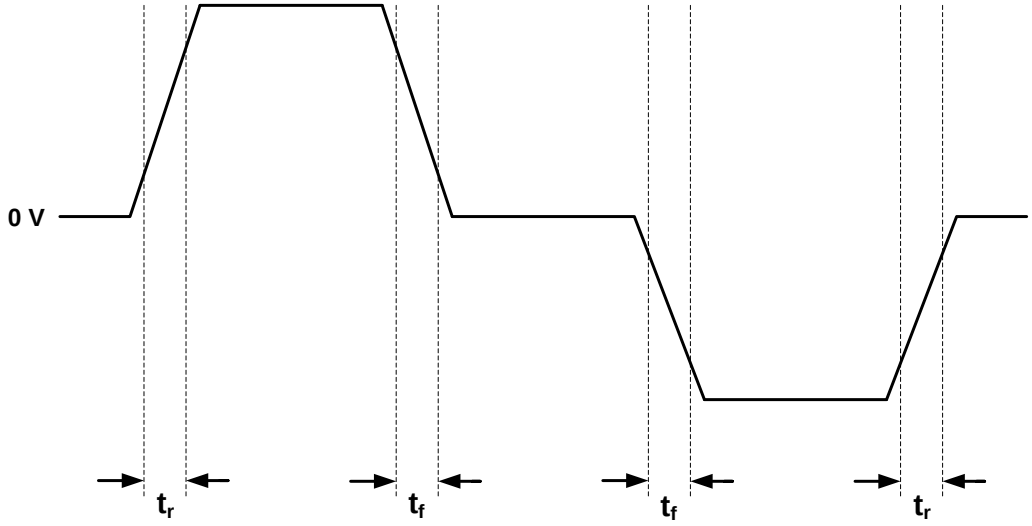
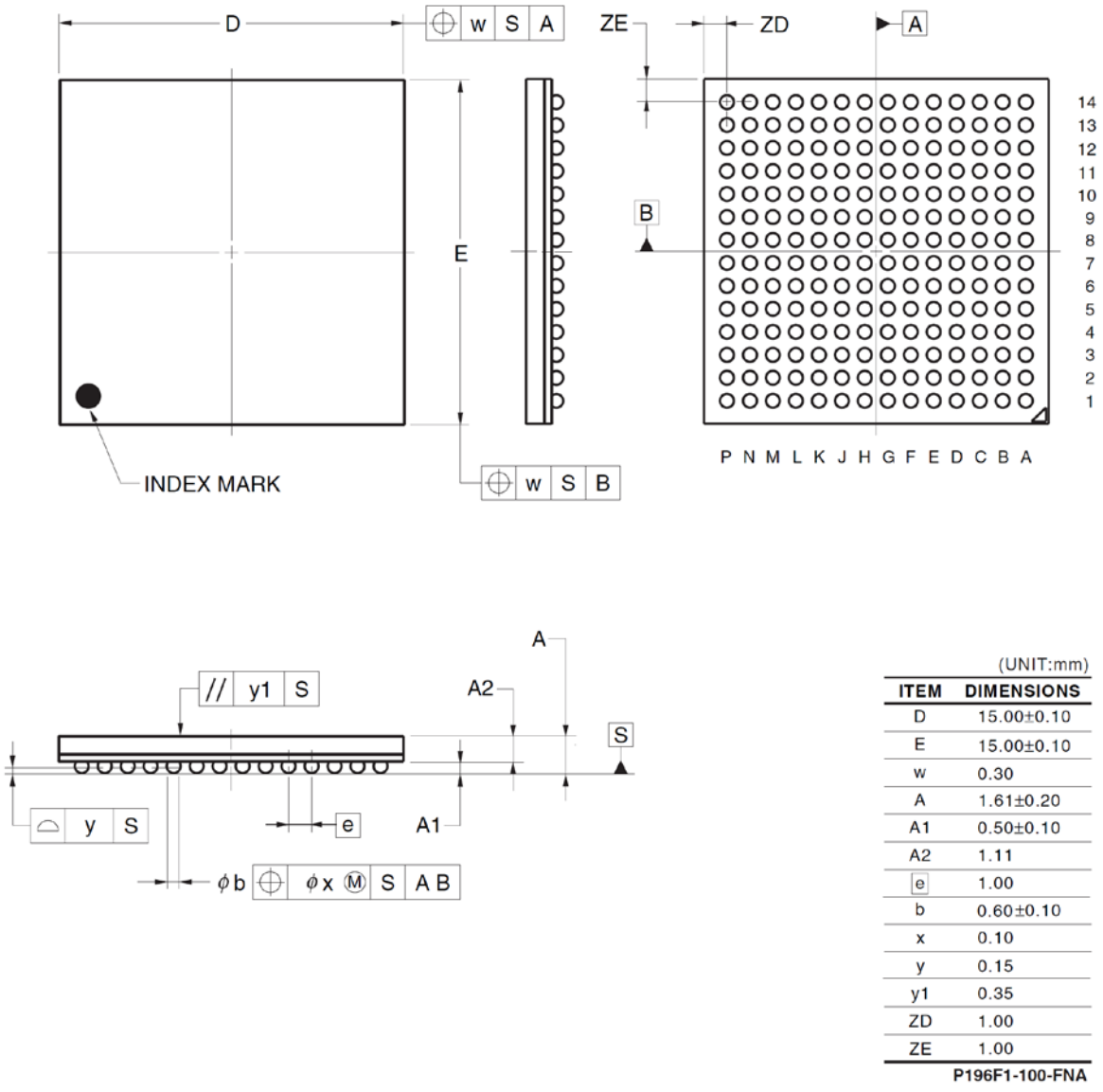


Figure 2-11: PHY AC Specification

3. Package Drawing

196-PIN PLASTIC BGA(15x15)



(UNIT:mm)

ITEM	DIMENSIONS
D	15.00±0.10
E	15.00±0.10
w	0.30
A	1.61±0.20
A1	0.50±0.10
A2	1.11
e	1.00
b	0.60±0.10
x	0.10
y	0.15
y1	0.35
ZD	1.00
ZE	1.00

P196F1-100-FNA

Figure 3-1: 196-ball FPBGA Package Drawing

Package:

Package	FPBGA 196 Pins
Ball Pitch	1.0 mm Pitch
Dimensions	15 mm * 15 mm

4. Recommended Soldering Conditions

Solder this product under the following recommended conditions.

For details of the recommended soldering conditions, refer to the information document.

Renesas Semiconductor Package Mount Manual, (Rev.5.0, Feb 2015) (R50ZZ0003EJ0500)

The applied standard is “IR60-107-3”.

Table 4-1: Recommended soldering conditions

Condition Symbol	Soldering Conditions
IR60	Package peak temperature: 260^{0}C, Time: 60 seconds max. (at 220^{0}C or higher).
-107	Exposure limit: 7 days[Note] (after that, prebake at 125^{0}C for 20 to 72 hours).
-3	Count: Three times or less.

Note: After opening the dry pack, store it at 25^{0}C or less and 65% RH or less for the allowable storage period.

Instructions for the use of product

In this section, the precautions are described for over whole of CMOS device.
Please refer to this manual about individual precaution.
When there is a mention unlike the text of this manual, a mention of the text takes first priority

1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
  In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
  In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

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