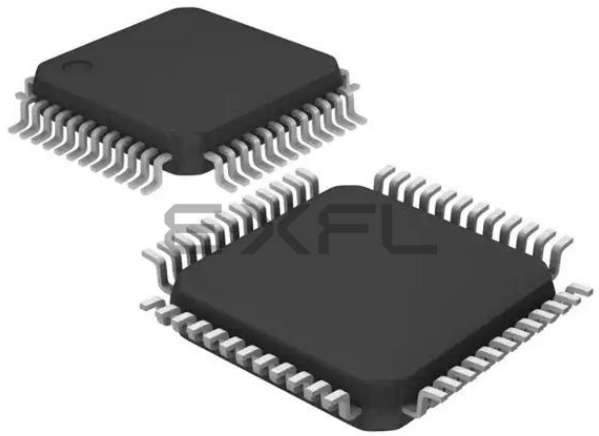

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	36MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	37
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f101c4t6a

Contents

List of Tables

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, general purpose timers TIMx and ADC.

2.3.14 RTC (real-time clock) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are ten 16-bit registers used to store 20 bytes of user application data when V_{DD} power is not present.

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a periodic interrupt. It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low power RC oscillator or the high-speed external clock divided by 128. The internal low power RC has a typical frequency of 40 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural crystal deviation. The RTC features a 32-bit programmable counter for long term measurement using the Compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

2.3.15 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

2.3.16 Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

2.3.17 SysTick timer

This timer is dedicated for OS, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

2.3.18 General-purpose timers (TIMx)

There areup to two synchronizable general-purpose timers embedded in the STM32F101xx Low-density access line devices. These timers are based on a 16-bit auto-reload up/down counter, a 16-bit prescaler and feature 4 independent channels each for input capture,

output compare, PWM or one pulse mode output. This gives up to 12 input captures / output compares / PWMs on the largest packages.
The general-purpose timers can work together via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs. They all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

2.3.19 I²C bus

The I²C bus interface can operate in multimaster and slave modes. It can support standard and fast modes.

It supports dual slave addressing (7-bit only) and both 7/10-bit addressing in master mode. A hardware CRC generation/verification is embedded.
The interface can be served by DMA and it supports SM Bus 2.0/PM Bus.

2.3.20 Universal synchronous/asynchronous receiver transmitter (USART)

The available USART interfaces communicate at up to 2.25 Mbit/s. They provide hardware management of the CTS and RTS signals, support IrDA SIR ENDEC, are ISO 7816 compliant and have LIN Master/Slave capability.

The USART interfaces can be served by the DMA controller.

2.3.21 Serial peripheral interface (SPI)

The SPI interface is able to communicate up to 18 Mbit/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

The SPI interface can be served by the DMA controller.

2.3.22 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current-capable.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

2.3.23 ADC (analog to digital converter)

The 12-bit analog to digital converter has up to 16 external channels and performs conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

2.3.24 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 2 V < V_{DDA} < 3.6 V. The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

2.3.25 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

Table 4. Low-density STM32F101xx pin definitions (continued)

Pins			Pin name	Type[1]	I / O level[2]	Main function[3] (after reset)	Alternate functions[3][4]	
LQFP48	LQFP64	VFQFPN36					Default	Remap
37	49	28	PA14	I/O	FT	JTCK/SWCLK	-	PA14
38	50	29	PA15	I/O	FT	JTDI	-	TIM2_CH1_ETR/ PA15 / SPI_NSS
-	51	-	PC10	I/O	FT	PC10	-	-
-	52	-	PC11	I/O	FT	PC11	-	-
-	53	-	PC12	I/O	FT	PC12	-	-
5	5	2	PD0	I/O	FT	OSC_IN[8]	-	-
6	6	3	PD1	I/O	FT	OSC_OUT[8]	-	-
-	54	-	PD2	I/O	FT	PD2	TIM3_ETR	-
39	55	30	PB3	I/O	FT	JTDO	-	TIM2_CH2 / PB3 TRACESWO SPI_SCK
40	56	31	PB4	I/O	FT	NJTRST	-	TIM3_CH1 / PB4 SPI_MISO
41	57	32	PB5	I/O	-	PB5	I2C_SMBA	TIM3_CH2 / SPI_MOSI
42	58	33	PB6	I/O	FT	PB6	I2C_SCL[7]	USART1_TX
43	59	34	PB7	I/O	FT	PB7	I2C_SDA[7]	USART1_RX
44	60	35	BOOT0	I	-	BOOT0	-	-
45	61	-	PB8	I/O	FT	PB8	-	I2C_SCL
46	62	-	PB9	I/O	FT	PB9	-	I2C_SDA
47	63	36	V_{SS_3}	S	-	V_{SS_3}	-	-
48	64	1	V_{DD_3}	S	-	V_{DD_3}	-	-

1. I = input, O = output, S = supply.
2. FT= 5 V tolerant.
3. Function availability depends on the chosen device. For devices having reduced peripheral counts, it is always the lower number of peripherals that is included. For example, if a device has only one SPI, two USARTs and two timers, they will be called SPI, USART1 & USART2 and TIM2 & TIM 3, respectively. Refer to *Table 2 on page 11*.
4. If several peripherals share the same I/O pin, to avoid conflict between these alternate functions only one peripheral should be enabled at a time through the peripheral clock enable bit (in the corresponding RCC peripheral clock enable register).
5. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited: the speed should not exceed 2 MHz with a maximum load of 30 pF and these IOs must not be used as a current source (e.g. to drive an LED).

Figure 8. Pin loading conditions

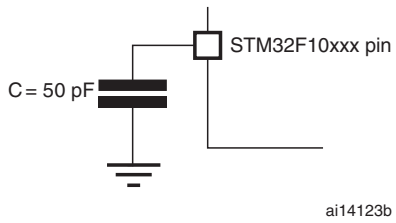
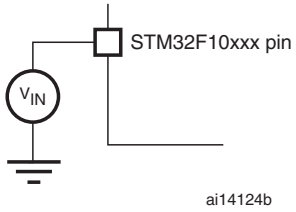
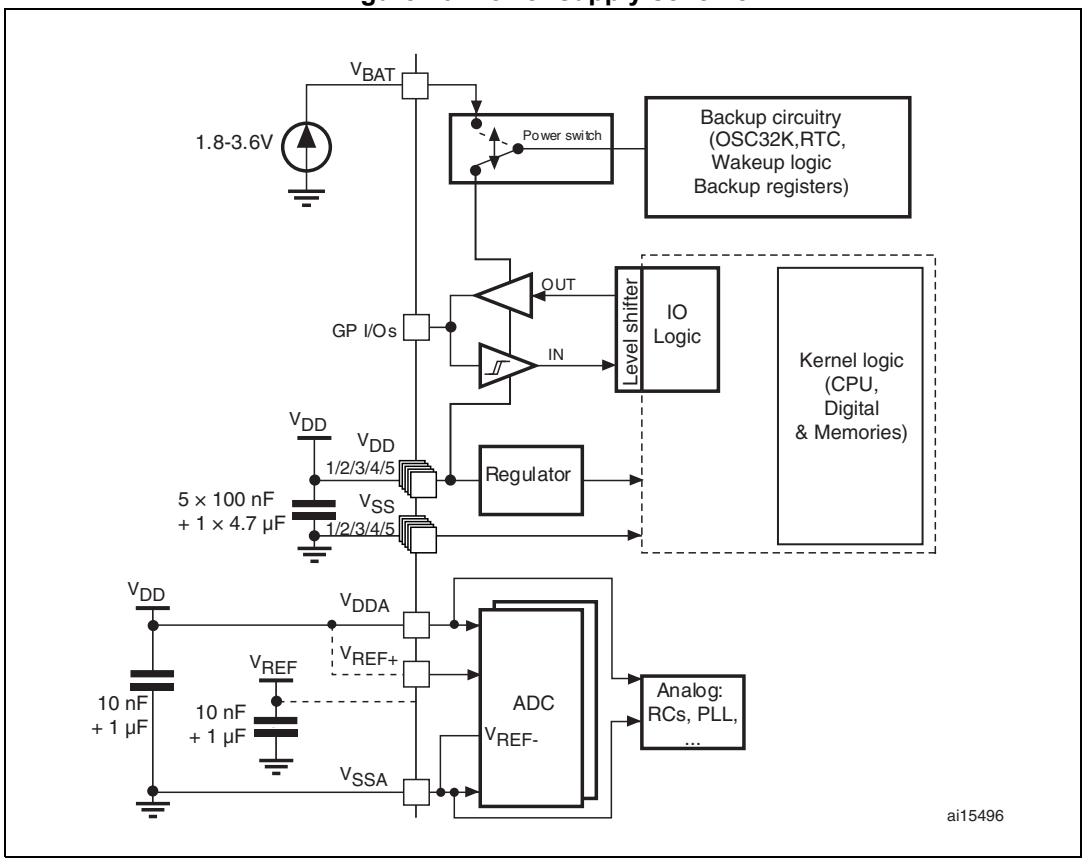


Figure 9. Pin input voltage



5.1.6 Power supply scheme

Figure 10. Power supply scheme



Caution: In *Figure 10*, the 4.7 µF capacitor must be connected to V_{DD3}.

Table 6. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} power lines (source)(1)	150	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(1)	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	–25	
$I_{INJ(PIN)}$(2)	Injected current on five volt tolerant pins(3)	-5/+0	
	Injected current on any other pin(4)	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(5)	± 25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. Negative injection disturbs the analog performance of the device. See note in *Section 5.3.17: 12-bit ADC characteristics*.
3. Positive injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 5: Voltage characteristics* for the maximum allowed input voltage values.
4. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 5: Voltage characteristics* for the maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 7. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

5.3 Operating conditions

5.3.1 General operating conditions

Table 8. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	36	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	36	
f_{PCLK2}	Internal APB2 clock frequency	-	0	36	
V_{DD}	Standard operating voltage	-	2	3.6	V
V_{DDA}(1)	Analog operating voltage (ADC not used)	Must be the same potential as V_{DD}(2)	2	3.6	
	Analog operating voltage (ADC used)		2.4	3.6	
V_{BAT}	Backup operating voltage	-	1.8	3.6	

Figure 12. Typical current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals enabled

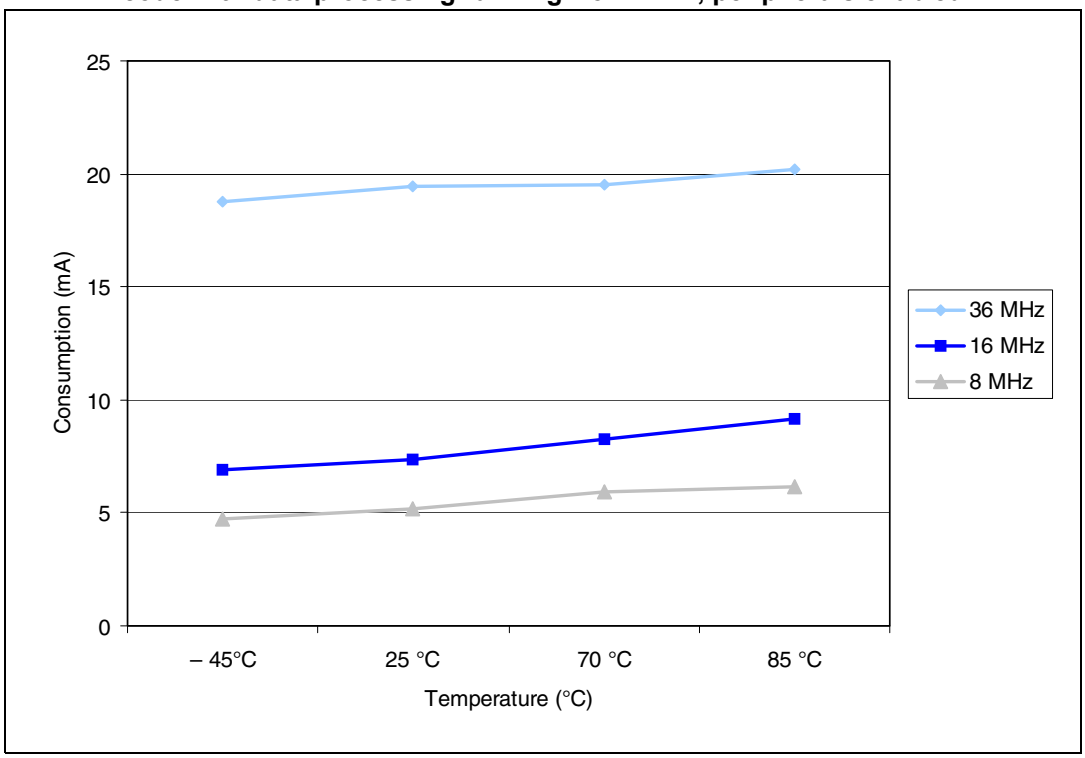


Figure 13. Typical current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals disabled

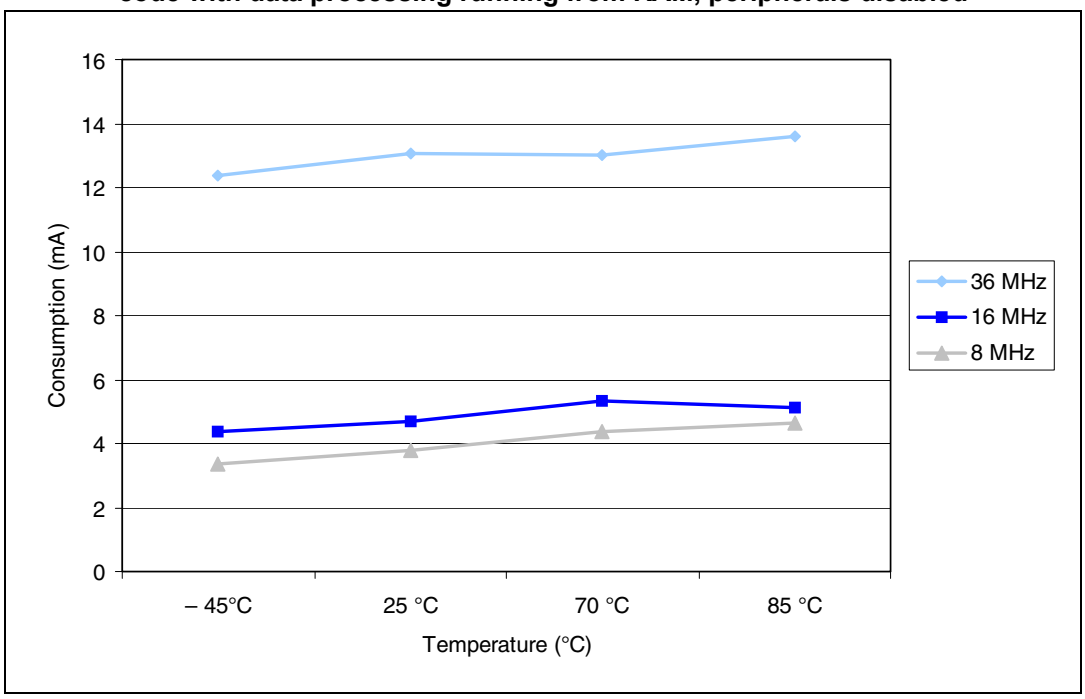


Table 18. Peripheral current consumption

Peripheral		Typical consumption at 25 °C	Unit
AHB (up to 36 MHz)	DMA1	15.97	µA/MHz
	CRC	1.67	
	BusMatrix(1)	8.33	
APB1 (up to 18 MHz)	APB1-Bridge	7.22	
	TIM2	33.33	
	TIM3	33.61	
	USART2	12.78	
	I2C1	10.83	
	WWDG	3.33	
	PWR	1.94	
	BKP	2.78	
	IWDG	1.39	
APB2 (up to 36 MHz)	APB2-Bridge	3.33	
	GPIO A	7.50	
	GPIO B	6.81	
	GPIO C	7.22	
	GPIO D	6.94	
	SPI1	4.86	
	USART1	12.78	
	ADC1(2)	15.54	

1. The BusMatrix is automatically active when at least one master is ON. (CPU, DMA1).
2. Specific conditions for measuring ADC current consumption: f_{HCLK} = 28 MHz, $f_{APB1} = f_{HCLK}$, $f_{APB2} = f_{HCLK}$, $f_{ADCCLK} = f_{APB2} / 2$. When ADON bit in the ADC_CR2 register is set to 1, a current consumption of analog part equal to 0.7 mA must be added.

5.3.6 External clock source characteristics

High-speed external user clock generated from an external source

The characteristics given in *Table 19* result from tests performed using an high-speed external clock source, and under the ambient temperature and supply voltage conditions summarized in *Table 8*.

Low-speed internal (LSI) RC oscillator

Table 24. LSI oscillator characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}(2)	Frequency	30	40	60	kHz
$t_{su(LSI)}$(3)	LSI oscillator startup time	-	-	85	µs
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-	0.65	1.2	µA

1. V_{DD} = 3 V, T_A = –40 to 85 °C unless otherwise specified.
2. Based on characterization, not tested in production.
3. Guaranteed by design, not tested in production.

Wakeup time from low-power mode

The wakeup times given in *Table 25* are measured on a wakeup phase with an 8-MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

All timings are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 25. Low-power mode wakeup timings

Symbol	Parameter	Typ	Unit
$t_{WUSLEEP}$(1)	Wakeup from Sleep mode	1.8	µs
t_{WUSTOP}(1)	Wakeup from Stop mode (regulator in run mode)	3.6	µs
	Wakeup from Stop mode (regulator in low-power mode)	5.4	
$t_{WUSTDBY}$(1)	Wakeup from Standby mode	50	µs

1. The wakeup times are measured from the wakeup event to the point at which the user application code reads the first instruction.

5.3.8 PLL characteristics

The parameters given in *Table 26* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 26. PLL characteristics

Symbol	Parameter	Value			Unit
		Min(1)	Typ	Max(1)	
f_{PLL_IN}	PLL input clock(2)	1	8.0	25	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL multiplier output clock	16	-	36	MHz

5.3.11 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 30. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to JESD22-A114	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to ANSI/ESD STM5.3.1	II	500	

1. Based on characterization results, not tested in production.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78 IC latch-up standard.

Table 31. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +85 °C conforming to JESD78A	II level A

5.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibilty to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation).

The test results are given in *Table 32*

Table 32. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on OSC_IN32, OSC_OUT32, PA4, PA5, PC13	-0	+0	mA
	Injected current on all FT pins	-5	+0	
	Injected current on any other pin	-5	+5	

5.3.13 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 33* are derived from tests performed under the conditions summarized in *Table 8*. All I/Os are CMOS and TTL compliant.

Table 33. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Standard IO input low level voltage	-	-0.3	-	0.28*(V_{DD}-2 V)+0.8 V(1)	V
	IO FT(2) input low level voltage		-0.3	-	0.32*(V_{DD}-2 V)+0.75 V(1)	
V_{IH}	Standard IO input high level voltage	-	0.41*(V_{DD}-2 V)+1.3 V(1)	-	V_{DD}+0.3	
	IO FT(2) input high level voltage	V_{DD} > 2 V	0.42*(V_{DD}-2 V)+1 V(1)	-	5.5	
		V_{DD} ≤ 2 V			5.2	
V_{hys}	Standard IO Schmitt trigger voltage hysteresis(3)	-	200	-	-	mV
	IO FT Schmitt trigger voltage hysteresis(3)	-	5% V_{DD}(4)	-	-	
I_{lkg}	Input leakage current (5)	V_{SS} ≤ V_{IN} ≤ V_{DD} Standard I/Os	-	-	±1	µA
		V_{IN} = 5 V I/O FT	-	-	3	
R_{PU}	Weak pull-up equivalent resistor(6)	V_{IN} = V_{SS}	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistor(6)	V_{IN} = V_{DD}	30	40	50	
C_{IO}	I/O pin capacitance	-	-	5	-	pF

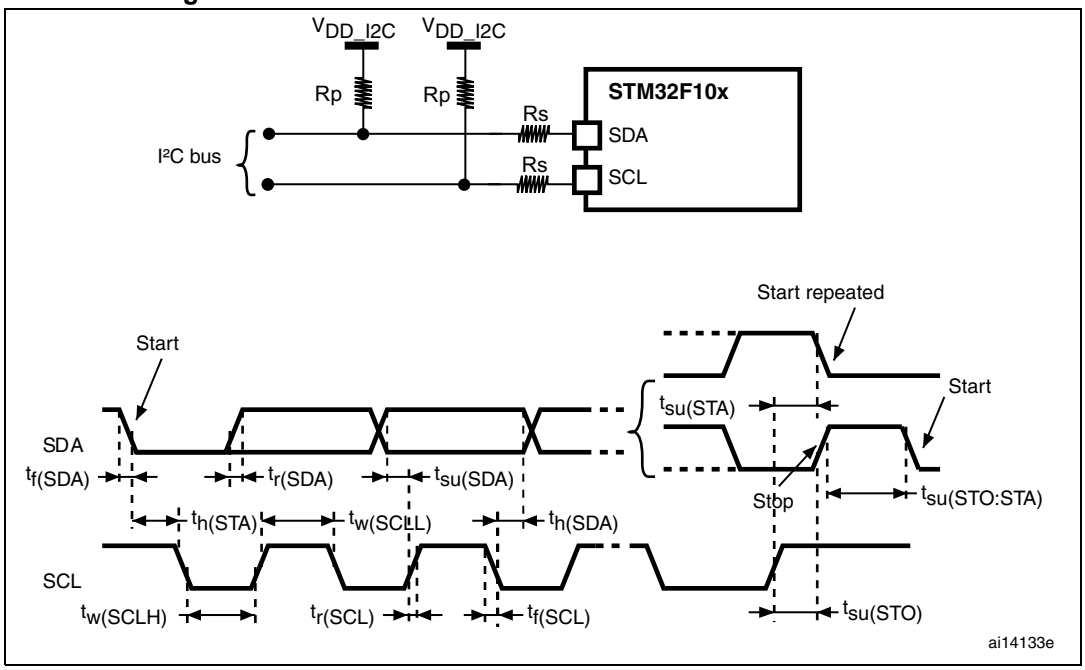
1. Data based on design simulation.
2. FT = Five-volt tolerant. In order to sustain a voltage higher than V_{DD}+0.3 the internal pull-up/pull-down resistors must be disabled.
3. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization, not tested in production.
4. With a minimum of 100 mV.
5. Leakage could be higher than max. if negative current is injected on adjacent pins.
6. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimum (~10% order).

Table 38. I^2C characteristics

Symbol	Parameter	Standard mode I^2C(1)		Fast mode I^2C(1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0	-	0(3)	900(4)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	20+0.1C_b	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated Start condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	Stop condition setup time	4.0	-	0.6	-	µs
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7	-	1.3	-	µs
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. Guaranteed by design, not tested in production.
2. f_{PCLK1} must be at least 2 MHz to achieve standard mode I^2C frequencies. It must be at least 4 MHz to achieve fast mode I^2C frequencies. It must be a multiple of 10 MHz to reach the 400 kHz maximum I2C fast mode clock.
3. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
4. The maximum Data hold time has only to be met if the interface does not stretch the low period of SCL signal.

Figure 28. I²C bus AC waveforms and measurement circuit(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.
2. Rs = Series protection resistors, Rp = Pull-up resistors, V_{DD_I2C} = I2C bus supply.

Table 39. SCL frequency (f_{PCLK1}= MHz, V_{DD_I2C} = 3.3 V)(1)(2)

f_{SCL} (kHz)	I2C_CCR value
	R_P = 4.7 kΩ
400	0x801E
300	0x8028
200	0x803C
100	0x00B4
50	0x0168
20	0x0384

1. R_P = External pull-up resistance, f_{SCL} = I²C speed,
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed ±2%. These variations depend on the accuracy of the external components used to design the application.

SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 40* are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 8*.

Refer to *Section 5.3.12: I/O current injection characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 40. SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	0	18	MHz
		Slave mode	0	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF		8	ns
$t_{su(NSS)}$ (1)	NSS setup time	Slave mode	4 t_{PCLK}	-	
$t_{h(NSS)}$ (1)	NSS hold time	Slave mode	73	-	
$t_{w(SCKH)}$ (1) $t_{w(SCKL)}$ (1)	SCK high and low time	Master mode, f_{PCLK} = 36 MHz, presc = 4	50	60	
$t_{su(MI)}$ (1)	Data input setup time Master mode	SPI	1	-	
$t_{su(SI)}$ (1)	Data input setup time Slave mode	-	1	-	
$t_{h(MI)}$ (1)	Data input hold time Master mode	SPI	1	-	
$t_{h(SI)}$ (1)	Data input hold time Slave mode	-	3	-	
$t_{a(SO)}$ (1)(2)	Data output access time	Slave mode, f_{PCLK} = 36 MHz, presc = 4	0	55	
		Slave mode, f_{PCLK} = 24 MHz	0	4 t_{PCLK}	
$t_{dis(SO)}$ (1)(3)	Data output disable time	Slave mode	10		
$t_{v(SO)}$ (1)	Data output valid time	Slave mode (after enable edge)	-	25	
$t_{v(MO)}$ (1)	Data output valid time	Master mode (after enable edge)	-	3	
$t_{h(SO)}$ (1)	Data output hold time	Slave mode (after enable edge)	25	-	
$t_{h(MO)}$ (1)		Master mode (after enable edge)	4	-	

1. Based on characterization, not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

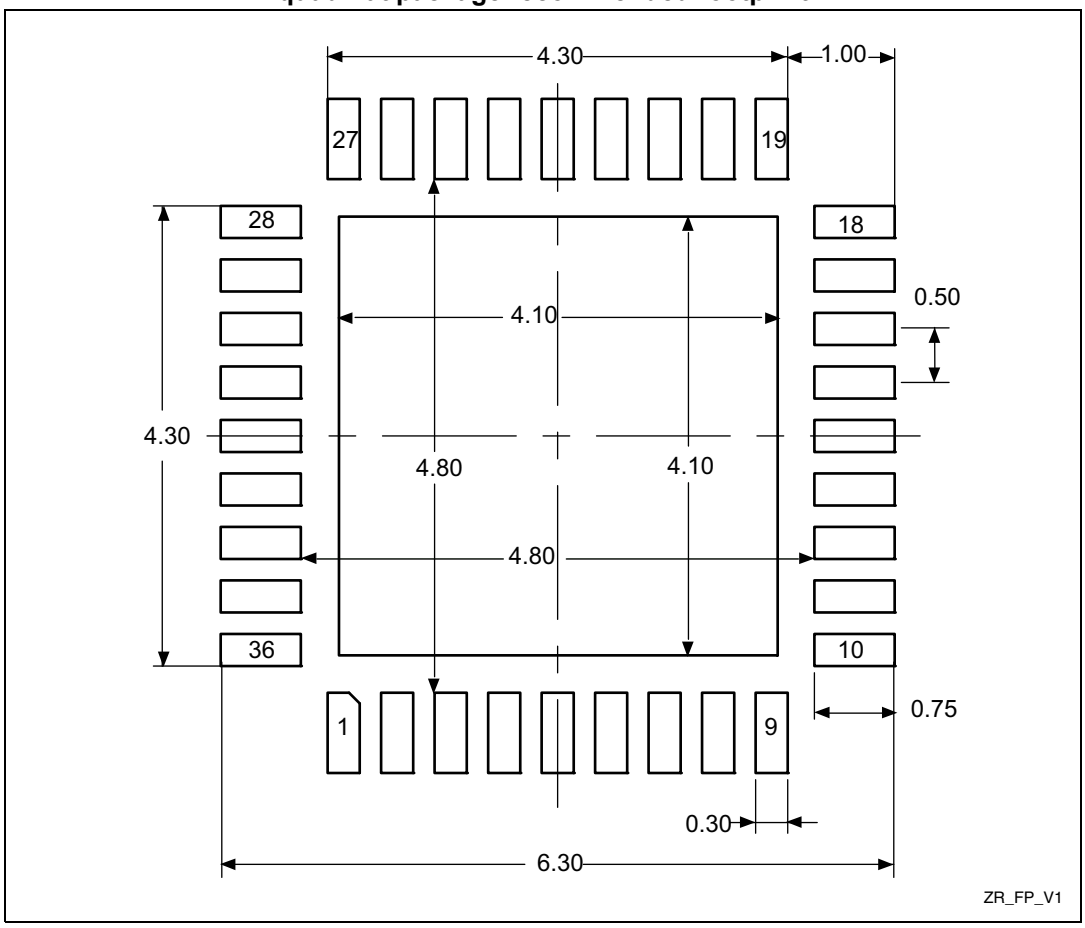
5.3.18 Temperature sensor characteristics

Table 45. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	4.0	4.3	4.6	mV/°C
V_{25}(1)	Voltage at 25°C	1.34	1.43	1.52	V
t_{START}(2)	Startup time	4	-	10	µs
T_{S_temp}(3)(2)	ADC sampling time when reading the temperature	-	-	17.1	µs

1. Guaranteed by characterization, not tested in production.
2. Guaranteed by design, not tested in production.
3. Shortest sampling time can be determined in the application by multiple iterations.

Figure 36. VFQFPN36 - 36-pin, 6x6 mm, 0.5 mm pitch very thin profile fine pitch quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

Table 51. Document revision history (continued)

Date	Revision	Changes
19-Apr-2011	5	Updated footnotes below *Table 5: Voltage characteristics on page 30* and *Table 6: Current characteristics on page 31* Updated tw min in *Table 19: High-speed external user clock characteristics on page 43* Updated startup time in *Table 22: LSE oscillator characteristics (fLSE = 32.768 kHz) on page 46* Added *Section 5.3.12: I/O current injection characteristics* Updated *Section 5.3.13: I/O port characteristics*
25-Sep-2015	6	Updated: – All GPIOs are high current...' in *Section 2.3.22: GPIOs (general-purpose inputs/outputs)* – first sentence in *Output driving current* – *Table 2: Low-density STM32F101xx device features and peripheral counts*, *Table 4: Low-density STM32F101xx pin definitions*, – *Table 6: Current characteristics* – *Table 8: General operating conditions* – *Table 18: Peripheral current consumption* – notes in *Table 38: I2C characteristics* – note *2.* in *Table 44: ADC accuracy* – title of *Table 39: SCL frequency (fPCLK1= MHz, VDD_I2C = 3.3 V)* – reference for '$V_{ESD(CDM)}$' in *Table 30: ESD absolute maximum ratings* – *Table 50: Ordering information scheme*, – *Table 49: Package thermal characteristics*, – *Figure 28: I2C bus AC waveforms and measurement circuit(1)* Added – note *5.* in *Table 23: HSI oscillator characteristics* – *Figure 37: VFQFPN36 marking example (package top view)* – *Figure 40: LQFP64 marking example (package top view)* – *Figure 43: LQFP48 marking example (package top view)* Corrected – Corrected 'tf(IO)out' in *Figure 26: I/O AC characteristics definition* – Sigma letter in *Section 5.1.1: Minimum and maximum values* Removed – UFDFPN48 package – First sentence in *Section 5.3.16: Communications interfaces*