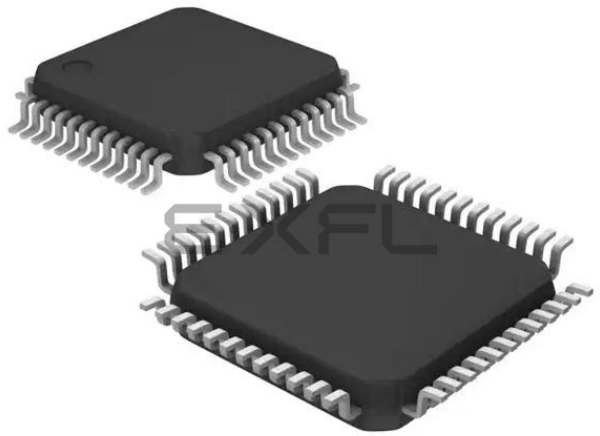

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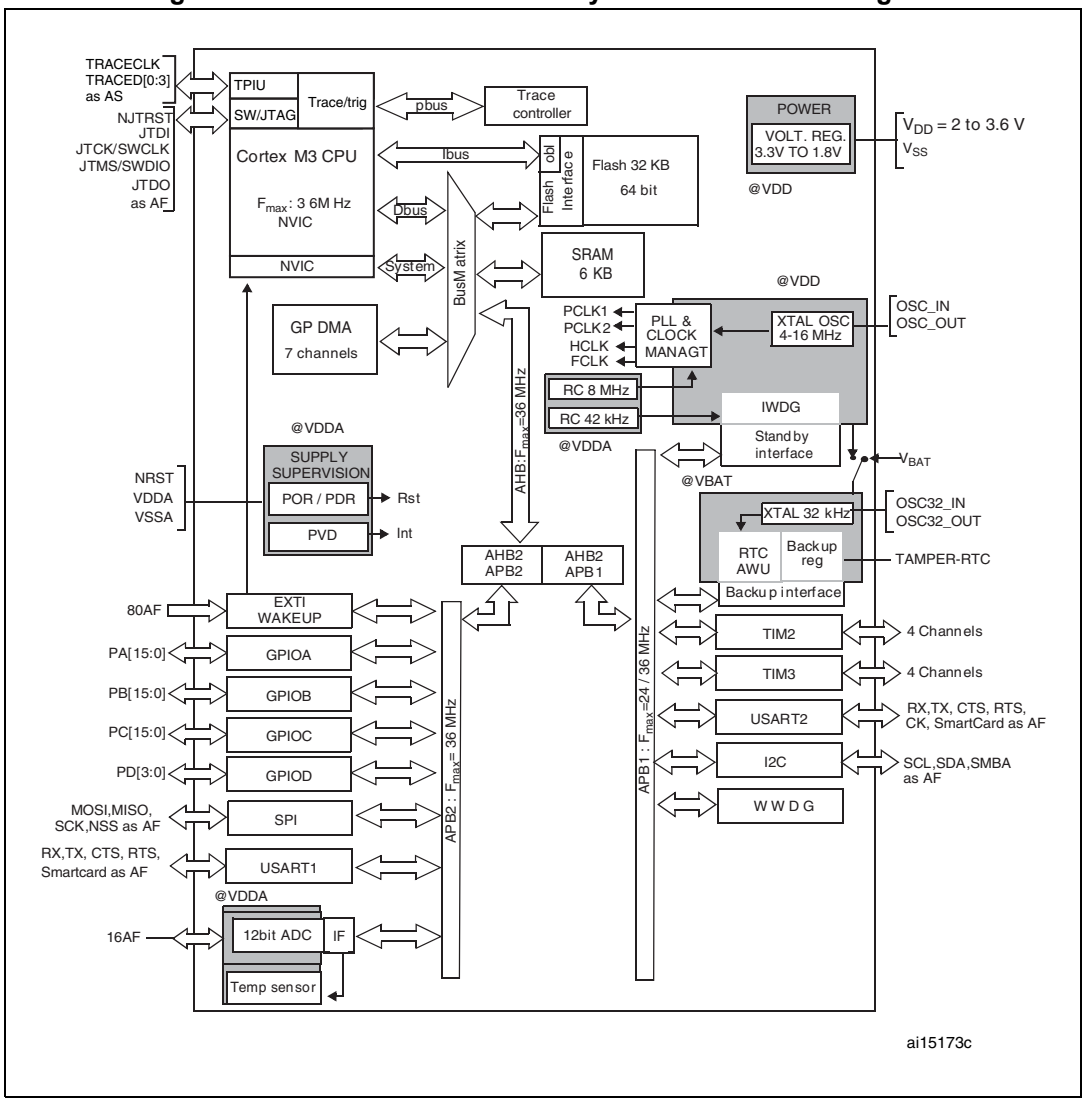
Applications of "Embedded - Microcontrollers"

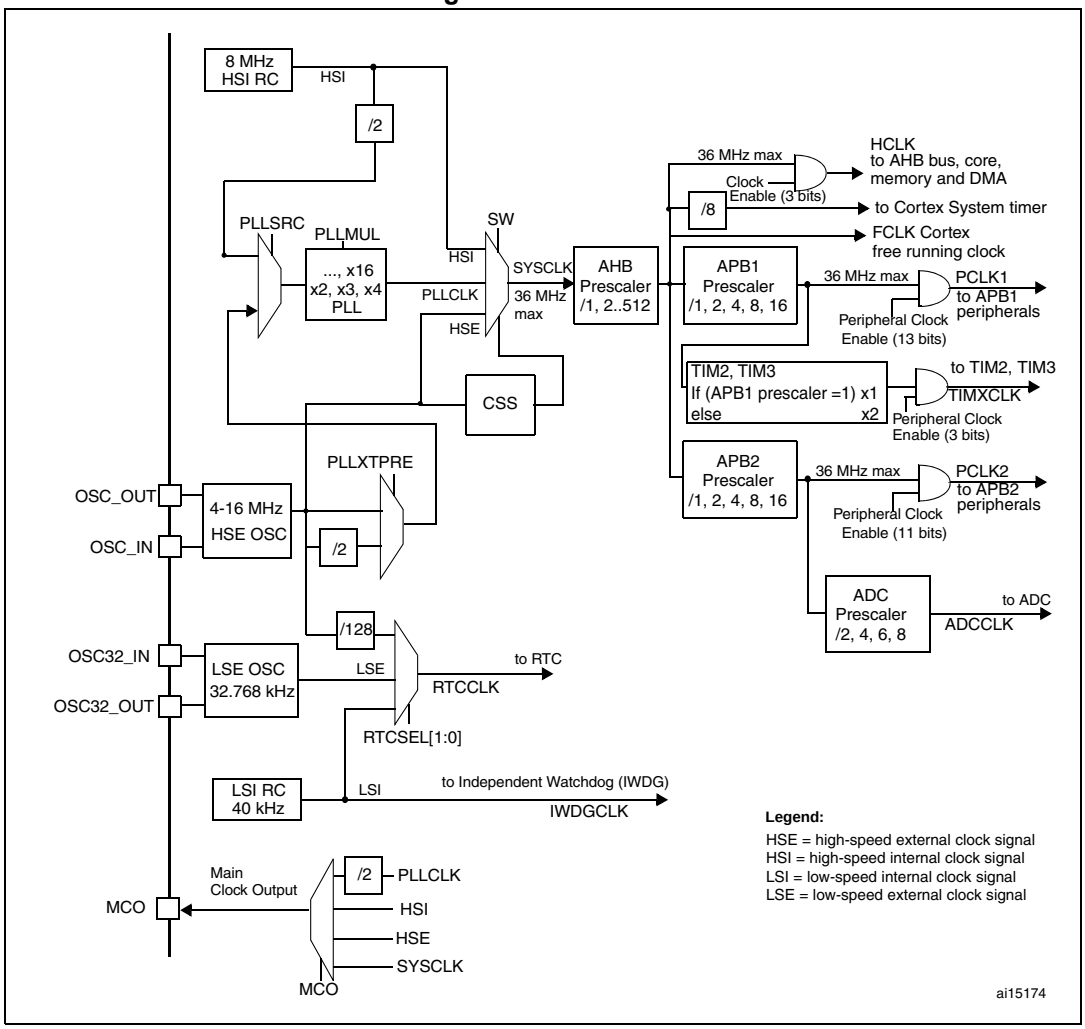
Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	36MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	37
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f101c6t6

Figure 1. STM32F101xx Low-density access line block diagram



1. AF = alternate function on I/O port pin.
2. T_A = –40 °C to +85 °C (junction temperature up to 105 °C).

Figure 2. Clock tree



1. When the HSI is used as a PLL clock input, the maximum system clock frequency that can be achieved is 36 MHz.
2. To have an ADC conversion time of 1 µs, APB2 must be at 14 MHz or 28 MHz.

Table 4. Low-density STM32F101xx pin definitions (continued)

Pins			Pin name	Type(1)	I / O level(2)	Main function(3) (after reset)	Alternate functions(3)(4)	
LQFP48	LQFP64	VFQFPN36					Default	Remap
37	49	28	PA14	I/O	FT	JTCK/SWCLK	-	PA14
38	50	29	PA15	I/O	FT	JTDI	-	TIM2_CH1_ETR/ PA15 / SPI_NSS
-	51	-	PC10	I/O	FT	PC10	-	-
-	52	-	PC11	I/O	FT	PC11	-	-
-	53	-	PC12	I/O	FT	PC12	-	-
5	5	2	PD0	I/O	FT	OSC_IN(8)	-	-
6	6	3	PD1	I/O	FT	OSC_OUT(8)	-	-
-	54	-	PD2	I/O	FT	PD2	TIM3_ETR	-
39	55	30	PB3	I/O	FT	JTDO	-	TIM2_CH2 / PB3 TRACESWO SPI_SCK
40	56	31	PB4	I/O	FT	NJTRST	-	TIM3_CH1 / PB4 SPI_MISO
41	57	32	PB5	I/O	-	PB5	I2C_SMBA	TIM3_CH2 / SPI_MOSI
42	58	33	PB6	I/O	FT	PB6	I2C_SCL(7)	USART1_TX
43	59	34	PB7	I/O	FT	PB7	I2C_SDA(7)	USART1_RX
44	60	35	BOOT0	I	-	BOOT0	-	-
45	61	-	PB8	I/O	FT	PB8	-	I2C_SCL
46	62	-	PB9	I/O	FT	PB9	-	I2C_SDA
47	63	36	V_{SS_3}	S	-	V_{SS_3}	-	-
48	64	1	V_{DD_3}	S	-	V_{DD_3}	-	-

1. I = input, O = output, S = supply.
2. FT= 5 V tolerant.
3. Function availability depends on the chosen device. For devices having reduced peripheral counts, it is always the lower number of peripherals that is included. For example, if a device has only one SPI, two USARTs and two timers, they will be called SPI, USART1 & USART2 and TIM2 & TIM 3, respectively. Refer to *Table 2 on page 11*.
4. If several peripherals share the same I/O pin, to avoid conflict between these alternate functions only one peripheral should be enabled at a time through the peripheral clock enable bit (in the corresponding RCC peripheral clock enable register).
5. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited: the speed should not exceed 2 MHz with a maximum load of 30 pF and these IOs must not be used as a current source (e.g. to drive an LED).

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V (for the 2 V ≤ V_{DD} ≤ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 8*.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 9*.

Table 8. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
P_D	Power dissipation at T_A = 85 °C(3)	LQFP64	-	444	mW
		LQFP48	-	363	
		VFQFPN36	-	1000	
T_A	Ambient temperature	Maximum power dissipation	–40	85	°C
		Low power dissipation(4)	–40	105	
T_J	Junction temperature range	-	–40	105	

1. When the ADC is used, refer to *Table 41: ADC characteristics*.
2. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and operation.
3. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed $T_J$max (see *Table 6.5: Thermal characteristics on page 82*).
4. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed $T_J$max (see *Table 6.5: Thermal characteristics on page 82*).

5.3.2 Operating conditions at power-up / power-down

Subject to general operating conditions for T_A.

Table 9. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	µs/V
	V_{DD} fall time rate		20	∞	

5.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 10* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

5.3.4 Embedded reference voltage

The parameters given in *Table 11* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 11. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +85 °C	1.16	1.20	1.24	V
$T_{S_vrefint}$(1)	ADC sampling time when reading the internal reference voltage	-	-	5.1	17.1(2)	µs
V_{RERINT}(2)	Internal reference voltage spread over the temperature range	V_{DD} = 3 V ±10 mV	-	-	10	mV
T_{Coeff}(2)	Temperature coefficient	-	-	-	100	ppm/ °C

1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design, not tested in production.

5.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.
The current consumption is measured as described in *Figure 11: Current consumption measurement scheme*.
All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code.

Maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except if it is explicitly mentioned
- The Flash access time is adjusted to f_{HCLK} frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 36 MHz)
- Prefetch in on (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK1} = f_{HCLK/2}$, $f_{PCLK2} = f_{HCLK}$

The parameters given in *Table 12* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Figure 18. High-speed external clock source AC timing diagram

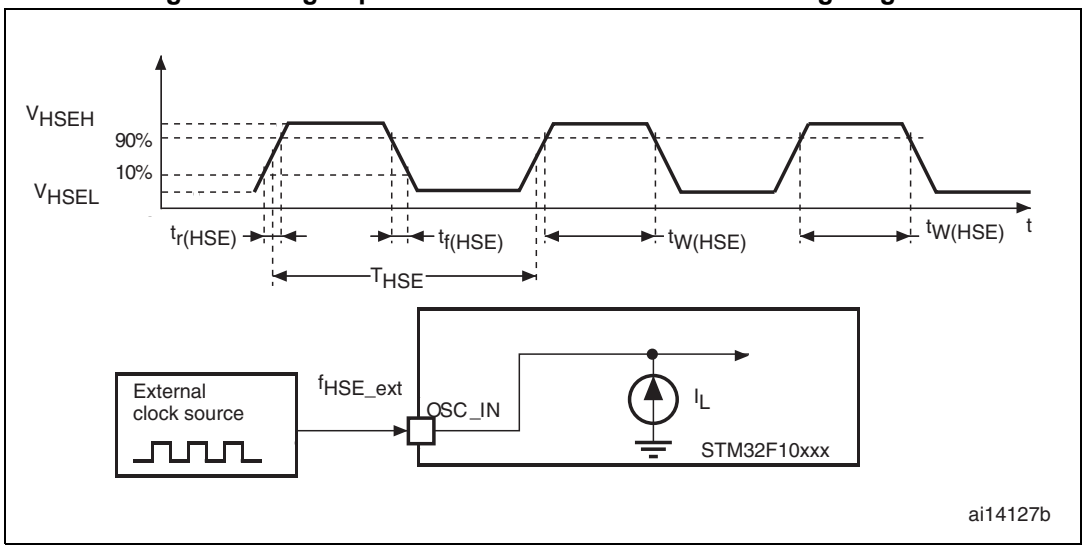
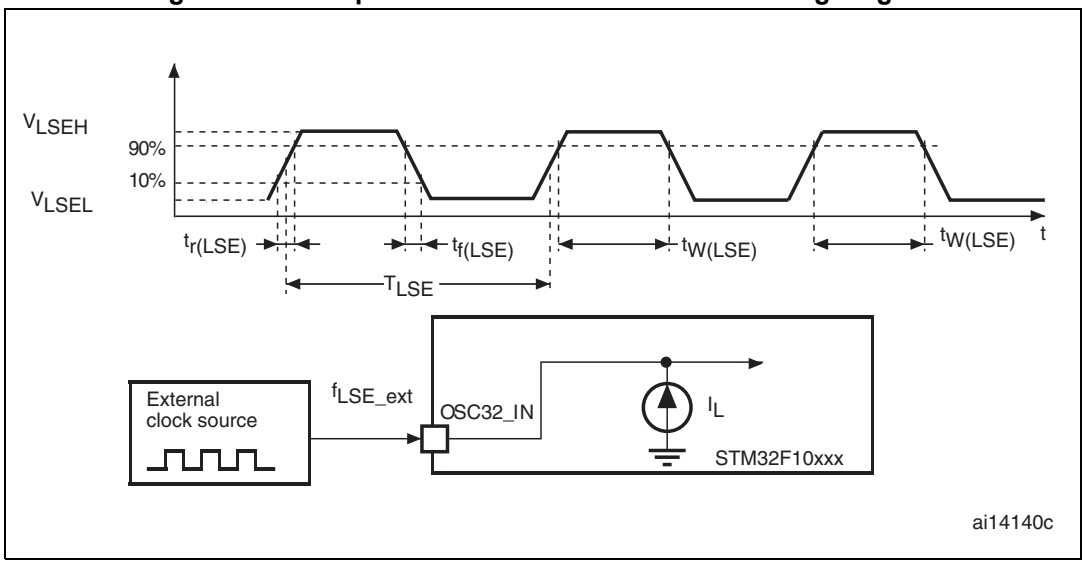


Figure 19. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 21*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 22. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1) (2)

Symbol	Parameter	Conditions	-	Min	Typ	Max	Unit
R_F	Feedback resistor	-	-	-	5	-	MΩ
C	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)	R_S = 30 KΩ	-	-	-	15	pF
I_2	LSE driving current	V_{DD} = 3.3 V V_{IN} = V_{SS}	-	-	-	1.4	µA
g_m	Oscillator transconductance	-	-	5	-	-	µA/V
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	T_A = 50 °C	-	1.5	-	s
			T_A = 25 °C	-	2.5	-	
			T_A = 10 °C	-	4	-	
			T_A = 0 °C	-	6	-	
			T_A = -10 °C	-	10	-	
			T_A = -20 °C	-	17	-	
			T_A = -30 °C	-	32	-	
			T_A = -40 °C	-	60	-	

1. Based on characterization, not tested in production.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

Note: For CL1 and CL2 it is recommended to use high-quality ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator. CL1 and CL2, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of CL1 and CL2.
Load capacitance CL *has the following formula:* CL = CL1 *x* CL2 / (CL1 + CL2) + C_{stray} *where* C_{stray} *is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.*

Caution: To avoid exceeding the maximum value of CL1 and CL2 (15 pF) it is strongly recommended to use a resonator with a load capacitance CL ≤7 pF. Never use a resonator with a load capacitance of 12.5 pF.
Example: if resonator with a load capacitance of CL = 6 pF, and C_{stray} = 2 pF is chosen, then CL1 = CL2 = 8 pF.

Low-speed internal (LSI) RC oscillator

Table 24. LSI oscillator characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}(2)	Frequency	30	40	60	kHz
$t_{su(LSI)}$(3)	LSI oscillator startup time	-	-	85	µs
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-	0.65	1.2	µA

1. V_{DD} = 3 V, T_A = –40 to 85 °C unless otherwise specified.
2. Based on characterization, not tested in production.
3. Guaranteed by design, not tested in production.

Wakeup time from low-power mode

The wakeup times given in *Table 25* are measured on a wakeup phase with an 8-MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

All timings are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 25. Low-power mode wakeup timings

Symbol	Parameter	Typ	Unit
$t_{WUSLEEP}$(1)	Wakeup from Sleep mode	1.8	µs
t_{WUSTOP}(1)	Wakeup from Stop mode (regulator in run mode)	3.6	µs
	Wakeup from Stop mode (regulator in low-power mode)	5.4	
$t_{WUSTDBY}$(1)	Wakeup from Standby mode	50	µs

1. The wakeup times are measured from the wakeup event to the point at which the user application code reads the first instruction.

5.3.8 PLL characteristics

The parameters given in *Table 26* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 26. PLL characteristics

Symbol	Parameter	Value			Unit
		Min(1)	Typ	Max(1)	
f_{PLL_IN}	PLL input clock(2)	1	8.0	25	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL multiplier output clock	16	-	36	MHz

Table 26. PLL characteristics (continued)

Symbol	Parameter	Value			Unit
		Min(1)	Typ	Max(1)	
t_{LOCK}	PLL lock time	-	-	200	µs
Jitter	Cycle-to-cycle jitter	-	-	300	ps

1. Based on device characterization, not tested in production.
2. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.

5.3.9 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 85 °C unless otherwise specified.

Table 27. Flash memory characteristics

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	16-bit programming time	T_A = –40 to +85 °C	40	52.5	70	µs
t_{ERASE}	Page (1 KB) erase time	T_A = –40 to +85 °C	20	-	40	ms
t_{ME}	Mass erase time	T_A = –40 to +85 °C	20	-	40	ms
I_{DD}	Supply current	Read mode f_{HCLK} = 36 MHz with 1 wait state, V_{DD} = 3.3 V	-	-	20	mA
		Write / Erase modes f_{HCLK} = 36 MHz, V_{DD} = 3.3 V	-	-	5	mA
		Power-down mode / Halt, V_{DD} = 3.0 to 3.6 V	-	-	50	µA
V_{prog}	Programming voltage	-	2	-	3.6	V

1. Guaranteed by design, not tested in production.

5.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (Electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation).

The test results are given in *Table 32*

Table 32. I/O current injection susceptibility

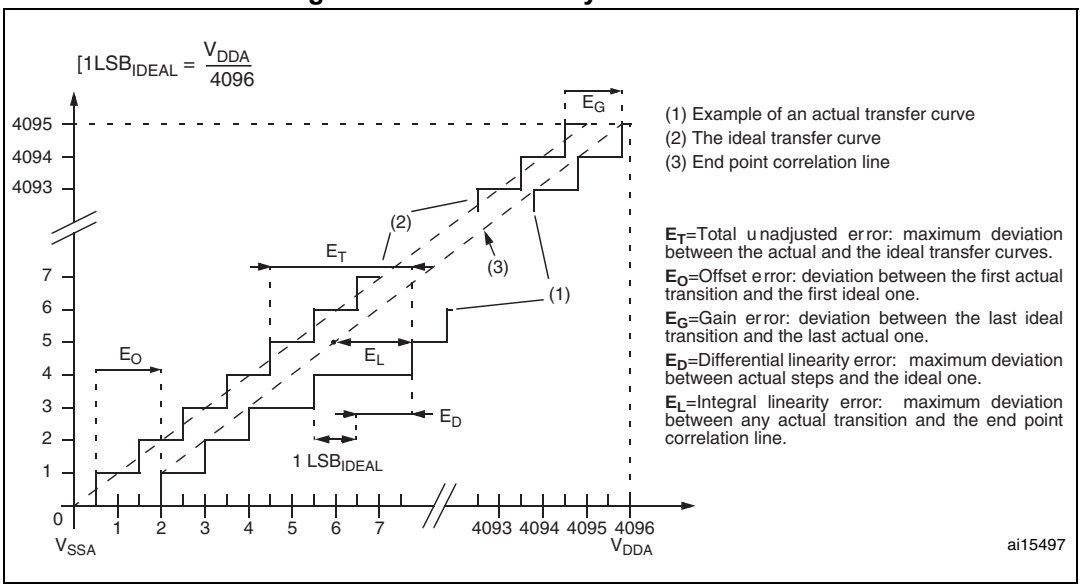
Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on OSC_IN32, OSC_OUT32, PA4, PA5, PC13	-0	+0	mA
	Injected current on all FT pins	-5	+0	
	Injected current on any other pin	-5	+5	

Table 44. ADC accuracy(1) (2) (3)

Symbol	Parameter	Test conditions	Typ	Max(4)	Unit
ET	Total unadjusted error	f_{PCLK2} = 28 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.4 V to 3.6 V Measurements made after ADC calibration	±2	±5	LSB
EO	Offset error		±1.5	±2.5	
EG	Gain error		±1.5	±3	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±1.5	±3	

1. ADC DC accuracy values are measured after internal calibration.
2. Better performance could be achieved in restricted V_{DD}, frequency and temperature ranges.
3. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 5.3.12* does not affect the ADC accuracy.
4. Based on characterization, not tested in production.

Figure 32. ADC accuracy characteristics



5.3.18 Temperature sensor characteristics

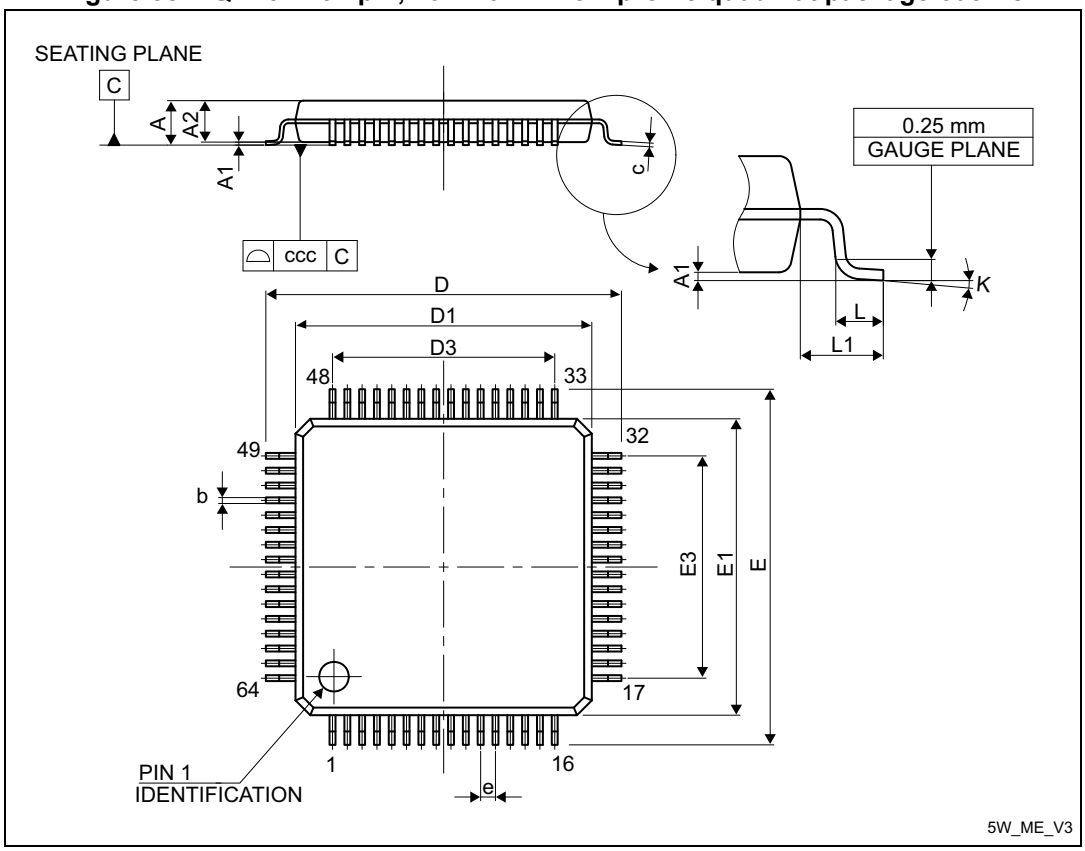
Table 45. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	4.0	4.3	4.6	mV/°C
V_{25}(1)	Voltage at 25°C	1.34	1.43	1.52	V
t_{START}(2)	Startup time	4	-	10	µs
T_{S_temp}(3)(2)	ADC sampling time when reading the temperature	-	-	17.1	µs

1. Guaranteed by characterization, not tested in production.
2. Guaranteed by design, not tested in production.
3. Shortest sampling time can be determined in the application by multiple iterations.

6.3 LQFP64 package information

Figure 38. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline



1. Drawing is not to scale.

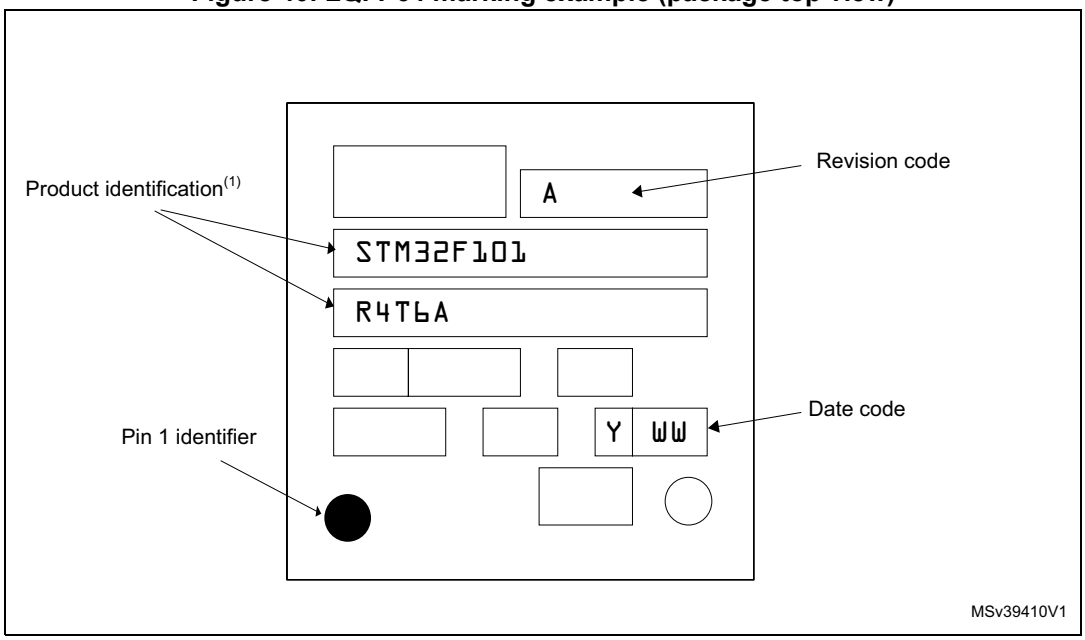
Table 47. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-

Device Marking for LQFP64

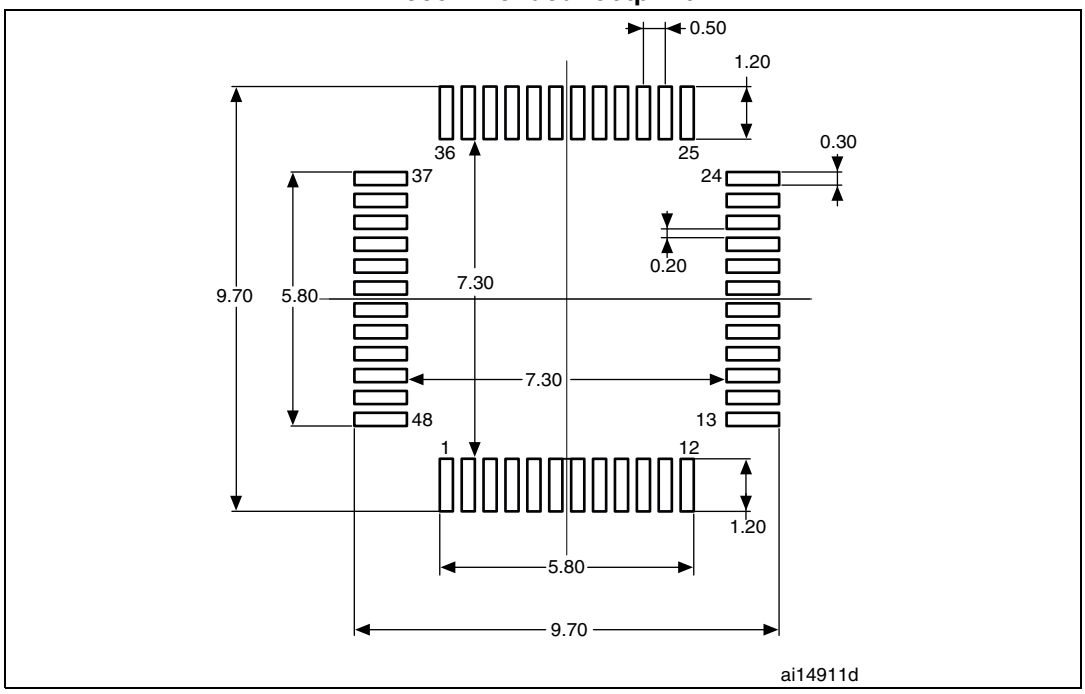
The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 40. LQFP64 marking example (package top view)



1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Figure 42. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint

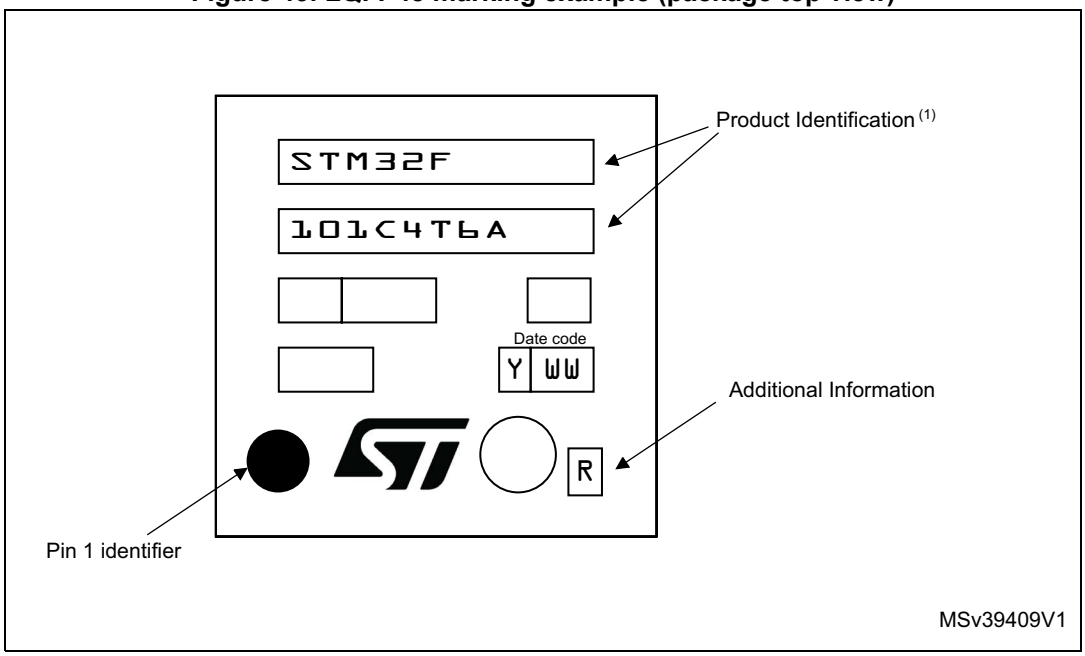


1. Dimensions are expressed in millimeters.

Device Marking for LQFP48

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 43. LQFP48 marking example (package top view)



1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7 Ordering information scheme

Table 50. Ordering information scheme

Example: STM32 F 101 C 4 T 6 A xxx

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = general-purpose

Device subfamily

101 = access line

Pin count

T = 36 pins

C = 48 pins

R = 64 pins

Flash memory size

4 = 16 Kbytes of Flash memory

6 = 32 Kbytes of Flash memory

Package

T = LQFP

U = VFQFPN

Temperature range

6 = Industrial temperature range, –40 to 85 °C.

Internal code

“A” or blank(1)

Options

xxx = programmed parts

TR = tape and real

1. For STM32F101x6 devices with a blank internal code, please refer to the STM32F103x6/8/B datasheet available from the ST website: www.st.com.

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact the nearest ST sales office.

8 Revision history

Table 51. Document revision history

Date	Revision	Changes
23-Sep-2008	1	Initial release.
07-Apr-2009	2	I/O information clarified *on page 1*. *Figure 7: Memory map* modified. In *Table 4: Low-density STM32F101xx pin definitions*: PB4, PB13, PB14, PB15, PB3/TRACESWO moved from Default column to Remap column. V_{REF-} is not available in the offered packages: *Figure 1: STM32F101xx Low-density access line block diagram*, *Figure 10: Power supply scheme* and *Figure 34: Power supply and reference decoupling* updated, *Figure 30: Power supply and reference decoupling (VREF+ not connected to VDDA)* removed. Note modified in *Table 12: Maximum current consumption in Run mode, code with data processing running from Flash* and *Table 14: Maximum current consumption in Sleep mode, code running from Flash or RAM*. *Figure 15*, *Figure 16* and *Figure 17* show typical curves. ACC_{HSI} max values modified in *Table 23: HSI oscillator characteristics*. Small text changes.
24-Sep-2009	3	*Note 5* updated and *Note 4* added in *Table 4: Low-density STM32F101xx pin definitions*. V_{RERINT} and T_{Coeff} added to *Table 11: Embedded internal reference voltage*. Typical I_{DD_VBAT}value added in *Table 15: Typical and maximum current consumptions in Stop and Standby modes*. *Figure 14: Typical current consumption on VBAT with RTC on versus temperature at different VBAT values* added. f_{HSE_ext} min modified in *Table 19: High-speed external user clock characteristics*. C_{L1} and C_{L2} replaced by C in *Table 21: HSE 4-16 MHz oscillator characteristics* and *Table 22: LSE oscillator characteristics (fLSE = 32.768 kHz)*, notes modified and moved below the tables. *Note 1* modified below *Figure 20: Typical application with an 8 MHz crystal*. *Table 23: HSI oscillator characteristics* modified. Conditions removed from *Table 25: Low-power mode wakeup timings*. *Figure 27: Recommended NRST pin protection* modified. IEC 1000 standard updated to IEC 61000 and SAE J1752/3 updated to IEC 61967-2 in *Section 5.3.10: EMC characteristics on page 49*. Jitter added to *Table 26: PLL characteristics*. C_{ADC} and R_{AIN} parameters modified in *Table 41: ADC characteristics*. R_{AIN} max values modified in *Table 42: RAIN max for fADC = 14 MHz*. Small text changes.
20-May-2010	4	Added VFQFPN48 package. Updated note 2 below *Table 38: I2C characteristics* Updated *Figure 28: I2C bus AC waveforms and measurement circuit(1)* Updated *Figure 27: Recommended NRST pin protection* Updated *Section 5.3.12: I/O current injection characteristics*