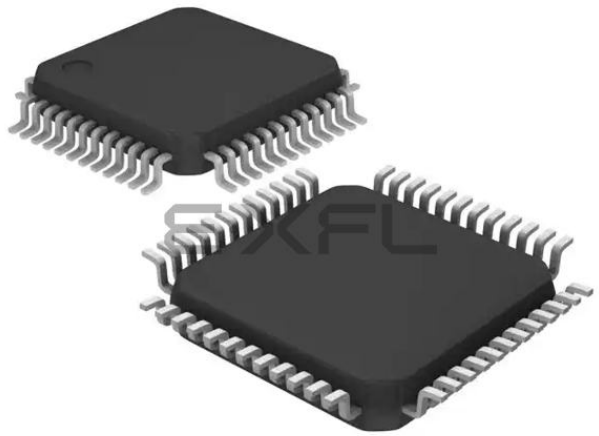

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	36MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	37
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f101c6t6atr

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F101x4 and STM32F101x6 low-density access line microcontrollers. For more details on the whole STMicroelectronics STM32F101xx family, please refer to *Section 2.2: Full compatibility throughout the family*.

The Low-density STM32F101xx datasheet should be read in conjunction with the low-, medium- and high-density STM32F10xxx reference manual.
For information on programming, erasing and protection of the internal Flash memory please refer to the *STM32F10xxx Flash programming manual.*
The reference and Flash programming manuals are both available from the STMicroelectronics website *www.st.com.*

For information on the Cortex®-M3 core please refer to the Cortex®-M3 Technical Reference Manual, available from the www.arm.com website.

2 Description

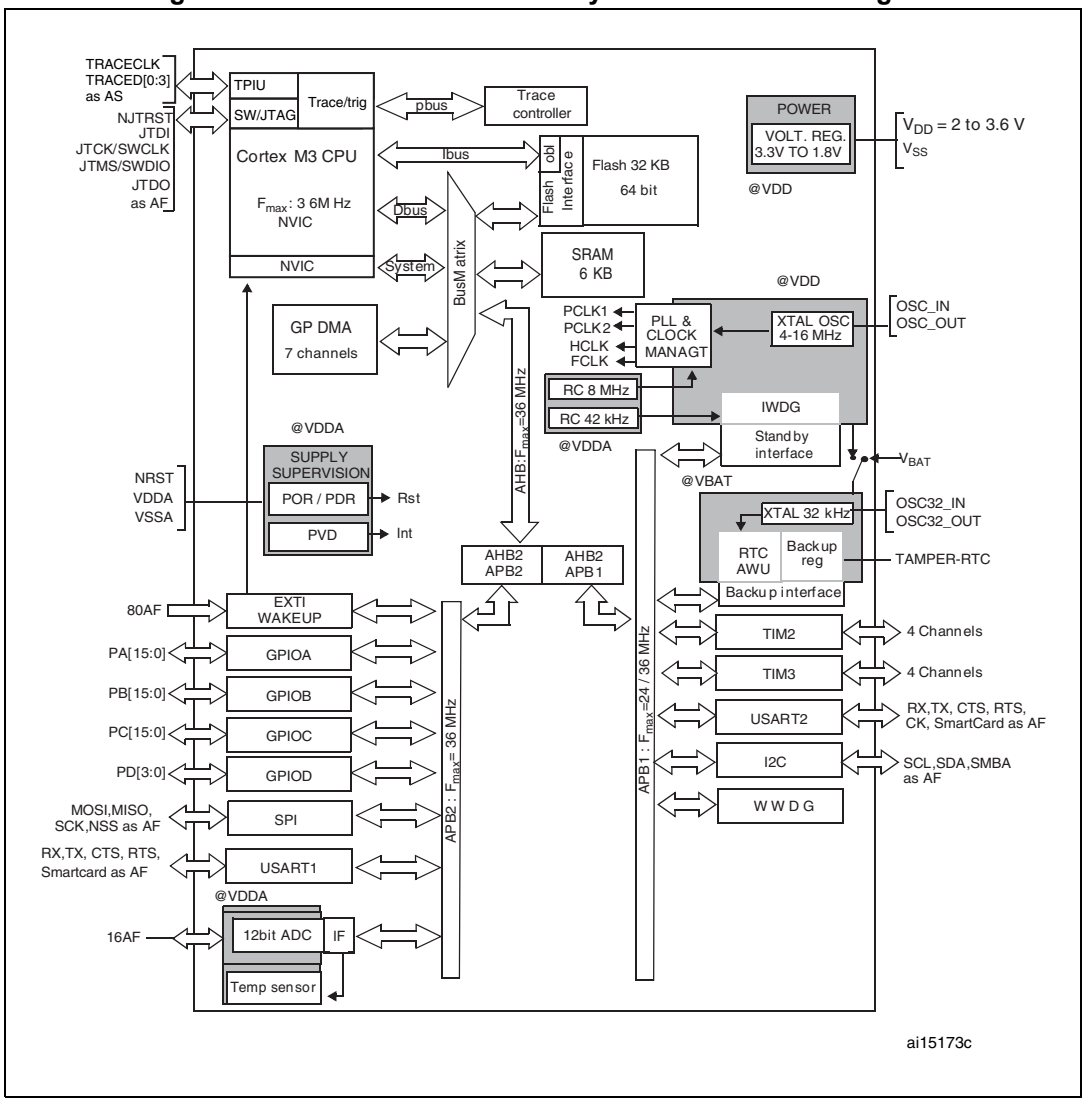
The STM32F101x4 and STM32F101x6 Low-density access line family incorporates the high-performance ARM Cortex®-M3 32-bit RISC core operating at a 36 MHz frequency, high-speed embedded memories (Flash memory of 16 to 32 Kbytes and SRAM of 4 to 6 Kbytes), and an extensive range of enhanced peripherals and I/Os connected to two APB buses. All devices offer standard communication interfaces (one I^2C, one SPI, and two USARTs), one 12-bit ADC and up to two general-purpose 16-bit timers.

The STM32F101xx Low-density access line family operates in the –40 to +85 °C temperature range, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F101xx Low-density access line family includes devices in three different packages ranging from 36 pins to 64 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the STM32F101xx Low-density access line microcontroller family suitable for a wide range of applications such as application control and user interface, medical and handheld equipment, PC peripherals, gaming and GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, Video intercoms, and HVACs.

Figure 1. STM32F101xx Low-density access line block diagram



1. AF = alternate function on I/O port pin.
2. T_A = –40 °C to +85 °C (junction temperature up to 105 °C).

3 Pinouts and pin description

Figure 3. STM32F101xx Low-density access line LQFP64 pinout

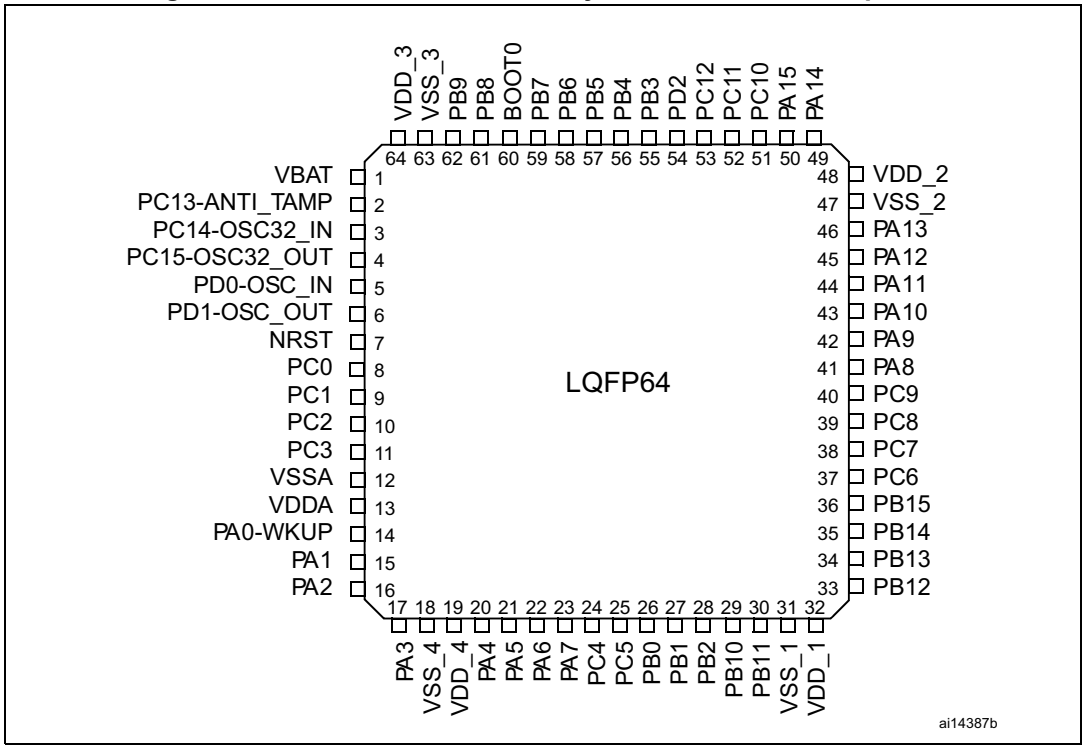
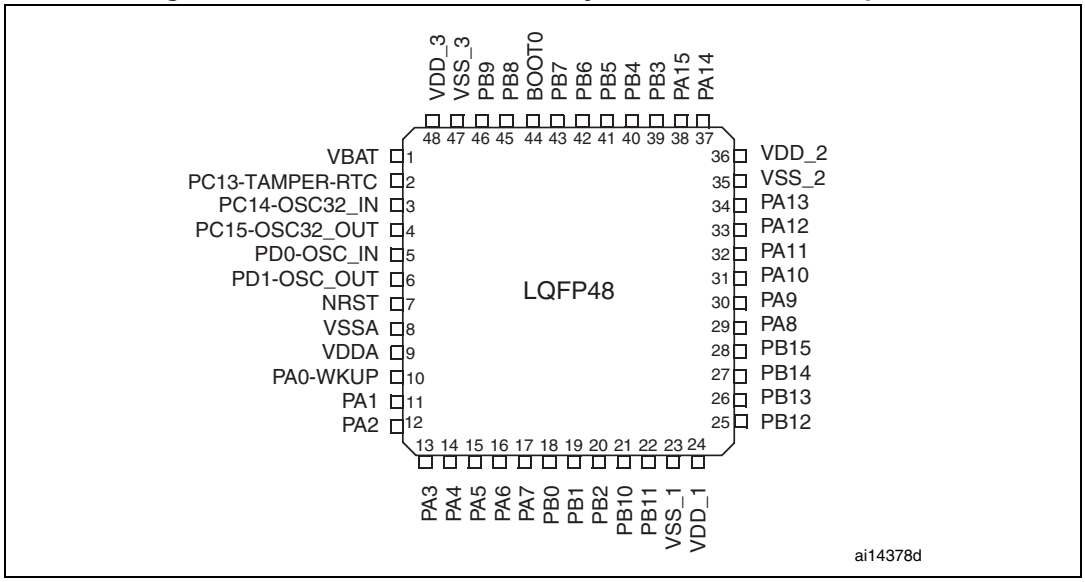


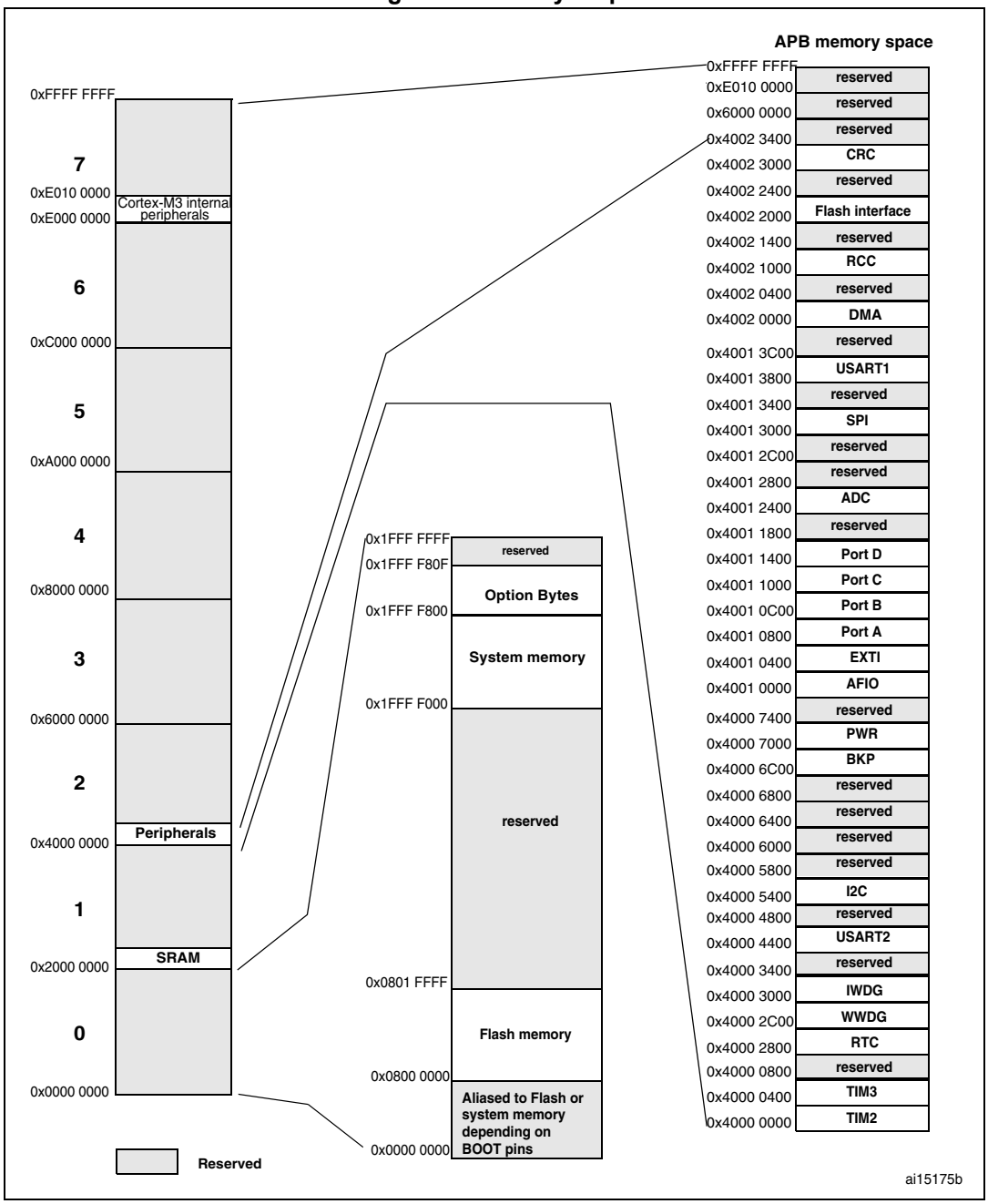
Figure 4. STM32F101xx Low-density access line LQFP48 pinout



4 Memory mapping

The memory map is shown in *Figure 7*.

Figure 7. Memory map



Typical current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except if it is explicitly mentioned
- The Flash access time is adjusted to f_{HCLK} frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 36 MHz)
- Prefetch is on (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK1} = f_{HCLK/4}$, $f_{PCLK2} = f_{HCLK/2}$, $f_{ADCCLK} = f_{PCLK2}/4$

The parameters given in *Table 16* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 16. Typical current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1) All peripherals enabled(2)	Typ(1) All peripherals disabled	Unit
I_{DD}	Supply current in Run mode	External clock(3)	36 MHz	17.2	13.8	mA
			24 MHz	11.2	8.9	
			16 MHz	8.1	6.6	
			8 MHz	5	4.2	
			4 MHz	3	2.6	
			2 MHz	2	1.8	
			1 MHz	1.5	1.4	
			500 kHz	1.2	1.2	
			125 kHz	1.05	1	
		Running on high speed internal RC (HSI), AHB prescaler used to reduce the frequency	36 MHz	16.5	13.1	
			24 MHz	10.5	8.2	
			16 MHz	7.4	5.9	
			8 MHz	4.3	3.6	
			4 MHz	2.4	2	
			2 MHz	1.5	1.3	
			1 MHz	1	0.9	
			500 kHz	0.7	0.65	
			125 kHz	0.5	0.45	

1. Typical values are measures at T_A = 25 °C, V_{DD} = 3.3 V.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 18. Peripheral current consumption

Peripheral		Typical consumption at 25 °C	Unit
AHB (up to 36 MHz)	DMA1	15.97	µA/MHz
	CRC	1.67	
	BusMatrix(1)	8.33	
APB1 (up to 18 MHz)	APB1-Bridge	7.22	
	TIM2	33.33	
	TIM3	33.61	
	USART2	12.78	
	I2C1	10.83	
	WWDG	3.33	
	PWR	1.94	
	BKP	2.78	
	IWDG	1.39	
APB2 (up to 36 MHz)	APB2-Bridge	3.33	
	GPIO A	7.50	
	GPIO B	6.81	
	GPIO C	7.22	
	GPIO D	6.94	
	SPI1	4.86	
	USART1	12.78	
	ADC1(2)	15.54	

1. The BusMatrix is automatically active when at least one master is ON. (CPU, DMA1).
2. Specific conditions for measuring ADC current consumption: f_{HCLK} = 28 MHz, $f_{APB1} = f_{HCLK}$, $f_{APB2} = f_{HCLK}$, $f_{ADCCLK} = f_{APB2} / 2$. When ADON bit in the ADC_CR2 register is set to 1, a current consumption of analog part equal to 0.7 mA must be added.

5.3.6 External clock source characteristics

High-speed external user clock generated from an external source

The characteristics given in *Table 19* result from tests performed using an high-speed external clock source, and under the ambient temperature and supply voltage conditions summarized in *Table 8*.

Figure 18. High-speed external clock source AC timing diagram

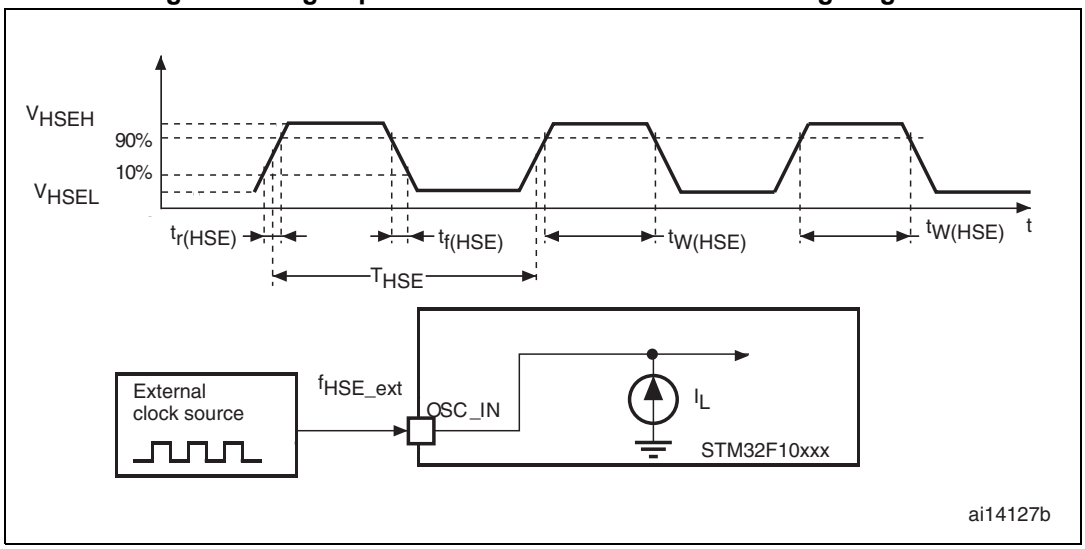
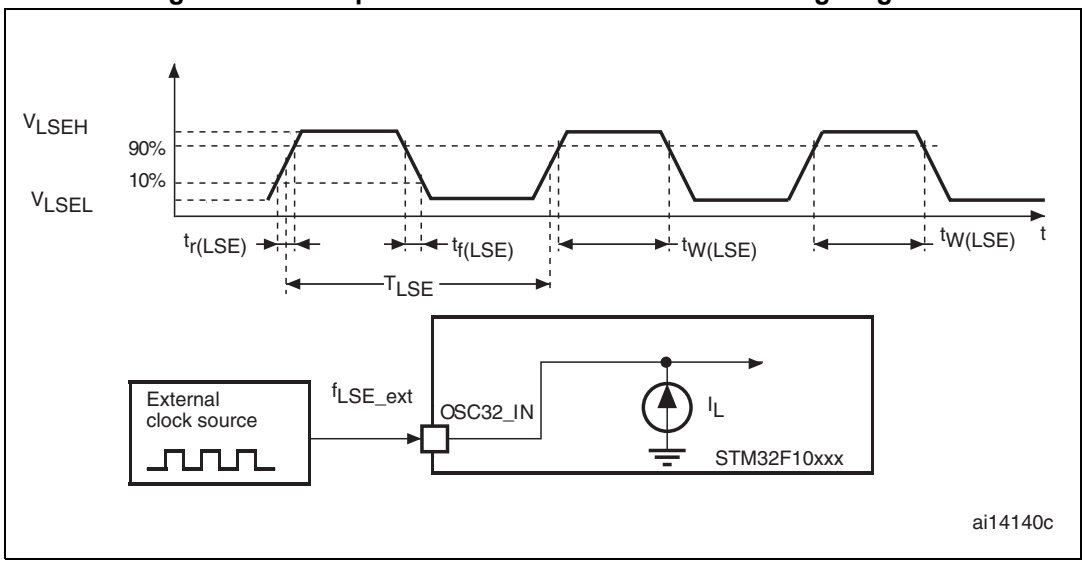


Figure 19. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 21*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

5.3.13 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 33* are derived from tests performed under the conditions summarized in *Table 8*. All I/Os are CMOS and TTL compliant.

Table 33. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Standard IO input low level voltage	-	-0.3	-	0.28*(V_{DD}-2 V)+0.8 V(1)	V
	IO FT(2) input low level voltage		-0.3	-	0.32*(V_{DD}-2 V)+0.75 V(1)	
V_{IH}	Standard IO input high level voltage	-	0.41*(V_{DD}-2 V)+1.3 V(1)	-	V_{DD}+0.3	
	IO FT(2) input high level voltage	V_{DD} > 2 V	0.42*(V_{DD}-2 V)+1 V(1)	-	5.5	
		V_{DD} ≤ 2 V			5.2	
V_{hys}	Standard IO Schmitt trigger voltage hysteresis(3)	-	200	-	-	mV
	IO FT Schmitt trigger voltage hysteresis(3)	-	5% V_{DD}(4)	-	-	
I_{lkg}	Input leakage current (5)	V_{SS} ≤ V_{IN} ≤ V_{DD} Standard I/Os	-	-	±1	µA
		V_{IN} = 5 V I/O FT	-	-	3	
R_{PU}	Weak pull-up equivalent resistor(6)	V_{IN} = V_{SS}	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistor(6)	V_{IN} = V_{DD}	30	40	50	
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Data based on design simulation.
2. FT = Five-volt tolerant. In order to sustain a voltage higher than V_{DD}+0.3 the internal pull-up/pull-down resistors must be disabled.
3. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization, not tested in production.
4. With a minimum of 100 mV.
5. Leakage could be higher than max. if negative current is injected on adjacent pins.
6. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimum (~10% order).

Figure 24. 5 V tolerant I/O input characteristics - CMOS port

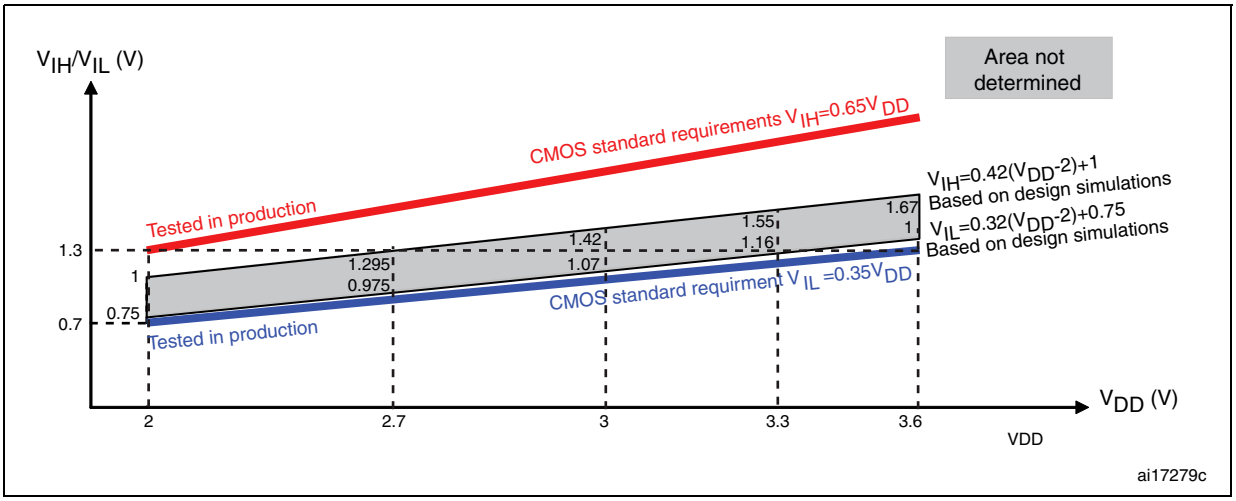


Figure 25. 5 V tolerant I/O input characteristics - TTL port

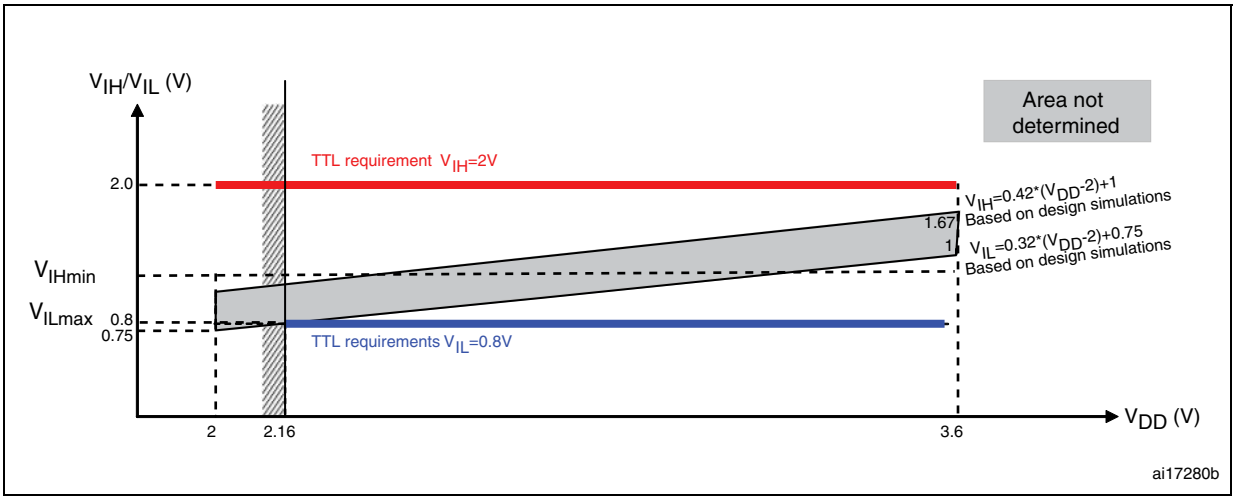
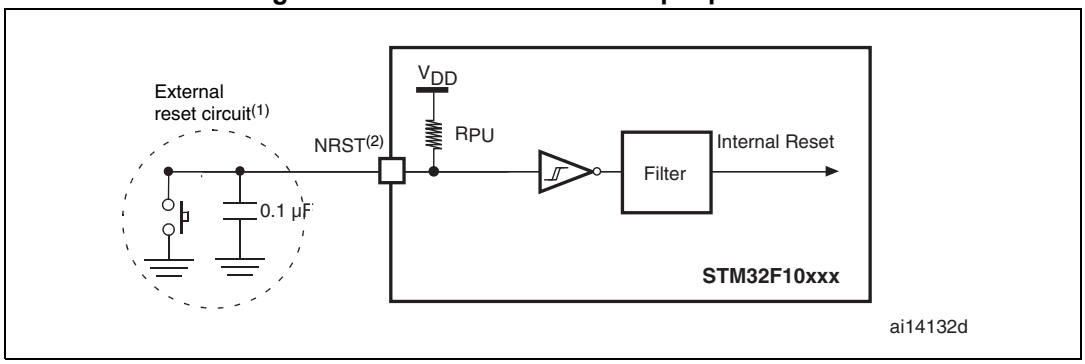


Figure 27. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 36*. Otherwise the reset will not be taken into account by the device.

5.3.15 TIM timer characteristics

The parameters given in *Table 37* are guaranteed by design.

Refer to *Section 5.3.12: I/O current injection characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 37. TIMx(1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 36 MHz	27.8	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4		0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 36 MHz	0	18	MHz
Res_{TIM}	Timer resolution	-	-	16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 36 MHz	0.0278	1820	µs
t_{MAX_COUNT}	Maximum possible count	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 36 MHz	-	119.2	s

1. TIMx is used as a general term to refer to the TIM2, TIM3 and TIM4 timers.

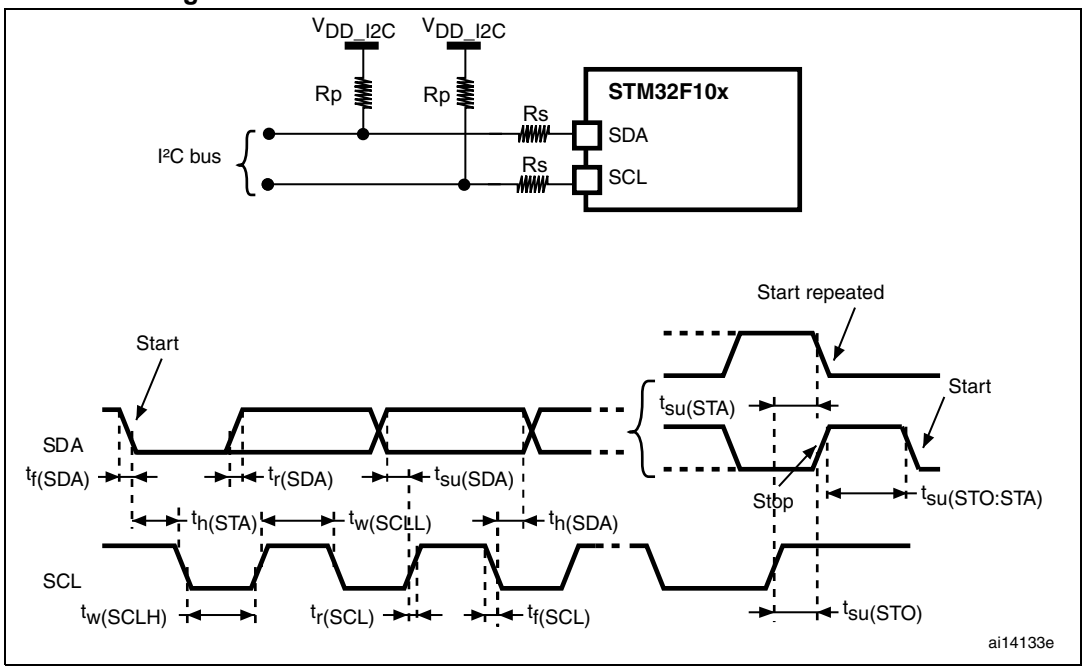
5.3.16 Communications interfaces

I^2C interface characteristics

The STM32F101xx Low-density access line I^2C interface meets the requirements of the standard I^2C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

The I^2C characteristics are described in *Table 38*. Refer also to *Section 5.3.12: I/O current injection characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

Figure 28. I²C bus AC waveforms and measurement circuit(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.
2. Rs = Series protection resistors, Rp = Pull-up resistors, V_{DD_I2C} = I2C bus supply.

Table 39. SCL frequency (f_{PCLK1}= MHz, V_{DD_I2C} = 3.3 V)(1)(2)

f_{SCL} (kHz)	I2C_CCR value
	R_P = 4.7 kΩ
400	0x801E
300	0x8028
200	0x803C
100	0x00B4
50	0x0168
20	0x0384

1. R_P = External pull-up resistance, f_{SCL} = I²C speed,
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed ±2%. These variations depend on the accuracy of the external components used to design the application.

Equation 1: R_{AIN} max formula:

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 42. R_{AIN} max for f_{ADC} = 14 MHz(1)

T_s (cycles)	t_S (µs)	R_{AIN} max (kΩ)
1.5	0.11	0.4
7.5	0.54	5.9
13.5	0.96	11.4
28.5	2.04	25.2
41.5	2.96	37.2
55.5	3.96	50
71.5	5.11	NA
239.5	17.1	NA

1. Guaranteed by design, not tested in production.

Table 43. ADC accuracy - limited test conditions(1) (2)

Symbol	Parameter	Test conditions	Typ	Max(3)	Unit
ET	Total unadjusted error	f_{PCLK2} = 28 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 3 V to 3.6 V T_A = 25 °C Measurements made after ADC calibration	±1.3	±2	LSB
EO	Offset error		±1	±1.5	
EG	Gain error		±0.5	±1.5	
ED	Differential linearity error		±0.7	±1	
EL	Integral linearity error		±0.8	±1.5	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 5.3.12* does not affect the ADC accuracy.
3. Based on characterization, not tested in production.

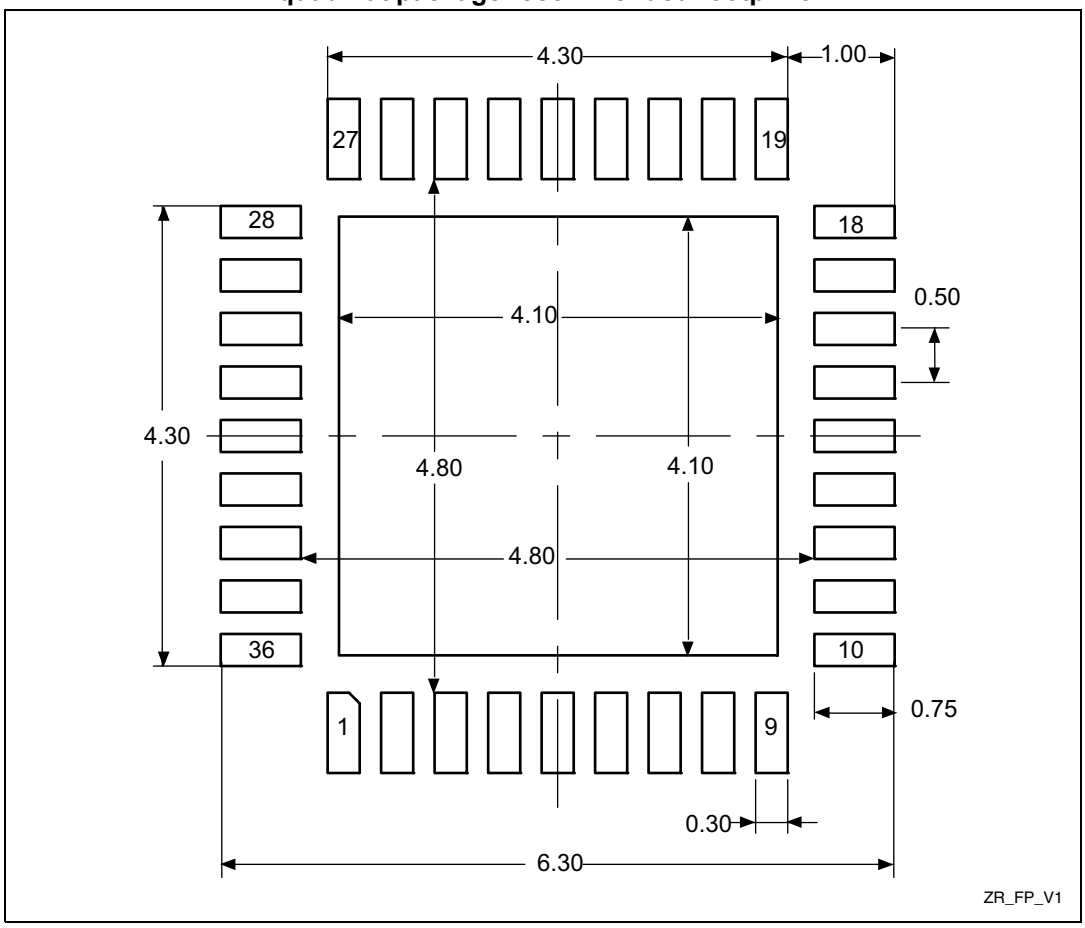
5.3.18 Temperature sensor characteristics

Table 45. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	4.0	4.3	4.6	mV/°C
V_{25}(1)	Voltage at 25°C	1.34	1.43	1.52	V
t_{START}(2)	Startup time	4	-	10	µs
T_{S_temp}(3)(2)	ADC sampling time when reading the temperature	-	-	17.1	µs

1. Guaranteed by characterization, not tested in production.
2. Guaranteed by design, not tested in production.
3. Shortest sampling time can be determined in the application by multiple iterations.

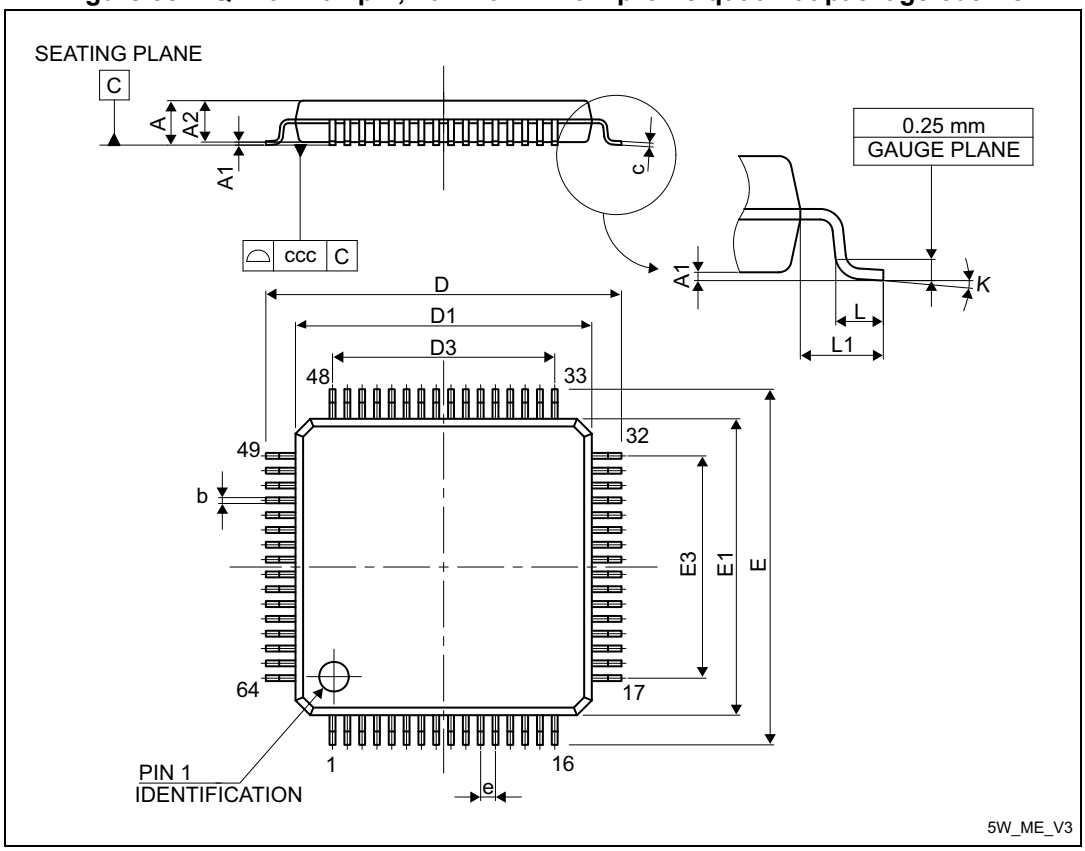
Figure 36. VFQFPN36 - 36-pin, 6x6 mm, 0.5 mm pitch very thin profile fine pitch quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

6.3 LQFP64 package information

Figure 38. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 47. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-

6.5.2 Evaluating the maximum junction temperature for an application

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Table 50: Ordering information scheme*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature. Here, only temperature range 6 is available (–40 to 85 °C).

The following example shows how to calculate the temperature range needed for a given application, making it possible to check whether the required temperature range is compatible with the STM32F101xx junction temperature range.

Example: high-performance application

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 8 I/Os used at the same time in output mode at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

P_{INTmax} = 50 mA × 3.5 V= 175 mW

P_{IOmax} = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW

P_{Dmax} = 175 + 272 = 447 mW

Thus: P_{Dmax} = 447 mW

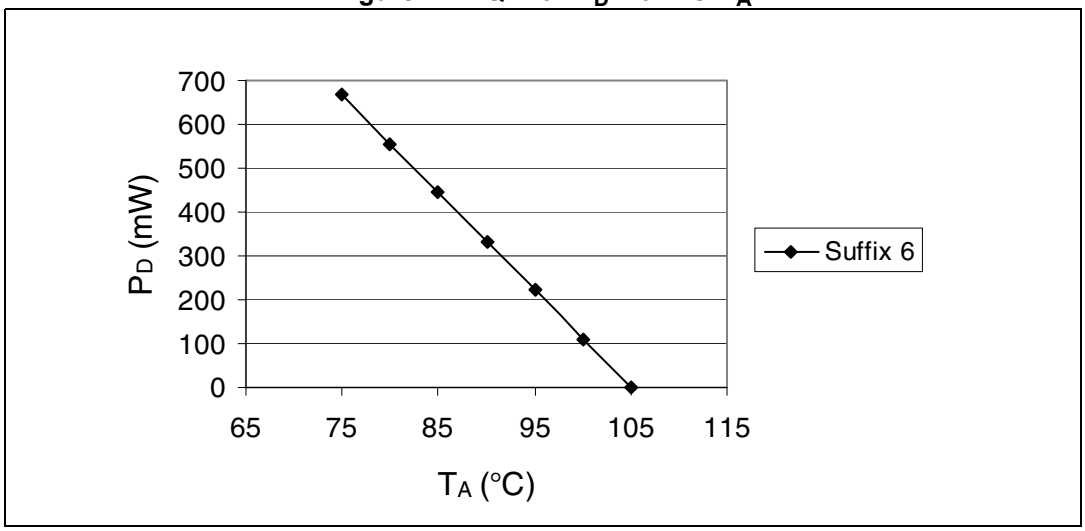
Using the values obtained in *Table 49* T_{Jmax} is calculated as follows:

– For LQFP64, 45 °C/W

T_{Jmax} = 82 °C + (45 °C/W × 447 mW) = 82 °C + 20.1 °C = 102.1 °C

This is within the junction temperature range of the STM32F101xx (–40 < T_J < 105 °C).

Figure 44. LQFP64 P_D max vs. T_A



7 Ordering information scheme

Table 50. Ordering information scheme

Example: STM32 F 101 C 4 T 6 A xxx

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = general-purpose

Device subfamily

101 = access line

Pin count

T = 36 pins

C = 48 pins

R = 64 pins

Flash memory size

4 = 16 Kbytes of Flash memory

6 = 32 Kbytes of Flash memory

Package

T = LQFP

U = VFQFPN

Temperature range

6 = Industrial temperature range, –40 to 85 °C.

Internal code

“A” or blank(1)

Options

xxx = programmed parts

TR = tape and real

1. For STM32F101x6 devices with a blank internal code, please refer to the STM32F103x6/8/B datasheet available from the ST website: www.st.com.

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact the nearest ST sales office.