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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	36MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	51
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f101r4t6a

Contents

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, general purpose timers TIMx and ADC.

2.3.14 RTC (real-time clock) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are ten 16-bit registers used to store 20 bytes of user application data when V_{DD} power is not present.

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a periodic interrupt. It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low power RC oscillator or the high-speed external clock divided by 128. The internal low power RC has a typical frequency of 40 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural crystal deviation. The RTC features a 32-bit programmable counter for long term measurement using the Compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

2.3.15 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

2.3.16 Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

2.3.17 SysTick timer

This timer is dedicated for OS, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

2.3.18 General-purpose timers (TIMx)

There areup to two synchronizable general-purpose timers embedded in the STM32F101xx Low-density access line devices. These timers are based on a 16-bit auto-reload up/down counter, a 16-bit prescaler and feature 4 independent channels each for input capture,

Table 4. Low-density STM32F101xx pin definitions (continued)

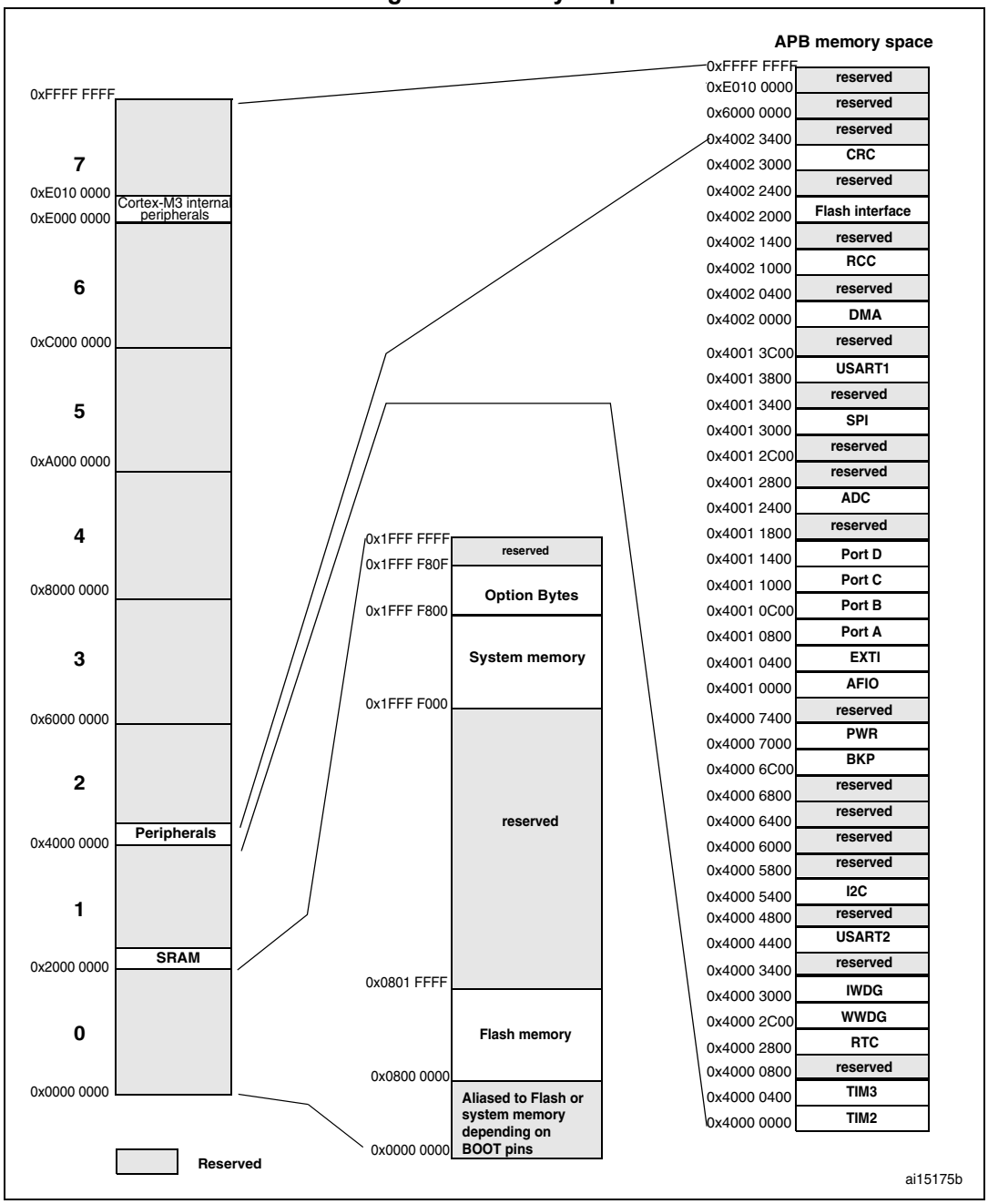
Pins			Pin name	Type[1]	I / O level[2]	Main function[3] (after reset)	Alternate functions[3][4]	
LQFP48	LQFP64	VFQFPN36					Default	Remap
37	49	28	PA14	I/O	FT	JTCK/SWCLK	-	PA14
38	50	29	PA15	I/O	FT	JTDI	-	TIM2_CH1_ETR/ PA15 / SPI_NSS
-	51	-	PC10	I/O	FT	PC10	-	-
-	52	-	PC11	I/O	FT	PC11	-	-
-	53	-	PC12	I/O	FT	PC12	-	-
5	5	2	PD0	I/O	FT	OSC_IN[8]	-	-
6	6	3	PD1	I/O	FT	OSC_OUT[8]	-	-
-	54	-	PD2	I/O	FT	PD2	TIM3_ETR	-
39	55	30	PB3	I/O	FT	JTDO	-	TIM2_CH2 / PB3 TRACESWO SPI_SCK
40	56	31	PB4	I/O	FT	NJTRST	-	TIM3_CH1 / PB4 SPI_MISO
41	57	32	PB5	I/O	-	PB5	I2C_SMBA	TIM3_CH2 / SPI_MOSI
42	58	33	PB6	I/O	FT	PB6	I2C_SCL[7]	USART1_TX
43	59	34	PB7	I/O	FT	PB7	I2C_SDA[7]	USART1_RX
44	60	35	BOOT0	I	-	BOOT0	-	-
45	61	-	PB8	I/O	FT	PB8	-	I2C_SCL
46	62	-	PB9	I/O	FT	PB9	-	I2C_SDA
47	63	36	V_{SS_3}	S	-	V_{SS_3}	-	-
48	64	1	V_{DD_3}	S	-	V_{DD_3}	-	-

1. I = input, O = output, S = supply.
2. FT= 5 V tolerant.
3. Function availability depends on the chosen device. For devices having reduced peripheral counts, it is always the lower number of peripherals that is included. For example, if a device has only one SPI, two USARTs and two timers, they will be called SPI, USART1 & USART2 and TIM2 & TIM 3, respectively. Refer to *Table 2 on page 11*.
4. If several peripherals share the same I/O pin, to avoid conflict between these alternate functions only one peripheral should be enabled at a time through the peripheral clock enable bit (in the corresponding RCC peripheral clock enable register).
5. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited: the speed should not exceed 2 MHz with a maximum load of 30 pF and these IOs must not be used as a current source (e.g. to drive an LED).

4 Memory mapping

The memory map is shown in *Figure 7*.

Figure 7. Memory map



5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V (for the 2 V ≤ V_{DD} ≤ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 8*.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 9*.

Table 10. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.1	2.18	2.26	V
		PLS[2:0]=000 (falling edge)	2	2.08	2.16	
		PLS[2:0]=001 (rising edge)	2.19	2.28	2.37	
		PLS[2:0]=001 (falling edge)	2.09	2.18	2.27	
		PLS[2:0]=010 (rising edge)	2.28	2.38	2.48	
		PLS[2:0]=010 (falling edge)	2.18	2.28	2.38	
		PLS[2:0]=011 (rising edge)	2.38	2.48	2.58	
		PLS[2:0]=011 (falling edge)	2.28	2.38	2.48	
		PLS[2:0]=100 (rising edge)	2.47	2.58	2.69	
		PLS[2:0]=100 (falling edge)	2.37	2.48	2.59	
		PLS[2:0]=101 (rising edge)	2.57	2.68	2.79	
		PLS[2:0]=101 (falling edge)	2.47	2.58	2.69	
		PLS[2:0]=110 (rising edge)	2.66	2.78	2.9	
		PLS[2:0]=110 (falling edge)	2.56	2.68	2.8	
		PLS[2:0]=111 (rising edge)	2.76	2.88	3	
		PLS[2:0]=111 (falling edge)	2.66	2.78	2.9	
$V_{PVDhyst}$(2)	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1.8(1)	1.88	1.96	V
		Rising edge	1.84	1.92	2.0	
$V_{PDRhyst}$(2)	PDR hysteresis	-	-	40	-	mV
$t_{RSTTEMPO}$(2)	Reset temporization	-	1.5	2.5	4.5	ms

1. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
2. Guaranteed by design, not tested in production.

Figure 14. Typical current consumption on V_{BAT} with RTC on versus temperature at different V_{BAT} values

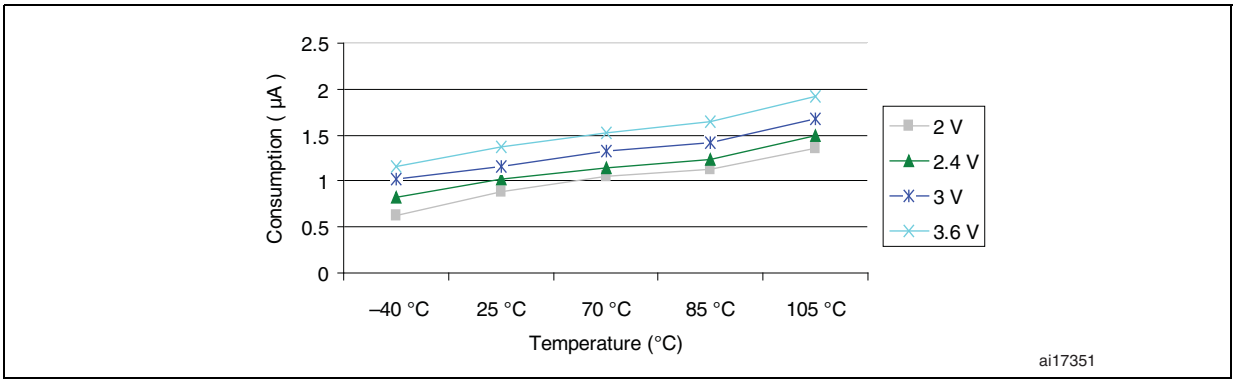


Figure 15. Typical current consumption in Stop mode with regulator in Run mode versus temperature at V_{DD} = 3.3 V and 3.6 V

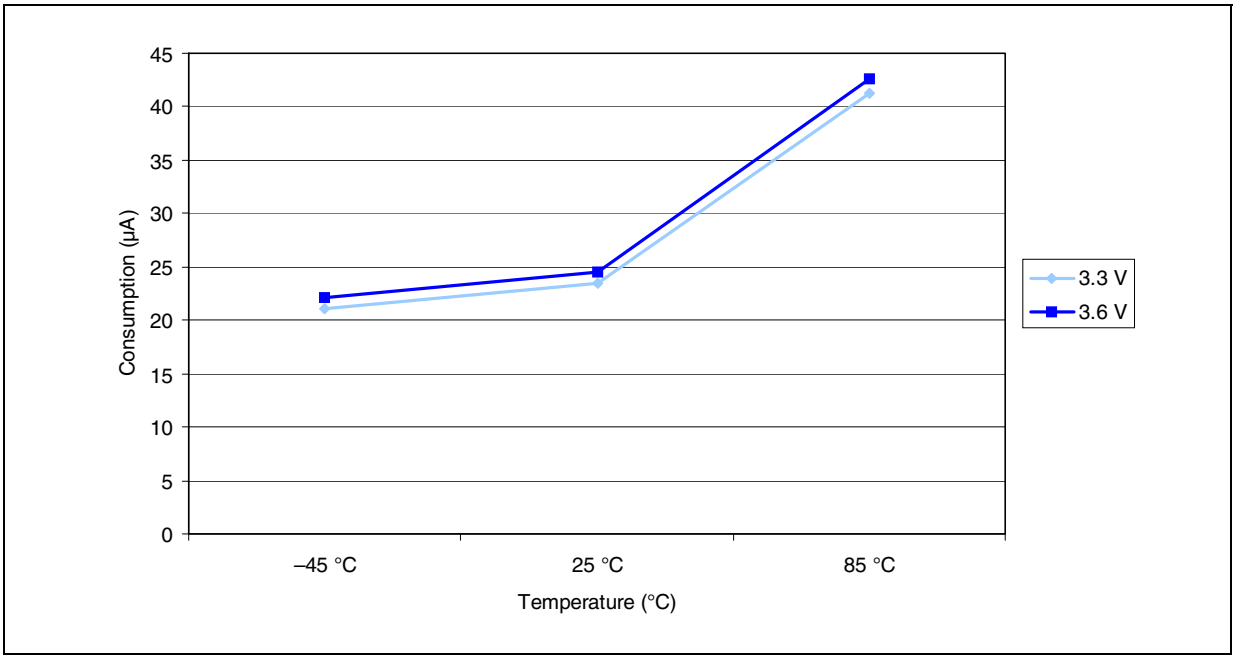


Figure 16. Typical current consumption in Stop mode with regulator in Low-power mode versus temperature at V_{DD} = 3.3 V and 3.6 V

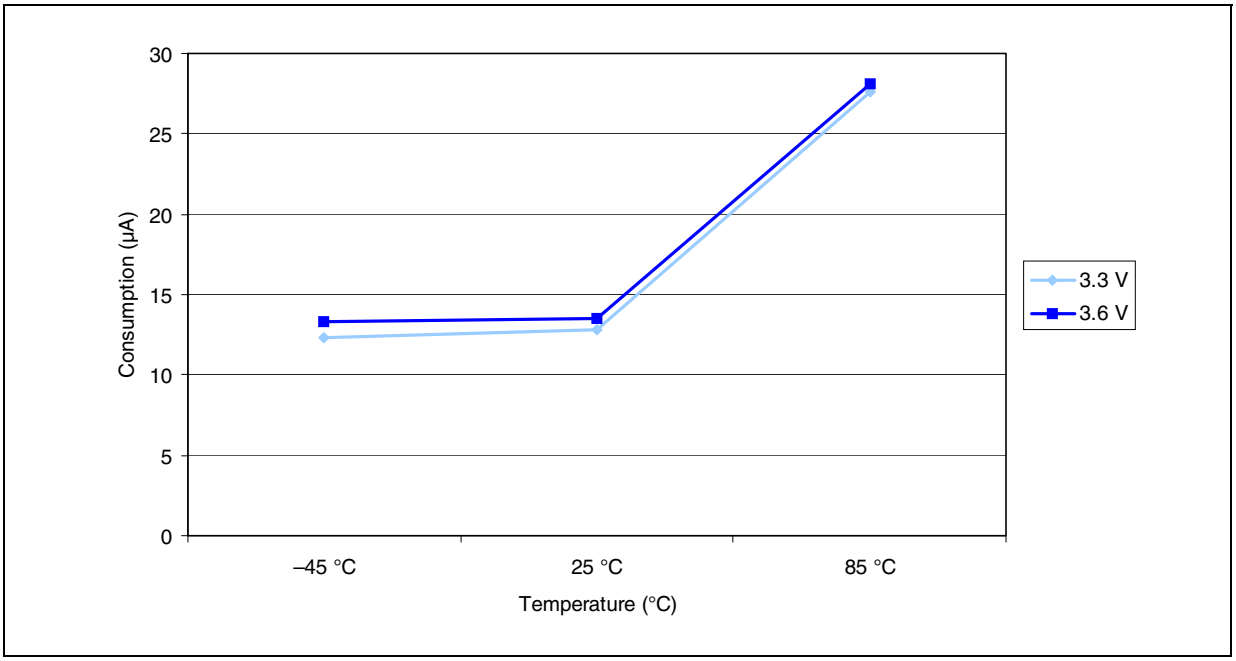


Figure 17. Typical current consumption in Standby mode versus temperature at V_{DD} = 3.3 V and 3.6 V

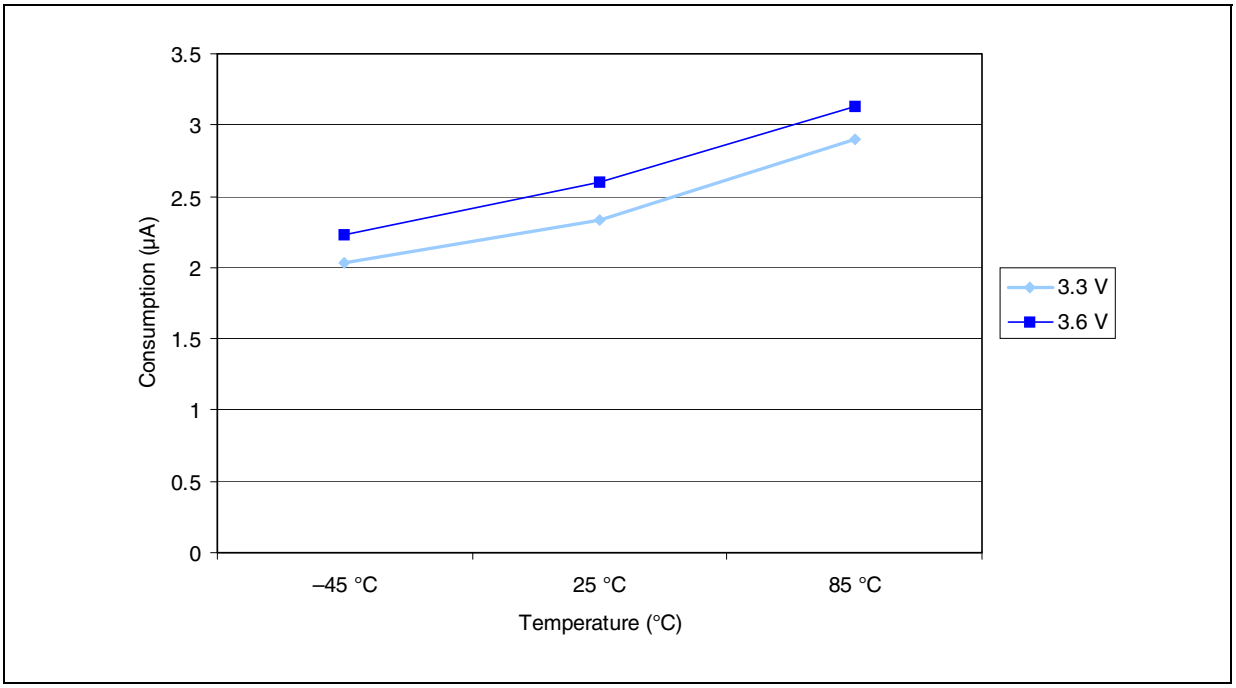


Figure 18. High-speed external clock source AC timing diagram

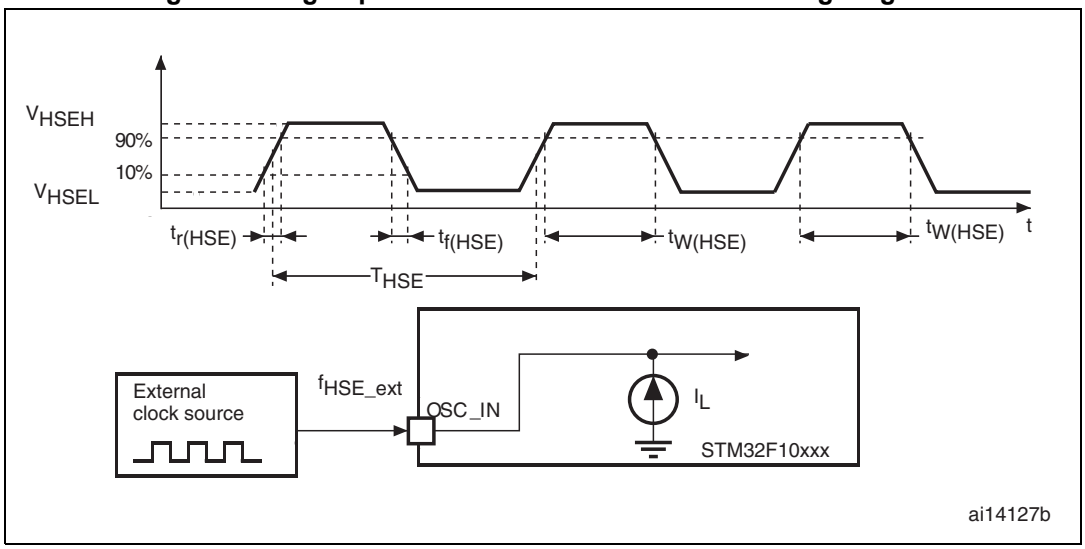
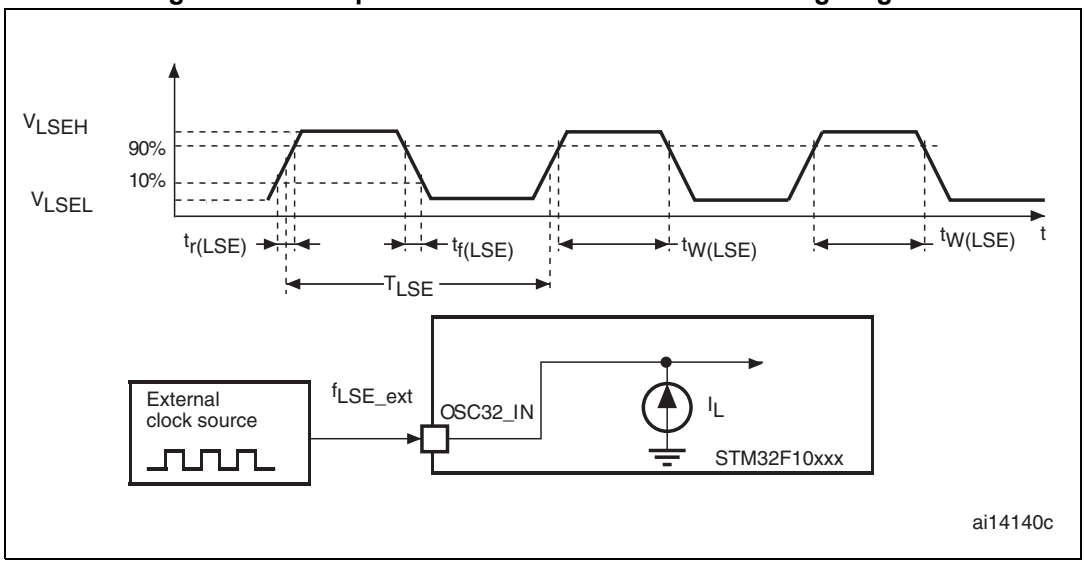


Figure 19. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 21*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 22. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1) (2)

Symbol	Parameter	Conditions	-	Min	Typ	Max	Unit
R_F	Feedback resistor	-	-	-	5	-	MΩ
C	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)	R_S = 30 KΩ	-	-	-	15	pF
I_2	LSE driving current	V_{DD} = 3.3 V V_{IN} = V_{SS}	-	-	-	1.4	µA
g_m	Oscillator transconductance	-	-	5	-	-	µA/V
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	T_A = 50 °C	-	1.5	-	s
			T_A = 25 °C	-	2.5	-	
			T_A = 10 °C	-	4	-	
			T_A = 0 °C	-	6	-	
			T_A = -10 °C	-	10	-	
			T_A = -20 °C	-	17	-	
			T_A = -30 °C	-	32	-	
			T_A = -40 °C	-	60	-	

1. Based on characterization, not tested in production.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

Note: For CL1 and CL2 it is recommended to use high-quality ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator. CL1 and CL2, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of CL1 and CL2.
Load capacitance CL *has the following formula:* CL = CL1 *x* CL2 */ (*CL1 + CL2*) +* C_{stray} *where* C_{stray} *is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.*

Caution: To avoid exceeding the maximum value of CL1 and CL2 (15 pF) it is strongly recommended to use a resonator with a load capacitance CL ≤7 pF. Never use a resonator with a load capacitance of 12.5 pF.
Example: if resonator with a load capacitance of CL = 6 pF, and C_{stray} = 2 pF is chosen, then CL1 = CL2 = 8 pF.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation).

The test results are given in *Table 32*

Table 32. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on OSC_IN32, OSC_OUT32, PA4, PA5, PC13	-0	+0	mA
	Injected current on all FT pins	-5	+0	
	Injected current on any other pin	-5	+5	

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 22* and *Figure 23* for standard I/Os, and in *Figure 24* and *Figure 25* for 5 V tolerant I/Os.

Figure 22. Standard I/O input characteristics - CMOS port

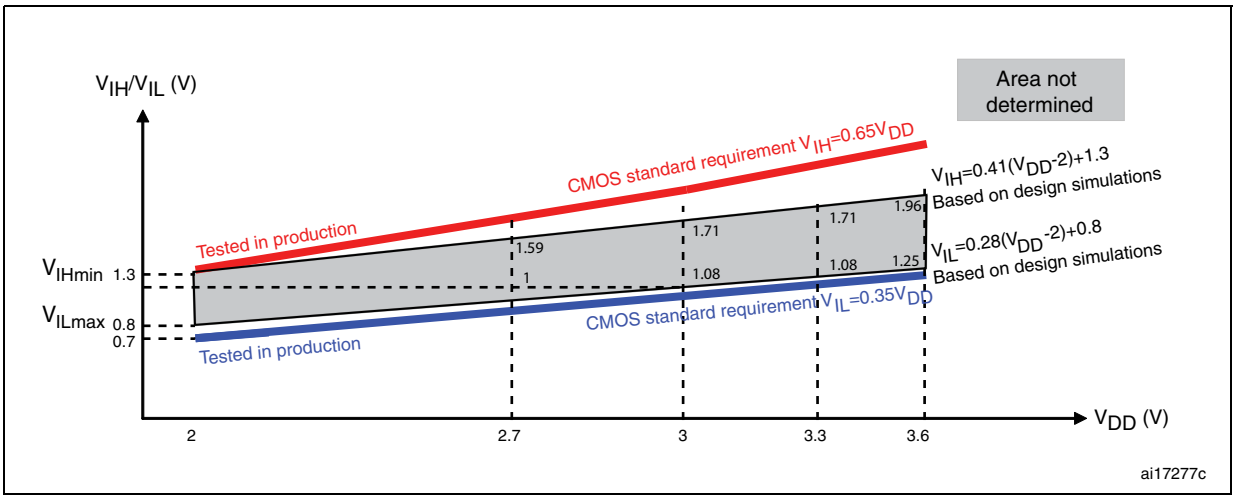


Figure 23. Standard I/O input characteristics - TTL port

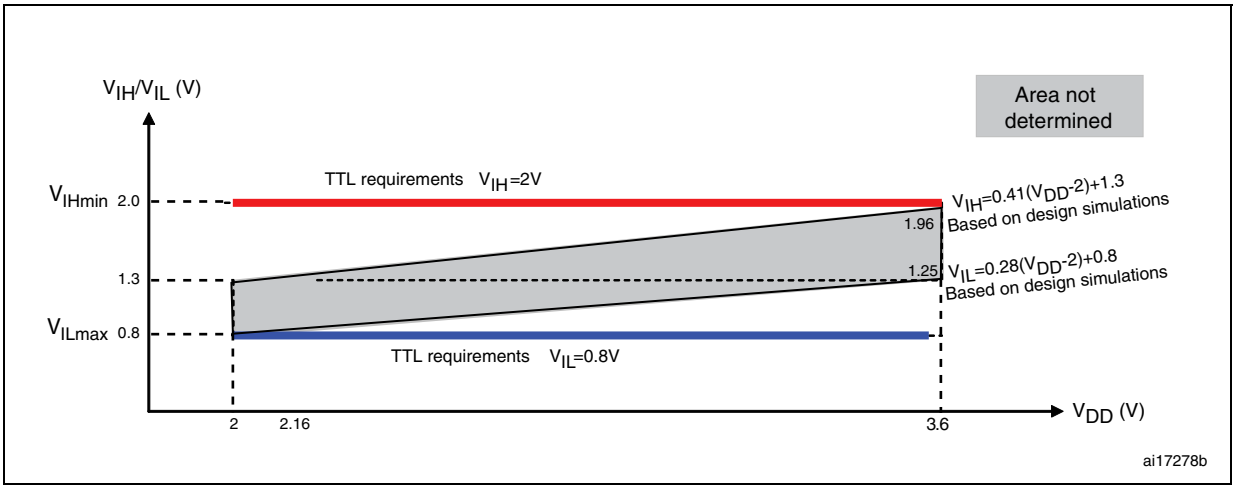
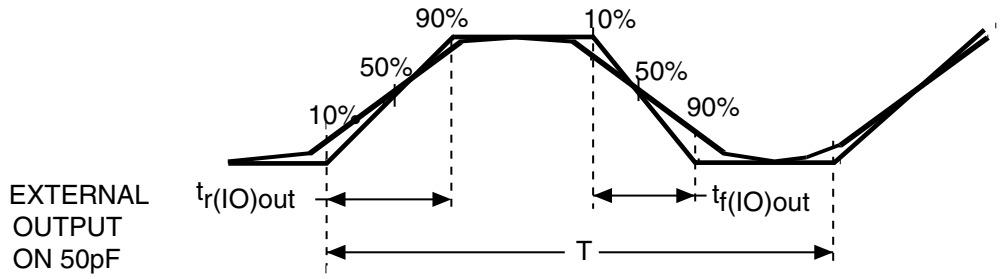


Figure 26. I/O AC characteristics definition



Maximum frequency is achieved if $(t_r + t_f) \leq 2/3)T$ and if the duty cycle is (45-55%) when loaded by 50pF

ai14131

5.3.14 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 33*).

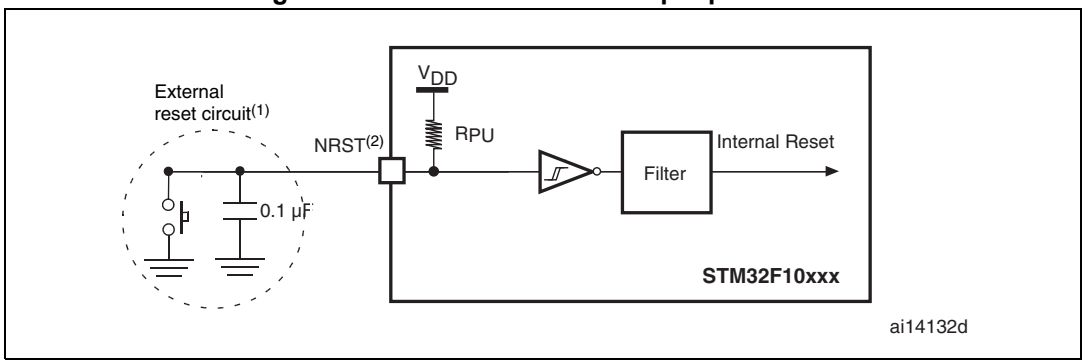
Unless otherwise specified, the parameters given in *Table 36* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 36. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST Input low level voltage	-	–0.5	-	0.8	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage	-	2	-	V_{DD}+0.5	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$(1)	NRST Input filtered pulse	-	-	-	100	ns
$V_{NF(NRST)}$(1)	NRST Input not filtered pulse	-	300	-	-	ns

1. Guaranteed by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

Figure 27. Recommended NRST pin protection

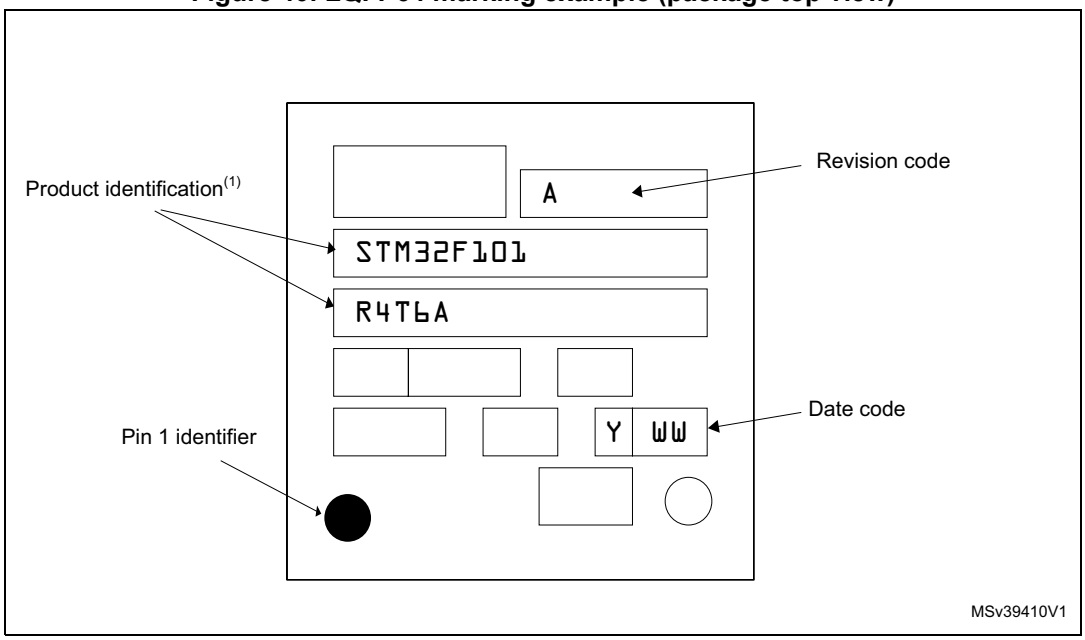


1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 36*. Otherwise the reset will not be taken into account by the device.

Device Marking for LQFP64

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

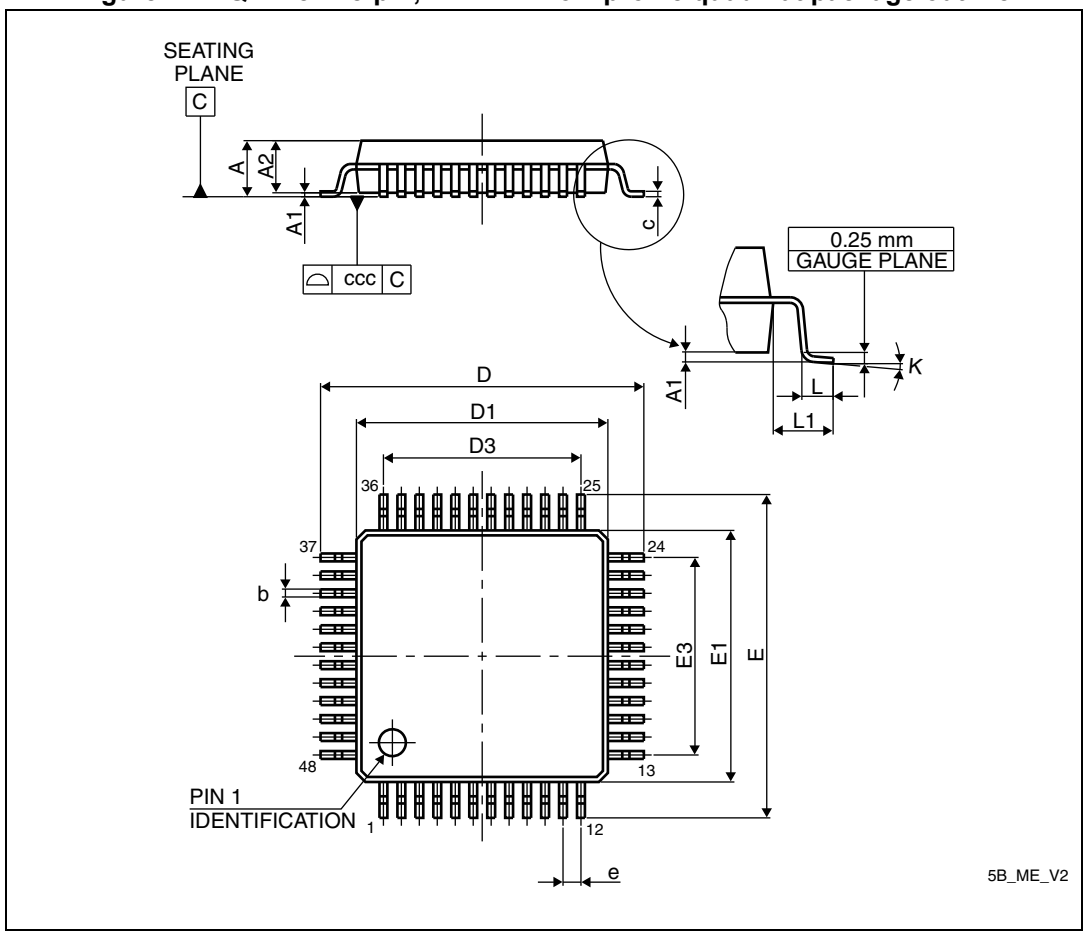
Figure 40. LQFP64 marking example (package top view)



1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

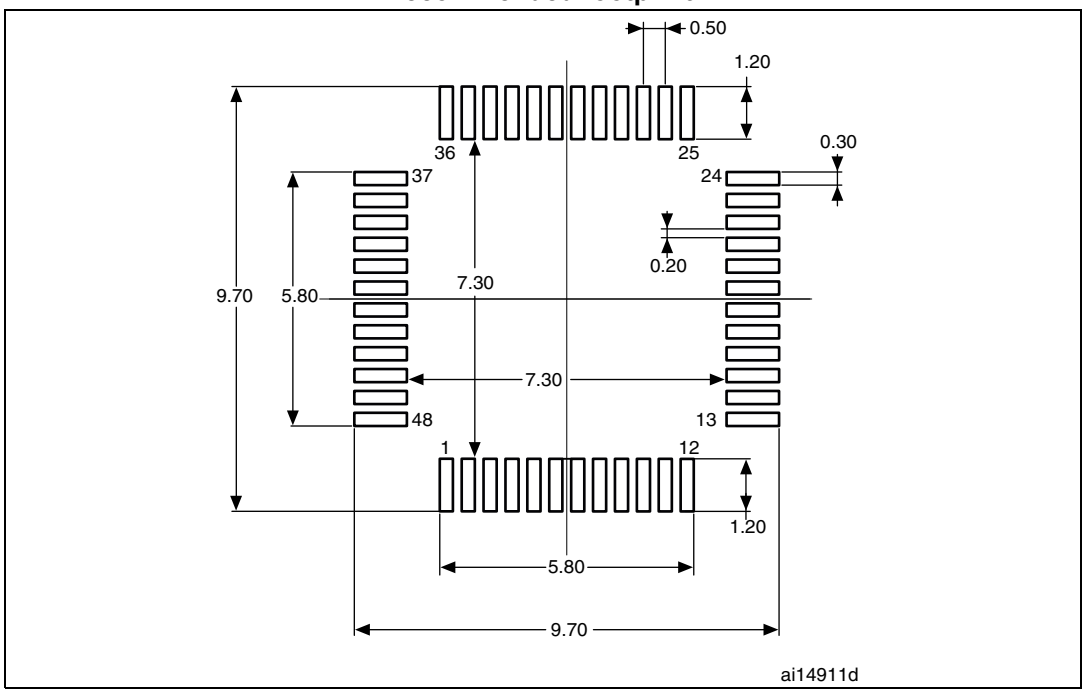
6.4 LQFP48 package information

Figure 41. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline



1. Drawing is not to scale.

Figure 42. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

7 Ordering information scheme

Table 50. Ordering information scheme

Example: STM32 F 101 C 4 T 6 A xxx

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = general-purpose

Device subfamily

101 = access line

Pin count

T = 36 pins

C = 48 pins

R = 64 pins

Flash memory size

4 = 16 Kbytes of Flash memory

6 = 32 Kbytes of Flash memory

Package

T = LQFP

U = VFQFPN

Temperature range

6 = Industrial temperature range, –40 to 85 °C.

Internal code

“A” or blank(1)

Options

xxx = programmed parts

TR = tape and real

1. For STM32F101x6 devices with a blank internal code, please refer to the STM32F103x6/8/B datasheet available from the ST website: www.st.com.

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact the nearest ST sales office.

8 Revision history

Table 51. Document revision history

Date	Revision	Changes
23-Sep-2008	1	Initial release.
07-Apr-2009	2	I/O information clarified *on page 1*. *Figure 7: Memory map* modified. In *Table 4: Low-density STM32F101xx pin definitions*: PB4, PB13, PB14, PB15, PB3/TRACESWO moved from Default column to Remap column. V_{REF-} is not available in the offered packages: *Figure 1: STM32F101xx Low-density access line block diagram*, *Figure 10: Power supply scheme* and *Figure 34: Power supply and reference decoupling* updated, *Figure 30: Power supply and reference decoupling (VREF+ not connected to VDDA)* removed. Note modified in *Table 12: Maximum current consumption in Run mode, code with data processing running from Flash* and *Table 14: Maximum current consumption in Sleep mode, code running from Flash or RAM*. *Figure 15*, *Figure 16* and *Figure 17* show typical curves. ACC_{HSI} max values modified in *Table 23: HSI oscillator characteristics*. Small text changes.
24-Sep-2009	3	*Note 5* updated and *Note 4* added in *Table 4: Low-density STM32F101xx pin definitions*. V_{RERINT} and T_{Coeff} added to *Table 11: Embedded internal reference voltage*. Typical I_{DD_VBAT}value added in *Table 15: Typical and maximum current consumptions in Stop and Standby modes*. *Figure 14: Typical current consumption on VBAT with RTC on versus temperature at different VBAT values* added. f_{HSE_ext} min modified in *Table 19: High-speed external user clock characteristics*. C_{L1} and C_{L2} replaced by C in *Table 21: HSE 4-16 MHz oscillator characteristics* and *Table 22: LSE oscillator characteristics (fLSE = 32.768 kHz)*, notes modified and moved below the tables. *Note 1* modified below *Figure 20: Typical application with an 8 MHz crystal*. *Table 23: HSI oscillator characteristics* modified. Conditions removed from *Table 25: Low-power mode wakeup timings*. *Figure 27: Recommended NRST pin protection* modified. IEC 1000 standard updated to IEC 61000 and SAE J1752/3 updated to IEC 61967-2 in *Section 5.3.10: EMC characteristics on page 49*. Jitter added to *Table 26: PLL characteristics*. C_{ADC} and R_{AIN} parameters modified in *Table 41: ADC characteristics*. R_{AIN} max values modified in *Table 42: RAIN max for fADC = 14 MHz*. Small text changes.
20-May-2010	4	Added VFQFPN48 package. Updated note 2 below *Table 38: I2C characteristics* Updated *Figure 28: I2C bus AC waveforms and measurement circuit(1)* Updated *Figure 27: Recommended NRST pin protection* Updated *Section 5.3.12: I/O current injection characteristics*