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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	36MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	51
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f101r6t6

2 Description

The STM32F101x4 and STM32F101x6 Low-density access line family incorporates the high-performance ARM Cortex®-M3 32-bit RISC core operating at a 36 MHz frequency, high-speed embedded memories (Flash memory of 16 to 32 Kbytes and SRAM of 4 to 6 Kbytes), and an extensive range of enhanced peripherals and I/Os connected to two APB buses. All devices offer standard communication interfaces (one I^2C, one SPI, and two USARTs), one 12-bit ADC and up to two general-purpose 16-bit timers.

The STM32F101xx Low-density access line family operates in the –40 to +85 °C temperature range, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F101xx Low-density access line family includes devices in three different packages ranging from 36 pins to 64 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the STM32F101xx Low-density access line microcontroller family suitable for a wide range of applications such as application control and user interface, medical and handheld equipment, PC peripherals, gaming and GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, Video intercoms, and HVACs.

2.1 Device overview

Figure 1 shows the general block diagram of the device family.

Table 2. Low-density STM32F101xx device features and peripheral counts

Peripheral		STM32F101Tx		STM32F101Cx		STM32F101Rx	
Flash - Kbytes		16	32	16	32	16	32
SRAM - Kbytes		4	6	4	6	4	6
Timers	General-purpose	2	2	2	2	2	2
Communication	SPI	1	1	1	1	1	1
	I^2C	1	1	1	1	1	1
	USART	2	2	2	2	2	2
12-bit synchronized ADC number of channels		1 10 channels		1 10 channels		1 16 channels	
GPIOs		26		37		51	
CPU frequency		36 MHz					
Operating voltage		2.0 to 3.6 V					
Operating temperatures		Ambient temperature: –40 to +85 °C (see *Table 8*) Junction temperature: –40 to +105 °C (see *Table 8*)					
Packages		VFQFPN36		LQFP48		LQFP64	

output compare, PWM or one pulse mode output. This gives up to 12 input captures / output compares / PWMs on the largest packages.
The general-purpose timers can work together via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs. They all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

2.3.19 I²C bus

The I²C bus interface can operate in multimaster and slave modes. It can support standard and fast modes.

It supports dual slave addressing (7-bit only) and both 7/10-bit addressing in master mode. A hardware CRC generation/verification is embedded.
The interface can be served by DMA and it supports SM Bus 2.0/PM Bus.

2.3.20 Universal synchronous/asynchronous receiver transmitter (USART)

The available USART interfaces communicate at up to 2.25 Mbit/s. They provide hardware management of the CTS and RTS signals, support IrDA SIR ENDEC, are ISO 7816 compliant and have LIN Master/Slave capability.

The USART interfaces can be served by the DMA controller.

2.3.21 Serial peripheral interface (SPI)

The SPI interface is able to communicate up to 18 Mbit/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

The SPI interface can be served by the DMA controller.

2.3.22 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current-capable.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

2.3.23 ADC (analog to digital converter)

The 12-bit analog to digital converter has up to 16 external channels and performs conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

3 Pinouts and pin description

Figure 3. STM32F101xx Low-density access line LQFP64 pinout

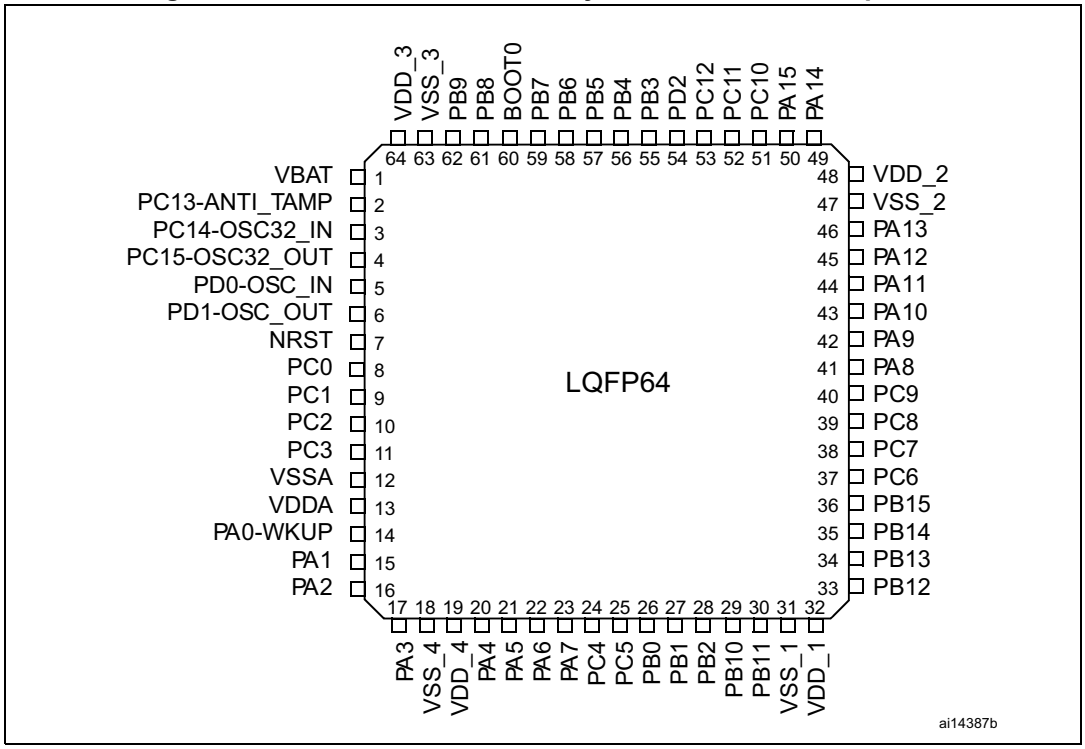


Figure 4. STM32F101xx Low-density access line LQFP48 pinout

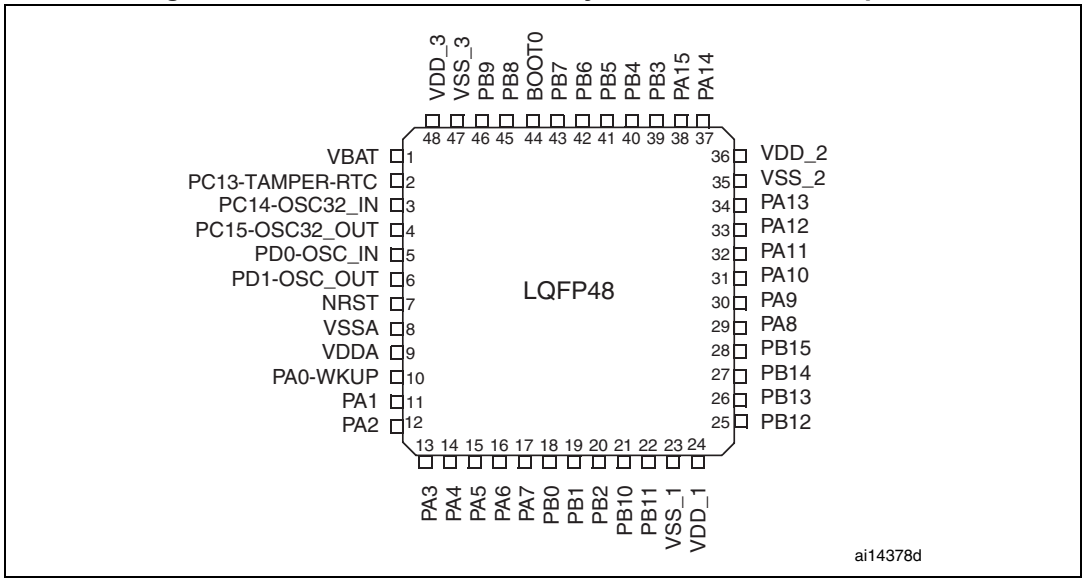


Table 4. Low-density STM32F101xx pin definitions

Pins			Pin name	Type(1)	I / O level(2)	Main function(3) (after reset)	Alternate functions(3)(4)	
LQFP48	LQFP64	VFQFPN36					Default	Remap
1	1	-	V_{BAT}	S	-	V_{BAT}	-	-
2	2	-	PC13-TAMPER-RTC(5)	I/O	-	PC13(6)	TAMPER-RTC	-
3	3	-	PC14-OSC32_IN(5)	I/O	-	PC14(6)	OSC32_IN	-
4	4	-	PC15-OSC32_OUT(5)	I/O	-	PC15(6)	OSC32_OUT	-
5	5	2	OSC_IN	I	-	OSC_IN	-	-
6	6	3	OSC_OUT	O	-	OSC_OUT	-	-
7	7	4	NRST	I/O	-	NRST	-	-
-	8	-	PC0	I/O	-	PC0	ADC_IN10	-
-	9	-	PC1	I/O	-	PC1	ADC_IN11	-
-	10	-	PC2	I/O	-	PC2	ADC_IN12	-
-	11	-	PC3	I/O	-	PC3	ADC_IN13	-
8	12	5	V_{SSA}	S	-	V_{SSA}	-	-
9	13	6	V_{DDA}	S	-	V_{DDA}	-	-
10	14	7	PA0-WKUP	I/O	-	PA0	WKUP/USART2_CTS/ ADC_IN0/ TIM2_CH1_ETR(7)	-
11	15	8	PA1	I/O	-	PA1	USART2_RTS/ ADC_IN1/TIM2_CH2(7)	-
12	16	9	PA2	I/O	-	PA2	USART2_TX/ ADC_IN2/TIM2_CH3(7)	-
13	17	10	PA3	I/O	-	PA3	USART2_RX/ ADC_IN3/TIM2_CH4(7)	-
-	18	-	V_{SS_4}	S	-	V_{SS_4}	-	-
-	19	-	V_{DD_4}	S	-	V_{DD_4}	-	-
14	20	11	PA4	I/O	-	PA4	SPI_NSS(7)/ADC_IN4 USART2_CK	-
15	21	12	PA5	I/O	-	PA5	SPI_SCK(7)/ADC_IN5	-
16	22	13	PA6	I/O	-	PA6	SPI_MISO(7)/ADC_IN6/ TIM3_CH1(7)	-

Figure 12. Typical current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals enabled

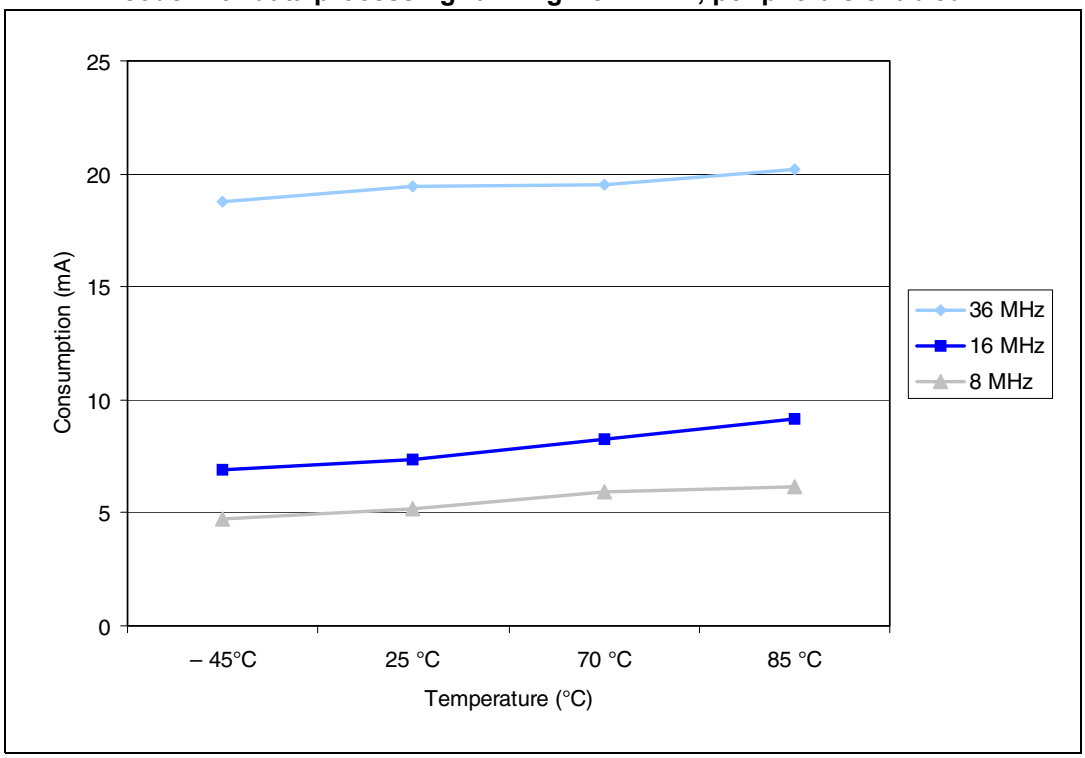


Figure 13. Typical current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals disabled

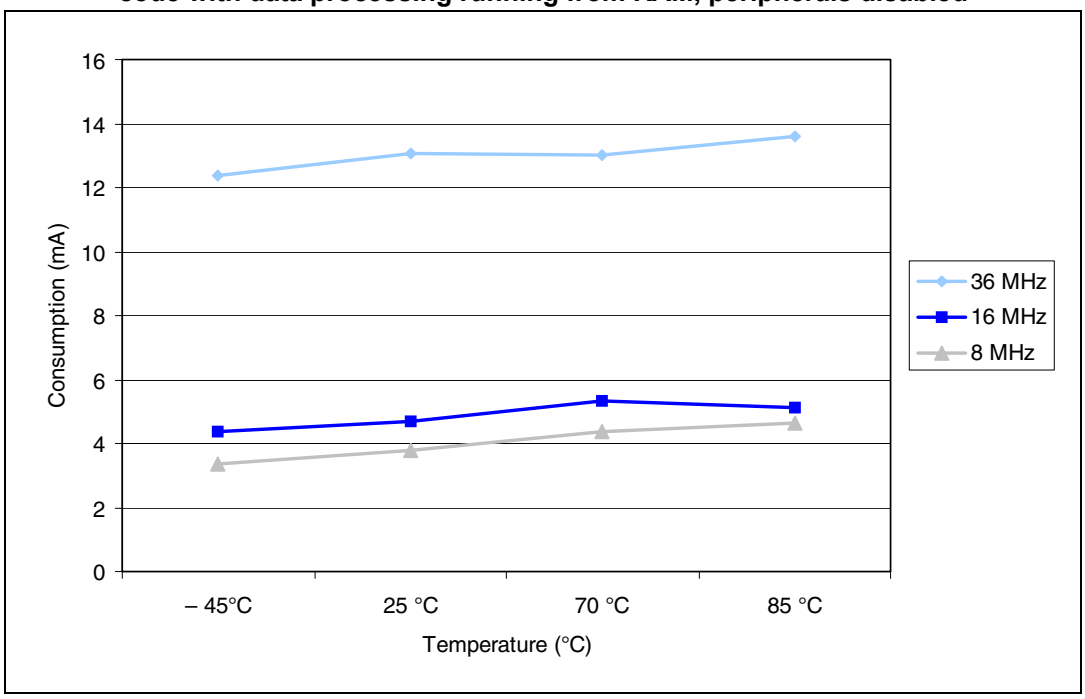


Figure 16. Typical current consumption in Stop mode with regulator in Low-power mode versus temperature at V_{DD} = 3.3 V and 3.6 V

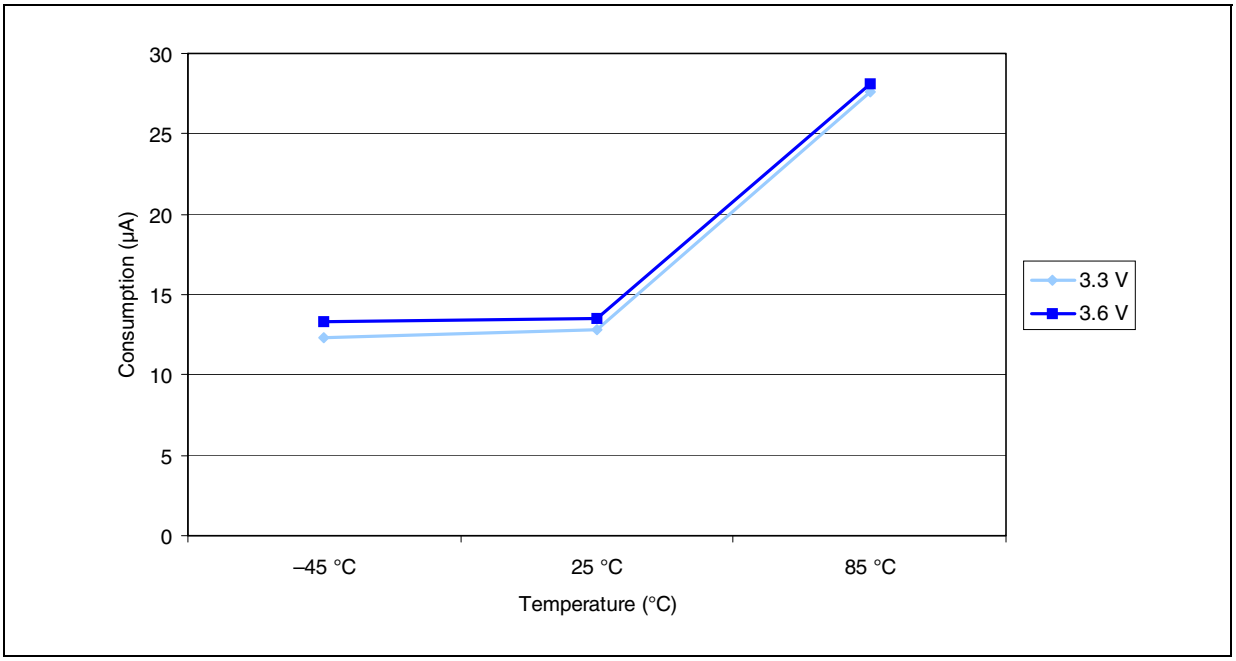
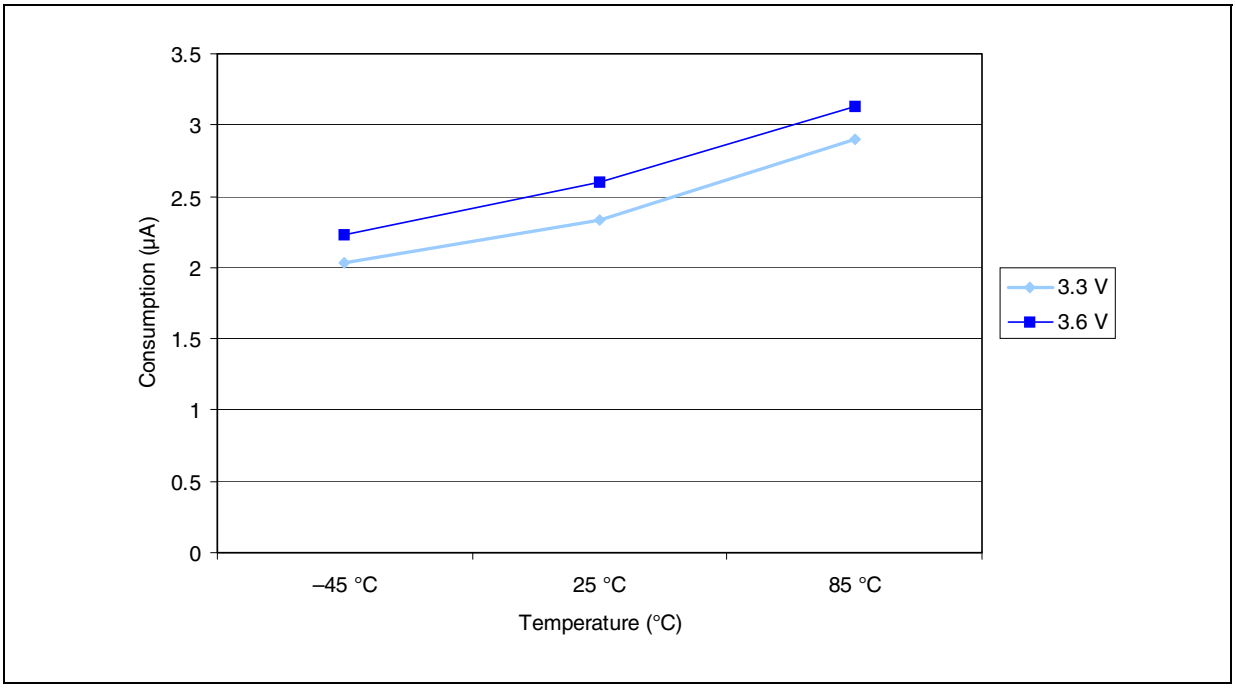


Figure 17. Typical current consumption in Standby mode versus temperature at V_{DD} = 3.3 V and 3.6 V



Typical current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except if it is explicitly mentioned
- The Flash access time is adjusted to f_{HCLK} frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 36 MHz)
- Prefetch is on (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK1} = f_{HCLK/4}$, $f_{PCLK2} = f_{HCLK/2}$, $f_{ADCCLK} = f_{PCLK2}/4$

The parameters given in *Table 16* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 16. Typical current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1) All peripherals enabled(2)	Typ(1) All peripherals disabled	Unit
I_{DD}	Supply current in Run mode	External clock(3)	36 MHz	17.2	13.8	mA
			24 MHz	11.2	8.9	
			16 MHz	8.1	6.6	
			8 MHz	5	4.2	
			4 MHz	3	2.6	
			2 MHz	2	1.8	
			1 MHz	1.5	1.4	
			500 kHz	1.2	1.2	
			125 kHz	1.05	1	
		Running on high speed internal RC (HSI), AHB prescaler used to reduce the frequency	36 MHz	16.5	13.1	
			24 MHz	10.5	8.2	
			16 MHz	7.4	5.9	
			8 MHz	4.3	3.6	
			4 MHz	2.4	2	
			2 MHz	1.5	1.3	
			1 MHz	1	0.9	
			500 kHz	0.7	0.65	
			125 kHz	0.5	0.45	

1. Typical values are measures at T_A = 25 °C, V_{DD} = 3.3 V.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 17. Typical current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1) All peripherals enabled(2)	Typ(1) All peripherals disabled	Unit
I_{DD}	Supply current in Sleep mode	External clock(3)	36 MHz	6.7	3.1	mA
			24 MHz	4.8	2.3	
			16 MHz	3.4	1.8	
			8 MHz	2	1.2	
			4 MHz	1.5	1.1	
			2 MHz	1.25	1	
			1 MHz	1.1	0.98	
			500 kHz	1.05	0.96	
			125 kHz	1	0.95	
		Running on High Speed Internal RC (HSI), AHB prescaler used to reduce the frequency	36 MHz	6.1	2.5	
			24 MHz	4.2	1.7	
			16 MHz	2.8	1.2	
			8 MHz	1.4	0.55	
			4 MHz	0.9	0.5	
			2 MHz	0.7	0.45	
			1 MHz	0.55	0.42	
			500 kHz	0.48	0.4	
			125 kHz	0.4	0.38	

1. Typical values are measures at T_A = 25 °C, V_{DD} = 3.3 V.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 18*. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- ambient operating temperature and V_{DD} supply voltage conditions summarized in *Table 5*.

5.3.11 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 30. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to JESD22-A114	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to ANSI/ESD STM5.3.1	II	500	

1. Based on characterization results, not tested in production.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78 IC latch-up standard.

Table 31. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +85 °C conforming to JESD78A	II level A

5.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibilty to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation).

The test results are given in *Table 32*

Table 32. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on OSC_IN32, OSC_OUT32, PA4, PA5, PC13	-0	+0	mA
	Injected current on all FT pins	-5	+0	
	Injected current on any other pin	-5	+5	

Output driving current

The GPIOs (general-purpose inputs/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with a relaxed V_{OL}/V_{OH}) except PC13, PC14 and PC15 which can sink or source up to +/-3mA. When using the GPIOs PC13 to PC15 in output mode, the speed should not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 5.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating I_{VDD} (see *Table 6*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS} (see *Table 6*).

Output voltage levels

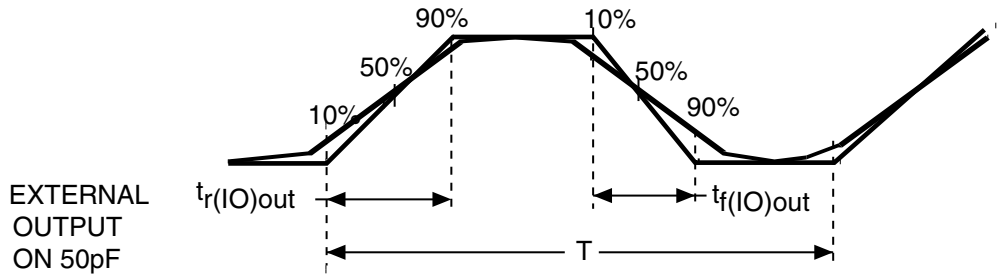
Unless otherwise specified, the parameters given in *Table 34* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*. All I/Os are CMOS and TTL compliant.

Table 34. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(1)	Output Low level voltage for an I/O pin when 8 pins are sunk at the same time	CMOS port(2),, I_{IO} = +8 mA, 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH}(3)	Output High level voltage for an I/O pin when 8 pins are sourced at the same time		V_{DD}–0.4	-	
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	TTL port(2) I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		2.4	-	
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	I_{IO} = +20 mA(4) 2.7 V < V_{DD} < 3.6 V	-	1.3	V
V_{OH} (3)	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		V_{DD}–1.3	-	
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	I_{IO} = +6 mA(4) 2 V < V_{DD} < 2.7 V	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		V_{DD}–0.4	-	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 6* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 6* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
4. Based on characterization data, not tested in production.

Figure 26. I/O AC characteristics definition



Maximum frequency is achieved if $(t_r + t_f) \leq 2/3)T$ and if the duty cycle is (45-55%) when loaded by 50pF

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5.3.14 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 33*).

Unless otherwise specified, the parameters given in *Table 36* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 36. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST Input low level voltage	-	–0.5	-	0.8	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage	-	2	-	V_{DD}+0.5	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$(1)	NRST Input filtered pulse	-	-	-	100	ns
$V_{NF(NRST)}$(1)	NRST Input not filtered pulse	-	300	-	-	ns

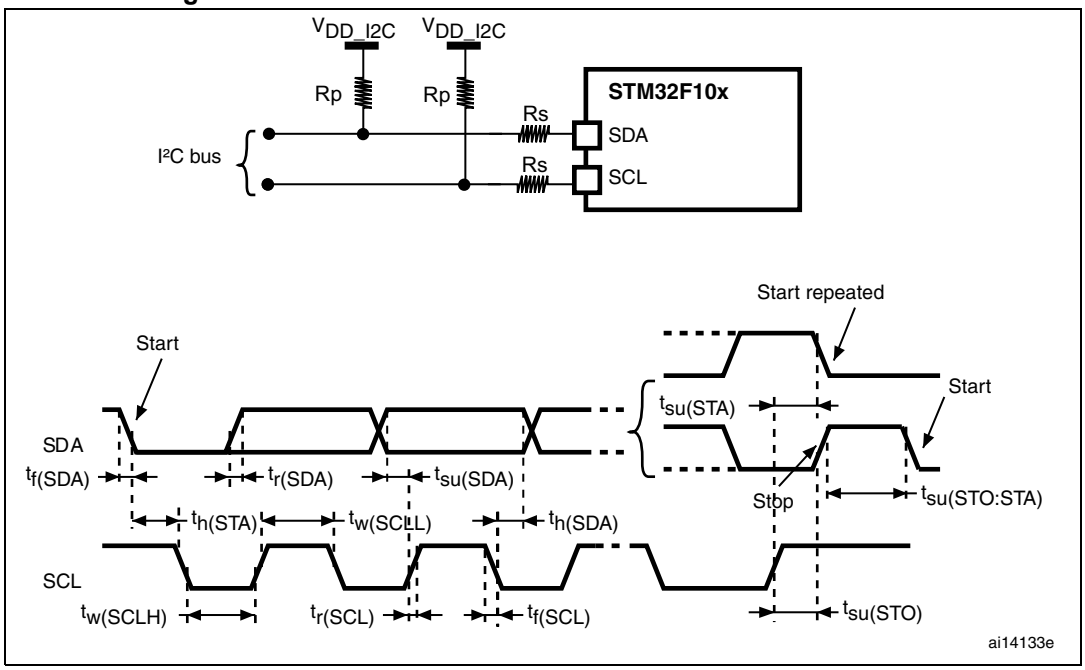
1. Guaranteed by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

Table 38. I^2C characteristics

Symbol	Parameter	Standard mode I^2C(1)		Fast mode I^2C(1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0	-	0(3)	900(4)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	20+0.1C_b	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated Start condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	Stop condition setup time	4.0	-	0.6	-	µs
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7	-	1.3	-	µs
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. Guaranteed by design, not tested in production.
2. f_{PCLK1} must be at least 2 MHz to achieve standard mode I^2C frequencies. It must be at least 4 MHz to achieve fast mode I^2C frequencies. It must be a multiple of 10 MHz to reach the 400 kHz maximum I2C fast mode clock.
3. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
4. The maximum Data hold time has only to be met if the interface does not stretch the low period of SCL signal.

Figure 28. I²C bus AC waveforms and measurement circuit(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.
2. Rs = Series protection resistors, Rp = Pull-up resistors, V_{DD_I2C} = I2C bus supply.

Table 39. SCL frequency (f_{PCLK1}= MHz, V_{DD_I2C} = 3.3 V)(1)(2)

f_{SCL} (kHz)	I2C_CCR value
	R_P = 4.7 kΩ
400	0x801E
300	0x8028
200	0x803C
100	0x00B4
50	0x0168
20	0x0384

1. R_P = External pull-up resistance, f_{SCL} = I²C speed,
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed ±2%. These variations depend on the accuracy of the external components used to design the application.

SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 40* are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 8*.

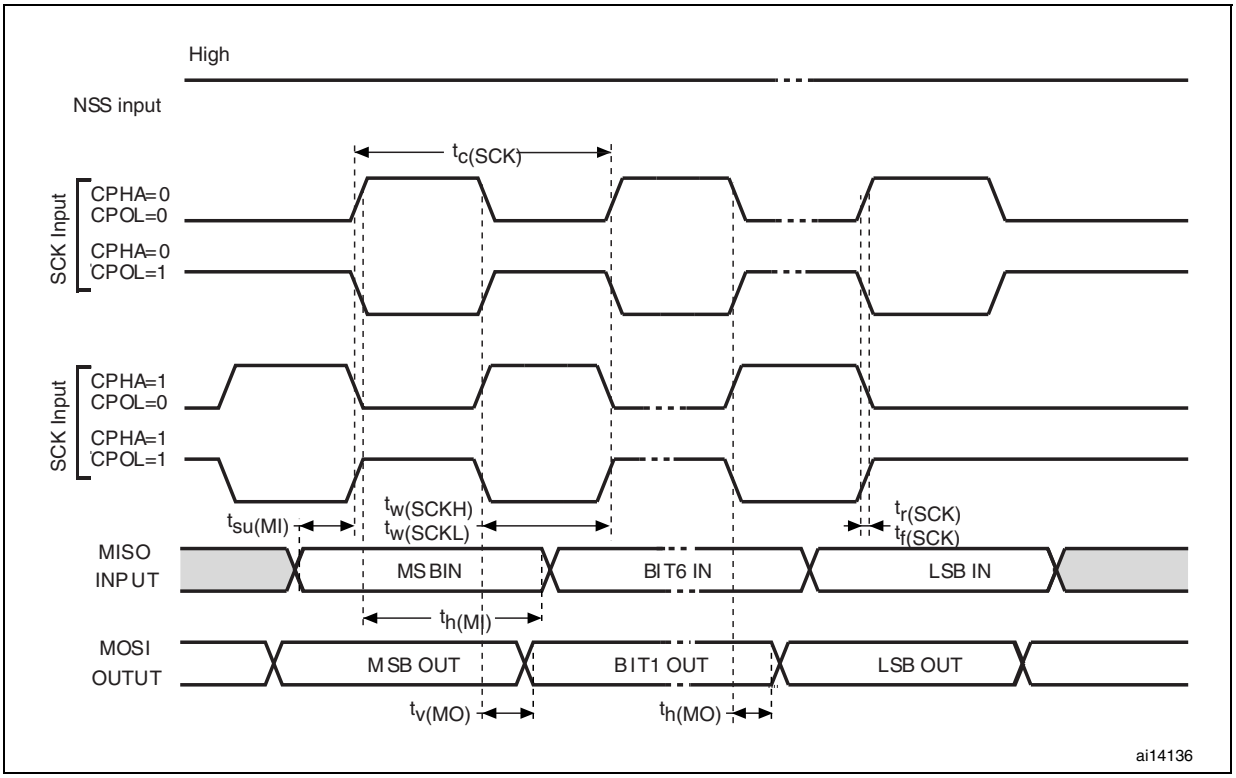
Refer to *Section 5.3.12: I/O current injection characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 40. SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	0	18	MHz
		Slave mode	0	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF		8	ns
$t_{su(NSS)}$ (1)	NSS setup time	Slave mode	4 t_{PCLK}	-	
$t_{h(NSS)}$ (1)	NSS hold time	Slave mode	73	-	
$t_{w(SCKH)}$ (1) $t_{w(SCKL)}$ (1)	SCK high and low time	Master mode, f_{PCLK} = 36 MHz, presc = 4	50	60	
$t_{su(MI)}$ (1)	Data input setup time Master mode	SPI	1	-	
$t_{su(SI)}$ (1)	Data input setup time Slave mode	-	1	-	
$t_{h(MI)}$ (1)	Data input hold time Master mode	SPI	1	-	
$t_{h(SI)}$ (1)	Data input hold time Slave mode	-	3	-	
$t_{a(SO)}$ (1)(2)	Data output access time	Slave mode, f_{PCLK} = 36 MHz, presc = 4	0	55	
		Slave mode, f_{PCLK} = 24 MHz	0	4 t_{PCLK}	
$t_{dis(SO)}$ (1)(3)	Data output disable time	Slave mode	10		
$t_{v(SO)}$ (1)	Data output valid time	Slave mode (after enable edge)	-	25	
$t_{v(MO)}$ (1)	Data output valid time	Master mode (after enable edge)	-	3	
$t_{h(SO)}$ (1)	Data output hold time	Slave mode (after enable edge)	25	-	
$t_{h(MO)}$ (1)		Master mode (after enable edge)	4	-	

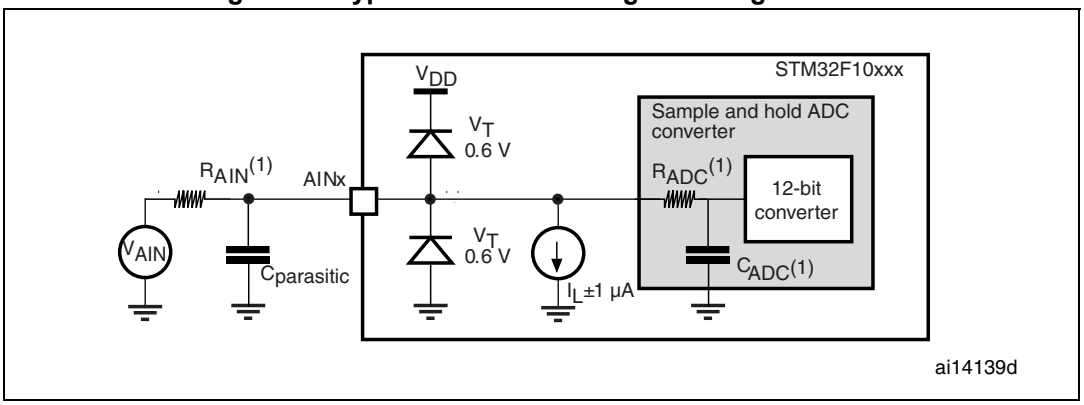
1. Based on characterization, not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

Figure 31. SPI timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 33. Typical connection diagram using the ADC



1. Refer to *Table 41* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 34*. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 34. Power supply and reference decoupling

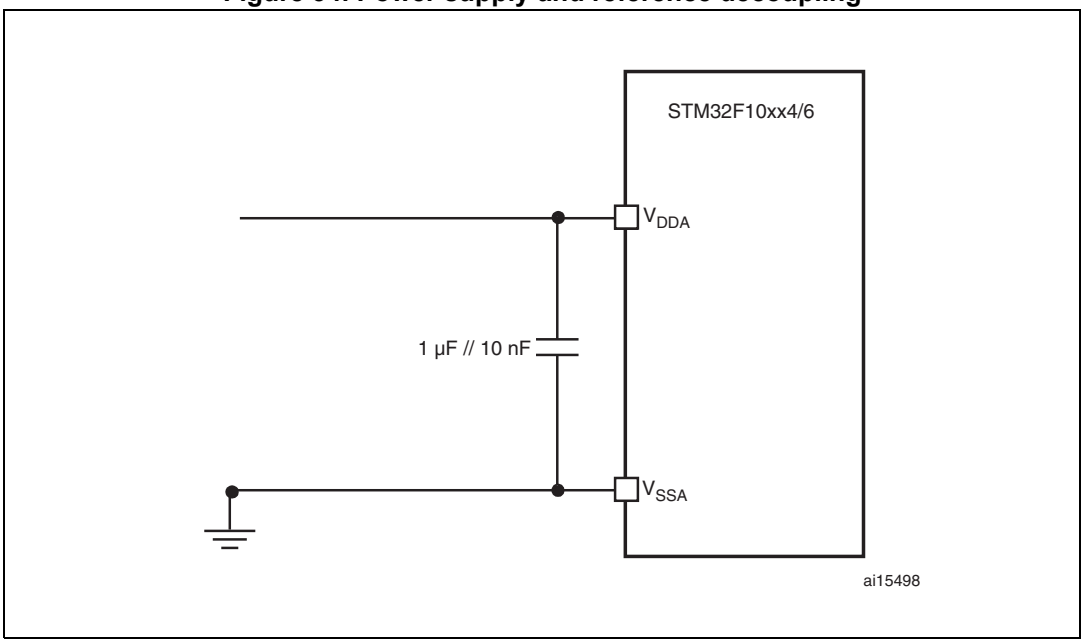
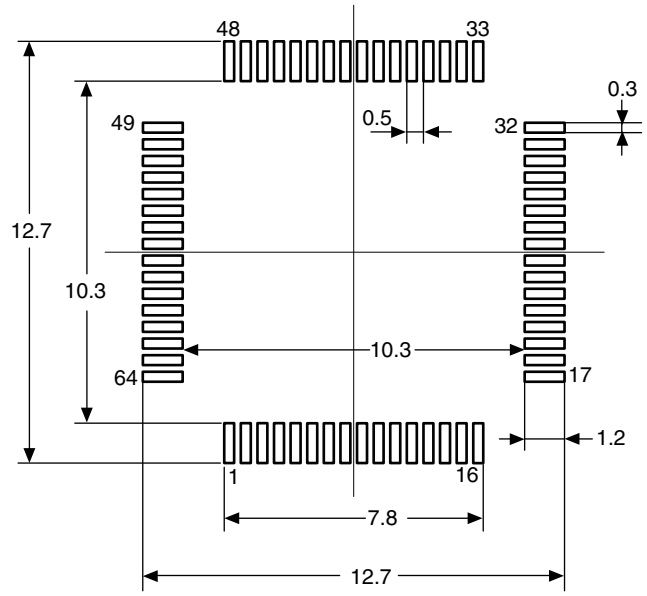


Table 47. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 39. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint

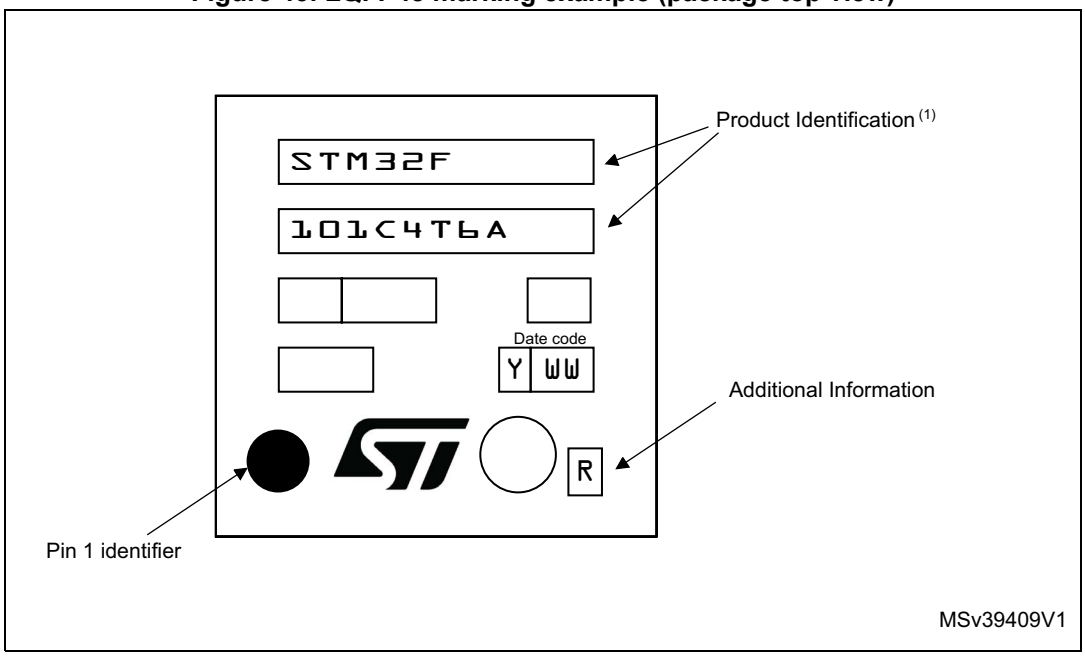


1. Dimensions are expressed in millimeters.

Device Marking for LQFP48

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 43. LQFP48 marking example (package top view)



1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.