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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	36MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	26
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	36-VFQFN Exposed Pad
Supplier Device Package	36-VFQFPN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f101t6u6a

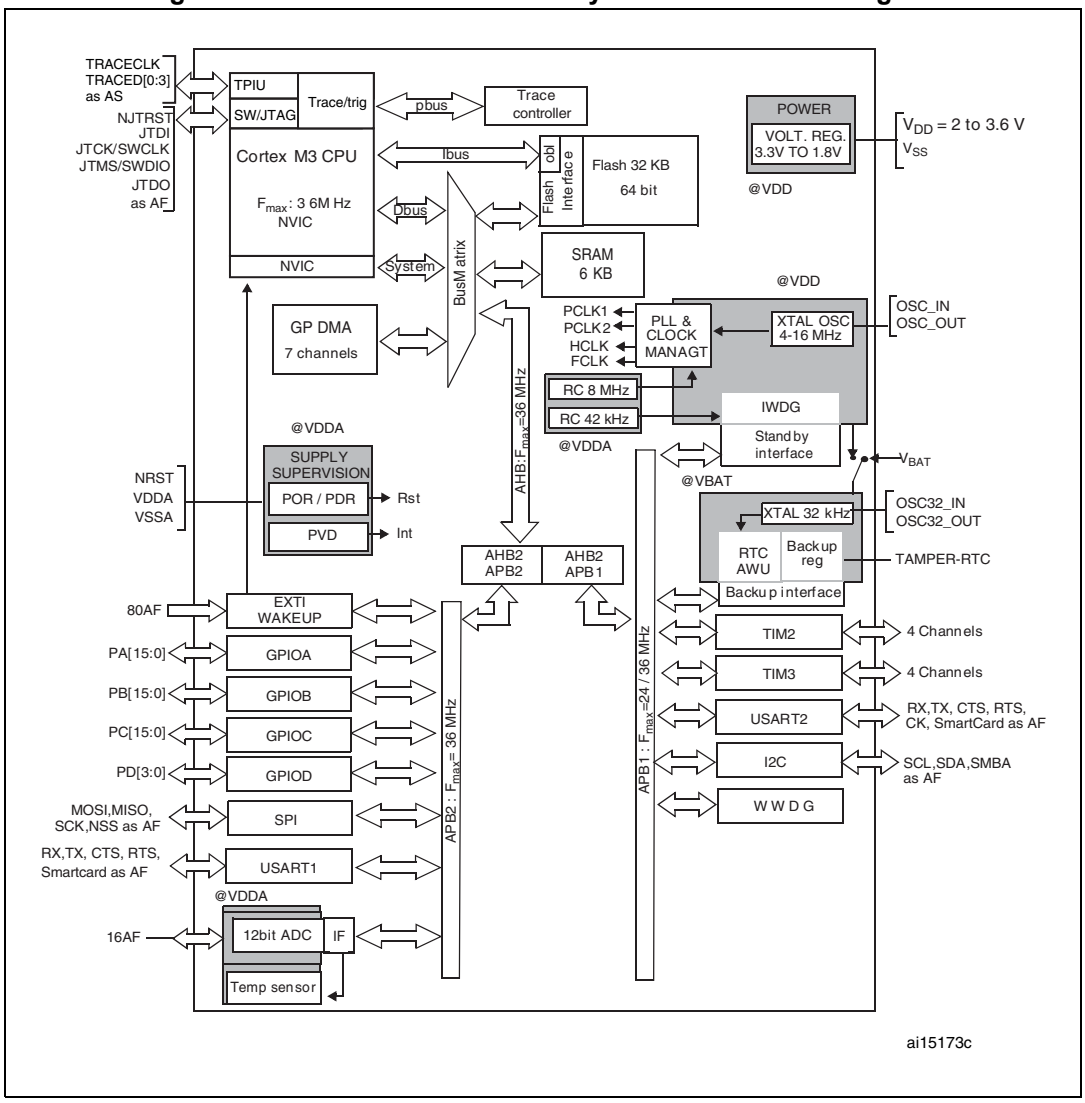
2.1 Device overview

Figure 1 shows the general block diagram of the device family.

Table 2. Low-density STM32F101xx device features and peripheral counts

Peripheral		STM32F101Tx		STM32F101Cx		STM32F101Rx	
Flash - Kbytes		16	32	16	32	16	32
SRAM - Kbytes		4	6	4	6	4	6
Timers	General-purpose	2	2	2	2	2	2
Communication	SPI	1	1	1	1	1	1
	I^2C	1	1	1	1	1	1
	USART	2	2	2	2	2	2
12-bit synchronized ADC number of channels		1 10 channels		1 10 channels		1 16 channels	
GPIOs		26		37		51	
CPU frequency		36 MHz					
Operating voltage		2.0 to 3.6 V					
Operating temperatures		Ambient temperature: –40 to +85 °C (see *Table 8*) Junction temperature: –40 to +105 °C (see *Table 8*)					
Packages		VFQFPN36		LQFP48		LQFP64	

Figure 1. STM32F101xx Low-density access line block diagram



1. AF = alternate function on I/O port pin.
2. T_A = –40 °C to +85 °C (junction temperature up to 105 °C).

higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

Refer to *Table 10: Embedded reset and power control block characteristics* for the values of $V_{POR/PDR}$ and V_{PVD}.

2.3.11 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in the nominal regulation mode (Run)
- LPR is used in the Stop mode
- Power down is used in Standby mode: the regulator output is in high impedance: the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost)

This regulator is always enabled after reset. It is disabled in Standby mode, providing high impedance output.

2.3.12 Low-power modes

The STM32F101xx Low-density access line supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop** mode

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low power mode.
  The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output or the RTC alarm.

- **Standby** mode

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), a IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

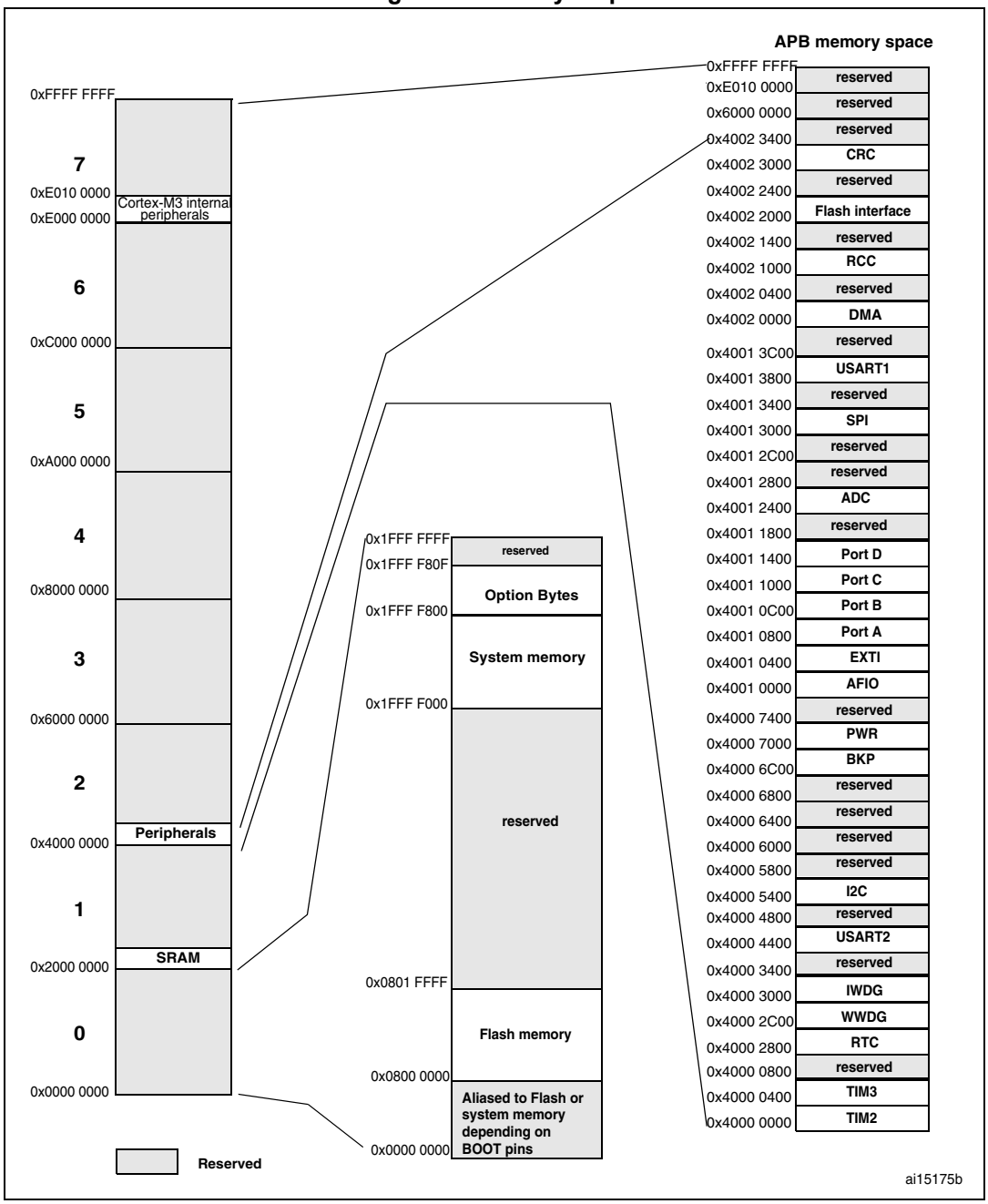
2.3.13 DMA

The flexible 7-channel general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management avoiding the generation of interrupts when the controller reaches the end of the buffer.

4 Memory mapping

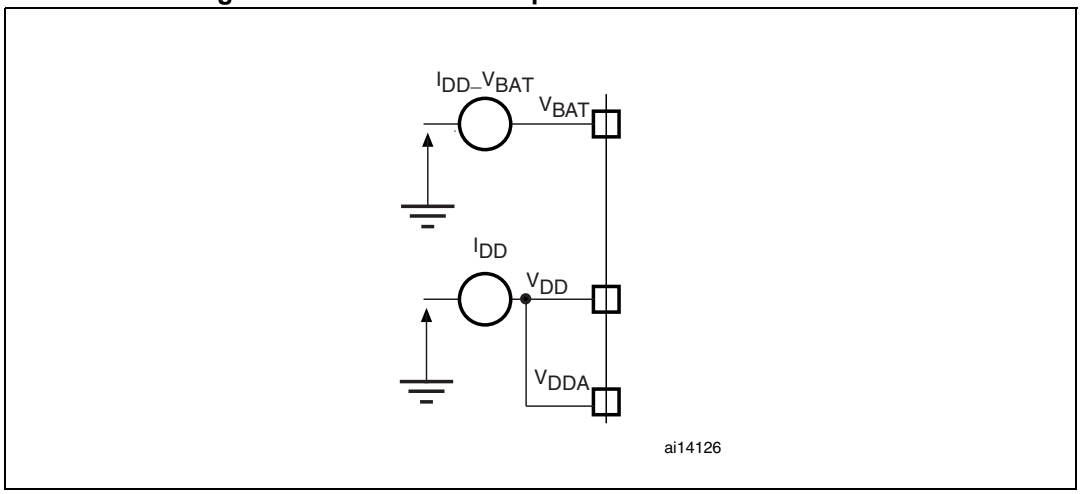
The memory map is shown in *Figure 7*.

Figure 7. Memory map



5.1.7 Current consumption measurement

Figure 11. Current consumption measurement scheme



5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 5: Voltage characteristics*, *Table 6: Current characteristics*, and *Table 7: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD} –V_{SS}	External main supply voltage (including V_{DDA} and V_{DD})(1)	–0.3	4.0	V
V_{IN}(2)	Input voltage on five volt tolerant pin	V_{SS} –0.3	V_{DD} +4.0	
	Input voltage on any other pin	V_{SS} –0.3	4.0	
$\|\Delta V_{DDx}\|$	Variations between different V_{DD} power pins	-	50	mV
$\|V_{SSX} - V_{SS}\|$	Variations between all the different ground pins	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 5.3.11: Absolute maximum ratings (electrical sensitivity)*		-

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 6: Current characteristics* for the maximum allowed injected current values.

Table 18. Peripheral current consumption

Peripheral		Typical consumption at 25 °C	Unit
AHB (up to 36 MHz)	DMA1	15.97	µA/MHz
	CRC	1.67	
	BusMatrix(1)	8.33	
APB1 (up to 18 MHz)	APB1-Bridge	7.22	
	TIM2	33.33	
	TIM3	33.61	
	USART2	12.78	
	I2C1	10.83	
	WWDG	3.33	
	PWR	1.94	
	BKP	2.78	
	IWDG	1.39	
APB2 (up to 36 MHz)	APB2-Bridge	3.33	
	GPIO A	7.50	
	GPIO B	6.81	
	GPIO C	7.22	
	GPIO D	6.94	
	SPI1	4.86	
	USART1	12.78	
	ADC1(2)	15.54	

1. The BusMatrix is automatically active when at least one master is ON. (CPU, DMA1).
2. Specific conditions for measuring ADC current consumption: f_{HCLK} = 28 MHz, $f_{APB1} = f_{HCLK}$, $f_{APB2} = f_{HCLK}$, $f_{ADCCLK} = f_{APB2} / 2$. When ADON bit in the ADC_CR2 register is set to 1, a current consumption of analog part equal to 0.7 mA must be added.

5.3.6 External clock source characteristics

High-speed external user clock generated from an external source

The characteristics given in *Table 19* result from tests performed using an high-speed external clock source, and under the ambient temperature and supply voltage conditions summarized in *Table 8*.

Table 19. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency(1)	-	1	8	25	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time(1)		5	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time(1)		-	-	20	
$C_{in(HSE)}$	OSC_IN input capacitance(1)	-	-	5	-	pF
$DuCy_{(HSE)}$	Duty cycle	-	45	-	55	%
I_L	OSC_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	µA

1. Guaranteed by design, not tested in production.

Low-speed external user clock generated from an external source

The characteristics given in *Table 20* result from tests performed using an low-speed external clock source, and under the ambient temperature and supply voltage conditions summarized in *Table 8*.

Table 20. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency(1)	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_IN high or low time(1)		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)		-	-	50	
$C_{in(LSE)}$	OSC32_IN input capacitance(1)	-	-	5	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	30	-	70	%
I_L	OSC32_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	µA

1. Guaranteed by design, not tested in production.

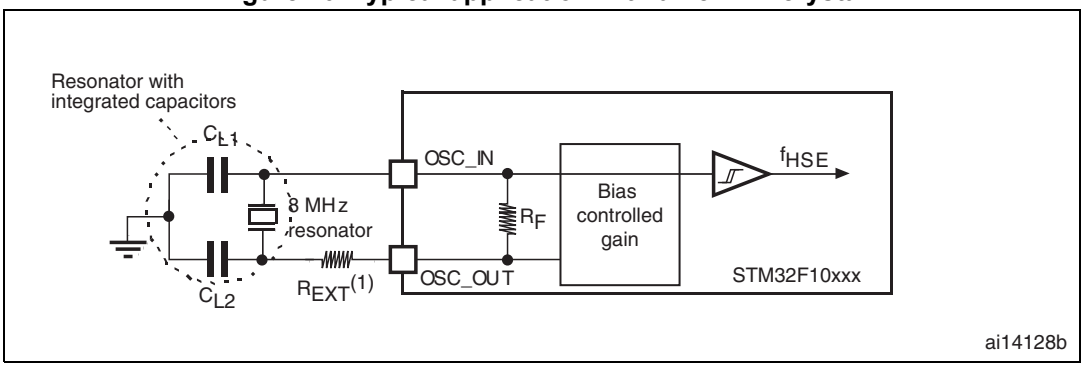
Table 21. HSE 4-16 MHz oscillator characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	16	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
C	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(3)	R_S = 30 Ω	-	30	-	pF
i_2	HSE driving current	V_{DD} = 3.3 V, V_{IN} = V_{SS} with 30 pF load	-	-	1	mA
g_m	Oscillator transconductance	Startup	25	-	-	mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Based on characterization, not tested in production.
3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 20*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}. Refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website *www.st.com*.

Figure 20. Typical application with an 8 MHz crystal

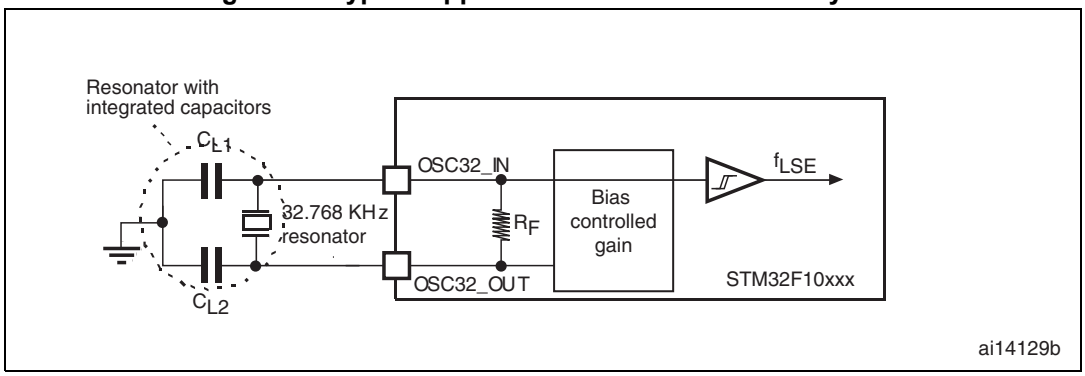


1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 22*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization

Figure 21. Typical application with a 32.768 kHz crystal



5.3.7 Internal clock source characteristics

The parameters given in *Table 23* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

High-speed internal (HSI) RC oscillator

Table 23. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{HSI}	Frequency	-		-	8	-	MHz
$DuCy_{(HSI)}$	Duty cycle	-		45	-	55	%
ACC_{HSI}	Accuracy of the HSI oscillator	User-trimmed with the RCC_CR register(2)		-	-	1(3)	%
		Factory-calibrated (4) (5)	T_A = –40 to 105 °C	–2	-	2.5	%
			T_A = –10 to 85 °C	–1.5	-	2.2	%
			T_A = 0 to 70 °C	–1.3	-	2	%
			T_A = 25 °C	–1.1	-	1.8	%
$t_{su(HSI)}$(4)	HSI oscillator startup time	-		1	-	2	µs
$I_{DD(HSI)}$(4)	HSI oscillator power consumption	-		-	80	100	µA

1. V_{DD} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Refer to application note AN2868 “STM32F10xxx internal RC oscillator (HSI) calibration” available from the ST website *www.st.com*.
3. Guaranteed by design, not tested in production.
4. Based on characterization, not tested in production.
5. The actual frequency of HSI oscillator may be impacted by a reflow, but does not drift out of the specified range.

The test results are given in *Table 28*. They are based on the EMS levels and classes defined in application note AN1709.

Table 28. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK}= 36 MHz conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 36 MHz conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and pre qualification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second. To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device is monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC61967-2 standard which specifies the test board and the pin loading.

Table 29. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]	Unit
				8/36 MHz	
S_{EMI}	Peak level	V_{DD} = 3.3 V, T_A = 25 °C, compliant with IEC 61967-2	0.1 MHz to 30 MHz	7	dBµV
			30 MHz to 130 MHz	8	
			130 MHz to 1GHz	13	
			EMI Level	3.5	-

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 22* and *Figure 23* for standard I/Os, and in *Figure 24* and *Figure 25* for 5 V tolerant I/Os.

Figure 22. Standard I/O input characteristics - CMOS port

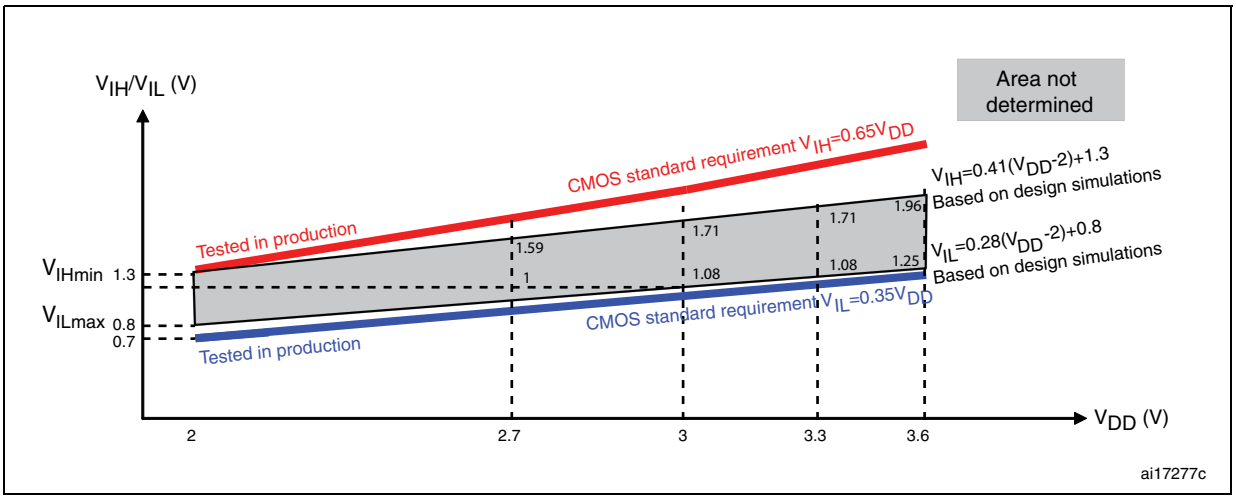
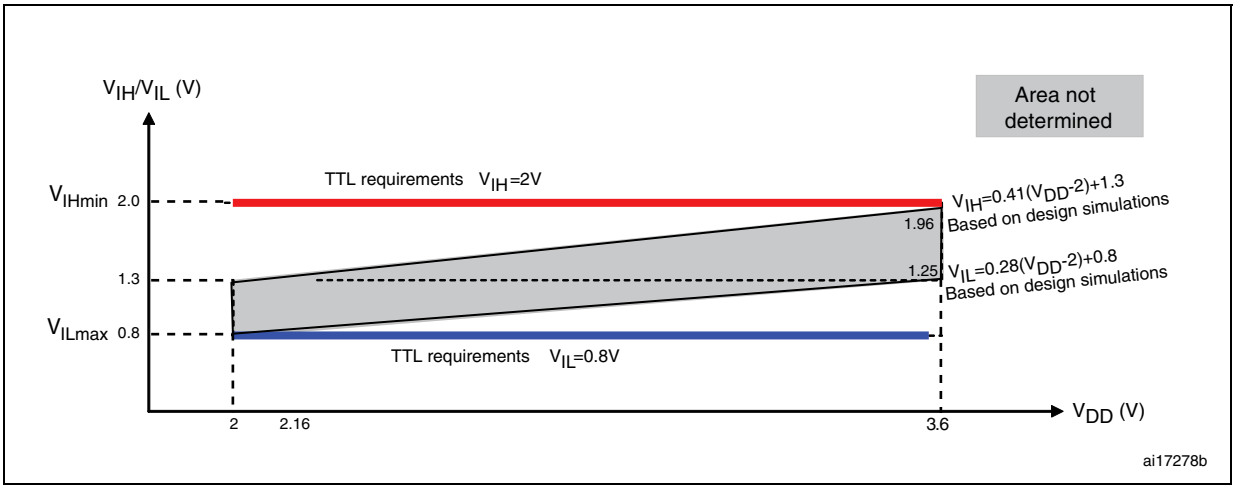


Figure 23. Standard I/O input characteristics - TTL port



Output driving current

The GPIOs (general-purpose inputs/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with a relaxed V_{OL}/V_{OH}) except PC13, PC14 and PC15 which can sink or source up to +/-3mA. When using the GPIOs PC13 to PC15 in output mode, the speed should not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 5.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating I_{VDD} (see *Table 6*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS} (see *Table 6*).

Output voltage levels

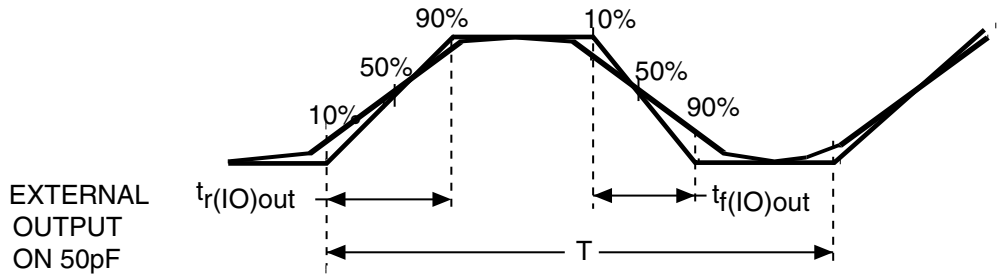
Unless otherwise specified, the parameters given in *Table 34* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*. All I/Os are CMOS and TTL compliant.

Table 34. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(1)	Output Low level voltage for an I/O pin when 8 pins are sunk at the same time	CMOS port(2),, I_{IO} = +8 mA, 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH}(3)	Output High level voltage for an I/O pin when 8 pins are sourced at the same time		V_{DD}–0.4	-	
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	TTL port(2) I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		2.4	-	
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	I_{IO} = +20 mA(4) 2.7 V < V_{DD} < 3.6 V	-	1.3	V
V_{OH} (3)	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		V_{DD}–1.3	-	
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	I_{IO} = +6 mA(4) 2 V < V_{DD} < 2.7 V	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		V_{DD}–0.4	-	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 6* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 6* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
4. Based on characterization data, not tested in production.

Figure 26. I/O AC characteristics definition



Maximum frequency is achieved if $(t_r + t_f) \leq 2/3)T$ and if the duty cycle is (45-55%) when loaded by 50pF

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5.3.14 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 33*).

Unless otherwise specified, the parameters given in *Table 36* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 36. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST Input low level voltage	-	–0.5	-	0.8	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage	-	2	-	V_{DD}+0.5	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$(1)	NRST Input filtered pulse	-	-	-	100	ns
$V_{NF(NRST)}$(1)	NRST Input not filtered pulse	-	300	-	-	ns

1. Guaranteed by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

5.3.17 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 41* are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 8*.

Note: It is recommended to perform a calibration after each power-up.

Table 41. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.4	-	3.6	V
f_{ADC}	ADC clock frequency	-	0.6	-	14	MHz
f_S(1)	Sampling rate	-	0.043	-	1	MHz
f_{TRIG}(1)	External trigger frequency	f_{ADC} = 14 MHz	-	-	823	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(2)	-	0 (V_{SSA} or V_{REF-} tied to ground)	-	V_{REF+}	V
R_{AIN}(1)	External input impedance	See *Equation 1* and *Table 42* for details	-	-	50	kΩ
R_{ADC}(1)	Sampling switch resistance	-	-	-	1	kΩ
C_{ADC}(1)	Internal sample and hold capacitor	-	-	-	8	pF
t_{CAL}(1)	Calibration time	f_{ADC} = 14 MHz	5.9			µs
		-	83			$1/f_{ADC}$
t_{lat}(1)	Injection trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.214	µs
		-	-	-	3(3)	$1/f_{ADC}$
t_{latr}(1)	Regular trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.143	µs
		-	-	-	2(3)	$1/f_{ADC}$
t_S(1)	Sampling time	f_{ADC} = 14 MHz	0.107	-	17.1	µs
			1.5	-	239.5	$1/f_{ADC}$
t_{STAB}(1)	Stabilization time	-	14			$1/f_{ADC}$
t_{CONV}(1)	Total conversion time (including sampling time)	f_{ADC} = 14 MHz	1	-	18	µs
		-	14 to 252 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

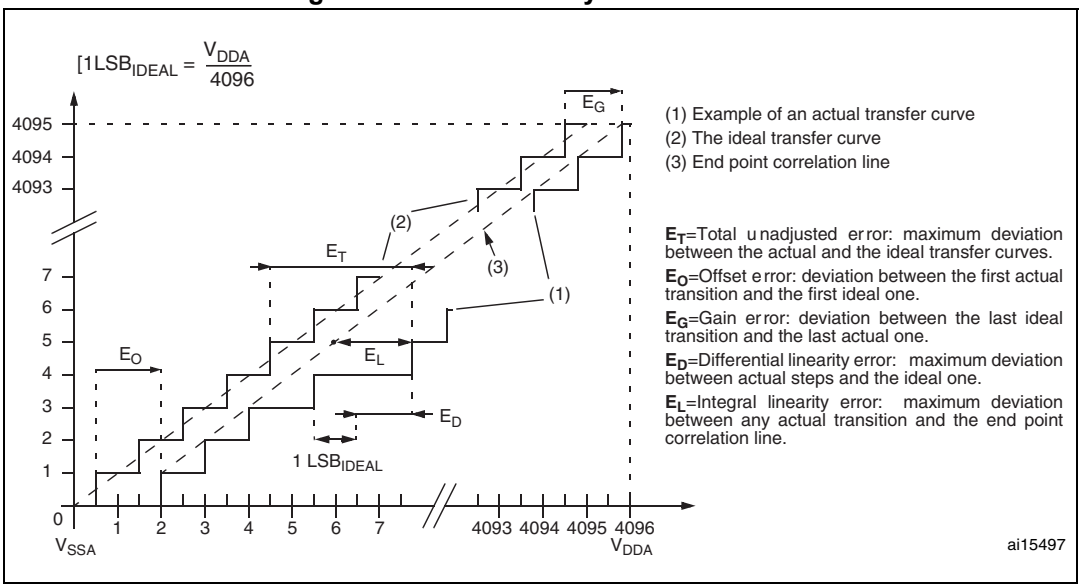
1. Guaranteed by design, not tested in production.
2. V_{REF+} is internally connected to V_{DDA} and V_{REF-} is be internally connected to V_{SSA}.
3. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 41*.

Table 44. ADC accuracy(1) (2) (3)

Symbol	Parameter	Test conditions	Typ	Max(4)	Unit
ET	Total unadjusted error	f_{PCLK2} = 28 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.4 V to 3.6 V Measurements made after ADC calibration	±2	±5	LSB
EO	Offset error		±1.5	±2.5	
EG	Gain error		±1.5	±3	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±1.5	±3	

1. ADC DC accuracy values are measured after internal calibration.
2. Better performance could be achieved in restricted V_{DD}, frequency and temperature ranges.
3. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 5.3.12* does not affect the ADC accuracy.
4. Based on characterization, not tested in production.

Figure 32. ADC accuracy characteristics



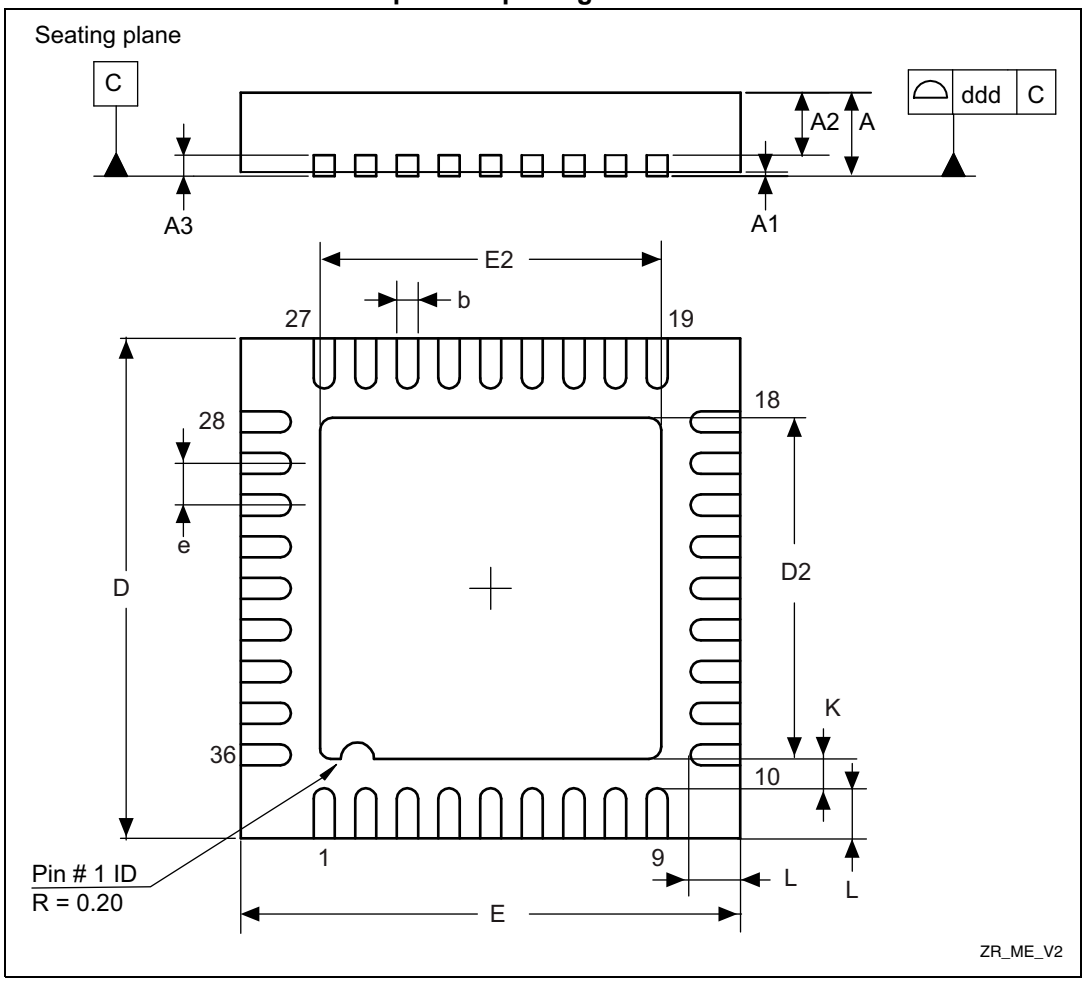
6 Package characteristics

6.1 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

6.2 VFQFPN36 package information

Figure 35. VFQFPN36 - 36-pin, 6x6 mm, 0.5 mm pitch very thin profile fine pitch quad flat package outline

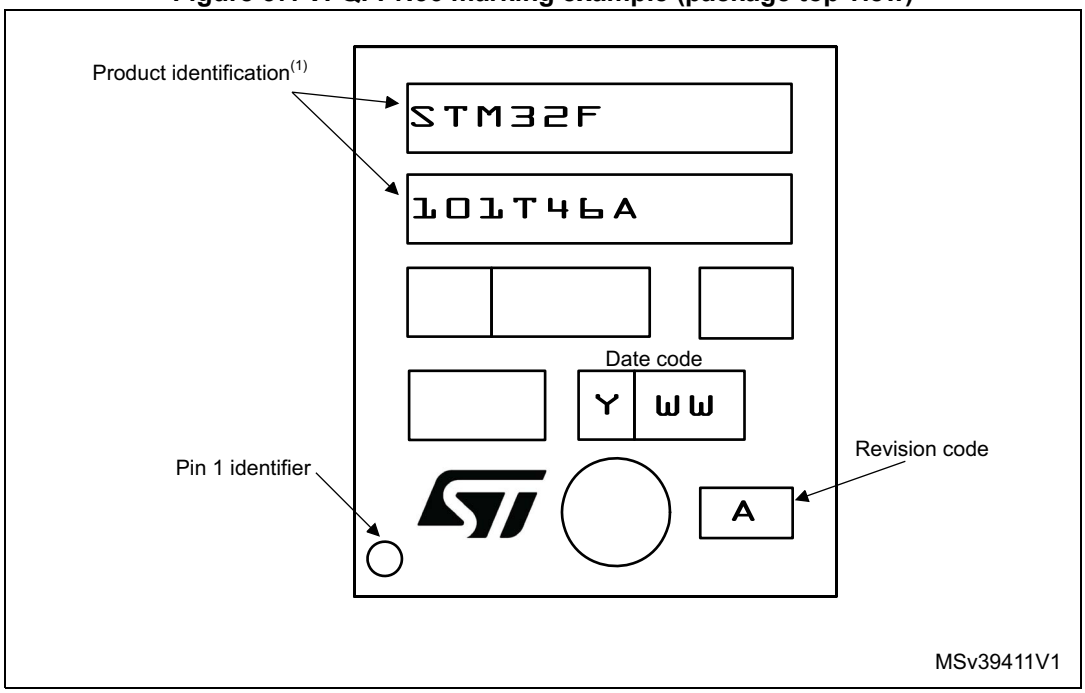


1. Drawing is not to scale.

Device Marking for VFQFPN36

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 37. VFQFPN36 marking example (package top view)

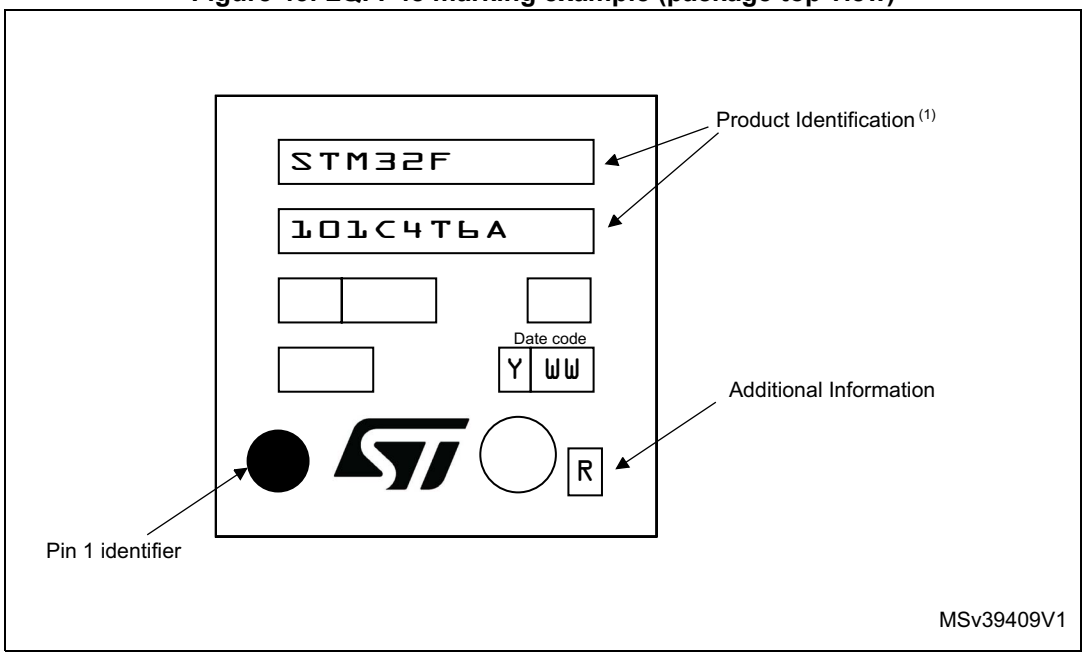


1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Device Marking for LQFP48

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 43. LQFP48 marking example (package top view)



1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

6.5.2 Evaluating the maximum junction temperature for an application

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Table 50: Ordering information scheme*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature. Here, only temperature range 6 is available (–40 to 85 °C).

The following example shows how to calculate the temperature range needed for a given application, making it possible to check whether the required temperature range is compatible with the STM32F101xx junction temperature range.

Example: high-performance application

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 8 I/Os used at the same time in output mode at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

P_{INTmax} = 50 mA × 3.5 V= 175 mW

P_{IOmax} = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW

P_{Dmax} = 175 + 272 = 447 mW

Thus: P_{Dmax} = 447 mW

Using the values obtained in *Table 49* T_{Jmax} is calculated as follows:

– For LQFP64, 45 °C/W

T_{Jmax} = 82 °C + (45 °C/W × 447 mW) = 82 °C + 20.1 °C = 102.1 °C

This is within the junction temperature range of the STM32F101xx (–40 < T_J < 105 °C).

Figure 44. LQFP64 P_D max vs. T_A