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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	48KB (24K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	3.8K x 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f2525t-i-so

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

NOTES:

TABLE 2-2:CAPACITOR SELECTION FOR
CRYSTAL OSCILLATOR

Osc Type	Crystal	Typical Capa Tes	acitor Values ted:
	Fieq	C1	C2
LP	32 kHz	30 pF	30 pF
ХТ	1 MHz 4 MHz	15 pF 15 pF	15 pF 15 pF
HS	4 MHz 10 MHz 20 MHz 25 MHz	15 pF 15 pF 15 pF 15 pF	15 pF 15 pF 15 pF 15 pF

Capacitor values are for design guidance only.

Different capacitor values may be required to produce acceptable oscillator operation. The user should test the performance of the oscillator over the expected VDD and temperature range for the application.

See the notes following this table for additional information.

- **Note 1:** Higher capacitance increases the stability of the oscillator but also increases the start-up time.
 - 2: When operating below 3V VDD, or when using certain ceramic resonators at any voltage, it may be necessary to use the HS mode or switch to a crystal oscillator.
 - Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.
 - Rs may be required to avoid overdriving crystals with low drive level specification.
 - **5:** Always verify oscillator performance over the VDD and temperature range that is expected for the application.

An external clock source may also be connected to the OSC1 pin in the HS mode, as shown in Figure 2-2.



2.3 External Clock Input

The EC and ECIO Oscillator modes require an external clock source to be connected to the OSC1 pin. There is no oscillator start-up time required after a Power-on Reset or after an exit from Sleep mode.

In the EC Oscillator mode, the oscillator frequency divided by 4 is available on the OSC2 pin. This signal may be used for test purposes or to synchronize other logic. Figure 2-3 shows the pin connections for the EC Oscillator mode.



EXTERNAL CLOCK INPUT OPERATION (EC CONFIGURATION)



The ECIO Oscillator mode functions like the EC mode, except that the OSC2 pin becomes an additional general purpose I/O pin. The I/O pin becomes bit 6 of PORTA (RA6). Figure 2-4 shows the pin connections for the ECIO Oscillator mode.

FIGURE 2-4:

EXTERNAL CLOCK INPUT OPERATION (ECIO CONFIGURATION)



2.7 Clock Sources and Oscillator Switching

Like previous PIC18 devices, the PIC18F2525/2620/ 4525/4620 family includes a feature that allows the device clock source to be switched from the main oscillator to an alternate, low-frequency clock source. PIC18F2525/2620/4525/4620 devices offer two alternate clock sources. When an alternate clock source is enabled, the various power-managed operating modes are available.

Essentially, there are three clock sources for these devices:

- Primary oscillators
- · Secondary oscillators
- Internal oscillator block

The **primary oscillators** include the External Crystal and Resonator modes, the External RC modes, the External Clock modes and the internal oscillator block. The particular mode is defined by the FOSC3:FOSC0 Configuration bits. The details of these modes are covered earlier in this chapter. The **secondary oscillators** are those external sources not connected to the OSC1 or OSC2 pins. These sources may continue to operate even after the controller is placed in a power-managed mode.

PIC18F2525/2620/4525/4620 devices offer the Timer1 oscillator as a secondary oscillator. This oscillator, in all power-managed modes, is often the time base for functions such as a Real-Time Clock (RTC).

Most often, a 32.768 kHz watch crystal is connected between the RC0/T1OSO/T13CKI and RC1/T1OSI pins. Like the LP Oscillator mode circuit, loading capacitors are also connected from each pin to ground.

The Timer1 oscillator is discussed in greater detail in **Section 12.3 "Timer1 Oscillator"**.

In addition to being a primary clock source, the **internal oscillator block** is available as a power-managed mode clock source. The INTRC source is also used as the clock source for several special features, such as the WDT and Fail-Safe Clock Monitor.

The clock sources for the PIC18F2525/2620/4525/4620 devices are shown in Figure 2-8. See **Section 23.0 "Special Features of the CPU"** for Configuration register details.





7.4 Erasing Flash Program Memory

The minimum erase block is 32 words or 64 bytes. Only through the use of an external programmer, or through ICSP control, can larger blocks of program memory be bulk erased. Word erase in the Flash array is not supported.

When initiating an erase sequence from the microcontroller itself, a block of 64 bytes of program memory is erased. The Most Significant 16 bits of the TBLPTR<21:6> point to the block being erased. TBLPTR<5:0> are ignored.

The EECON1 register commands the erase operation. The EEPGD bit must be set to point to the Flash program memory. The WREN bit must be set to enable write operations. The FREE bit is set to select an erase operation.

For protection, the write initiate sequence for EECON2 must be used.

A long write is necessary for erasing the internal Flash. Instruction execution is halted while in a long write cycle. The long write will be terminated by the internal programming timer.

7.4.1 FLASH PROGRAM MEMORY ERASE SEQUENCE

The sequence of events for erasing a block of internal program memory location is:

- 1. Load Table Pointer register with address of row being erased.
- 2. Set the EECON1 register for the erase operation:
 - set EEPGD bit to point to program memory;
 - clear the CFGS bit to access program memory;
 - set WREN bit to enable writes;
 - set FREE bit to enable the erase.
- 3. Disable interrupts.
- 4. Write 55h to EECON2.
- 5. Write 0AAh to EECON2.
- 6. Set the WR bit. This will begin the row erase cycle.
- 7. The CPU will stall for duration of the erase (about 2 ms using internal timer).
- 8. Re-enable interrupts.

	MOVLW MOVWF MOVLW MOVWF MOVLW	CODE_ADDR_UPPER TBLPTRU CODE_ADDR_HIGH TBLPTRH CODE_ADDR_LOW	; load TBLPTR with the base ; address of the memory block
	MOVWF	TBLPTRL	
ERASE_ROW			
	BSF	EECON1, EEPGD	; point to Flash program memory
	BCF	EECON1, CFGS	; access Flash program memory
	BSF	EECON1, WREN	; enable write to memory
	BSF	EECON1, FREE	; enable Row Erase operation
	BCF	INTCON, GIE	; disable interrupts
Required	MOVLW	55h	
Sequence	MOVWF	EECON2	; write 55h
	MOVLW	0AAh	
	MOVWF	EECON2	; write OAAh
	BSF	EECON1, WR	; start erase (CPU stall)
	BSF	INTCON, GIE	; re-enable interrupts

EXAMPLE 7-2: ERASING A FLASH PROGRAM MEMORY ROW

REGISTER 10-3: INTCON3: INTERRUPT CONTROL REGISTER 3

R/W-1	R/W-1	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
INT2IP	P INT1IP	_	INT2IE	INT1IE	—	INT2IF	INT1IF
bit 7							bit C
Legend:							
R = Read	able bit	W = Writable	bit	U = Unimplem	nented bit, rea	d as '0'	
-n = Value	e at POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown
1		-					
Dit /		External Interr	upt Priority bit				
	$\perp = Hign prid0 = Low prid$	rity					
bit 6	INT1IP: INT1	External Interr	upt Priority bit				
	1 = High prio	rity	, ,				
	0 = Low prior	rity					
bit 5	Unimplemen	ted: Read as '	כי				
bit 4	INT2IE: INT2	External Interr	upt Enable bit				
	1 = Enables	the INT2 extern	nal interrupt				
	0 = Disables	the INT2 extern	nal interrupt				
bit 3	INT1IE: INT1	External Interr	upt Enable bit				
	1 = Enables	the INT1 extern	nal interrupt				
bit 2	Unimplemen	ted: Read as '	na interrupt o'				
bit 1	INT2IF: INT2	External Interru	upt Flag bit				
	$1 = \text{The INT}_2$	external interr	upt occurred (must be cleared	d in software)		
	0 = The INT2	2 external interr	upt did not occ	cur	,		
bit 0	INT1IF: INT1	External Interru	upt Flag bit				
	1 = The INT	external interr	upt occurred (must be cleared	d in software)		
	0 = The INT	external interr	upt did not occ	cur			
Note:	Interrupt flag bits	are set when a	an interrupt co	ndition occurs.	regardless of	the state of its	corresponding
	enable bit or the	global interrupt	enable bit. Us	er software sho	uld ensure the	appropriate int	errupt flag bit
	are clear prior to	enabling an inte	errupt. This fea	ature allows for	software pollir	ng.	

16.4.4 HALF-BRIDGE MODE

In the Half-Bridge Output mode, two pins are used as outputs to drive push-pull loads. The PWM output signal is output on the P1A pin, while the complementary PWM output signal is output on the P1B pin (Figure 16-4). This mode can be used for half-bridge applications, as shown in Figure 16-5, or for full-bridge applications where four power switches are being modulated with two PWM signals.

In Half-Bridge Output mode, the programmable deadband delay can be used to prevent shoot-through current in half-bridge power devices. The value of bits, PDC6:PDC0, sets the number of instruction cycles before the output is driven active. If the value is greater than the duty cycle, the corresponding output remains inactive during the entire cycle. See **Section 16.4.6 "Programmable Dead-Band Delay"** for more details of the dead-band delay operations.

Since the P1A and P1B outputs are multiplexed with the PORTC<2> and PORTD<5> data latches, the TRISC<2> and TRISD<5> bits must be cleared to configure P1A and P1B as outputs.

FIGURE 16-4: HALF-BRIDGE PWM OUTPUT



FIGURE 16-5: EXAMPLES OF HALF-BRIDGE OUTPUT MODE APPLICATIONS



17.4 I²C Mode

The MSSP module in I^2C mode fully implements all master and slave functions (including general call support) and provides interrupts on Start and Stop bits in hardware to determine a free bus (multi-master function). The MSSP module implements the standard mode specifications, as well as 7-bit and 10-bit addressing.

Two pins are used for data transfer:

- Serial clock (SCL) RC3/SCK/SCL
- Serial data (SDA) RC4/SDI/SDA

The user must configure these pins as inputs or outputs through the TRISC<4:3> bits.

FIGURE 17-7: MSSP BLOCK DIAGRAM (I²C™ MODE)



17.4.1 REGISTERS

The MSSP module has six registers for $\mathsf{I}^2\mathsf{C}$ operation. These are:

- MSSP Control Register 1 (SSPCON1)
- MSSP Control Register 2 (SSPCON2)
- MSSP Status Register (SSPSTAT)
- Serial Receive/Transmit Buffer Register (SSPBUF)
- MSSP Shift Register (SSPSR) Not directly accessible
- MSSP Address Register (SSPADD)

SSPCON1, SSPCON2 and SSPSTAT are the control and status registers in I^2C mode operation. The SSPCON1 and SSPCON2 registers are readable and writable. The lower 6 bits of the SSPSTAT are read-only. The upper two bits of the SSPSTAT are read/write.

SSPSR is the shift register used for shifting data in or out. SSPBUF is the buffer register to which data bytes are written to or read from.

SSPADD register holds the slave device address when the MSSP is configured in I²C Slave mode. When the MSSP is configured in Master mode, the lower seven bits of SSPADD act as the Baud Rate Generator reload value.

In receive operations, SSPSR and SSPBUF together create a double-buffered receiver. When SSPSR receives a complete byte, it is transferred to SSPBUF and the SSPIF interrupt is set.

During transmission, the SSPBUF is not doublebuffered. A write to SSPBUF will write to both SSPBUF and SSPSR.

17.4.7 BAUD RATE

In I²C Master mode, the Baud Rate Generator (BRG) reload value is placed in the lower 7 bits of the SSPADD register (Figure 17-17). When a write occurs to SSPBUF, the Baud Rate Generator will automatically begin counting. The BRG counts down to '0' and stops until another reload has taken place. The BRG count is decremented twice per instruction cycle (TcY) on the Q2 and Q4 clocks. In I²C Master mode, the BRG is reloaded automatically.

Once the given operation is complete (i.e., transmission of the last data bit is followed by ACK), the internal clock will automatically stop counting and the SCL pin will remain in its last state.

Table 17-3 demonstrates clock rates based on instruction cycles and the BRG value loaded into SSPADD.

FIGURE 17-17: BAUD RATE GENERATOR BLOCK DIAGRAM



TABLE 17-3: I²C[™] CLOCK RATE W/BRG

Fosc	Fcy	Fcy * 2	BRG Value	FscL (2 Rollovers of BRG)
40 MHz	10 MHz	20 MHz	18h	400 kHz ⁽¹⁾
40 MHz	10 MHz	20 MHz	1Fh	312.5 kHz
40 MHz	10 MHz	20 MHz	63h	100 kHz
16 MHz	4 MHz	8 MHz	09h	400 kHz ⁽¹⁾
16 MHz	4 MHz	8 MHz	0Ch	308 kHz
16 MHz	4 MHz	8 MHz	27h	100 kHz
4 MHz	1 MHz	2 MHz	02h	333 kHz ⁽¹⁾
4 MHz	1 MHz	2 MHz	09h	100 kHz
4 MHz	1 MHz	2 MHz	00h	1 MHz ⁽¹⁾

Note 1: The I²C interface does not conform to the 400 kHz I²C specification (which applies to rates greater than 100 kHz) in all details, but may be used with care where higher rates are required by the application.

17.4.9 I²C MASTER MODE REPEATED START CONDITION TIMING

A Repeated Start condition occurs when the RSEN bit (SSPCON2<1>) is programmed high and the I²C logic module is in the Idle state. When the RSEN bit is set, the SCL pin is asserted low. When the SCL pin is sampled low, the Baud Rate Generator is loaded with the contents of SSPADD<5:0> and begins counting. The SDA pin is released (brought high) for one Baud Rate Generator count (TBRG). When the Baud Rate Generator times out, if SDA is sampled high, the SCL pin will be deasserted (brought high). When SCL is sampled high, the Baud Rate Generator is reloaded with the contents of SSPADD<6:0> and begins counting. SDA and SCL must be sampled high for one TBRG. This action is then followed by assertion of the SDA pin (SDA = 0) for one TBRG while SCL is high. Following this, the RSEN bit (SSPCON2<1>) will be automatically cleared and the Baud Rate Generator will not be reloaded, leaving the SDA pin held low. As soon as a Start condition is detected on the SDA and SCL pins, the S bit (SSPSTAT<3>) will be set. The SSPIF bit will not be set until the Baud Rate Generator has timed out.

- Note 1: If RSEN is programmed while any other event is in progress, it will not take effect.
 - **2:** A bus collision during the Repeated Start condition occurs if:
 - SDA is sampled low when SCL goes from low-to-high.
 - SCL goes low before SDA is asserted low. This may indicate that another master is attempting to transmit a data '1'.

Immediately following the SSPIF bit getting set, the user may write the SSPBUF with the 7-bit address in 7-bit mode, or the default first address in 10-bit mode. After the first eight bits are transmitted and an ACK is received, the user may then transmit an additional eight bits of address (10-bit mode) or eight bits of data (7-bit mode).

17.4.9.1 WCOL Status Flag

If the user writes the SSPBUF when a Repeated Start sequence is in progress, the WCOL is set and the contents of the buffer are unchanged (the write doesn't occur).

Note: Because queueing of events is not allowed, writing of the lower 5 bits of SSPCON2 is disabled until the Repeated Start condition is complete.

FIGURE 17-20: REPEAT START CONDITION WAVEFORM





FIGURE 18-7: ASYNCHRONOUS RECEPTION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INTOIE	RBIE	TMR0IF	INT0IF	RBIF	49
PIR1	PSPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	52
PIE1	PSPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	52
IPR1	PSPIP ⁽¹⁾	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	52
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	51
RCREG	EUSART R	leceive Regis	ster						51
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	51
BAUDCON	ABDOVF	RCIDL	RXDTP	TXCKP	BRG16		WUE	ABDEN	51
SPBRGH	EUSART B	aud Rate Ge	enerator Reg	gister High I	Byte				51
SPBRG	EUSART B	aud Rate Ge	enerator Reg	gister Low E	Byte				51

TABLE 18-6: REGISTERS ASSOCIATED WITH ASYNCHRONOUS RECEPTION

Legend: — = unimplemented locations read as '0'. Shaded cells are not used for asynchronous reception.

Note 1: These bits are unimplemented on 28-pin devices and read as '0'.

18.2.4 AUTO-WAKE-UP ON SYNC BREAK CHARACTER

During Sleep mode, all clocks to the EUSART are suspended. Because of this, the Baud Rate Generator is inactive and a proper byte reception cannot be performed. The auto-wake-up feature allows the controller to wake-up due to activity on the RX/DT line while the EUSART is operating in Asynchronous mode.

The auto-wake-up feature is enabled by setting the WUE bit (BAUDCON<1>). Once set, the typical receive sequence on RX/DT is disabled and the EUSART remains in an Idle state, monitoring for a wake-up event independent of the CPU mode. A wake-up event consists of a high-to-low transition on the RX/DT line. (This coincides with the start of a Sync Break or a Wake-up Signal character for the LIN protocol.)

Following a wake-up event, the module generates an RCIF interrupt. The interrupt is generated synchronously to the Q clocks in normal operating modes (Figure 18-8) and asynchronously, if the device is in Sleep mode (Figure 18-9). The interrupt condition is cleared by reading the RCREG register.

The WUE bit is automatically cleared once a low-tohigh transition is observed on the RX line following the wake-up event. At this point, the EUSART module is in Idle mode and returns to normal operation. This signals to the user that the Sync Break event is over.

18.4 EUSART Synchronous Slave Mode

Synchronous Slave mode is entered by clearing bit, CSRC (TXSTA<7>). This mode differs from the Synchronous Master mode in that the shift clock is supplied externally at the CK pin (instead of being supplied internally in Master mode). This allows the device to transfer or receive data while in any low-power mode.

18.4.1 EUSART SYNCHRONOUS SLAVE TRANSMISSION

The operation of the Synchronous Master and Slave modes is identical, except in the case of the Sleep mode.

If two words are written to the TXREG and then the SLEEP instruction is executed, the following will occur:

- a) The first word will immediately transfer to the TSR register and transmit.
- b) The second word will remain in the TXREG register.
- c) Flag bit, TXIF, will not be set.
- d) When the first word has been shifted out of TSR, the TXREG register will transfer the second word to the TSR and flag bit, TXIF, will now be set.
- e) If enable bit, TXIE, is set, the interrupt will wake the chip from Sleep. If the global interrupt is enabled, the program will branch to the interrupt vector.

To set up a Synchronous Slave Transmission:

- 1. Enable the synchronous slave serial port by setting bits, SYNC and SPEN, and clearing bit, CSRC.
- 2. Clear bits, CREN and SREN.
- 3. If interrupts are desired, set enable bit, TXIE.
- 4. If 9-bit transmission is desired, set bit, TX9.
- 5. Enable the transmission by setting enable bit, TXEN.
- 6. If 9-bit transmission is selected, the ninth bit should be loaded in bit, TX9D.
- 7. Start transmission by loading data to the TXREGx register.
- If using interrupts, ensure that the GIE and PEIE bits in the INTCON register (INTCON<7:6>) are set.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	49
PIR1	PSPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	52
PIE1	PSPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	52
IPR1	PSPIP ⁽¹⁾	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	52
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	51
TXREG	EUSART T	ransmit Regi	ister						51
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	51
BAUDCON	ABDOVF	RCIDL	RXDTP	TXCKP	BRG16	—	WUE	ABDEN	51
SPBRGH	EUSART B	Baud Rate Ge	enerator Re	gister High	Byte				51
SPBRG	EUSART B	aud Rate Ge	enerator Re	gister Low I	Byte				51

TABLE 18-9: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE TRANSMISSION

Legend: — = unimplemented, read as '0'. Shaded cells are not used for synchronous slave transmission.

Note 1: These bits are unimplemented on 28-pin devices and read as '0'.

23.3 Two-Speed Start-up

The Two-Speed Start-up feature helps to minimize the latency period from oscillator start-up to code execution by allowing the microcontroller to use the INTOSC oscillator as a clock source until the primary clock source is available. It is enabled by setting the IESO Configuration bit.

Two-Speed Start-up should be enabled only if the primary oscillator mode is LP, XT, HS or HSPLL (Crystal-Based modes). Other sources do not require an OST start-up delay; for these, Two-Speed Start-up should be disabled.

When enabled, Resets and wake-ups from Sleep mode cause the device to configure itself to run from the internal oscillator block as the clock source, following the time-out of the Power-up Timer after a Power-on Reset is enabled. This allows almost immediate code execution while the primary oscillator starts and the OST is running. Once the OST times out, the device automatically switches to PRI_RUN mode.

To use a higher clock speed on wake-up, the INTOSC or postscaler clock sources can be selected to provide a higher clock speed by setting bits, IRCF2:IRCF0, immediately after Reset. For wake-ups from Sleep, the INTOSC or postscaler clock sources can be selected by setting the IRCF2:IRCF0 bits prior to entering Sleep mode. In all other power-managed modes, Two-Speed Startup is not used. The device will be clocked by the currently selected clock source until the primary clock source becomes available. The setting of the IESO bit is ignored.

23.3.1 SPECIAL CONSIDERATIONS FOR USING TWO-SPEED START-UP

While using the INTOSC oscillator in Two-Speed Startup, the device still obeys the normal command sequences for entering power-managed modes, including multiple SLEEP instructions (refer to **Section 3.1.4 "Multiple Sleep Commands"**). In practice, this means that user code can change the SCS1:SCS0 bit settings or issue SLEEP instructions before the OST times out. This would allow an application to briefly wake-up, perform routine "housekeeping" tasks and return to Sleep before the device starts to operate from the primary oscillator.

User code can also check if the primary clock source is currently providing the device clocking by checking the status of the OSTS bit (OSCCON<3>). If the bit is set, the primary oscillator is providing the clock. Otherwise, the internal oscillator block is providing the clock during wake-up from Reset or Sleep mode.



Bit Clear	f			E
BCF f, b	{,a}			S
$\begin{array}{l} 0\leq f\leq 255\\ 0\leq b\leq 7\\ a\in [0,1] \end{array}$				c
$0 \rightarrow f < b >$				S
None				E
1001	bbba	ffff	ffff	
Bit 'b' in reg If 'a' is '0', t If 'a' is '1', t GPR bank. If 'a' is '0' a set is enab in Indexed mode wher Section 24 Bit-Oriente Literal Offe	gister 'f' is the Access the BSR i led, this i Literal O never f ≤ I.2.3 "By ed Instru set Mode	s cleared. ss Bank is is used to extended in nstruction ffset Addre 95 (5Fh). te-Oriente ctions in e" for deta	selected. select the struction operates essing See ed and Indexed ills.	v C
1				I
1				
Q2	Q3	3	Q4	
Read register 'f'	Proce Dat	ess a re	Write gister 'f'	
BCF F ion EG = C7 n EG = 47	FLAG_RE 7h ′h	G, 7,	0	E
	Bit Clear BCF f, b $0 \le f \le 255$ $0 \le b \le 7$ $a \in [0,1]$ $0 \rightarrow f < b>$ None 1001 Bit 'b' in reg If 'a' is '0', i If 'a' is '0' a set is enab in Indexed mode when Section 24 Bit-Oriente Literal Offe 1 1 2 Read register 'f' BCF I ion EG = C7 n EG = 47	Bit Clear fBCFf, b {,a} $0 \le f \le 255$ $0 \le b \le 7$ $a \in [0,1]$ $0 \rightarrow f < b >$ None1001bbbaBit 'b' in register 'f' isIf 'a' is '0', the AccessIf 'a' is '0', the AccessIf 'a' is '0' and the exist is enabled, this isin Indexed Literal Ofmode whenever $f \le$ Section 24.2.3 "ByBit-Oriented InstructionLiteral Offset Model11Q2Q3ReadProcessorregister 'f'DateBCFFLAG_REionEG =CG =47h	Bit Clear fBCFf, b {,a} $0 \le f \le 255$ $0 \le b \le 7$ $a \in [0,1]$ $0 \rightarrow f < b >$ None1001bbbafffBit 'b' in register 'f' is cleared.If 'a' is '0', the Access Bank isIf 'a' is '0', the Access Bank isIf 'a' is '0' and the extended inset is enabled, this instructionin Indexed Literal Offset Addredmode whenever $f \le 95$ (5Fh).Section 24.2.3 "Byte-OrientedBit-Oriented Instructions inLiteral Offset Mode" for deta11Q2Q3Readregister 'f'Dataregister 'f'DatarefBCFFLAG_REG, 7,ionEG =C7hneG =47h	Bit Clear fBCFf, b {,a} $0 \le f \le 255$ $0 \le b \le 7$ $a \in [0,1]$ $0 \rightarrow f cb>$ None1001bbbaffffffffBit 'b' in register 'f' is cleared.If 'a' is '0', the Access Bank is selected.If 'a' is '0', the Access Bank is selected.If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). SeeSection 24.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode" for details.11Q2Q3Q4ReadProcesswrite register 'f'BCFFLAG_REG, 7, 0ionEG =C7hneG =47h

BN		Branch if	Negative	
Synta	ax:	BN n		
Oper	ands:	-128 ≤ n ≤ ′	27	
Oper	ation:	if Negative (PC) + 2 + 2	bit is '1', 2n → PC	
Statu	is Affected:	None		
Enco	oding:	1110	0110 nn	nn nnnn
Desc	ription:	If the Negar program wi The 2's con added to the incremente instruction, PC + 2 + 2r two-cycle ir	tive bit is '1', t Il branch. nplement nun e PC. Since th d to fetch the the new addr n. This instruction.	hen the nber '2n' is ne PC will have next ess will be tion is then a
Word	ls:	1		
Cycle	es:	1(2)		
Q C If Ju	ycle Activity: Imp:			
	Q1	Q2	Q3	Q4
	Decode	Read literal 'n'	Process Data	Write to PC
	No operation	No operation	No operation	No operation
lf No	o Jump:			
	Q1	Q2	Q3	Q4
	Decode	Read literal 'n'	Process Data	No operation
Exan	nple:	HERE	BN Jump	
	Before Instruc PC After Instructio If Negativ PC If Negativ PC	tion = ad on = 1; /e = 1; /e = 0; /e = 0;	dress (HERE dress (Jump dress (HERE)))+2))

CPF	SGT	Compare	f with W, Sk	ip if f > W
Synta	ax:	CPFSGT	f {,a}	
Oper	ands:	0 ≤ f ≤ 255 a ∈ [0,1]		
Oper	ation:	(f) – (W), skip if (f) > (unsigned c	(W) comparison)	
Statu	s Affected:	None		
Enco	ding:	0110	010a fff	ff ffff
Desc	ription:	Compares to location 'f' to performing If the contection in executed in two-cycle in If 'a' is '0', to If 'a' is '0', to If 'a' is '0', to GPR bank. If 'a' is '0' a set is enabli in Indexed mode when Section 24 Bit-Orientection	the contents of the contents of the contents an unsigned s nts of 'f' are gro WREG, then the sidiscarded ar istead, making histruction. The Access Bar he BSR is used and the extended led, this instruct Literal Offset A never $f \le 95$ (5F .2.3 "Byte-Ori and Instructions set Mode" for	data memory of the W by ubtraction. eater than the the fetched and a NOP is this a hk is selected. d to select the ed instruction ction operates addressing Fh). See ented and s in Indexed details.
Word	ls:	1		
Cycle	es:	1(2) Note: 3 cy by a	cles if skip and 2-word instrue	d followed ction.
QC	ycle Activity:			
	Q1	Q2	Q3	Q4
	Decode	Read	Process	No
lf sk	in [.]	register i	Dala	operation
ii on	Q1	Q2	Q3	Q4
	No	No	No	No
	operation	operation	operation	operation
lf sk	ip and followed	d by 2-word in	struction:	
	Q1	Q2	Q3	Q4
	NO	NO	NO	NO
	No	No	No	No
	operation	operation	operation	operation
<u>Exan</u>	nple:	HERE NGREATER GREATER	CPFSGT RE : :	G, 0
	Refore Instruc	tion		
	PC	= Ad	dress (HERE)
	W	= ?		
	After Instructio	n		
	If REG	> W;		
	PC	= Ad	dress (GREAT	FER)
	If REG PC	≤ W; = Ad	dress (NGREA	ATER)

CPF	SLT	Compare	f with W	, Skip	if f < W
Synta	ax:	CPFSLT	f {,a}		
Oper	ands:	0 ≤ f ≤ 255 a ∈ [0,1]			
Oper	ation:	(f) – (W), skip if (f) < (unsigned o	(W) compariso	n)	
Statu	s Affected:	None			
Enco	ding:	0110	000a	ffff	ffff
Desc	ription:	Compares i location 'f' t performing If the conte contents of instruction i executed in two-cycle ir If 'a' is '0', t If 'a' is '1', t GPR bank.	the conten o the cont an unsign nts of 'f' a W, then th is discarde istead, ma istruction. he Access he BSR is	ts of dat ents of ' ed subtr re less t he fetch ed and a king this s Bank is used to	ta memory W by raction. han the ed n NOP is s a s selected. s select the
Word	s:	1			
Cycle	es:	1(2) Note: 3 c by	ycles if sk a 2-word i	ip and fo	ollowed on.
QC	ycle Activity:				
	Q1	Q2	Q3		Q4
	Decode	Read register 'f'	Proces Data	s c	No operation
lf sk	ip:				
	Q1	Q2	Q3		Q4
	No	No	No		No
	operation	operation	operatio	on c	peration
lt sk	ip and followed	d by 2-word in	struction:		04
ĺ	Q1	Q2	Q3		Q4
	operation	operation	operatio	on c	operation
	No	No	No		No
	operation	operation	operatio	on c	peration
Exam	<u>iple:</u>	HERE (NLESS LESS	CPFSLT F : :	EG, 1	
	Before Instruc	tion			
	PC W	= Ad	ldress (H	ERE)	
	After Instructio	n – :			
	If REG	< W:			
	PC	= Ad	ldress (L	ESS)	
	If REG	≥ W;	drase (N		
		- A0	GIUGO (II	ן מטייי	

c: nds: tion: Affected: ing: ption: ::	MULLW $0 \le k \le 254$ (W) x k \rightarrow None 0000 An unsign out betwee 8-bit literal placed in t pair. PROI W is unch None of th Note that n possible in is possible 1	k 5 PRODH:PRO 1101 kk ed multiplicatio en the contents 1 'k'. The 16-bit he PRODH:PF DH contains th anged. ee Status flags neither Overflo n this operation e but not detect	DL kk kkkk on is carried s of W and the result is RODL register e high byte. are affected. w nor Carry is A Zero result ted.	
nds: tion: Affected: ing: ption:	$0 \le k \le 25$ (W) x k \rightarrow None An unsign out betwee 8-bit literal placed in t pair. PROI W is unch None of th Note that n possible in is possible 1	5 PRODH:PRO 1101 kk ed multiplicatio en the contents I 'k'. The 16-bit the PRODH:PF DH contains th anged. the Status flags neither Overflo this operation e but not detect	DL kk kkkk on is carried s of W and the result is RODL register e high byte. are affected. w nor Carry is A Zero result ted.	
tion: Affected: ing: ption: ::	 (W) x k → None 0000 An unsign out betwee 8-bit literal placed in t pair. PROI W is unchas None of th Note that n possible in is possible 1 	PRODH:PRO	DL kk kkkk on is carried s of W and the result is RODL register e high byte. are affected. w nor Carry is A Zero result ted.	
Affected: ing: ption: ::	None 0000 An unsign out betwee 8-bit literal placed in t pair. PROI W is unch None of th Note that n possible in is possible 1	1101 kk ed multiplicatio en the contents 1 'k'. The 16-bit the PRODH:PF DH contains th anged. the Status flags neither Overflo this operation this operation	kk kkkk on is carried s of W and the result is RODL register e high byte. are affected. w nor Carry is A Zero result ted.	
ing: ption: ::	0000 An unsign out betwee 8-bit literal placed in t pair. PROI W is unch None of th Note that i possible in is possible 1	1101 kk ed multiplicatio en the contents i 'k'. The 16-bit the PRODH:PF DH contains th anged. the Status flags neither Overflo this operation but not detect	kk kkkk on is carried s of W and the result is RODL register e high byte. are affected. w nor Carry is A Zero result ted.	
ption: :: s:	An unsign out betwee 8-bit literal placed in t pair. PROI W is unch None of th Note that n possible ir is possible 1	ed multiplicatic en the contents I 'k'. The 16-bit he PRODH:PF DH contains th anged. le Status flags neither Overflo n this operation e but not detect	on is carried s of W and the result is RODL register e high byte. are affected. w nor Carry is A Zero result ted.	
:: 5:	1 1			
S:	1			
cle Activity:				
Q1	Q2	Q3	Q4	
Decode	Read literal 'k'	Process Data	Write registers PRODH: PRODL	
ole:	MULLW	0C4h		
efore Instruc	tion			
W PRODH PRODL fter Instructio	= E = ? = ?	2h		
W PRODH PRODL	= E = A = 08	2h Dh 8h		
D Se	le: efore Instruc PRODH PRODL ter Instructio W PRODH PRODL	literal 'k' literal 'k' literal 'k' efore Instruction W = E PRODL = ? PRODL = ? ter Instruction W = E PRODH = A PRODH = 0	Iteral 'k' Data literal 'k' Data literal 'k' Data efore Instruction 0C4h W = PRODH = PRODL = V = Etal 'k' Data	Iteral 'k' Data registers PRODH: PRODH: le: MULLW 0C4h efore Instruction W = W = E2h PRODH = PRODL = 'ter Instruction W = E2h PRODL = PRODL = W = E2h PRODL = PRODH = 08h

MULWF	Multiply	W with f	
Syntax:	MULWF	f {,a}	
Operands:	0 ≤ f ≤ 255 a ∈ [0,1]	5	
Operation:	(W) x (f) –	> PRODH:PR	ODL
Status Affected:	None		
Encoding:	0000	001a ff	ff ffff
Description:	An unsign out betwee register file result is st register pa high byte. unchange None of th Note that r possible ir result is po If 'a' is '0', selected. I to select th If 'a' is '0' a set is enal operates i Addressin $f \le 95$ (5FF "Byte-Orie Instructio Mode" for	ed multiplication en the contents e location 'f'. T ored in the PR air. PRODH co Both W and 'f d. the Status flags neither Overflo the Access B f 'a' is '1', the en GPR bank. and the extend oled, this instru- n Indexed Lite g mode when any. See Section ented and Bit ns in Indexed details.	on is carried s of W and the The 16-bit CODH:PRODL Intains the are affected. w nor Carry is n. A Zero t detected. ank is BSR is used ded instruction uction ral Offset ever n 24.2.3 -Oriented Literal Offset
Words:	1		
Cycles:	1		
Q Cycle Activity:			
Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write registers PRODH: PRODL
Example:	MIT ME	DEC 1	
Before Instruc	tion	REG, I	
W REG PRODH PRODL After Instructio	= C4 = B5 = ? = ?	lh h	
W REG PRODH PRODL	= C4 = B5 = 8A = 94	lh ih h h	





TABLE 26-12: CAPTURE/COMPARE/PWM REQUIREMENTS (ALL CCP MODULES)

Param No.	Symbol	с	haracteristi	c	Min	Max	Units	Conditions	
50	TccL	CCPx Input Low	No prescal	er	0.5 TCY + 20		ns		
		Time	With	PIC18FXXXX	10		ns		
			prescaler	PIC18LFXXXX	20		ns	VDD = 2.0V	
51	TccH	CCPx Input	No prescale	er	0.5 TCY + 20		ns		
		High Time	With	PIC18FXXXX	10	_	ns		
			prescaler	PIC18LFXXXX	20	-	ns	VDD = 2.0V	
52	TccP	CCPx Input Perio	bd		<u>3 Tcy + 40</u> N	_	ns	N = prescale value (1, 4 or 16)	
53	TccR	CCPx Output Fa	ll Time	PIC18FXXXX	—	25	ns		
				PIC18LFXXXX	_	45	ns	VDD = 2.0V	
54	TccF	CCPx Output Fa	ll Time	PIC18FXXXX	—	25	ns		
				PIC18LFXXXX	_	45	ns	VDD = 2.0V	

FIGURE 27-9: TYPICAL WDT CURRENT vs. VDD ACROSS TEMPERATURE (WDT DELTA CURRENT IN SLEEP MODE)



FIGURE 27-10: MAXIMUM WDT CURRENT vs. VDD ACROSS TEMPERATURE (WDT DELTA CURRENT IN SLEEP MODE)



44-Lead Plastic Quad Flat, No Lead Package (ML) – 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging







	Units		MILLIMETERS	3
Dimensio	n Limits	MIN	NOM	MAX
Number of Pins	Ν		44	
Pitch	е	0.65 BSC		
Overall Height	А	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E	8.00 BSC		
Exposed Pad Width	E2	6.30	6.45	6.80
Overall Length	D	8.00 BSC		
Exposed Pad Length	D2	6.30	6.45	6.80
Contact Width	b	0.25	0.30	0.38
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	К	0.20	-	_

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Package is saw singulated.

3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

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