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Details

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Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	48KB (24K × 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	3.8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf4525t-i-ml

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Pin Name	Pin Number	Pin	Buffer	Description
	SPDIP, SOIC	Туре	Туре	Description
				PORTA is a bidirectional I/O port.
RA0/AN0 RA0 AN0	2	I/O I	TTL Analog	Digital I/O. Analog input 0.
RA1/AN1 RA1 AN1	3	I/O I	TTL Analog	Digital I/O. Analog input 1.
RA2/AN2/VREF-/CVREF RA2 AN2 VREF- CVREF	4	I/O I I O	TTL Analog Analog Analog	Digital I/O. Analog input 2. A/D reference voltage (low) input. Comparator reference voltage output.
RA3/AN3/VREF+ RA3 AN3 VREF+	5	I/O I I	TTL Analog Analog	Digital I/O. Analog input 3. A/D reference voltage (high) input.
RA4/T0CKI/C1OUT RA4 T0CKI C1OUT	6	I/O I O	ST ST	Digital I/O. Timer0 external clock input. Comparator 1 output.
RA5/AN4/SS/HLVDIN/ C2OUT RA5 AN4 SS HLVDIN C2OUT	7	I/O 0	TTL Analog TTL Analog —	Digital I/O. Analog input 4. SPI slave select input. High/Low-Voltage Detect input. Comparator 2 output.
RA6				See the OSC2/CLKO/RA6 pin.
RA7				See the OSC1/CLKI/RA7 pin.
Legend: TTL = TTL co	mpatible inpu	t		CMOS = CMOS compatible input or output
ST = Schmit O = Output	t Trigger inpu	t with CI	MOS lev	els I = Input P = Power

TABLE 1-2: PIC18F2525/2620 PINOUT I/O DESCRIPTIONS (CONTINUED)

Note 1: Default assignment for CCP2 when the CCP2MX Configuration bit is set.

2: Alternate assignment for CCP2 when the CCP2MX Configuration bit is cleared.

NOTES:

7.2.2 TABLAT – TABLE LATCH REGISTER

The Table Latch (TABLAT) is an 8-bit register mapped into the SFR space. The Table Latch register is used to hold 8-bit data during data transfers between program memory and data RAM.

7.2.3 TBLPTR – TABLE POINTER REGISTER

The Table Pointer (TBLPTR) register addresses a byte within the program memory. The TBLPTR is comprised of three SFR registers: Table Pointer Upper Byte, Table Pointer High Byte and Table Pointer Low Byte (TBLPTRU:TBLPTRH:TBLPTRL). These three registers join to form a 22-bit wide pointer. The low-order 21 bits allow the device to address up to 2 Mbytes of program memory space. The 22nd bit allows access to the Device ID, the user ID and the Configuration bits.

The Table Pointer register, TBLPTR, is used by the TBLRD and TBLWT instructions. These instructions can update the TBLPTR in one of four ways based on the table operation. These operations are shown in Table 7-1. These operations on the TBLPTR only affect the low-order 21 bits.

7.2.4 TABLE POINTER BOUNDARIES

TBLPTR is used in reads, writes and erases of the Flash program memory.

When a TBLRD is executed, all 22 bits of the TBLPTR determine which byte is read from program memory into TABLAT.

When a TBLWT is executed, the six LSbs of the Table Pointer register (TBLPTR<5:0>) determine which of the 64 program memory holding registers is written to. When the timed write to program memory begins (via the WR bit), the 16 MSbs of the TBLPTR (TBLPTR<21:6>) determine which program memory block of 64 bytes is written to. For more detail, see **Section 7.5 "Writing to Flash Program Memory"**.

When an erase of program memory is executed, the 16 MSbs of the Table Pointer register (TBLPTR<21:6>) point to the 64-byte block that will be erased. The Least Significant bits (TBLPTR<5:0>) are ignored.

Figure 7-3 describes the relevant boundaries of TBLPTR based on Flash program memory operations.

TABLE 7-1	TABLE POINTER OPERATIONS WITH TRUED AND TRUET INSTRUCTIONS

Example	Operation on Table Pointer						
TBLRD* TBLWT*	TBLPTR is not modified						
TBLRD*+ TBLWT*+	TBLPTR is incremented after the read/write						
TBLRD*- TBLWT*-	TBLPTR is decremented after the read/write						
TBLRD+* TBLWT+*	TBLPTR is incremented before the read/write						

FIGURE 7-3: TABLE POINTER BOUNDARIES BASED ON OPERATION



NOTES:

16.4.4 HALF-BRIDGE MODE

In the Half-Bridge Output mode, two pins are used as outputs to drive push-pull loads. The PWM output signal is output on the P1A pin, while the complementary PWM output signal is output on the P1B pin (Figure 16-4). This mode can be used for half-bridge applications, as shown in Figure 16-5, or for full-bridge applications where four power switches are being modulated with two PWM signals.

In Half-Bridge Output mode, the programmable deadband delay can be used to prevent shoot-through current in half-bridge power devices. The value of bits, PDC6:PDC0, sets the number of instruction cycles before the output is driven active. If the value is greater than the duty cycle, the corresponding output remains inactive during the entire cycle. See **Section 16.4.6 "Programmable Dead-Band Delay"** for more details of the dead-band delay operations.

Since the P1A and P1B outputs are multiplexed with the PORTC<2> and PORTD<5> data latches, the TRISC<2> and TRISD<5> bits must be cleared to configure P1A and P1B as outputs.

FIGURE 16-4: HALF-BRIDGE PWM OUTPUT



FIGURE 16-5: EXAMPLES OF HALF-BRIDGE OUTPUT MODE APPLICATIONS



17.3.5 MASTER MODE

The master can initiate the data transfer at any time because it controls the SCK. The master determines when the slave (Processor 2, Figure 17-2) is to broadcast data by the software protocol.

In Master mode, the data is transmitted/received as soon as the SSPBUF register is written to. If the SPI operation is only going to receive, the SDO output could be disabled (programmed as an input). The SSPSR register will continue to shift in the signal present on the SDI pin at the programmed clock rate. As each byte is received, it will be loaded into the SSPBUF register as if a normal received byte (interrupts and status bits appropriately set). This could be useful in receiver applications as a "Line Activity Monitor" mode. The clock polarity is selected by appropriately programming the CKP bit (SSPCON1<4>). This then, would give waveforms for SPI communication, as shown in Figure 17-3, Figure 17-5 and Figure 17-6, where the MSB is transmitted first. In Master mode, the SPI clock rate (bit rate) is user programmable to be one of the following:

- Fosc/4 (or Tcy)
- Fosc/16 (or 4 Tcy)
- Fosc/64 (or 16 Tcy)
- Timer2 output/2

This allows a maximum data rate (at 40 MHz) of 10.00 Mbps.

Figure 17-3 shows the waveforms for Master mode. When the CKE bit is set, the SDO data is valid before there is a clock edge on SCK. The change of the input sample is shown based on the state of the SMP bit. The time when the SSPBUF is loaded with the received data is shown.



FIGURE 17-3: SPI MODE WAVEFORM (MASTER MODE)

17.4.5 GENERAL CALL ADDRESS SUPPORT

The addressing procedure for the I²C bus is such that the first byte after the Start condition usually determines which device will be the slave addressed by the master. The exception is the general call address which can address all devices. When this address is used, all devices should, in theory, respond with an Acknowledge.

The general call address is one of eight addresses reserved for specific purposes by the I^2C protocol. It consists of all '0's with R/W = 0.

The general call address is recognized when the General Call Enable bit, GCEN, is enabled (SSPCON2<7> is set). Following a Start bit detect, 8 bits are shifted into the SSPSR and the address is compared against the SSPADD. It is also compared to the general call address and fixed in hardware.

If the general call address matches, the SSPSR is transferred to the SSPBUF, the BF flag bit is set (eighth bit) and on the falling edge of the ninth bit (ACK bit), the SSPIF interrupt flag bit is set.

When the interrupt is serviced, the source for the interrupt can be checked by reading the contents of the SSPBUF. The value can be used to determine if the address was device specific or a general call address.

In 10-bit mode, the SSPADD is required to be updated for the second half of the address to match and the UA bit (SSPSTAT<1>) is set. If the general call address is sampled when the GCEN bit is set, while the slave is configured in 10-Bit Addressing mode, then the second half of the address is not necessary, the UA bit will not be set and the slave will begin receiving data after the Acknowledge (Figure 17-15).





17.4.6.1 I²C Master Mode Operation

The master device generates all of the serial clock pulses and the Start and Stop conditions. A transfer is ended with a Stop condition or with a Repeated Start condition. Since the Repeated Start condition is also the beginning of the next serial transfer, the I²C bus will not be released.

In Master Transmitter mode, serial data is output through SDA, while SCL outputs the serial clock. The first byte transmitted contains the slave address of the receiving device (7 bits) and the Read/Write (R/W) bit. In this case, the R/W bit will be logic '0'. Serial data is transmitted 8 bits at a time. After each byte is transmitted, an Acknowledge bit is received. Start and Stop conditions are output to indicate the beginning and the end of a serial transfer.

In Master Receive mode, the first byte transmitted contains the slave address of the transmitting device (7 bits) and the R/W bit. In this case, the R/W bit will be logic '1'. Thus, the first byte transmitted is a 7-bit slave address followed by a '1' to indicate the receive bit. Serial data is received via SDA, while SCL outputs the serial clock. Serial data is received 8 bits at a time. After each byte is received, an Acknowledge bit is transmitted. Start and Stop conditions indicate the beginning and end of transmission.

The Baud Rate Generator used for the SPI mode operation is used to set the SCL clock frequency for either 100 kHz, 400 kHz or 1 MHz I²C operation. See **Section 17.4.7 "Baud Rate"** for more detail.

A typical transmit sequence would go as follows:

- 1. The user generates a Start condition by setting the Start Enable bit, SEN (SSPCON2<0>).
- 2. SSPIF is set. The MSSP module will wait the required start time before any other operation takes place.
- 3. The user loads the SSPBUF with the slave address to transmit.
- 4. Address is shifted out the SDA pin until all 8 bits are transmitted.
- 5. The MSSP module shifts in the ACK bit from the slave device and writes its value into the SSPCON2 register.
- 6. The MSSP module generates an interrupt at the end of the ninth clock cycle by setting the SSPIF bit.
- 7. The user loads the SSPBUF with eight bits of data.
- 8. Data is shifted out the SDA pin until all 8 bits are transmitted.
- The MSSP module shifts in the ACK bit from the slave device and writes its value into the SSPCON2 register.
- 10. The MSSP module generates an interrupt at the end of the ninth clock cycle by setting the SSPIF bit.
- 11. The user generates a Stop condition by setting the Stop Enable bit, PEN (SSPCON2<2>).
- 12. Interrupt is generated once the Stop condition is complete.

17.4.8 I²C MASTER MODE START CONDITION TIMING

To initiate a Start condition, the user sets the Start Enable bit, SEN (SSPCON2<0>). If the SDA and SCL pins are sampled high, the Baud Rate Generator is reloaded with the contents of SSPADD<6:0> and starts its count. If SCL and SDA are both sampled high when the Baud Rate Generator times out (TBRG), the SDA pin is driven low. The action of the SDA being driven low while SCL is high is the Start condition and causes the S bit (SSPSTAT<3>) to be set. Following this, the Baud Rate Generator is reloaded with the contents of SSPADD<6:0> and resumes its count. When the Baud Rate Generator times out (TBRG), the SEN bit (SSPCON2<0>) will be automatically cleared by hardware; the Baud Rate Generator is suspended, leaving the SDA line held low and the Start condition is complete.

Note: If at the beginning of the Start condition, the SDA and SCL pins are already sampled low, or if during the Start condition, the SCL line is sampled low before the SDA line is driven low, a bus collision occurs, the Bus Collision Interrupt Flag, BCLIF, is set, the Start condition is aborted and the I²C module is reset into its Idle state.

17.4.8.1 WCOL Status Flag

If the user writes the SSPBUF when a Start sequence is in progress, the WCOL is set and the contents of the buffer are unchanged (the write doesn't occur).

Note: Because queueing of events is not allowed, writing to the lower 5 bits of SSPCON2 is disabled until the Start condition is complete.



FIGURE 17-19: FIRST START BIT TIMING

NOTES:

		SYNC = 0, BRGH = 0, BRG16 = 0												
BAUD	Fosc = 40.000 MHz			Fosc = 20.000 MHz			Fosc = 10.000 MHz			Fosc = 8.000 MHz				
(K)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)		
0.3	_	_			_	_		_	_	_	_			
1.2	—	—	—	1.221	1.73	255	1.202	0.16	129	1.201	-0.16	103		
2.4	2.441	1.73	255	2.404	0.16	129	2.404	0.16	64	2.403	-0.16	51		
9.6	9.615	0.16	64	9.766	1.73	31	9.766	1.73	15	9.615	-0.16	12		
19.2	19.531	1.73	31	19.531	1.73	15	19.531	1.73	7	—	_	_		
57.6	56.818	-1.36	10	62.500	8.51	4	52.083	-9.58	2	—	_	_		
115.2	125.000	8.51	4	104.167	-9.58	2	78.125	-32.18	1	—	_	_		

TABLE 18-3: BAUD RATES FOR ASYNCHRONOUS MODES

		SYNC = 0, BRGH = 0, BRG16 = 0											
BAUD	Fos	c = 4.000	MHz	Fos	c = 2.000	MHz	Fosc = 1.000 MHz						
(K)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)				
0.3	0.300	0.16	207	0.300	-0.16	103	0.300	-0.16	51				
1.2	1.202	0.16	51	1.201	-0.16	25	1.201	-0.16	12				
2.4	2.404	0.16	25	2.403	-0.16	12	—	—	—				
9.6	8.929	-6.99	6	—	—	—	—	—	—				
19.2	20.833	8.51	2	—	_	—	—	_	_				
57.6	62.500	8.51	0	—	_	_	—	_	_				
115.2	62.500	-45.75	0	—	—	—	—	—	—				

		SYNC = 0, BRGH = 1, BRG16 = 0												
BAUD	Fosc = 40.000 MHz			Fosc = 20.000 MHz			Fosc = 10.000 MHz			Fosc = 8.000 MHz				
(К)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)		
0.3	_	_	_	_	_	_	_	_	_	—	_	_		
1.2	—	—	—	—	—	—	—	—	—	—	—	—		
2.4	-	_	—	—	_	—	2.441	1.73	255	2.403	-0.16	207		
9.6	9.766	1.73	255	9.615	0.16	129	9.615	0.16	64	9.615	-0.16	51		
19.2	19.231	0.16	129	19.231	0.16	64	19.531	1.73	31	19.230	-0.16	25		
57.6	58.140	0.94	42	56.818	-1.36	21	56.818	-1.36	10	55.555	3.55	8		
115.2	113.636	-1.36	21	113.636	-1.36	10	125.000	8.51	4	—	—	_		

		SYNC = 0, BRGH = 1, BRG16 = 0										
BAUD	Fost	c = 4.000	MHz	Fos	c = 2.000	MHz	Fosc = 1.000 MHz					
(К)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)			
0.3	—	_	_		_	_	0.300	-0.16	207			
1.2	1.202	0.16	207	1.201	-0.16	103	1.201	-0.16	51			
2.4	2.404	0.16	103	2.403	-0.16	51	2.403	-0.16	25			
9.6	9.615	0.16	25	9.615	-0.16	12	—	_	—			
19.2	19.231	0.16	12	—	_	_	—	_	—			
57.6	62.500	8.51	3	—	—	—	—	—	—			
115.2	125.000	8.51	1	_	_	_	_	—	_			

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REGISTER 23-14: WDTCON: WATCHDOG TIMER CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	SWDTEN ⁽¹⁾
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-1	Unimplemented: Read as '0'
1.11.0	

bit 0 SWDTEN: Software Controlled Watchdog Timer Enable bit⁽¹⁾

- 1 = Watchdog Timer is on
- 0 = Watchdog Timer is off

Note 1: This bit has no effect if the Configuration bit, WDTEN, is enabled.

TABLE 23-2: SUMMARY OF WATCHDOG TIMER REGISTERS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
RCON	IPEN	SBOREN ⁽¹⁾		RI	TO	PD	POR	BOR	50
WDTCON		—	_				_	SWDTEN	50

Legend: — = unimplemented, read as '0'. Shaded cells are not used by the Watchdog Timer.

Note 1: The SBOREN bit is only available when the BOREN1:BOREN0 Configuration bits = 01; otherwise, it is disabled and reads as '0'. See Section 4.4 "Brown-out Reset (BOR)".

COMF	Complement f	CPFSEQ Compare f with W, Skip if f = W						
Syntax:	COMF f {,d {,a}}		C	CPFSEQ f {,a}				
Operands:	0 ≤ f ≤ 255 d ∈ [0,1]	Operands	: 0 a	≤ f ≤ 255 ∈ [0,1]				
	a ∈ [0,1]	Operation	: (f)) – (W),	(14/)			
Operation:	$(\overline{f}) \rightarrow dest$		SK (U	skip if (f) = (W) (unsigned comparison)				
Status Affected:	N, Z	Status Affe	ected: N	one	,			
Encoding:	0001 11da ffff fi	Encoding:	:	0110	001a ff:	ff ffff		
Description: Words: Cycles: Q Cycle Activity:	The contents of register 'f' are complemented. If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in register 'f' (default). If 'a' is '0', the Access Bank is sele If 'a' is '1', the BSR is used to select GPR bank. If 'a' is '0' and the extended instruct set is enabled, this instruction ope in Indexed Literal Offset Addressin mode whenever $f \le 95$ (5Fh). See Section 24.2.3 "Byte-Oriented an Bit-Oriented Instructions in Index Literal Offset Mode" for details. 1	Descriptio ed. he on es sd	n: C lo pe ff di in in If G G If S E L	ompares i cation 'f' t erforming 'f' = W, th scarded a stead, ma struction. 'a' is '0', t 'a' is '0', t 'a' is '0', t 'a' is '0' a et is enabl Indexed ode wher ection 24 it-Oriente iteral Offs	the contents of o the contents an unsigned s en the fetchec and a NOP is ex- aking this a two he Access Bai he BSR is use nd the extende led, this instruc- Literal Offset A never $f \le 95$ (50 .2.3 "Byte-Or ed Instruction set Mode" for	f data memory of W by subtraction. I instruction is xecuted o-cycle nk is selected. d to select the ed instruction ction operates Addressing Fh). See iented and s in Indexed details.		
	02 03 04	Words:	1					
Decode	Read Process Write register 'f' Data destina	n Cycles:	1(N /	2) ote: 3 c by ;	ycles if skip ar a 2-word instru	nd followed		
		Q Cycle /	Activity:	5				
Example:	COMF REG, 0, 0		Q1	Q2	Q3	Q4		
Before Instruc	tion	D	ecode	Read	Process	No		
REG After Instructio	= 13n on	lf skin:	re	gister T	Data	operation		
REG	= 13h	n okip.	Q1	Q2	Q3	Q4		
W	= ECh		No	No	No	No		
		ор	eration or	peration	operation	operation		
		If skip an	d followed by	2-word in	struction:	04		
			No	No	No	No		
		ор	eration or	peration	operation	operation		
			No	No	No	No		
		ор	eration op	peration	operation	operation		
		Example:	HI NJ E(ERE EQUAL SIIAT.	CPFSEQ REG : :	B, O		
		Befor After	re Instruction PC Address W REG Instruction If REG PC If REG	= HE = ? = ? = Ad ≠ W;	RE Idress (Equa	L)		
			PC	= Ad	Idress (NEQU	AL)		

LFS	R	Load FSF	R		MOVF		Move f			
Synta	ax:	LFSR f, k			Syntax:		MOVF f {,d {,a}}			
Oper	ands:	$\begin{array}{l} 0 \leq f \leq 2 \\ 0 \leq k \leq 409 \end{array}$	5		Operand	s:	$\begin{array}{l} 0\leq f\leq 255\\ d\in[0,1] \end{array}$			
Oper	ation:	$k\toFSRf$					a ∈ [0,1]			
Statu	s Affected:	None			Operatio	n:	$f \rightarrow dest$			
Enco	ding:	1110 1111	1110 00 0000 k ₇ k	ff k ₁₁ kkk kk kkkk	Status A Encoding	ffected: g:	N, Z	00da f	Efff	ffff
Desc	Description: The 12-bit literal 'k' is loaded into the File Select Register pointed to by 'f'.				Descript	on:	The conten a destinatio	ts of registe n depender	r 'f' are nt upon	moved to the
Word	ls:	2				status of 'd'. If 'd' is '0', the result is				
Cycle	es:	2					placed in w	k in register	f' (defa	ault).
QC	ycle Activity:						Location 'f'	can be any	where i	n the
	Q1	Q2	Q3	Q4			256-byte ba	ank. he Access F	Rank ie	soloctod
	Decode	Read literal 'k' MSB	Process Data	Write literal 'k' MSB to FSRfH			If 'a' is '1', the GPR bank. If 'a' is '0' a set is enable	select the struction		
	Decode	Read literal 'k' LSB	Process Data	Write literal 'k' to FSRfL			in Indexed I mode when	Literal Offse ever $f \le 95$	t Addre (5Fh).	essing See
<u>Exan</u>	nple:	LFSR 2,	3ABh				Bit-Oriente	ed Instructionset Mode" f	ons in or deta	Indexed ils.
	After Instructio	on – 03	h		Words:		1			
	FSR2L	= 03 = AE	Bh		Cycles:		1			
					Q Cycle	Activity:				
						Q1	Q2	Q3		Q4
						Decode	Read register 'f'	Process Data	V	Vrite W
					Example	<u>c</u>	MOVF RI	EG, 0, 0		
					Bef	ore Instruc REG	tion = 22	h		
					Afte	vv er Instructio RFG	= FF on = 22	n h		

=

22h

W

24.2.3 BYTE-ORIENTED AND BIT-ORIENTED INSTRUCTIONS IN INDEXED LITERAL OFFSET MODE

Note:	Enabling	the	PIC18	instruction	set
	extension	may	cause le	gacy applicat	tions
	to behave	errat	ically or fa	ail entirely.	

In addition to eight new commands in the extended set, enabling the extended instruction set also enables Indexed Literal Offset Addressing mode (**Section 5.5.1 "Indexed Addressing with Literal Offset**"). This has a significant impact on the way that many commands of the standard PIC18 instruction set are interpreted.

When the extended set is disabled, addresses embedded in opcodes are treated as literal memory locations: either as a location in the Access Bank ('a' = 0) or in a GPR bank designated by the BSR ('a' = 1). When the extended instruction set is enabled and 'a' = 0, however, a file register argument of 5Fh or less is interpreted as an offset from the pointer value in FSR2 and not as a literal address. For practical purposes, this means that all instructions that use the Access RAM bit as an argument – that is, all byte-oriented and bitoriented instructions, or almost half of the core PIC18 instructions – may behave differently when the extended instruction set is enabled.

When the content of FSR2 is 00h, the boundaries of the Access RAM are essentially remapped to their original values. This may be useful in creating backward compatible code. If this technique is used, it may be necessary to save the value of FSR2 and restore it when moving back and forth between C and assembly routines in order to preserve the Stack Pointer. Users must also keep in mind the syntax requirements of the extended instruction set (see Section 24.2.3.1 "Extended Instruction Syntax with Standard PIC18 Commands").

Although the Indexed Literal Offset Addressing mode can be very useful for dynamic stack and pointer manipulation, it can also be very annoying if a simple arithmetic operation is carried out on the wrong register. Users who are accustomed to the PIC18 programming must keep in mind that, when the extended instruction set is enabled, register addresses of 5Fh or less are used for Indexed Literal Offset Addressing mode.

Representative examples of typical byte-oriented and bit-oriented instructions in the Indexed Literal Offset Addressing mode are provided on the following page to show how execution is affected. The operand conditions shown in the examples are applicable to all instructions of these types.

24.2.3.1 Extended Instruction Syntax with Standard PIC18 Commands

When the extended instruction set is enabled, the file register argument, 'f', in the standard byte-oriented and bit-oriented commands is replaced with the literal offset value, 'k'. As already noted, this occurs only when 'f' is less than or equal to 5Fh. When an offset value is used, it must be indicated by square brackets ("[]"). As with the extended instructions, the use of brackets indicates to the compiler that the value is to be interpreted as an index or an offset. Omitting the brackets, or using a value greater than 5Fh within brackets, will generate an error in the MPASM Assembler.

If the index argument is properly bracketed for Indexed Literal Offset Addressing mode, the Access RAM argument is never specified; it will automatically be assumed to be '0'. This is in contrast to standard operation (extended instruction set disabled) when 'a' is set on the basis of the target address. Declaring the Access RAM bit in this mode will also generate an error in the MPASM Assembler.

The destination argument, 'd', functions as before.

In the latest versions of the MPASM assembler, language support for the extended instruction set must be explicitly invoked. This is done with either the command line option, $/_{Y}$, or the PE directive in the source listing.

24.2.4 CONSIDERATIONS WHEN ENABLING THE EXTENDED INSTRUCTION SET

It is important to note that the extensions to the instruction set may not be beneficial to all users. In particular, users who are not writing code that uses a software stack may not benefit from using the extensions to the instruction set.

Additionally, the Indexed Literal Offset Addressing mode may create issues with legacy applications written to the PIC18 assembler. This is because instructions in the legacy code may attempt to address registers in the Access Bank below 5Fh. Since these addresses are interpreted as literal offsets to FSR2 when the instruction set extension is enabled, the application may read or write to the wrong data addresses.

When porting an application to the PIC18F2525/2620/ 4525/4620, it is very important to consider the type of code. A large, re-entrant application that is written in 'C' and would benefit from efficient compilation will do well when using the instruction set extensions. Legacy applications that heavily use the Access Bank will most likely not benefit from using the extended instruction set.

26.2 DC Characteristics: Power-Down and Supply Current PIC18F2525/2620/4525/4620 (Industrial) PIC18LF2525/2620/4525/4620 (Industrial) (Continued)

PIC18LF2525/2620/4525/4620 (Industrial)		Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial							
PIC18F2525/2620/4525/4620 (Industrial, Extended)		Standa Operat	ard Ope ing tem	perating ($\begin{array}{l} \text{Conditions (unletermine)}\\ -40^\circ\text{C} \leq \text{T}\\ -40^\circ\text{C} \leq \text{T}\\ \end{array}$	ess otherwise states a state of the set of	ted) strial ended		
Param No.	Device	Тур	Max	Units	Conditions				
	Supply Current (IDD) ⁽²⁾								
	PIC18LFX525/X620	0.8	1.1	mA	-40°C				
		0.8	1.1	mA	+25°C	VDD = 2.0V			
		0.8	1.1	mA	+85°C				
	PIC18LFX525/X620	1.3	1.7	mA	-40°C				
		1.3	1.7	mA	+25°C	VDD = 3.0V	FOSC = 4 MHz		
		1.3	1.7	mA	+85°C		INTOSC source)		
	All devices	2.5	3.5	mA	-40°C				
		2.5	3.5	mA	+25°C				
		2.5	3.5	mA	+85°C	VDD = 5.0V			
	Extended devices only	2.5	3.5	mA	+125°C				
	PIC18LFX525/X620	2.9	5	μA	-40°C				
		3.1	5	μA	+25°C	VDD = 2.0V			
		3.6	9.5	μA	+85°C				
	PIC18LFX525/X620	4.5	8	μA	-40°C				
		4.8	8	μA	+25°C	VDD = 3.0V	FOSC = 31 kHz		
		5.8	15	μA	+85°C		INTRC source)		
	All devices	9.2	16	μΑ	-40°C				
		9.8	16	μA	+25°C				
		11.0	35	μA	+85°C	VDD = 3.0V			
	Extended devices only	21	160	μA	+125°C				

Legend: Shading of rows is to assist in readability of the table.

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSs and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD or VSS;

MCLR = VDD; WDT enabled/disabled as specified.

3: When operation below -10°C is expected, use T1OSC High-Power mode, where LPT1OSC (CONFIG3H<2>) = 0. When operation will always be above -10°C, then the low-power Timer1 oscillator may be selected.

4: BOR and HLVD enable internal band gap reference. With both modules enabled, current consumption will be less than the sum of both specifications.

26.2 DC Characteristics: Power-Down and Supply Current PIC18F2525/2620/4525/4620 (Industrial) PIC18LF2525/2620/4525/4620 (Industrial) (Continued)

PIC18LF2525/2620/4525/4620 (Industrial)		Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial							
PIC18F252 (Indust	Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for extended								
Param No.	Тур	Max	Units		Conditions				
	Supply Current (IDD) ⁽²⁾								
	PIC18LFX525/X620	250	350	μA	-40°C				
		260	350	μA	+25°C	VDD = 2.0V			
		250	350	μA	+85°C				
	PIC18LFX525/X620	550	650	μA	-40°C				
		480	640	μA	+25°C	VDD = 3.0V			
		460	600	μA	+85°C		EC oscillator)		
	All devices	1.2	1.5	mA	-40°C				
		1.1	1.4	mA	+25°C				
		1.0	1.3	mA	+85°C	VDD = 3.0V			
	Extended devices only	1.0	3.0	mA	+125°C				
	PIC18LFX525/X620	0.72	1.0	mA	-40°C				
		0.74	1.0	mA	+25°C	VDD = 2.0V			
		0.74	1.0	mA	+85°C				
	PIC18LFX525/X620	1.3	1.8	mA	-40°C				
		1.3	1.8	mA	+25°C	VDD = 3.0V			
		1.3	1.8	mA	+85°C		EC oscillator)		
	All devices	2.7	4.0	mA	-40°C		,		
		2.6	4.0	mA	+25°C				
		2.5	4.0	mA	+85°C	VDD = 3.0V			
	Extended devices only	2.6	5.0	mA	+125°C				
	Extended devices only	8.4	13	mA	+125°C	VDD = 4.2V	Fosc = 25 MHz		
		11	16	mA	+125°C	VDD = 5.0V	(PRI_RUN , EC oscillator)		
	All devices	15	20	mA	-40°C	_			
			20	mA	+25°C	VDD = 4.2V			
		15	20	mA	+85°C		FOSC = 40 MHZ		
	All devices	20	25	mA	-40°C		EC oscillator)		
		20	25	mA	+25°C	VDD = 5.0V			
		20	25	mA	+85°C				

Legend: Shading of rows is to assist in readability of the table.

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSs and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD or VSS;

- MCLR = VDD; WDT enabled/disabled as specified.
- **3:** When operation below -10°C is expected, use T1OSC High-Power mode, where LPT1OSC (CONFIG3H<2>) = 0. When operation will always be above -10°C, then the low-power Timer1 oscillator may be selected.
- 4: BOR and HLVD enable internal band gap reference. With both modules enabled, current consumption will be less than the sum of both specifications.





TABLE 26-12: CAPTURE/COMPARE/PWM REQUIREMENTS (ALL CCP MODULES)

Param No.	Symbol	Characteristic			Min	Max	Units	Conditions
50	TccL	CCPx Input Low	No prescal	er	0.5 TCY + 20		ns	
		Time	With	PIC18FXXXX	10		ns	
			prescaler	PIC18LFXXXX	20		ns	VDD = 2.0V
51	TccH	CCPx Input	No prescale	er	0.5 TCY + 20		ns	
		High Time	With prescaler	PIC18FXXXX	10	_	ns	
				PIC18LFXXXX	20	-	ns	VDD = 2.0V
52	TccP	CCPx Input Perio	CPx Input Period			_	ns	N = prescale value (1, 4 or 16)
53	TccR	CCPx Output Fa	ll Time	PIC18FXXXX	—	25	ns	
				PIC18LFXXXX	_	45	ns	VDD = 2.0V
54	TccF	CCPx Output Fall Time		PIC18FXXXX	—	25	ns	
				PIC18LFXXXX	_	45	ns	VDD = 2.0V



FIGURE 26-14: EXAMPLE SPI MASTER MODE TIMING (CKE = 1)

TABLE 26-15: EXAMPLE SPI MODE REQUIREMENTS (MASTER MODE, CKE = 1)

Param. No.	Symbol	Characterist	Min	Max	Units	Conditions	
71	TscH	SCK Input High Time	Continuous	1.25 Tcy + 30	—	ns	
71A		(Slave mode)	Single Byte	40	-	ns	(Note 1)
72	TscL	SCK Input Low Time	Continuous	1.25 Tcy + 30	_	ns	
72A		(Slave mode)	Single Byte	40		ns	(Note 1)
73	TdiV2scH, TdiV2scL	Setup Time of SDI Data Input	20	_	ns		
73A	Tb2b	Last Clock Edge of Byte 1 to the of Byte 2	1.5 Tcy + 40	_	ns	(Note 2)	
74	TscH2diL, TscL2diL	Hold Time of SDI Data Input t	40	_	ns		
75	TdoR	SDO Data Output Rise Time	SDO Data Output Rise Time PIC18FXXXX		25	ns	
			PIC18LFXXXX		45	ns	VDD = 2.0V
76	TdoF	SDO Data Output Fall Time		—	25	ns	
78	TscR	SCK Output Rise Time	PIC18FXXXX	—	25	ns	
		(Master mode)	PIC18LFXXXX		45	ns	VDD = 2.0V
79	TscF	SCK Output Fall Time (Master mode)		—	25	ns	
80	TscH2doV,	SDO Data Output Valid after	PIC18FXXXX	—	50	ns	
	TscL2doV	SCK Edge PIC18LFXX			100	ns	VDD = 2.0V
81	TdoV2scH, TdoV2scL	SDO Data Output Setup to SO	CK Edge	Тсү		ns	

Note 1: Requires the use of Parameter #73A.

2: Only if Parameter #71A and #72A are used.

40-Lead Plastic Dual In-Line (P) – 600 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	INCHES			
Dimension	n Limits	MIN	NOM	MAX	
Number of Pins	N		40		
Pitch	е		.100 BSC		
Top to Seating Plane	А	-	-	.250	
Molded Package Thickness	A2	.125	-	.195	
Base to Seating Plane	A1	.015	-	-	
Shoulder to Shoulder Width	Е	.590	-	.625	
Molded Package Width	E1	.485	-	.580	
Overall Length	D	1.980	-	2.095	
Tip to Seating Plane	L	.115	-	.200	
Lead Thickness	С	.008	-	.015	
Upper Lead Width	b1	.030	-	.070	
Lower Lead Width	b	.014	_	.023	
Overall Row Spacing §	eB	_	_	.700	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. § Significant Characteristic.

3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.

4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-016B