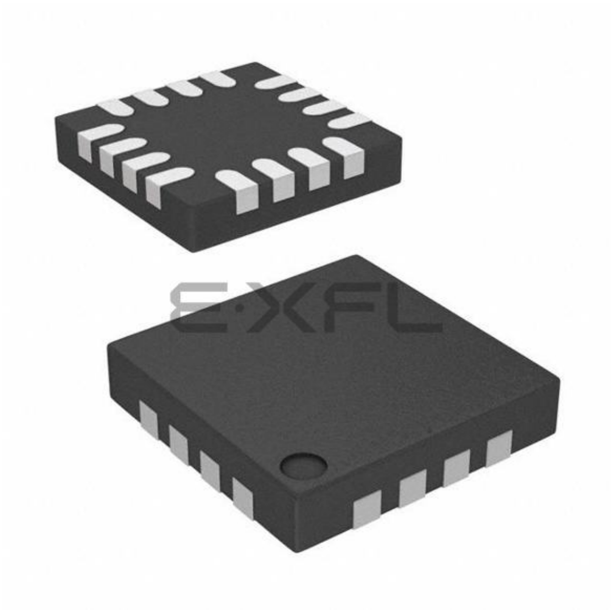

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Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	USB Microcontroller
Core Processor	M8C
Program Memory Type	FLASH (16kB)
Controller Series	CY7C643xx
RAM Size	1K x 8
Interface	I²C, SPI, USB
Number of I/O	11
Voltage - Supply	3V ~ 5.5V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	16-UFQFN
Supplier Device Package	16-QFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy7c64315-16lkxct

Contents

Development Tools

PSoC Designer™ is the revolutionary Integrated Design Environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
  - Hardware and software I^2C slaves and masters
  - Full-speed USB 2.0
  - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are analog-to-digital converters (ADCs), digital-to-analog converters (DACs), amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this allows you to use more than 100 percent of PSoC's resources for a given application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows you to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer.

In-Circuit Emulator

A low-cost, high-functionality In-Circuit Emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24-MHz) operation.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed-function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and lowering inventory costs. These configurable resources, called PSoC blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is:

1. Select user modules.
2. Configure user modules.
3. Organize and connect.
4. Generate, verify, and debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called user modules. User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a Pulse width modulator (PWM) user module configures one or more digital PSoC blocks, one for each eight bits of resolution. Using these parameters, you can establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All of the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module data sheets explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information that you may need to successfully implement your design.

Organize and Connect

Build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. Perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides APIs with high-level functions to control and respond to hardware events at run time, and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in C, assembly language, or both.

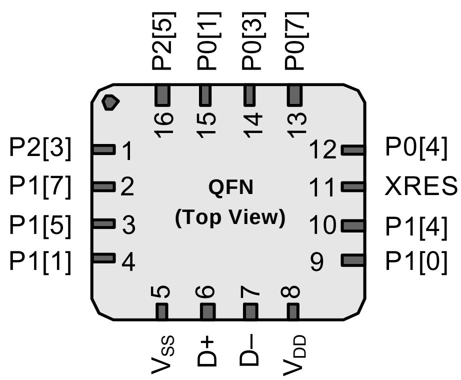
The last step in the development process takes place inside PSoC Designer’s Debugger (accessed by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer. It allows you to define complex breakpoint events that include monitoring address and data bus values, memory locations, and external signals.

Pin Information

The enCoRe V USB device is available in a variety of packages which are listed and illustrated in the subsequent tables.

16-pin part pinout

Figure 6. CY7C64315/CY7C64316 16-pin enCoRe V USB Device



Pin Definitions

16-pin part pinout (QFN)

Pin No.	Type	Name	Description
1	I/O	P2[3]	Digital I/O, crystal input (Xin)
2	I/OHR	P1[7]	Digital I/O, SPI SS, I^2C SCL
3	I/OHR	P1[5]	Digital I/O, SPI MISO, I^2C SDA
4	I/OHR	P1[1][1, 2]	Digital I/O, ISSP CLK, I^2C SCL, SPI MOSI
5	Power	V_{SS}	Ground connection
6	USB line	D+	USB PHY
7	USB line	D–	USB PHY
8	Power	V_{DD}	Supply
9	I/OHR	P1[0][1, 2]	Digital I/O, ISSP DATA, I^2C SDA, SPI CLK
10	I/OHR	P1[4]	Digital I/O, optional external clock input (EXTCLK)
11	Input	XRES	Active high external reset with internal pull-down
12	I/OH	P0[4]	Digital I/O
13	I/OH	P0[7]	Digital I/O
14	I/OH	P0[3]	Digital I/O
15	I/OH	P0[1]	Digital I/O
16	I/O	P2[5]	Digital I/O, crystal output (Xout)

LEGEND I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output

Notes
1. During power up or reset event, device P1[0] and P1[1] may disturb the I^2C bus. Use alternate pins if issues are encountered.
2. These are the in-system serial programming (ISSP) pins that are not High Z at power on reset (POR).

Pin Definitions

48-pin Part Pinout (QFN)

Pin No.	Type	Pin Name	Description
24	I/OHR	P1[4]	Digital I/O, optional external clock input (EXTCLK)
25	I/OHR	P1[6]	Digital I/O
26	XRES	Ext Reset	Active high external reset with internal pull down
27	I/O	P3[0]	Digital I/O
28	I/O	P3[2]	Digital I/O
29	I/O	P3[4]	Digital I/O
30	I/O	P3[6]	Digital I/O
31	I/O	P4[0]	Digital I/O
32	I/O	P4[2]	Digital I/O
33	I/O	P2[0]	Digital I/O
34	I/O	P2[2]	Digital I/O
35	I/O	P2[4]	Digital I/O
36	I/O	P2[6]	Digital I/O
37	I/OH	P0[0]	Digital I/O
38	I/OH	P0[2]	Digital I/O
39	I/OH	P0[4]	Digital I/O
40	I/OH	P0[6]	Digital I/O
41	Power	V_{DD}	Supply voltage
42	NC	NC	No connection
43	NC	NC	No connection
44	I/OH	P0[7]	Digital I/O
45	I/OH	P0[5]	Digital I/O
46	I/OH	P0[3]	Digital I/O
47	Power	V_{SS}	Supply ground
48	I/OH	P0[1]	Digital I/O
CP	Power	V_{SS}	Ensure the center pad is connected to ground

LEGEND I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output

Register Reference

The section discusses the registers of the enCoRe V device. It lists all the registers in mapping tables, in address order.

Register Conventions

The register conventions specific to this section are listed in the following table.

Table 1. Register Conventions

Convention	Description
R	Read register or bits
W	Write register or bits
L	Logical register or bits
C	Clearable register or bits
#	Access is bit specific

Register Mapping Tables

The enCoRe V device has a total register address space of 512 bytes. The register space is also referred to as I/O space and is broken into two parts: Bank 0 (user space) and Bank 1 (configuration space). The XIO bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XIO bit is set, the user is said to be in the “extended” address space or the “configuration” registers.

Table 3. Register Map Bank 1 Table: Configuration Space

Name	Addr (1, Hex)	Access	Name	Addr (1, Hex)	Access	Name	Addr (1, Hex)	Access	Name	Addr (1, Hex)	Access
PRT0DM0	00	RW	PMA4_RA	40	RW		80			C0	
PRT0DM1	01	RW	PMA5_RA	41	RW		81			C1	
	02		PMA6_RA	42	RW		82			C2	
	03		PMA7_RA	43	RW		83			C3	
PRT1DM0	04	RW	PMA8_WA	44	RW		84			C4	
PRT1DM1	05	RW	PMA9_WA	45	RW		85			C5	
	06		PMA10_WA	46	RW		86			C6	
	07		PMA11_WA	47	RW		87			C7	
PRT2DM0	08	RW	PMA12_WA	48	RW		88			C8	
PRT2DM1	09	RW	PMA13_WA	49	RW		89			C9	
	0A		PMA14_WA	4A	RW		8A			CA	
	0B		PMA15_WA	4B	RW		8B			CB	
PRT3DM0	0C	RW	PMA8_RA	4C	RW		8C			CC	
PRT3DM1	0D	RW	PMA9_RA	4D	RW		8D			CD	
	0E		PMA10_RA	4E	RW		8E			CE	
	0F		PMA11_RA	4F	RW		8F			CF	
PRT4DM0	10	RW	PMA12_RA	50	RW		90			D0	
PRT4DM1	11	RW	PMA13_RA	51	RW		91			D1	
	12		PMA14_RA	52	RW		92		ECO_ENBUS	D2	RW
	13		PMA15_RA	53	RW		93		ECO_TRIM	D3	RW
	14		EP1_CR0	54	#		94			D4	
	15		EP2_CR0	55	#		95			D5	
	16		EP3_CR0	56	#		96			D6	
	17		EP4_CR0	57	#		97			D7	
	18		EP5_CR0	58	#		98		MUX_CR0	D8	RW
	19		EP6_CRO	59	#		99		MUX_CR1	D9	RW
	1A		EP7_CR0	5A	#		9A		MUX_CR2	DA	RW
	1B		EP8_CR0	5B	#		9B		MUX_CR3	DB	RW
	1C			5C			9C		IO_CFG1	DC	RW
	1D			5D			9D		OUT_P1	DD	RW
	1E			5E			9E		IO_CFG2	DE	RW
	1F			5F			9F		MUX_CR4	DF	RW
	20			60			A0		OSC_CR0	E0	RW
	21			61			A1		ECO_CFG	E1	#
	22			62			A2		OSC_CR2	E2	RW
	23			63			A3		VLT_CR	E3	RW
	24			64			A4		VLT_CMP	E4	R
	25			65			A5			E5	
	26			66			A6			E6	
	27			67			A7			E7	
	28			68			A8		IMO_TR	E8	W
SPI_CFG	29	RW		69			A9		ILO_TR	E9	W
	2A			6A			AA			EA	
	2B			6B			AB		SLP_CFG	EB	RW
	2C		TMP_DR0	6C	RW		AC		SLP_CFG2	EC	RW
	2D		TMP_DR1	6D	RW		AD		SLP_CFG3	ED	RW
	2E		TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
USB_CR1	30	#		70			B0			F0	
	31			71			B1			F1	
	32			72			B2			F2	
	33			73			B3			F3	
PMA0_WA	34	RW		74			B4			F4	
PMA1_WA	35	RW		75			B5			F5	
PMA2_WA	36	RW		76			B6			F6	
PMA3_WA	37	RW		77			B7		CPU_F	F7	RL
PMA4_WA	38	RW		78			B8			F8	
PMA5_WA	39	RW		79			B9			F9	
PMA6_WA	3A	RW		7A			BA		IMO_TR1	FA	RW
PMA7_WA	3B	RW		7B			BB			FB	
PMA0_RA	3C	RW		7C			BC			FC	
PMA1_RA	3D	RW		7D		USB_MISC_CR	BD	RW		FD	
PMA2_RA	3E	RW		7E			BE			FE	
PMA3_RA	3F	RW		7F			BF			FF	

Gray fields are reserved; do not access these fields. # Access is bit specific.

Electrical Specifications

This section presents the DC and AC electrical specifications of the enCoRe V USB devices. For the most up-to-date electrical specifications, verify that you have the most recent data sheet available by visiting the company web site at http://www.cypress.com

Figure 9. Voltage versus CPU Frequency

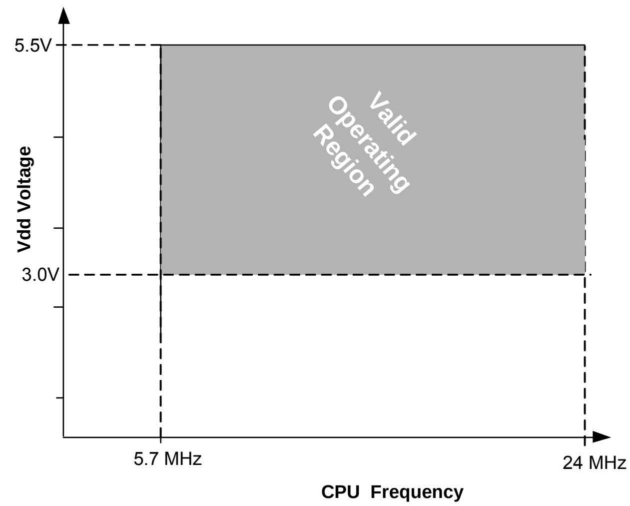
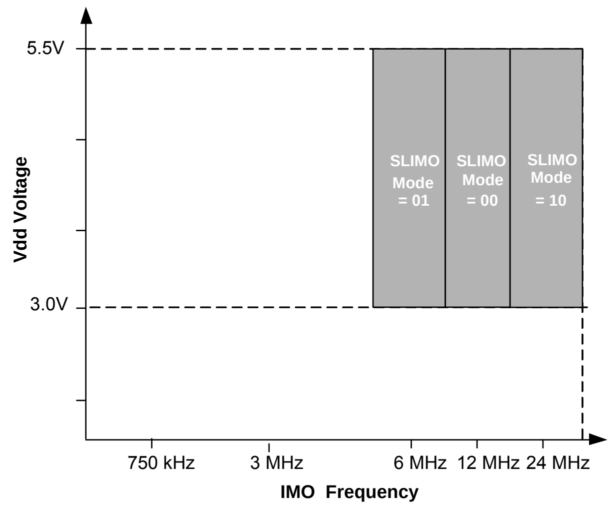


Figure 10. IMO Frequency Trim Options



Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 4. Absolute Maximum Ratings

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{STG}	Storage temperature[10]	Higher storage temperatures reduces data retention time. Recommended Storage Temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 85°C degrades reliability.	–55	+25	+125	°C
V_{DD}	Supply voltage relative to V_{SS}		–0.5	–	+6.0	V
V_{IO}	DC input voltage		V_{SS} – 0.5	–	V_{DD} + 0.5	V
V_{IOZ}	DC voltage applied to tristate		V_{SS} – 0.5	–	V_{DD} + 0.5	V
I_{MIO}	Maximum current into any port pin		–25	–	+50	mA
ESD	Electrostatic discharge voltage	Human body model ESD	2000	–	–	V
LU [8]	Latch up current	In accordance with JESD78 standard	–	–	200	mA

Operating Temperature

Table 5. Operating Temperature

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{AI}	Ambient industrial temperature		–40	–	+85	°C
T_{AC}	Ambient commercial temperature		0	–	+70	°C
T_{JI}	Operational industrial die temperature [11]	The temperature rise from ambient to junction is package specific. Refer the table Thermal Impedances per Package on page 31. The user must limit the power consumption to comply with this requirement.	–40	–	+100	°C
T_{JC}	Operational commercial die temperature	The temperature rise from ambient to junction is package specific. Refer the table Thermal Impedances per Package on page 31. The user must limit the power consumption to comply with this requirement.	0	–	+85	°C

Notes

7. When V_{DD} remains in the range from 1.71 V to 1.9 V for more than 50 µsec, the slew rate when moving from the 1.71 V to 1.9 V range to greater than 2 V must be slower than 1 V/500 µsec to avoid triggering POR. The only other restriction on slew rates for any other voltage range or transition is the SRPOWER_UP parameter.
8. Errata: For Port 1 pins P1[1], P1[4], and P1[5] 300 Ohm external resistor is needed to meet this spec. Refer to "Errata" on page 35 for more details.
9. If powering down in standby sleep mode, to properly detect and recover from a V_{DD} brown out condition any of the following actions must be taken:
   - Bring the device out of sleep before powering down.
   - Assure that V_{DD} falls below 100 mV before powering back up.
   - Set the No Buzz bit in the OSC_CR0 register to keep the voltage monitoring circuit powered during sleep.
   - Increase the buzz rate to assure that the falling edge of V_{DD} is captured. The rate is configured through the PSSDC bits in the SLP_CFG register.
   For the referenced registers, refer to the enCoRe V Technical Reference Manual. In deep sleep mode, additional low power voltage monitoring circuitry allows V_{DD} brown out conditions to be detected for edge rates slower than 1 V/ms.

DC Electrical Characteristics

DC Chip Level Specifications

Table 6 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 6. DC Chip Level Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{DD}	Operating voltage [7, 9]	No USB activity.	3.0	–	5.5	V
$I_{DD24,3}$	Supply current, CPU = 24 MHz	Conditions are V_{DD} = 3.0 V, T_A = 25 °C, CPU = 24 MHz, No USB/I^2C/SPI.	–	2.9	4.0	mA
$I_{DD12,3}$	Supply current, CPU = 12 MHz	Conditions are V_{DD} = 3.0 V, T_A = 25 °C, CPU = 12 MHz, No USB/I^2C/SPI.	–	1.7	2.6	mA
$I_{DD6,3}$	Supply current, CPU = 6 MHz	Conditions are V_{DD} = 3.0 V, T_A = 25 °C, CPU = 6 MHz, No USB/I^2C/SPI.	–	1.2	1.8	mA
$I_{SB1,3}$	Standby current with POR, LVD, and sleep timer	V_{DD} = 3.0 V, T_A = 25 °C, I/O regulator turned off.	–	1.1	1.5	µA
$I_{SB0,3}$	Deep sleep current	V_{DD} = 3.0 V, T_A = 25 °C, I/O regulator turned off.	–	0.1	–	µA
V_{DDUSB}	Operating voltage	USB activity, USB regulator enabled	4.35	–	5.25	V
$I_{DD24,5}$	Supply current, CPU = 24 MHz	Conditions are V_{DD} = 5.0 V, T_A = 25 °C, CPU = 24 MHz, IMO = 24 MHz USB Active, No I^2C/SPI.	–	7.1	–	mA
$I_{DD12,5}$	Supply current, CPU = 12 MHz	Conditions are V_{DD} = 5.0 V, T_A = 25 °C, CPU = 12 MHz, IMO = 24 MHz USB Active, No I^2C/SPI.	–	6.2	–	mA
$I_{DD6,5}$	Supply current, CPU = 6 MHz	Conditions are V_{DD} = 5.0 V, T_A = 25 °C, CPU = 6 MHz, IMO = 24 MHz USB Active, No I^2C/SPI	–	5.8	–	mA
$I_{SB1,5}$	Standby current with POR, LVD, and sleep timer	V_{DD} = 5.0 V, T_A = 25 °C, I/O regulator turned off.	–	1.1	–	µA
$I_{SB0,5}$	Deep sleep current	V_{DD} = 5.0 V, T_A = 25 °C, I/O regulator turned off.	–	0.1	–	µA
V_{DDUSB}	Operating voltage	USB activity, USB regulator bypassed	3.15	3.3	3.60	V

Notes

10. Higher storage temperatures reduce data retention time. Recommended storage temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 85 °C degrade reliability.
11. The temperature rise from ambient to junction is package specific. See Package Handling on page 31. The user must limit the power consumption to comply with this requirement.

Table 7. DC Characteristics – USB Interface

Symbol	Description	Conditions	Min	Typ	Max	Units
Rusbi	USB D+ pull-up resistance	With idle bus	0.900	–	1.575	kΩ
Rusba	USB D+ pull-up resistance	While receiving traffic	1.425	–	3.090	kΩ
Vohusb	Static output high		2.8	–	3.6	V
Volusb	Static output low		–	–	0.3	V
Vdi	Differential input sensitivity		0.2	–	–	V
Vcm	Differential input common mode range		0.8	–	2.5	V
Vse	Single-ended receiver threshold		0.8	–	2.0	V
Cin	Transceiver capacitance			–	50	pF
Iio	High Z state data Line Leakage	On D+ or D– line	–10	–	+10	μA
Rps2	PS/2 Pull Up Resistance		3	5	7	kΩ
Rext	External USB Series Resistor	In series with each USB pin	21.78	22.0	22.22	Ω

ADC Electrical Specifications

Table 8. ADC User Module Electrical Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
Input						
V_{IN}	Input voltage range		0	–	VREFADC	V
C_{IIN}	Input capacitance		–	–	5	pF
R_{IN}	Input resistance	Equivalent switched cap input resistance for 8-, 9-, or 10-bit resolution	1/(500fF* Data Clock)	1/(400fF* Data Clock)	1/(300fF* Data Clock)	Ω
Reference						
V_{REFADC}	ADC reference voltage		1.14	–	1.26	V
Conversion Rate						
F_{CLK}	Data clock	Source is chip's internal main oscillator. See AC Chip-Level Specifications for accuracy	2.25	–	6	MHz
S8	8-bit sample rate	Data Clock set to 6 MHz. Sample Rate = 0.001/ (2^Resolution/Data Clock)	–	23.4375	–	ksps
S10	10-bit sample rate	Data Clock set to 6 MHz. Sample Rate = 0.001/ (2^Resolution/Data Clock)	–	5.859	–	ksps
DC Accuracy						
RES	Resolution	Can be set to 8-, 9-, or 10-bit	8	–	10	bits
DNL	Differential nonlinearity		–1	–	+2	LSB
INL	Integral nonlinearity		–2	–	+2	LSB
E_{Offset}	Offset error	8-bit resolution	0	3.2	19.2	LSB
		10-bit resolution	0	12.8	76.8	LSB
E_{gain}	Gain error	For any resolution	–5	–	+5	%FSR
Power						
I_{ADC}	Operating current		–	2.1	2.6	mA
PSRR	Power supply rejection ratio	PSRR (V_{DD} > 3.0 V)	–	24	–	dB
		PSRR (V_{DD} < 3.0 V)	–	30	–	dB

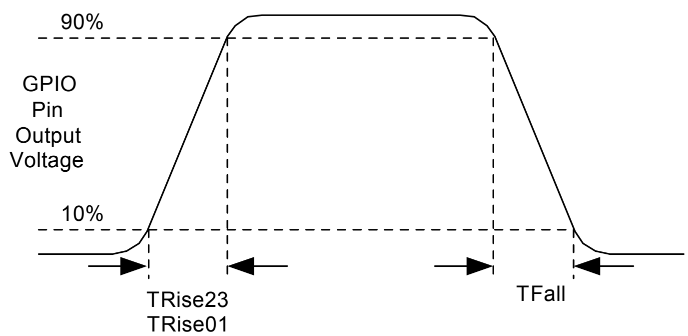
AC General Purpose I/O Specifications

Table 15 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 15. AC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{GPIO}	GPIO operating frequency	Normal strong mode, Ports 0, 1	–	–	12	MHz
TRise23	Rise time, strong mode Ports 2, 3	V_{DD} = 3.0 to 3.6 V, 10% - 90%	15	–	80	ns
TRise01	Rise time, strong mode Ports 0, 1	V_{DD} = 3.0 to 3.6 V, 10% - 90%	10	–	50	ns
TFall	Fall time, strong mode All Ports	V_{DD} = 3.0 to 3.6 V, 10% - 90%	10	–	50	ns

Figure 11. GPIO Timing Diagram



AC External Clock Specifications

Table 16 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 16. AC External Clock Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{OSCEXT}	Frequency		0.750	–	25.2	MHz
–	High period		20.6	–	5300	ns
–	Low period		20.6	–	–	ns
–	Power-up IMO to switch		150	–	–	µs

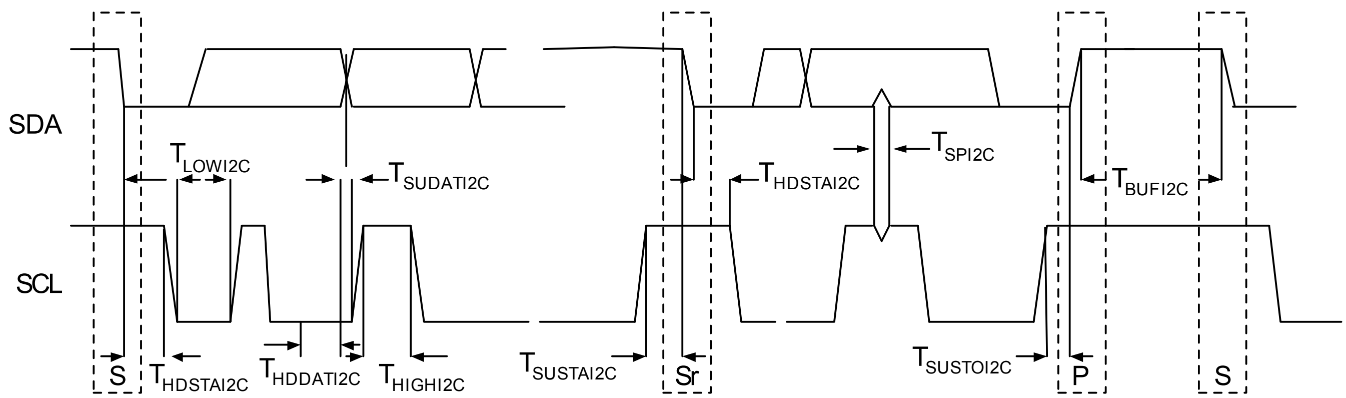
AC I^{2}C Specifications

Table 18 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 18. AC Characteristics of the I^{2}C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
F_{SCLI2C}	SCL clock frequency	0	100	0	400	kHz
$T_{HDSTAI2C}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4.0	–	0.6	–	µs
T_{LOWI2C}	LOW period of the SCL clock	4.7	–	1.3	–	µs
$T_{HIGHI2C}$	HIGH period of the SCL clock	4.0	–	0.6	–	µs
$T_{SUSTAI2C}$	Setup time for a repeated START condition	4.7	–	0.6	–	µs
$T_{HDDATI2C}$	Data hold time	0	–	0	–	µs
$T_{SUDATI2C}$	Data setup time	250	–	100[20]	–	ns
$T_{SUSTOI2C}$	Setup time for STOP condition	4.0	–	0.6	–	µs
T_{BUFI2C}	Bus free time between a STOP and START condition	4.7	–	1.3	–	µs
T_{SPI2C}	Pulse width of spikes are suppressed by the input filter	–	–	0	50	ns

Figure 13. Definition of Timing for Fast/Standard Mode on the I^{2}C Bus



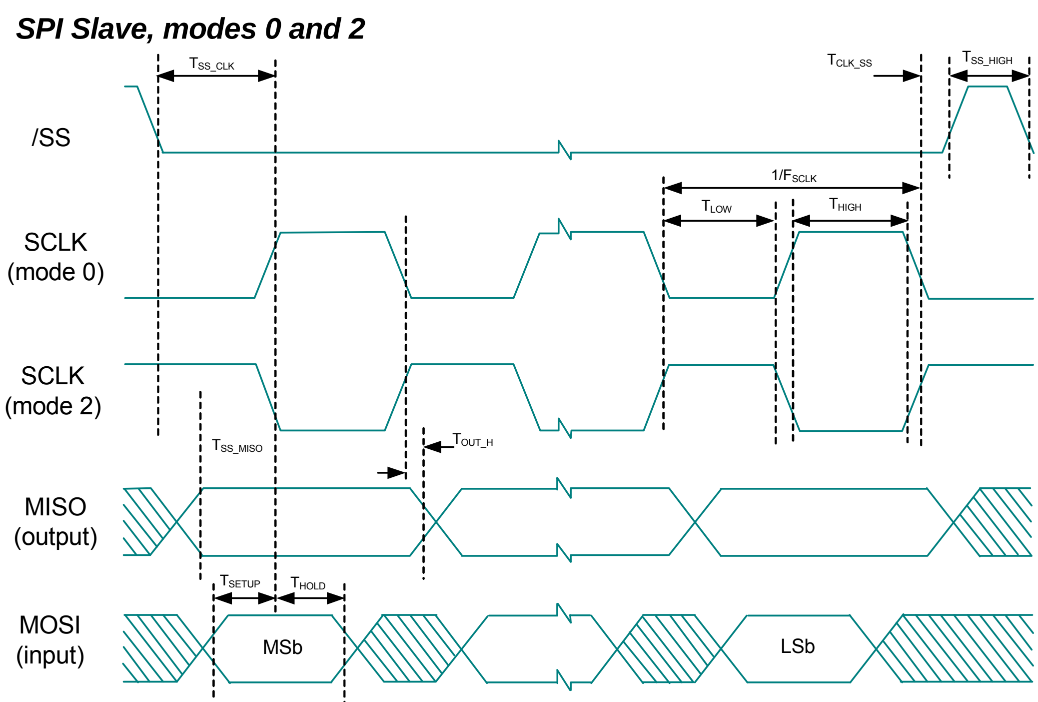
Note

20. A Fast mode I^{2}C bus device can be used in a standard mode I^{2}C bus system, but the requirement $t_{SUDAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SUDAT} = 1000 + 250 = 1250$ ns (according to the standard mode I^{2}C bus specification) before the SCL line is released.

Table 20. SPI Slave AC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{SCLK}	SCLK clock frequency		0.0469	–	12	MHz
T_{LOW}	SCLK low time		41.67	–	–	ns
T_{HIGH}	SCLK high time		41.67	–	–	ns
T_{SETUP}	MOSI to SCLK setup time		30	–	–	ns
T_{HOLD}	SCLK to MOSI hold time		50	–	–	ns
T_{SS_MISO}	SS low to MISO valid		–	–	153	ns
T_{SCLK_MISO}	SCLK to MISO valid		–	–	125	ns
T_{SS_HIGH}	SS high time		50	–	–	ns
T_{SS_CLK}	Time from SS low to first SCLK		$2/F_{SCLK}$	–	–	ns
T_{CLK_SS}	Time from last SCLK to SS high		$2/F_{SCLK}$	–	–	ns

Figure 16. SPI Slave Mode 0 and 2



Package Handling

Some IC packages require baking before they are soldered onto a PCB to remove moisture that may have been absorbed after leaving the factory. A label on the package has details about the actual bake temperature and the minimum bake time to remove this moisture. The maximum bake time is the aggregate time that the parts exposed to the bake temperature. Exceeding this exposure may degrade device reliability.

Table 21. Package Handling

Parameter	Description	Minimum	Typical	Maximum	Unit
TBAKETEMP	Bake temperature	–	125	See package label	°C
TBAKETIME	Bake time	See package label	–	72	hours

Thermal Impedances

Table 22. Thermal Impedances per Package

Package	Typical θ_{JA}[21]
16-pin QFN	32.69 °C / W
32-pin QFN[22]	19.51 °C / W
48-pin QFN[22]	17.68 °C / W

Capacitance on Crystal Pins

Table 23. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
32-pin QFN	3.2 pF
48-pin QFN	3.3 pF

Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Table 24. Solder Reflow Peak Temperature

Package	Minimum Peak Temperature [23]	Maximum Peak Temperature
16-pin QFN	240 °C	260 °C
32-pin QFN	240 °C	260 °C
48-pin QFN	240 °C	260 °C

Notes

21. $T_J = T_A + \text{Power} \times \theta_{JA}$.
22. To achieve the thermal impedance specified for the package, solder the center thermal pad to the PCB ground plane.
23. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5 °C with Sn-Pb or 245 ± 5 °C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

Ordering Code Definitions

CY 7C64 XXX- XX XXX C/I (T)

Tape and reel

Temperature range:
Commercial/Industrial

Package type:
LK/LQ/LT: QFN Pb-free

Pin count:

16 = 16 pins,

32 = 32 pins,

48 = 48 pins

Base part number

Marketing Code: 7C64 = enCoRe Full-Speed USB Controller

Company ID: CY = Cypress

Acronyms

Acronym	Description
API	Application Programming Interface
CPU	Central Processing Unit
GPIO	General Purpose I/O
ICE	In-Circuit Emulator
ILO	Internal Low speed Oscillator
IMO	Internal Main Oscillator
I/O	Input/Output
LSb	Least Significant Bit
LVD	Low Voltage Detect
MSb	Most Significant Bit
POR	Power On Reset
PPOR	Precision Power On Reset
PSoC	Programmable System-on-Chip
SLIMO	Slow IMO
SRAM	Static Random Access Memory

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
dB	decibel
fF	femtofarad
Hz	hertz
KB	1024 bytes
Kbit	1024 bits
kHz	kilohertz
kΩ	kilohm
MHz	megahertz
MΩ	megaohm
μA	microampere
μF	microfarad
μH	microhenry
μs	microsecond
μV	microvolt
μVrms	microvolts root-mean-square
μW	microwatt
mA	milliampere
ms	milli-second
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
W	ohm
pA	picoampere
pF	picofarad
pp	peak-to-peak
ppm	parts per million
ps	picosecond
sps	samples per second
σ	sigma: one standard deviation
V	volt

Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, ‘01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’, ‘b’, or ‘0x’ are decimal.

Errata

This section describes the errata for the enCoRe V – CY7C643xx. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability.

Contact your local Cypress Sales Representative if you have questions.

CY7C643xx Errata Summary

The following Errata item applies to the **CY7C643xx** data sheets.

1. Latch up susceptibility when maximum I/O sink current exceeded

- **PROBLEM DEFINITION**

  P1[3], P1[6], and P1[7] pins are susceptible to latch up when the I/O sink current exceeds 25 mA per pin on these pins.

- **PARAMETERS AFFECTED**

  LU – Latch up current. Per JESD78A, the maximum allowable latch up current per pin is 100 mA. Cypress internal specification is 200 mA latch up current limit.

- **TRIGGER CONDITIONS**

  Latch up occurs when both the following conditions are met:

  A. The offending I/O is externally connected to a voltage higher than the I/O high state, causing a current to flow into the pin that exceeds 25 mA.

  B. A Port1 I/O (P1[1], P1[4], and P1[5] respectively) adjacent to the offending I/O is connected to a voltage lower than the I/O low state. This causes a signal that drops below Vss (signal undershoot) and a current greater than 200 mA to flow out of the pin.

- **SCOPE OF IMPACT**

  The trigger conditions outlined in this item exceed the maximum ratings specified in the CY7C643xx data sheets.

- **WORKAROUND**

  Add a series resistor > 300 Ω to P1[3], P1[6], and P1[7] pins to restrict current to within latch up limits.

- **FIX STATUS**

  This issue will be corrected in the next new silicon revision.

2. Does not meet USB 2.0 specification for D+ and D- rise/fall matching when supply voltage is under 3.3 V

- **PROBLEM DEFINITION**

  Rising to falling rate matching of the USB D+ and D- lines has a corner case at lower supply voltages, such as those under 3.3 V.

- **PARAMETERS AFFECTED**

  Rising to falling rate matching of the USB data lines.

- **TRIGGER CONDITION(S)**

  Operating the VCC supply voltage at the low end of the chip's specification (under 3.3 V) may cause a mismatch in the rising to falling rate.

- **SCOPE OF IMPACT**

  This condition does not affect USB communications but could cause corner case issues with USB lines' rise/fall matching specification. Signal integrity tests were run using the Cypress development kit and excellent eye was observed with supply voltage of 3.15 V.

Document History Page *(continued)*

Document Title: CY7C6431x/CY7C6434x/CY7C6435x, enCoRe™ V Full Speed USB Controller Document Number: 001-12394				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*F	2583853	TYJ / PYRS / HMT	10/10/08	Converted from Preliminary to Final Added operating voltage ranges with USB ADC resolution changed from 10-bit to 8-bit Rephrased battery monitoring clause in page 1 to include “with external components” Included ADC specifications table Included Voh7, Voh8, Voh9, Voh10 specs Flash data retention – condition added to Note [11] Input leakage spec changed to 25 nA max Under AC Char, Frequency accuracy of ILO corrected GPIO rise time for ports 0,1 and ports 2,3 made common AC Programming specifications updated Included AC Programming cycle timing diagram AC SPI specification updated Spec change for 32-QFN package Input Leakage Current maximum value changed to 1 µA Updated V_{OHV} parameter in Table 13 Updated thermal impedances for the packages Update Development Tools, add Designing with PSoC Designer. Edit, fix links and table format. Update TMs.
*G	2653717	DVJA / PYRS	02/04/09	Updated Features, Functional Overview, Development Tools, and Designing with PSoC Designer sections with edits. Removed ‘GUI - graphical user interface’ from Document Conventions acronym table. Removed ‘O - Only a read/write register or bits’ in Table 4 Edited Table 8: removed 10-bit resolution information and corrected units column. Added package handling section Added 8K part ‘CY7C64343-32LQXC’ to Ordering Information.
*H	2714694	DVJA / AESA	06/04/2009	Updated Block Diagram. Added Full Speed USB, 10-bit ADC, SPI, and I2C Slave sections. ADC Resolution changed from 8-bit to 10-bit Updated Table 9 DC Chip Level Specs Updated Table10 DC Char - USB Interface Updated Table 12 DC POR and LDV Specs Changed operating temperature from Commercial to Industrial Changed Temperature Range to Industrial: –40 to 85°C Figure 9: Changed minimum CPU Frequency from 750 kHz to 5.7 MHz Table 14: Removed “Maximum” from the F_{CPU} description Ordering Information: Replaced ‘C’ with ‘I’ in all part numbers to denote Industrial Temp Range
*I	2764460	DVJA / AESA	09/16/2009	Changed Table 12: ADC Specs Added F_{32K2} (Untrimmed) spec to Table 16: AC Chip level Specs Changed T_{RAMP} spec to SR_{POWER_UP} in Table 16: AC Chip Level Specs Added Table 27: Typical Package Capacitance on Crystal Pins
*J	2811903	DVJA	11/20/2009	Added USB-IF TID number in Features on page 1. Added Note 5 on page 18. Changed V_{IHP} in Table 12 on page 22.

Document History Page *(continued)*

Document Title: CY7C6431x/CY7C6434x/CY7C6435x, enCoRe™ V Full Speed USB Controller Document Number: 001-12394				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*S	4578605	GINS	12/11/2014	Updated Pin Information: Updated 32-pin part pinout: Updated Figure 7 (No change in figure, included CY7C64346 in figure caption). Updated Package Diagrams: spec 001-09116 – Changed revision from *I to *J. Updated Ordering Information: Updated Table 25: Updated part numbers.
*T	5548557	ANKC	12/12/2016	Updated Cypress Logo, Sales Page and Disclaimer. Updated Figure 20 (spec 001-13191 *G to *H) in Package Diagrams. Removed the following obsolete part numbers (Table 26) in Ordering Information: CY7C64343-32LQXI, CY7C64343-32LQXIT, CY7C64345-32LQXI, CY7C64345-32LQXIT, CY7C64356-48LTXI, CY7C64356-48LTXIT.