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[Embedded - Microcontrollers - Application Specific](#) represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are [Embedded - Microcontrollers - Application Specific](#)?

Application specific microcontrollers are engineered to

Details

Product Status	Active
Applications	USB Microcontroller
Core Processor	M8C
Program Memory Type	FLASH (16kB)
Controller Series	CY7C643xx
RAM Size	1K x 8
Interface	I ² C, SPI, USB
Number of I/O	11
Voltage - Supply	3V ~ 5.5V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	16-UFQFN
Supplier Device Package	16-QFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy7c64315-16lkxit

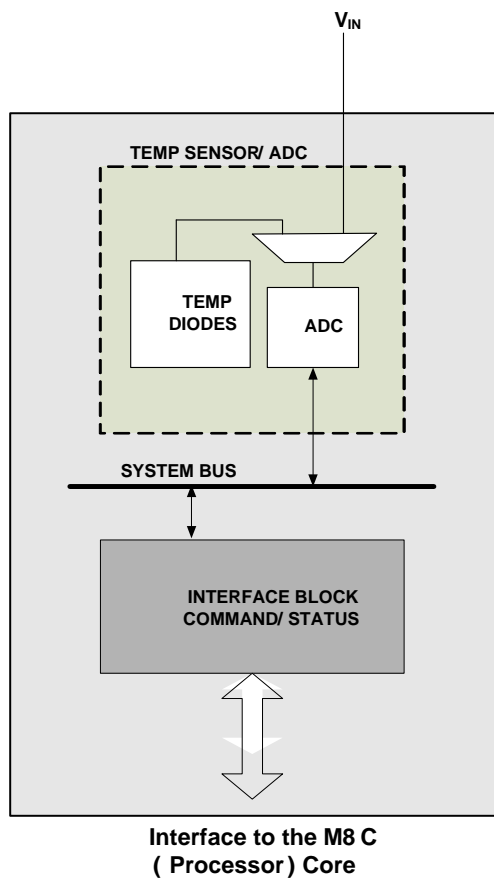
Firmware is required to handle various parts of the USB interface. The SIE issues interrupts after key USB events to direct firmware to appropriate tasks:

- Fill and empty the USB data buffers in USB SRAM.
- Enable PMA channels appropriately.
- Coordinate enumeration by decoding USB device requests.
- Suspend and resume coordination.
- Verify and select data toggle values.

10-bit ADC

The ADC on enCoRe V device is an independent block with a state machine interface to control accesses to the block. The ADC is housed together with the temperature sensor core and can be connected to this or the Analog mux bus. As a default operation, the ADC is connected to the temperature sensor diodes to give digital values of the temperature.

Figure 2. ADC System Performance Block Diagram



The ADC User Module contains an integrator block and one comparator with positive and negative input set by the MUXes. The input to the integrator stage comes from the analog global

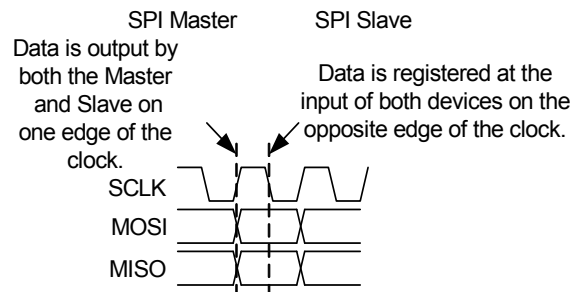
input mux or the temperature sensor with an input voltage range of 0 V to V_{REFADC} .

In the ADC only configuration (the ADC MUX selects the Analog mux bus, not the default temperature sensor connection), an external voltage can be connected to the input of the modulator for voltage conversion. The ADC is run for a number of cycles set by the timer, depending upon the desired resolution of the ADC. A counter counts the number of trips by the comparator, which is proportional to the input voltage. The Temp Sensor block clock speed is 36 MHz and is divided down to 1 to 12 MHz for ADC operation.

SPI

The serial peripheral interconnect (SPI) 3-wire protocol uses both edges of the clock to enable synchronous communication without the need for stringent setup and hold requirements.

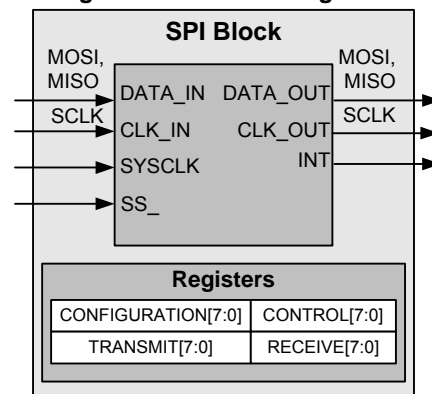
Figure 3. Basic SPI Configuration



A device can be a master or slave. A master outputs clock and data to the slave device and inputs slave data. A slave device inputs clock and data from the master device and outputs data for input to the master. Together, the master and slave are essentially a circular Shift register, where the master generates the clocking and initiates data transfers.

A basic data transfer occurs when the master sends eight bits of data, along with eight clocks. In any transfer, both master and slave transmit and receive simultaneously. If the master only sends data, the received data from the slave is ignored. If the master wishes to receive data from the slave, the master must send dummy bytes to generate the clocking for the slave to send data back.

Figure 4. SPI Block Diagram



SPI configuration register (SPI_CFG) sets master/slave functionality, clock speed, and interrupt select. SPI control register (SPI_CR) provides four control bits and four status bits for device interfacing and synchronization.

The SPIM hardware has no support for driving the Slave Select (SS_) signal. The behavior and use of this signal is dependent on the application and enCoRe V device and, if required, must be implemented in firmware.

There is an additional data input in the SPIS, Slave Select (SS_), which is an active low signal. SS_ must be asserted to enable the SPIS to receive and transmit. SS_ has two high level functions:

- To allow for the selection of a given slave in a multi-slave environment.
- To provide additional clocking for TX data queuing in SPI modes 0 and 1.

I²C Slave

The I²C slave enhanced communications block is a serial-to-parallel processor, designed to interface the enCoRe V device to a two-wire I²C serial communications bus. To eliminate the need for excessive CPU intervention and overhead, the block provides I²C-specific support for status detection and generation of framing bits. By default, the I²C slave enhanced module is firmware compatible with the previous generation of I²C slave functionality. However, this module provides new features that are configurable to implement significant flexibility for both internal and external interfacing. The basic I²C features include:

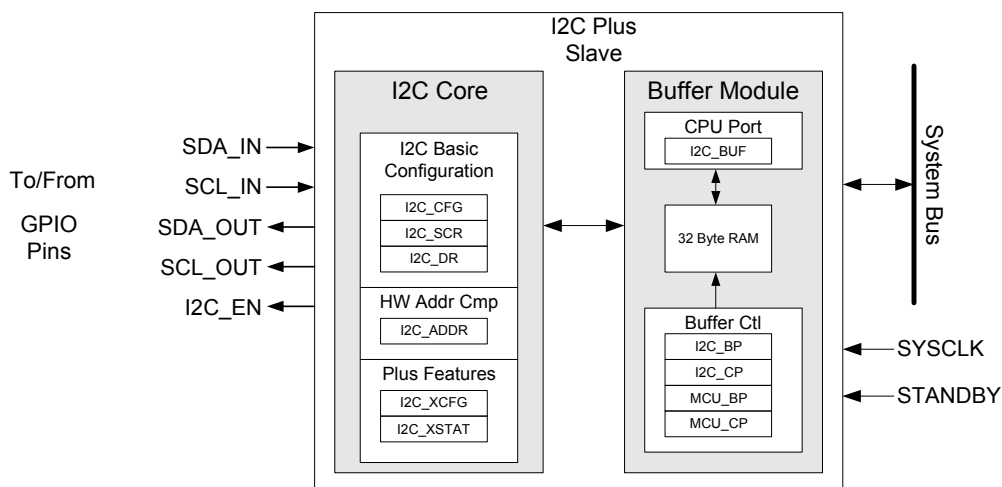
- Slave, transmitter, and receiver operation.
- Byte processing for low CPU overhead.

- Interrupt or polling CPU interface.
 - Support for clock rates of up to 400 kHz.
 - 7- or 10-bit addressing (through firmware support).
 - SMBus operation (through firmware support).
- Enhanced features of the I²C Slave Enhanced Module include:
- Support for 7-bit hardware address compare.
 - Flexible data buffering schemes.
 - A “no bus stalling” operating mode.
 - A low power bus monitoring mode.

The I²C block controls the data (SDA) and the clock (SCL) to the external I²C interface through direct connections to two dedicated GPIO pins. When I²C is enabled, these GPIO pins are not available for general purpose use. The enCoRe V CPU firmware interacts with the block through I/O register reads and writes, and firmware synchronization is implemented through polling and/or interrupts.

In the default operating mode, which is firmware compatible with previous versions of I²C slave modules, the I²C bus is stalled upon every received address or byte, and the CPU is required to read the data or supply data as required before the I²C bus continues. However, this I²C Slave Enhanced module provides new data buffering capability as an enhanced feature. In the EZI²C buffering mode, the I²C slave interface appears as a 32-byte RAM buffer to the external I²C master. Using a simple predefined protocol, the master controls the read and write pointers into the RAM. When this method is enabled, the slave never stalls the bus. In this protocol, the data available in the RAM (this is managed by the CPU) is valid.

Figure 5. I²C Block Diagram



Development Tools

PSoC Designer™ is the revolutionary Integrated Design Environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
 - Hardware and software I²C slaves and masters
 - Full-speed USB 2.0
 - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are analog-to-digital converters (ADCs), digital-to-analog converters (DACs), amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this allows you to use more than 100 percent of PSoC's resources for a given application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows you to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer.

In-Circuit Emulator

A low-cost, high-functionality In-Circuit Emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24-MHz) operation.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed-function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and lowering inventory costs. These configurable resources, called PSoC blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is:

1. Select [user modules](#).
2. Configure user modules.
3. Organize and connect.
4. Generate, verify, and debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called user modules. User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a Pulse width modulator (PWM) user module configures one or more digital PSoC blocks, one for each eight bits of resolution. Using these parameters, you can establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All of the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These [user module](#)

[data sheets](#) explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information that you may need to successfully implement your design.

Organize and Connect

Build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. Perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

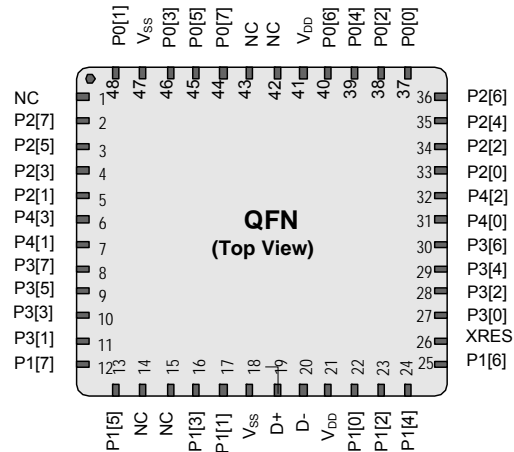
When you are ready to test the hardware configuration or move on to developing code for the project, perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides APIs with high-level functions to control and respond to hardware events at run time, and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer's Debugger (accessed by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer. It allows you to define complex breakpoint events that include monitoring address and data bus values, memory locations, and external signals.

48-pin Part Pinout

Figure 8. CY7C64355/CY7C64356 48-pin enCoRe V USB Device



Pin Definitions

48-pin Part Pinout (QFN)

Pin No.	Type	Pin Name	Description
1	NC	NC	No connection
2	I/O	P2[7]	Digital I/O
3	I/O	P2[5]	Digital I/O, crystal out (Xout)
4	I/O	P2[3]	Digital I/O, crystal in (Xin)
5	I/O	P2[1]	Digital I/O
6	I/O	P4[3]	Digital I/O
7	I/O	P4[1]	Digital I/O
8	I/O	P3[7]	Digital I/O
9	I/O	P3[5]	Digital I/O
10	I/O	P3[3]	Digital I/O
11	I/O	P3[1]	Digital I/O
12	I/OHR	P1[7]	Digital I/O, I ² C SCL, SPI SS
13	I/OHR	P1[5]	Digital I/O, I ² C SDA, SPI MISO
14	NC	NC	No connection
15	NC	NC	No connection
16	I/OHR	P1[3]	Digital I/O, SPI CLK
17	I/OHR	P1[1] ^[5, 6]	Digital I/O, ISSP CLK, I ² C SCL, SPI MOSI
18	Power	V _{SS}	Supply ground
19	I/O	D+	USB
20	I/O	D-	USB
21	Power	V _{DD}	Supply voltage
22	I/OHR	P1[0] ^[5, 6]	Digital I/O, ISSP DATA, I ² C SDA, SPI CLK
23	I/OHR	P1[2]	Digital I/O

Notes

- During power up or reset event, device P1[0] and P1[1] may disturb the I²C bus. Use alternate pins if issues are encountered.
- These are the in-system serial programming (ISSP) pins that are not High Z at power on reset (POR).

Table 3. Register Map Bank 1 Table: Configuration Space

Name	Addr (1, Hex)	Access	Name	Addr (1, Hex)	Access	Name	Addr (1, Hex)	Access	Name	Addr (1, Hex)	Access
PRT0DM0	00	RW	PMA4_RA	40	RW		80			C0	
PRT0DM1	01	RW	PMA5_RA	41	RW		81			C1	
	02		PMA6_RA	42	RW		82			C2	
	03		PMA7_RA	43	RW		83			C3	
PRT1DM0	04	RW	PMA8_WA	44	RW		84			C4	
PRT1DM1	05	RW	PMA9_WA	45	RW		85			C5	
	06		PMA10_WA	46	RW		86			C6	
	07		PMA11_WA	47	RW		87			C7	
PRT2DM0	08	RW	PMA12_WA	48	RW		88			C8	
PRT2DM1	09	RW	PMA13_WA	49	RW		89			C9	
	0A		PMA14_WA	4A	RW		8A			CA	
	0B		PMA15_WA	4B	RW		8B			CB	
PRT3DM0	0C	RW	PMA8_RA	4C	RW		8C			CC	
PRT3DM1	0D	RW	PMA9_RA	4D	RW		8D			CD	
	0E		PMA10_RA	4E	RW		8E			CE	
	0F		PMA11_RA	4F	RW		8F			CF	
PRT4DM0	10	RW	PMA12_RA	50	RW		90			D0	
PRT4DM1	11	RW	PMA13_RA	51	RW		91			D1	
	12		PMA14_RA	52	RW		92		ECO_ENBUS	D2	RW
	13		PMA15_RA	53	RW		93		ECO_TRIM	D3	RW
	14		EP1_CR0	54	#		94			D4	
	15		EP2_CR0	55	#		95			D5	
	16		EP3_CR0	56	#		96			D6	
	17		EP4_CR0	57	#		97			D7	
	18		EP5_CR0	58	#		98		MUX_CR0	D8	RW
	19		EP6_CRO	59	#		99		MUX_CR1	D9	RW
	1A		EP7_CR0	5A	#		9A		MUX_CR2	DA	RW
	1B		EP8_CR0	5B	#		9B		MUX_CR3	DB	RW
	1C			5C			9C		IO_CFG1	DC	RW
	1D			5D			9D		OUT_P1	DD	RW
	1E			5E			9E		IO_CFG2	DE	RW
	1F			5F			9F		MUX_CR4	DF	RW
	20			60			A0		OSC_CR0	E0	RW
	21			61			A1		ECO_CFG	E1	#
	22			62			A2		OSC_CR2	E2	RW
	23			63			A3		VLT_CR	E3	RW
	24			64			A4		VLT_CMP	E4	R
	25			65			A5			E5	
	26			66			A6			E6	
	27			67			A7			E7	
	28			68			A8		IMO_TR	E8	W
SPI_CFG	29	RW		69			A9		ILO_TR	E9	W
	2A			6A			AA			EA	
	2B			6B			AB		SLP_CFG	EB	RW
	2C		TMP_DR0	6C	RW		AC		SLP_CFG2	EC	RW
	2D		TMP_DR1	6D	RW		AD		SLP_CFG3	ED	RW
	2E		TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
USB_CR1	30	#		70			B0			F0	
	31			71			B1			F1	
	32			72			B2			F2	
	33			73			B3			F3	
PMA0_WA	34	RW		74			B4			F4	
PMA1_WA	35	RW		75			B5			F5	
PMA2_WA	36	RW		76			B6			F6	
PMA3_WA	37	RW		77			B7		CPU_F	F7	RL
PMA4_WA	38	RW		78			B8			F8	
PMA5_WA	39	RW		79			B9			F9	
PMA6_WA	3A	RW		7A			BA		IMO_TR1	FA	RW
PMA7_WA	3B	RW		7B			BB			FB	
PMA0_RA	3C	RW		7C			BC			FC	
PMA1_RA	3D	RW		7D		USB_MISC_CR	BD	RW		FD	
PMA2_RA	3E	RW		7E			BE			FE	
PMA3_RA	3F	RW		7F			BF			FF	

Gray fields are reserved; do not access these fields. # Access is bit specific.

Electrical Specifications

This section presents the DC and AC electrical specifications of the enCoRe V USB devices. For the most up-to-date electrical specifications, verify that you have the most recent data sheet available by visiting the company web site at <http://www.cypress.com>

Figure 9. Voltage versus CPU Frequency

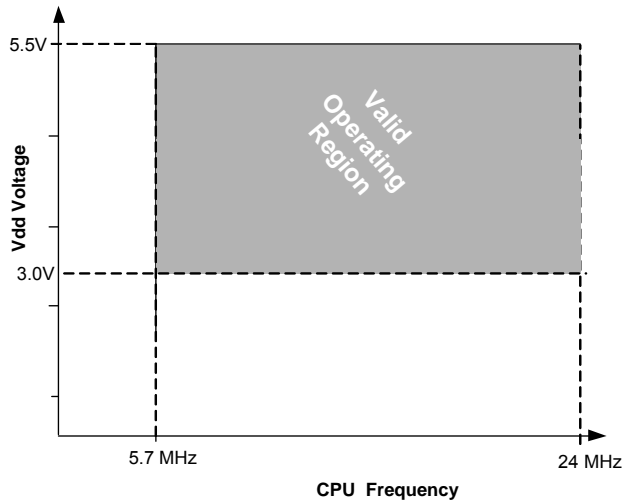
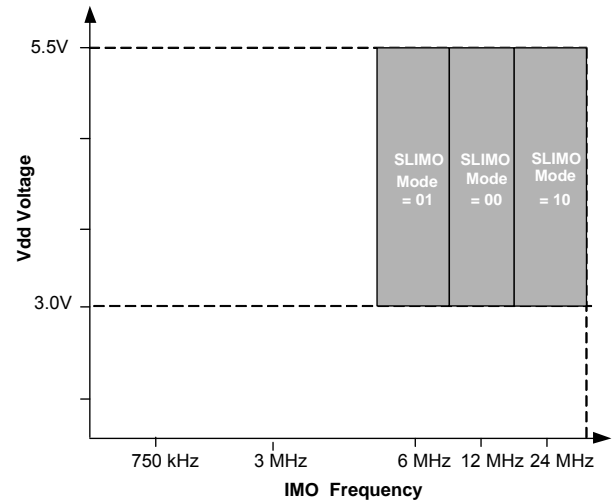


Figure 10. IMO Frequency Trim Options



DC Electrical Characteristics

DC Chip Level Specifications

Table 6 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 6. DC Chip Level Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{DD}	Operating voltage ^[7, 9]	No USB activity.	3.0	–	5.5	V
$I_{DD24,3}$	Supply current, CPU = 24 MHz	Conditions are $V_{DD} = 3.0\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$, CPU = 24 MHz, No USB/I ² C/SPI.	–	2.9	4.0	mA
$I_{DD12,3}$	Supply current, CPU = 12 MHz	Conditions are $V_{DD} = 3.0\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$, CPU = 12 MHz, No USB/I ² C/SPI.	–	1.7	2.6	mA
$I_{DD6,3}$	Supply current, CPU = 6 MHz	Conditions are $V_{DD} = 3.0\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$, CPU = 6 MHz, No USB/I ² C/SPI.	–	1.2	1.8	mA
$I_{SB1,3}$	Standby current with POR, LVD, and sleep timer	$V_{DD} = 3.0\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$, I/O regulator turned off.	–	1.1	1.5	μA
$I_{SB0,3}$	Deep sleep current	$V_{DD} = 3.0\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$, I/O regulator turned off.	–	0.1	–	μA
V_{DDUSB}	Operating voltage	USB activity, USB regulator enabled	4.35	–	5.25	V
$I_{DD24,5}$	Supply current, CPU = 24 MHz	Conditions are $V_{DD} = 5.0\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$, CPU = 24 MHz, $I_{MO} = 24\text{ MHz}$ USB Active, No I ² C/SPI.	–	7.1	–	mA
$I_{DD12,5}$	Supply current, CPU = 12 MHz	Conditions are $V_{DD} = 5.0\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$, CPU = 12 MHz, $I_{MO} = 24\text{ MHz}$ USB Active, No I ² C/SPI.	–	6.2	–	mA
$I_{DD6,5}$	Supply current, CPU = 6 MHz	Conditions are $V_{DD} = 5.0\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$, CPU = 6 MHz, $I_{MO} = 24\text{ MHz}$ USB Active, No I ² C/SPI.	–	5.8	–	mA
$I_{SB1,5}$	Standby current with POR, LVD, and sleep timer	$V_{DD} = 5.0\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$, I/O regulator turned off.	–	1.1	–	μA
$I_{SB0,5}$	Deep sleep current	$V_{DD} = 5.0\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$, I/O regulator turned off.	–	0.1	–	μA
V_{DDUSB}	Operating voltage	USB activity, USB regulator bypassed	3.15	3.3	3.60	V

Notes

10. Higher storage temperatures reduce data retention time. Recommended storage temperature is $+25\text{ }^{\circ}\text{C} \pm 25\text{ }^{\circ}\text{C}$. Extended duration storage temperatures above $85\text{ }^{\circ}\text{C}$ degrade reliability.
11. The temperature rise from ambient to junction is package specific. See [Package Handling on page 31](#). The user must limit the power consumption to comply with this requirement.

Table 7. DC Characteristics – USB Interface

Symbol	Description	Conditions	Min	Typ	Max	Units
Rusbi	USB D+ pull-up resistance	With idle bus	0.900	–	1.575	k Ω
Rusba	USB D+ pull-up resistance	While receiving traffic	1.425	–	3.090	k Ω
Vohusb	Static output high		2.8	–	3.6	V
Volusb	Static output low		–	–	0.3	V
Vdi	Differential input sensitivity		0.2	–	–	V
Vcm	Differential input common mode range		0.8	–	2.5	V
Vse	Single-ended receiver threshold		0.8	–	2.0	V
Cin	Transceiver capacitance			–	50	pF
Iio	High Z state data Line Leakage	On D+ or D– line	–10	–	+10	μ A
Rps2	PS/2 Pull Up Resistance		3	5	7	k Ω
Rext	External USB Series Resistor	In series with each USB pin	21.78	22.0	22.22	Ω

ADC Electrical Specifications

Table 8. ADC User Module Electrical Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
Input						
V _{IN}	Input voltage range		0	–	VREFADC	V
C _{IIN}	Input capacitance		–	–	5	pF
R _{IN}	Input resistance	Equivalent switched cap input resistance for 8-, 9-, or 10-bit resolution	1/(500fF* Data Clock)	1/(400fF* Data Clock)	1/(300fF* Data Clock)	Ω
Reference						
V _{REFADC}	ADC reference voltage		1.14	–	1.26	V
Conversion Rate						
F _{CLK}	Data clock	Source is chip's internal main oscillator. See AC Chip-Level Specifications for accuracy	2.25	–	6	MHz
S8	8-bit sample rate	Data Clock set to 6 MHz. Sample Rate = 0.001/ (2 [^] Resolution/Data Clock)	–	23.4375	–	ksps
S10	10-bit sample rate	Data Clock set to 6 MHz. Sample Rate = 0.001/ (2 [^] Resolution/Data Clock)	–	5.859	–	ksps
DC Accuracy						
RES	Resolution	Can be set to 8-, 9-, or 10-bit	8	–	10	bits
DNL	Differential nonlinearity		–1	–	+2	LSB
INL	Integral nonlinearity		–2	–	+2	LSB
E _{Offset}	Offset error	8-bit resolution	0	3.2	19.2	LSB
		10-bit resolution	0	12.8	76.8	LSB
E _{gain}	Gain error	For any resolution	–5	–	+5	%FSR
Power						
I _{ADC}	Operating current		–	2.1	2.6	mA
PSRR	Power supply rejection ratio	PSRR (V _{DD} > 3.0 V)	–	24	–	dB
		PSRR (V _{DD} < 3.0 V)	–	30	–	dB

DC General Purpose I/O Specifications

Table 9 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and package specific temperature range. Typical parameters apply to 5 V and 3.3 V at 25 °C. These are for design guidance only.

Table 9. 3.0 V and 5.5 V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R _{PU}	Pull-up resistor		4	5.6	8	kΩ
V _{OH1}	High output voltage Port 2 or 3 pins	I _{OH} ≤ 10 μA, maximum of 10 mA source current in all I/Os.	V _{DD} – 0.2	–	–	V
V _{OH2}	High output voltage Port 2 or 3 Pins	I _{OH} = 1 mA, maximum of 20 mA source current in all I/Os.	V _{DD} – 0.9	–	–	V
V _{OH3}	High output voltage Port 0 or 1 pins with LDO regulator disabled	I _{OH} < 10 μA, maximum of 10 mA source current in all I/Os.	V _{DD} – 0.2	–	–	V
V _{OH4}	High output voltage Port 0 or 1 pins with LDO regulator disabled	I _{OH} = 5 mA, maximum of 20 mA source current in all I/Os.	V _{DD} – 0.9	–	–	V
V _{OH5}	High output voltage Port 1 pins with LDO regulator enabled for 3 V Out	I _{OH} < 10 μA, V _{DD} > 3.1 V, maximum of 4 I/Os all sourcing 5 mA	2.85	3.00	3.3	V
V _{OH6}	High output voltage Port 1 pins with LDO regulator enabled for 3 V out	I _{OH} = 5 mA, V _{DD} > 3.1 V, maximum of 20 mA source current in all I/Os	2.20	–	–	V
V _{OH7}	High output voltage Port 1 pins with LDO enabled for 2.5 V out	I _{OH} < 10 μA, V _{DD} > 3.0 V, maximum of 20 mA source current in all I/Os	2.35	2.50	2.75	V
V _{OH8}	High output voltage Port 1 pins with LDO enabled for 2.5 V out	I _{OH} = 2 mA, V _{DD} > 3.0 V, maximum of 20 mA source current in all I/Os	1.90	–	–	V
V _{OH9}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	I _{OH} < 10 μA, V _{DD} > 3.0 V, maximum of 20 mA source current in all I/Os	1.60	1.80	2.1	V
V _{OH10}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	I _{OH} = 1 mA, V _{DD} > 3.0 V, maximum of 20 mA source current in all I/Os	1.20	–	–	V
V _{OL}	Low output voltage	I _{OL} = 25 mA, V _{DD} > 3.3 V, maximum of 60 mA sink current on even port pins (for example, P0[2] and P1[4]) and 60 mA sink current on odd port pins (for example, P0[3] and P1[5]).	–	–	0.75	V
V _{IL}	Input low voltage		–	–	0.8	V
V _{IH}	Input high voltage		2.0	–	–	V
V _H	Input hysteresis voltage		–	80	–	mV
I _{IL}	Input leakage (absolute value)		–	0.001	1	μA
C _{PIN}	Pin capacitance	Package and pin dependent. Temp = 25 °C.	0.5	1.7	5	pF

AC Electrical Characteristics

AC Chip Level Specifications

The following tables list guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 12. AC Chip Level Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F _{CPU}	Processing frequency ^[16]		5.7	–	25.2	MHz
F _{32K1}	Internal low-speed oscillator (ILO) frequency	Trimmed ^[17]	19	32	50	kHz
F _{32K U}	ILO untrimmed frequency)		13	32	82	kHz
F _{32K2}	ILO frequency	Untrimmed	13	32	82	kHz
F _{IMO24}	Internal main oscillator (IMO) stability for 24 MHz \pm 5% ⁽¹²⁾		22.8	24	25.2	MHz
F _{IMO12}	IMO stability for 12 MHz ^[17]		11.4	12	12.6	MHz
F _{IMO6}	IMO stability for 6 MHz ^[17]		5.7	6.0	6.3	MHz
DC _{IMO}	Duty cycle of IMO		40	50	60	%
DC _{ILO}	ILO duty cycle		40	50	60	%
SR _{POWER_UP}	Power supply slew rate		–	–	250	V/ms
T _{XRST}	External reset pulse width at power-up	After supply voltage is valid	1	–	–	ms
T _{XRST2}	External reset pulse width after power-up ^[18]	Applies after part has booted	10	–	–	μs

Table 13. AC Characteristics – USB Data Timings

Symbol	Description	Conditions	Min	Typ	Max	Units
Td _{rate}	Full speed data rate	Average bit rate	11.97	12	12.03	MHz
Td _{jr1}	Receiver data jitter tolerance	To next transition	–18.5	–	18.5	ns
Td _{jr2}	Receiver data jitter tolerance	To pair transition	–9	–	9	ns
Td _{uj1}	Driver differential jitter	To next transition	–3.5	–	3.5	ns
Td _{uj2}	Driver differential jitter	To pair transition	–4.0	–	4.0	ns
Tf _{deop}	Source jitter for differential transition	To SE0 transition	–2	–	5	ns
Tf _{eo_{pt}}	Source SE0 interval of EOP		160	–	175	ns
Tf _{eo_{pr}}	Receiver SE0 interval of EOP		82	–	–	ns
Tf _{st}	Width of SE0 interval during differential transition		–	–	14	ns

Table 14. AC Characteristics – USB Driver

Symbol	Description	Conditions	Min	Typ	Max	Units
Tr	Transition rise time	50 pF	4	–	20	ns
Tf	Transition fall time	50 pF	4	–	20	ns
TR ^[19]	Rise/fall time matching		90.00	–	111.1	%
V _{crs}	Output signal crossover voltage		1.3	–	2.0	V

Notes

16. V_{DD} = 3.0 V and T_J = 85 °C, CPU speed.

17. Trimmed for 3.3 V operation using factory trim values.

18. The minimum required XRES pulse length is longer when programming the device (see [Table 17 on page 24](#)).

19. **Errata:** Rising to falling rate matching of the USB D+ and D- lines has a corner case issue when operating voltage is below 3.3 V. Refer to “[Errata](#)” on page 35 for more details.

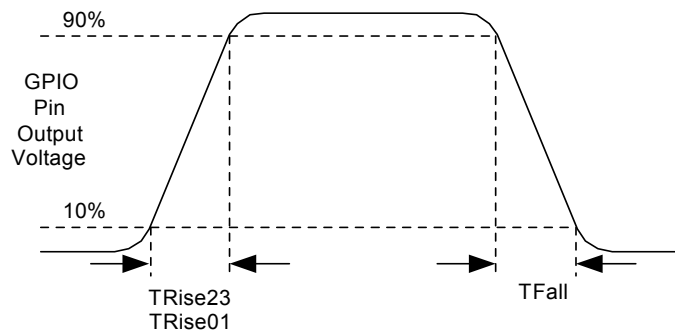
AC General Purpose I/O Specifications

Table 15 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 15. AC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{GPIO}	GPIO operating frequency	Normal strong mode, Ports 0, 1	–	–	12	MHz
TRise23	Rise time, strong mode Ports 2, 3	$V_{DD} = 3.0$ to 3.6 V, 10% - 90%	15	–	80	ns
TRise01	Rise time, strong mode Ports 0, 1	$V_{DD} = 3.0$ to 3.6 V, 10% - 90%	10	–	50	ns
TFall	Fall time, strong mode All Ports	$V_{DD} = 3.0$ to 3.6 V, 10% - 90%	10	–	50	ns

Figure 11. GPIO Timing Diagram



AC External Clock Specifications

Table 16 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 16. AC External Clock Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{OSCEXT}	Frequency		0.750	–	25.2	MHz
–	High period		20.6	–	5300	ns
–	Low period		20.6	–	–	ns
–	Power-up IMO to switch		150	–	–	μs

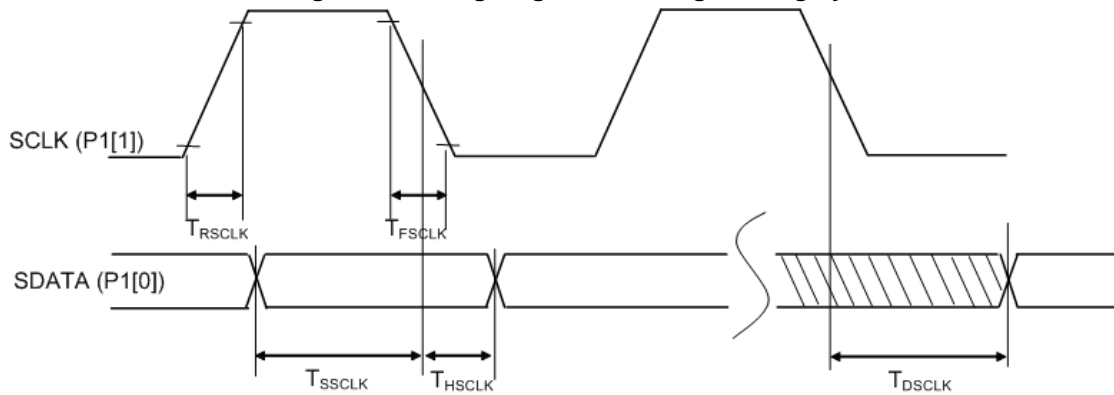
AC Programming Specifications

Table 17 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 17. AC Programming Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{RSCLK}	Rise time of SCLK		1	–	20	ns
T_{FSCLK}	Fall time of SCLK		1	–	20	ns
T_{SSCLK}	Data setup time to falling edge of SCLK		40	–	–	ns
T_{HSCLK}	Data hold time from falling edge of SCLK		40	–	–	ns
F_{SCLK}	Frequency of SCLK		0	–	8	MHz
T_{ERASEB}	Flash erase time (Block)		–	–	18	ms
T_{WRITE}	Flash block write time		–	–	25	ms
T_{DSCLK1}	Data out delay from falling edge of SCLK,	$V_{DD} > 3.6\text{ V}$	–	–	60	ns
T_{DSCLK2}	Data out delay from falling edge of SCLK	$3.0\text{ V} < V_{DD} < 3.6\text{ V}$	–	–	85	ns
T_{XRST3}	External reset pulse width after power-up	Required to enter programming mode when coming out of sleep	263	–	–	μs

Figure 12. Timing Diagram - AC Programming Cycle



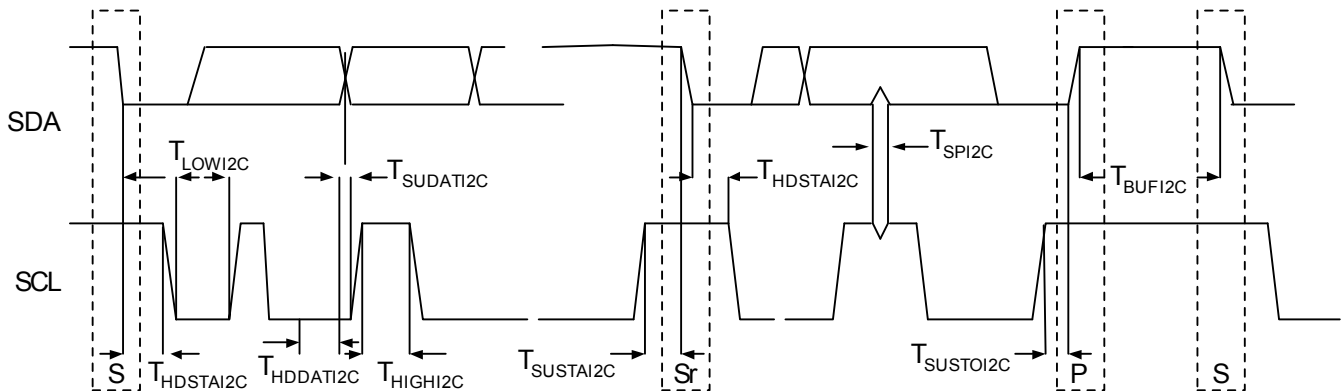
AC I²C Specifications

Table 18 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 18. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
F _{SCL I2C}	SCL clock frequency	0	100	0	400	kHz
T _{HDSTAI2C}	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4.0	–	0.6	–	μs
T _{LOWI2C}	LOW period of the SCL clock	4.7	–	1.3	–	μs
T _{HIGHI2C}	HIGH period of the SCL clock	4.0	–	0.6	–	μs
T _{SUSTAI2C}	Setup time for a repeated START condition	4.7	–	0.6	–	μs
T _{HDDATI2C}	Data hold time	0	–	0	–	μs
T _{SUDATI2C}	Data setup time	250	–	100 ^[20]	–	ns
T _{SUSTOI2C}	Setup time for STOP condition	4.0	–	0.6	–	μs
T _{BUFI2C}	Bus free time between a STOP and START condition	4.7	–	1.3	–	μs
T _{SPI2C}	Pulse width of spikes are suppressed by the input filter	–	–	0	50	ns

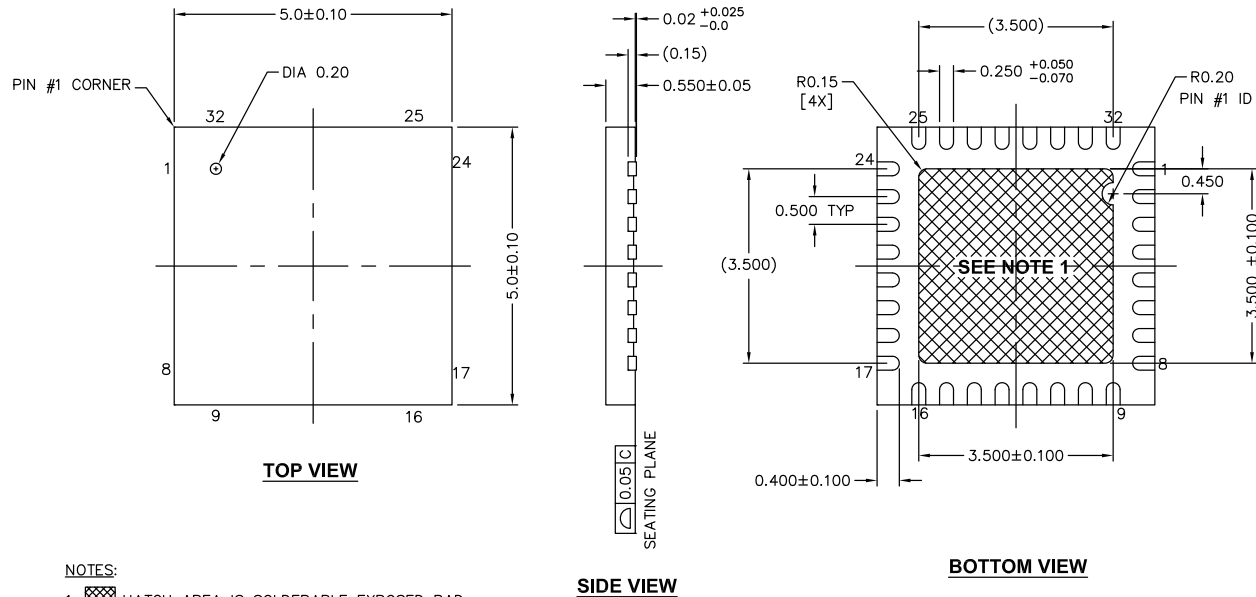
Figure 13. Definition of Timing for Fast/Standard Mode on the I²C Bus



Note

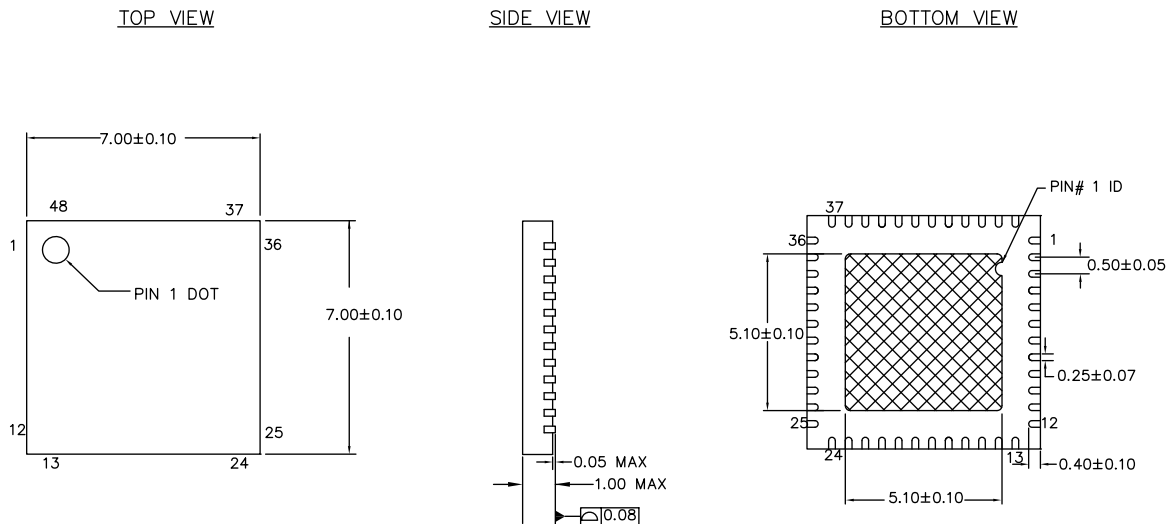
20. A Fast mode I²C bus device can be used in a standard mode I²C bus system, but the requirement $t_{SUDAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SUDAT} = 1000 + 250 = 1250$ ns (according to the standard mode I²C bus specification) before the SCL line is released.

Figure 19. 32-pin QFN (5 × 5 × 0.55 mm) LQ32 3.5 × 3.5 E-Pad (Sawn) Package Outline, 001-42168



001-42168 *E

Figure 20. 48-pin QFN (7 × 7 × 1.00 mm) LT48A 5.1 × 5.1 E-Pad (Sawn) Package Outline, 001-13191



001-13191 *H

Package Handling

Some IC packages require baking before they are soldered onto a PCB to remove moisture that may have been absorbed after leaving the factory. A label on the package has details about the actual bake temperature and the minimum bake time to remove this moisture. The maximum bake time is the aggregate time that the parts exposed to the bake temperature. Exceeding this exposure may degrade device reliability.

Table 21. Package Handling

Parameter	Description	Minimum	Typical	Maximum	Unit
TBAKETEMP	Bake temperature	–	125	See package label	°C
TBAKETIME	Bake time	See package label	–	72	hours

Thermal Impedances

Table 22. Thermal Impedances per Package

Package	Typical θ_{JA} ^[21]
16-pin QFN	32.69 °C / W
32-pin QFN ^[22]	19.51 °C / W
48-pin QFN ^[22]	17.68 °C / W

Capacitance on Crystal Pins

Table 23. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
32-pin QFN	3.2 pF
48-pin QFN	3.3 pF

Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Table 24. Solder Reflow Peak Temperature

Package	Minimum Peak Temperature ^[23]	Maximum Peak Temperature
16-pin QFN	240 °C	260 °C
32-pin QFN	240 °C	260 °C
48-pin QFN	240 °C	260 °C

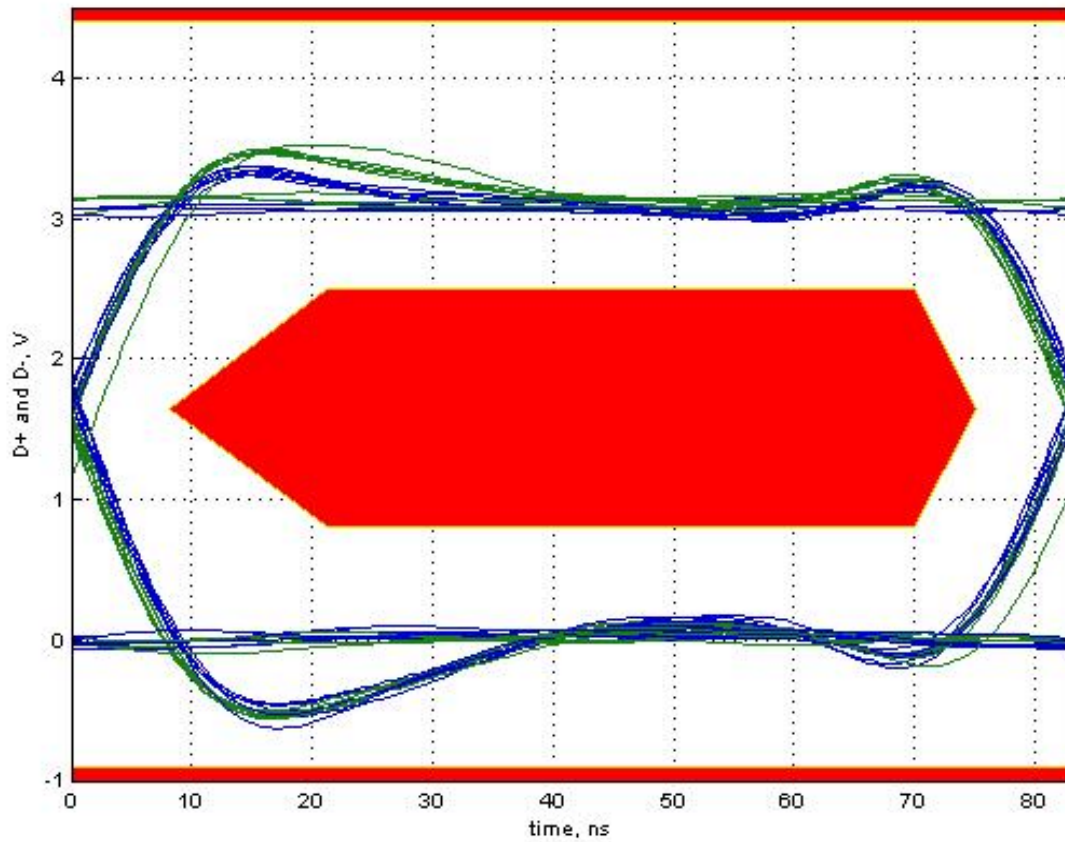
Notes

21. $T_J = T_A + \text{Power} \times \theta_{JA}$

22. To achieve the thermal impedance specified for the package, solder the center thermal pad to the PCB ground plane.

23. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5 °C with Sn-Pb or 245 ± 5 °C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

Figure 21. Eye Diagram



■WORKAROUND

Avoid the trigger condition by using lower tolerance voltage regulators.

■FIX STATUS

This issue will not be corrected in the next new silicon revision.

Document History Page *(continued)*

Document Title: CY7C6431x/CY7C6434x/CY7C6435x, enCoRe™ V Full Speed USB Controller Document Number: 001-12394				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*F	2583853	TYJ / PYRS / HMT	10/10/08	<p>Converted from Preliminary to Final</p> <p>Added operating voltage ranges with USB</p> <p>ADC resolution changed from 10-bit to 8-bit</p> <p>Rephrased battery monitoring clause in page 1 to include “with external components”</p> <p>Included ADC specifications table</p> <p>Included Voh7, Voh8, Voh9, Voh10 specs</p> <p>Flash data retention – condition added to Note [11]</p> <p>Input leakage spec changed to 25 nA max</p> <p>Under AC Char, Frequency accuracy of ILO corrected</p> <p>GPIO rise time for ports 0,1 and ports 2,3 made common</p> <p>AC Programming specifications updated</p> <p>Included AC Programming cycle timing diagram</p> <p>AC SPI specification updated</p> <p>Spec change for 32-QFN package</p> <p>Input Leakage Current maximum value changed to 1 μA</p> <p>Updated V_{OHV} parameter in Table 13</p> <p>Updated thermal impedances for the packages</p> <p>Update Development Tools, add Designing with PSoC Designer. Edit, fix links and table format. Update TMs.</p>
*G	2653717	DVJA / PYRS	02/04/09	<p>Updated Features, Functional Overview, Development Tools, and Designing with PSoC Designer sections with edits.</p> <p>Removed ‘GUI - graphical user interface’ from Document Conventions acronym table.</p> <p>Removed ‘O - Only a read/write register or bits’ in Table 4</p> <p>Edited Table 8: removed 10-bit resolution information and corrected units column.</p> <p>Added package handling section</p> <p>Added 8K part ‘CY7C64343-32LQXC’ to Ordering Information.</p>
*H	2714694	DVJA / AESA	06/04/2009	<p>Updated Block Diagram.</p> <p>Added Full Speed USB, 10-bit ADC, SPI, and I2C Slave sections.</p> <p>ADC Resolution changed from 8-bit to 10-bit</p> <p>Updated Table 9 DC Chip Level Specs</p> <p>Updated Table 10 DC Char - USB Interface</p> <p>Updated Table 12 DC POR and LDV Specs</p> <p>Changed operating temperature from Commercial to Industrial</p> <p>Changed Temperature Range to Industrial: –40 to 85°C</p> <p>Figure 9: Changed minimum CPU Frequency from 750 kHz to 5.7 MHz</p> <p>Table 14: Removed “Maximum” from the F_{CPU} description</p> <p>Ordering Information: Replaced ‘C’ with ‘I’ in all part numbers to denote Industrial Temp Range</p>
*I	2764460	DVJA / AESA	09/16/2009	<p>Changed Table 12: ADC Specs</p> <p>Added F_{32K2} (Untrimmed) spec to Table 16: AC Chip level Specs</p> <p>Changed T_{RAMP} spec to SR_{POWER_UP} in Table 16: AC Chip Level Specs</p> <p>Added Table 27: Typical Package Capacitance on Crystal Pins</p>
*J	2811903	DVJA	11/20/2009	<p>Added USB-IF TID number in Features on page 1. Added Note 5 on page 18.</p> <p>Changed V_{IHP} in Table 12 on page 22.</p>

Document History Page *(continued)*

Document Title: CY7C6431x/CY7C6434x/CY7C6435x, enCoRe™ V Full Speed USB Controller Document Number: 001-12394				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*K	2874274	KKU / PYRS	02/05/10	On page 4, changed the input voltage range from '0 V to 1.3 V' to '0 V to V _{REFADC} '. Added note for Operating Voltage in Table 6 . Updated Register Map. Added SPI slave and master mode diagrams; in Table 19 , changed T _{OUT_HIGH} parameter to T _{OUT_H} and modified description; in Table 20 , updated T _{SS_CLK} and T _{CLK_SS} min values to 2/F _{SCLK} and changed description of T _{SS_MISO} . Added V _{dd_USB} parameter in Table 6 . Updated package diagrams.
*L	3028310	XUT	09/13/2010	Removed HPOR bit reference from DC POR and LVD Specifications . Updated Development Tools and Designing with PSoC Designer . Added Ordering Code Definitions . Moved Acronyms and Document Conventions to end of document.
*M	3048308	NXZ	10/06/2010	Updated Features section as furnished in the CDT 74890 Updated datasheet as per new template All footnotes updated sequentially
*N	3557631	CSAI	03/21/2012	Updated Getting Started . Updated Package Diagrams . Updated in new template.
*O	3912957	NXZ	03/06/2013	Updated Functional Overview (Updated The enCoRe V Core (Updated contents in the section), updated Full-Speed USB (Updated contents in the section)). Updated Register Mapping Tables (Updated Table 3 (Replaced "ECO_ENBUS" with "ECO_ENBUS" and replaced "ECO_TRIM" with "ECO_TRIM")). Updated Package Diagrams : spec 001-09116 – Changed revision from *F to *H. spec 001-42168 – Changed revision from *D to *E. spec 001-13191 – Changed revision from *F to *G.
*P	3979449	ANKC	04/23/2013	Added Errata .
*Q	4074443	ANKC	07/23/2013	Added Errata footnotes (Note 8, 19). Updated Electrical Specifications : Updated Absolute Maximum Ratings : Added Note 8 and referred the same note in LU parameter. Updated AC Electrical Characteristics Updated AC Chip Level Specifications : Added Note 19 and referred the same note in TR parameter in Table 14 . Updated to new template.
*R	4197134	ANKC	11/20/2013	Updated Package Diagrams : spec 001-09116 – Changed revision from *H to *I. Completing Sunset Review.

Document History Page *(continued)*

Document Title: CY7C6431x/CY7C6434x/CY7C6435x, enCoRe™ V Full Speed USB Controller Document Number: 001-12394				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*S	4578605	GINS	12/11/2014	Updated Pin Information : Updated 32-pin part pinout : Updated Figure 7 (No change in figure, included CY7C64346 in figure caption). Updated Package Diagrams : spec 001-09116 – Changed revision from *I to *J. Updated Ordering Information : Updated Table 25 : Updated part numbers.
*T	5548557	ANKC	12/12/2016	Updated Cypress Logo, Sales Page and Disclaimer. Updated Figure 20 (spec 001-13191 *G to *H) in Package Diagrams . Removed the following obsolete part numbers (Table 26) in Ordering Information : CY7C64343-32LQXI, CY7C64343-32LQXIT, CY7C64345-32LQXI, CY7C64345-32LQXIT, CY7C64356-48LTXI, CY7C64356-48LTXIT.