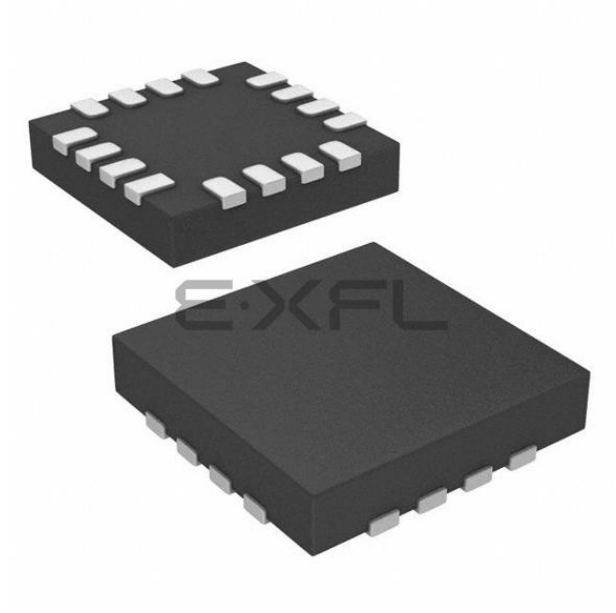

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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	USB Microcontroller
Core Processor	M8C
Program Memory Type	FLASH (32kB)
Controller Series	CY7C643xx
RAM Size	2K x 8
Interface	I²C, SPI, USB
Number of I/O	11
Voltage - Supply	3V ~ 5.5V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	16-UFQFN
Supplier Device Package	16-QFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy7c64316-16lkxc

Contents

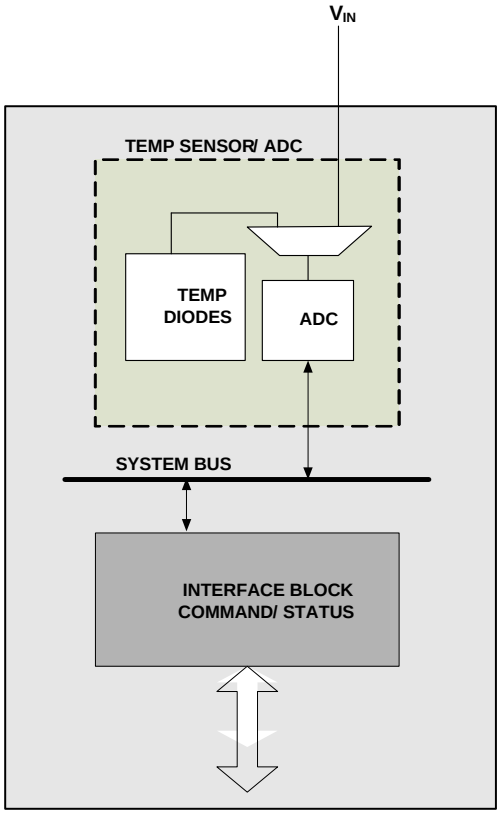
Firmware is required to handle various parts of the USB interface. The SIE issues interrupts after key USB events to direct firmware to appropriate tasks:

- Fill and empty the USB data buffers in USB SRAM.
- Enable PMA channels appropriately.
- Coordinate enumeration by decoding USB device requests.
- Suspend and resume coordination.
- Verify and select data toggle values.

10-bit ADC

The ADC on enCoRe V device is an independent block with a state machine interface to control accesses to the block. The ADC is housed together with the temperature sensor core and can be connected to this or the Analog mux bus. As a default operation, the ADC is connected to the temperature sensor diodes to give digital values of the temperature.

Figure 2. ADC System Performance Block Diagram



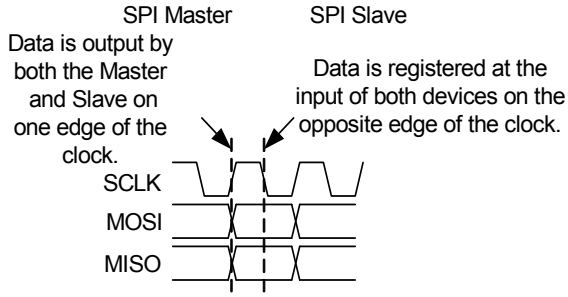
The ADC User Module contains an integrator block and one comparator with positive and negative input set by the MUXes. The input to the integrator stage comes from the analog global input mux or the temperature sensor with an input voltage range of 0 V to V_{REFADC}.

In the ADC only configuration (the ADC MUX selects the Analog mux bus, not the default temperature sensor connection), an external voltage can be connected to the input of the modulator for voltage conversion. The ADC is run for a number of cycles set by the timer, depending upon the desired resolution of the ADC. A counter counts the number of trips by the comparator, which is proportional to the input voltage. The Temp Sensor block clock speed is 36 MHz and is divided down to 1 to 12 MHz for ADC operation.

SPI

The serial peripheral interconnect (SPI) 3-wire protocol uses both edges of the clock to enable synchronous communication without the need for stringent setup and hold requirements.

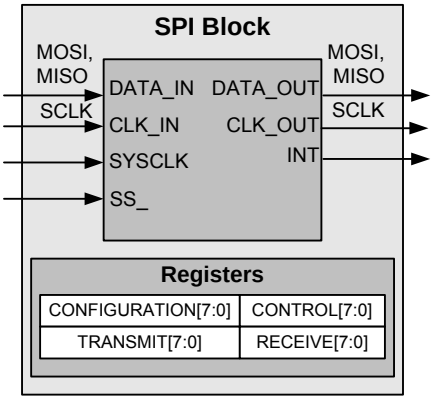
Figure 3. Basic SPI Configuration



A device can be a master or slave. A master outputs clock and data to the slave device and inputs slave data. A slave device inputs clock and data from the master device and outputs data for input to the master. Together, the master and slave are essentially a circular Shift register, where the master generates the clocking and initiates data transfers.

A basic data transfer occurs when the master sends eight bits of data, along with eight clocks. In any transfer, both master and slave transmit and receive simultaneously. If the master only sends data, the received data from the slave is ignored. If the master wishes to receive data from the slave, the master must send dummy bytes to generate the clocking for the slave to send data back.

Figure 4. SPI Block Diagram



SPI configuration register (SPI_CFG) sets master/slave functionality, clock speed, and interrupt select. SPI control register (SPI_CR) provides four control bits and four status bits for device interfacing and synchronization.

The SPIM hardware has no support for driving the Slave Select (SS_) signal. The behavior and use of this signal is dependent on the application and enCoRe V device and, if required, must be implemented in firmware.

There is an additional data input in the SPIS, Slave Select (SS_), which is an active low signal. SS_ must be asserted to enable the SPIS to receive and transmit. SS_ has two high level functions:

- To allow for the selection of a given slave in a multi-slave environment.
- To provide additional clocking for TX data queuing in SPI modes 0 and 1.

I²C Slave

The I²C slave enhanced communications block is a serial-to-parallel processor, designed to interface the enCoRe V device to a two-wire I²C serial communications bus. To eliminate the need for excessive CPU intervention and overhead, the block provides I²C-specific support for status detection and generation of framing bits. By default, the I²C slave enhanced module is firmware compatible with the previous generation of I²C slave functionality. However, this module provides new features that are configurable to implement significant flexibility for both internal and external interfacing. The basic I²C features include:

- Slave, transmitter, and receiver operation.
- Byte processing for low CPU overhead.
- Interrupt or polling CPU interface.
- Support for clock rates of up to 400 kHz.
- 7- or 10-bit addressing (through firmware support).
- SMBus operation (through firmware support).

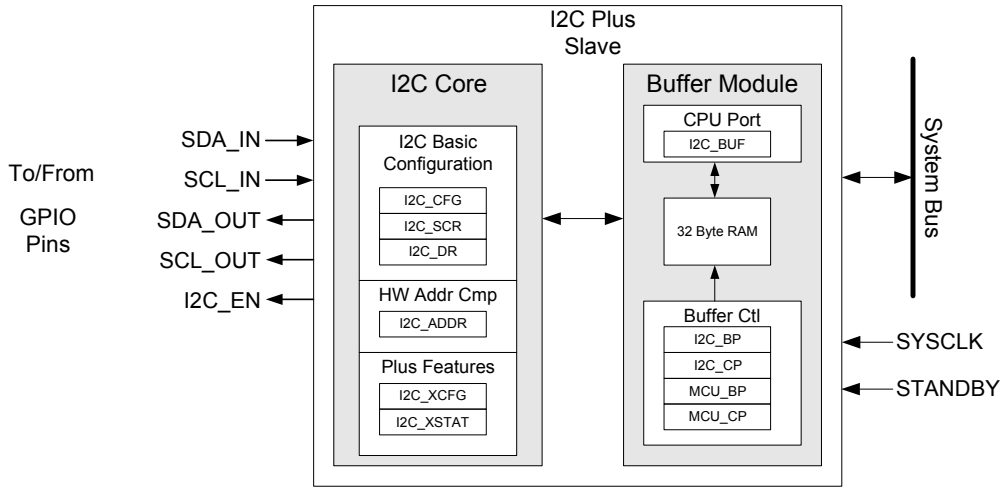
Enhanced features of the I²C Slave Enhanced Module include:

- Support for 7-bit hardware address compare.
- Flexible data buffering schemes.
- A “no bus stalling” operating mode.
- A low power bus monitoring mode.

The I²C block controls the data (SDA) and the clock (SCL) to the external I²C interface through direct connections to two dedicated GPIO pins. When I²C is enabled, these GPIO pins are not available for general purpose use. The enCoRe V CPU firmware interacts with the block through I/O register reads and writes, and firmware synchronization is implemented through polling and/or interrupts.

In the default operating mode, which is firmware compatible with previous versions of I²C slave modules, the I²C bus is stalled upon every received address or byte, and the CPU is required to read the data or supply data as required before the I²C bus continues. However, this I²C Slave Enhanced module provides new data buffering capability as an enhanced feature. In the EZI²C buffering mode, the I²C slave interface appears as a 32-byte RAM buffer to the external I²C master. Using a simple predefined protocol, the master controls the read and write pointers into the RAM. When this method is enabled, the slave never stalls the bus. In this protocol, the data available in the RAM (this is managed by the CPU) is valid.

Figure 5. I²C Block Diagram



Additional System Resources

System resources, some of which have been previously listed, provide additional capability useful to complete systems. Additional resources include low voltage detection and power on reset. The following statements describe the merits of each system resource.

- Low voltage detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR (power on reset) circuit eliminates the need for a system supervisor.
- The 5 V maximum input, 1.8, 2.5, or 3 V selectable output, LDO regulator provides regulation for I/Os. A register controlled bypass mode enables the user to disable the LDO.
- Standard Cypress PSoC IDE tools are available for debugging the enCoRe V family of parts.

Getting Started

The quickest path to understanding the enCoRe V silicon is by reading this data sheet and using the PSoC Designer Integrated Development Environment (IDE). This datasheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications. For in-depth information, along with detailed programming information, see the *enCoRe™ V CY7C643xx, enCoRe™ V LV CY7C604xx Technical Reference Manual (TRM)* for this PSoC device.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device data sheets on the web at http://www.cypress.com.

Application Notes

Application notes are an excellent introduction to the wide variety of possible PSoC designs and are available at http://www.cypress.com.

Development Kits

PSoC development kits are available online from Cypress at http://www.cypress.com and through a growing number of regional and global distributors, including Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops) is available online at http://www.cypress.com. The training covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant, go to http://www.cypress.com and look for CYPros Consultants.

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Visit our growing library of solution-focused designs at http://www.cypress.com. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

For assistance with technical issues, search KnowledgeBase articles and forums at http://www.cypress.com. If you cannot find an answer to your question, call technical support at 1-800-541-4736.

Development Tools

PSoC Designer™ is the revolutionary Integrated Design Environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
  - Hardware and software I^2C slaves and masters
  - Full-speed USB 2.0
  - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are analog-to-digital converters (ADCs), digital-to-analog converters (DACs), amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this allows you to use more than 100 percent of PSoC's resources for a given application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows you to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer.

In-Circuit Emulator

A low-cost, high-functionality In-Circuit Emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24-MHz) operation.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed-function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and lowering inventory costs. These configurable resources, called PSoC blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is:

1. Select user modules.
2. Configure user modules.
3. Organize and connect.
4. Generate, verify, and debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called user modules. User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a Pulse width modulator (PWM) user module configures one or more digital PSoC blocks, one for each eight bits of resolution. Using these parameters, you can establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All of the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module data sheets explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information that you may need to successfully implement your design.

Organize and Connect

Build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. Perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

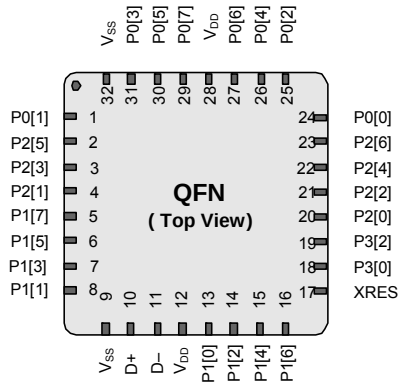
When you are ready to test the hardware configuration or move on to developing code for the project, perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides APIs with high-level functions to control and respond to hardware events at run time, and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer’s Debugger (accessed by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer. It allows you to define complex breakpoint events that include monitoring address and data bus values, memory locations, and external signals.

32-pin part pinout

Figure 7. CY7C64343/CY7C64345/CY7C64346 32-pin enCoRe V USB Device



Pin Definitions

32-pin part pinout (QFN)

Pin No.	Type	Name	Description
1	I/OH	P0[1]	Digital I/O
2	I/O	P2[5]	Digital I/O, crystal output (Xout)
3	I/O	P2[3]	Digital I/O, crystal Input (Xin)
4	I/O	P2[1]	Digital I/O
5	I/OHR	P1[7]	Digital I/O, I^2C SCL, SPI SS
6	I/OHR	P1[5]	Digital I/O, I^2C SDA, SPI MISO
7	I/OHR	P1[3]	Digital I/O, SPI CLK
8	I/OHR	P1[1][3, 4]	Digital I/O, ISSP CLK, I^2C SCL, SPI MOSI
9	Power	V_{SS}	Ground
10	I/O	D+	USB PHY
11	I/O	D–	USB PHY
12	Power	V_{DD}	Supply voltage
13	I/OHR	P1[0][3, 4]	Digital I/O, ISSP DATA, I^2C SDA, SPI CLK
14	I/OHR	P1[2]	Digital I/O
15	I/OHR	P1[4]	Digital I/O, optional external clock input (EXTCLK)
16	I/OHR	P1[6]	Digital I/O
17	Reset	XRES	Active high external reset with internal pull down
18	I/O	P3[0]	Digital I/O
19	I/O	P3[2]	Digital I/O
20	I/O	P2[0]	Digital I/O
21	I/O	P2[2]	Digital I/O
22	I/O	P2[4]	Digital I/O
23	I/O	P2[6]	Digital I/O
24	I/OH	P0[0]	Digital I/O
25	I/OH	P0[2]	Digital I/O
26	I/OH	P0[4]	Digital I/O
27	I/OH	P0[6]	Digital I/O
28	Power	V_{DD}	Supply voltage
29	I/OH	P0[7]	Digital I/O
30	I/OH	P0[5]	Digital I/O
31	I/OH	P0[3]	Digital I/O
32	Power	V_{SS}	Ground
CP	Power	V_{SS}	Ensure the center pad is connected to ground

LEGEND I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output

Notes
3. During power up or reset event, device P1[0] and P1[1] may disturb the I^2C bus. Use alternate pins if issues are encountered.
4. These are the in-system serial programming (ISSP) pins that are not High Z at power on reset (POR).

Pin Definitions

48-pin Part Pinout (QFN)

Pin No.	Type	Pin Name	Description
24	I/OHR	P1[4]	Digital I/O, optional external clock input (EXTCLK)
25	I/OHR	P1[6]	Digital I/O
26	XRES	Ext Reset	Active high external reset with internal pull down
27	I/O	P3[0]	Digital I/O
28	I/O	P3[2]	Digital I/O
29	I/O	P3[4]	Digital I/O
30	I/O	P3[6]	Digital I/O
31	I/O	P4[0]	Digital I/O
32	I/O	P4[2]	Digital I/O
33	I/O	P2[0]	Digital I/O
34	I/O	P2[2]	Digital I/O
35	I/O	P2[4]	Digital I/O
36	I/O	P2[6]	Digital I/O
37	I/OH	P0[0]	Digital I/O
38	I/OH	P0[2]	Digital I/O
39	I/OH	P0[4]	Digital I/O
40	I/OH	P0[6]	Digital I/O
41	Power	V_{DD}	Supply voltage
42	NC	NC	No connection
43	NC	NC	No connection
44	I/OH	P0[7]	Digital I/O
45	I/OH	P0[5]	Digital I/O
46	I/OH	P0[3]	Digital I/O
47	Power	V_{SS}	Supply ground
48	I/OH	P0[1]	Digital I/O
CP	Power	V_{SS}	Ensure the center pad is connected to ground

LEGEND I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 4. Absolute Maximum Ratings

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{STG}	Storage temperature[10]	Higher storage temperatures reduces data retention time. Recommended Storage Temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 85°C degrades reliability.	–55	+25	+125	°C
V_{DD}	Supply voltage relative to V_{SS}		–0.5	–	+6.0	V
V_{IO}	DC input voltage		V_{SS} – 0.5	–	V_{DD} + 0.5	V
V_{IOZ}	DC voltage applied to tristate		V_{SS} – 0.5	–	V_{DD} + 0.5	V
I_{MIO}	Maximum current into any port pin		–25	–	+50	mA
ESD	Electrostatic discharge voltage	Human body model ESD	2000	–	–	V
LU [8]	Latch up current	In accordance with JESD78 standard	–	–	200	mA

Operating Temperature

Table 5. Operating Temperature

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{AI}	Ambient industrial temperature		–40	–	+85	°C
T_{AC}	Ambient commercial temperature		0	–	+70	°C
T_{JI}	Operational industrial die temperature [11]	The temperature rise from ambient to junction is package specific. Refer the table Thermal Impedances per Package on page 31. The user must limit the power consumption to comply with this requirement.	–40	–	+100	°C
T_{JC}	Operational commercial die temperature	The temperature rise from ambient to junction is package specific. Refer the table Thermal Impedances per Package on page 31. The user must limit the power consumption to comply with this requirement.	0	–	+85	°C

Notes

7. When V_{DD} remains in the range from 1.71 V to 1.9 V for more than 50 µsec, the slew rate when moving from the 1.71 V to 1.9 V range to greater than 2 V must be slower than 1 V/500 µsec to avoid triggering POR. The only other restriction on slew rates for any other voltage range or transition is the SRPOWER_UP parameter.
8. Errata: For Port 1 pins P1[1], P1[4], and P1[5] 300 Ohm external resistor is needed to meet this spec. Refer to "Errata" on page 35 for more details.
9. If powering down in standby sleep mode, to properly detect and recover from a V_{DD} brown out condition any of the following actions must be taken:
   - Bring the device out of sleep before powering down.
   - Assure that V_{DD} falls below 100 mV before powering back up.
   - Set the No Buzz bit in the OSC_CR0 register to keep the voltage monitoring circuit powered during sleep.
   - Increase the buzz rate to assure that the falling edge of V_{DD} is captured. The rate is configured through the PSSDC bits in the SLP_CFG register. For the referenced registers, refer to the enCoRe V Technical Reference Manual. In deep sleep mode, additional low power voltage monitoring circuitry allows V_{DD} brown out conditions to be detected for edge rates slower than 1 V/ms.

DC Electrical Characteristics

DC Chip Level Specifications

Table 6 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 6. DC Chip Level Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{DD}	Operating voltage [7, 9]	No USB activity.	3.0	–	5.5	V
$I_{DD24,3}$	Supply current, CPU = 24 MHz	Conditions are V_{DD} = 3.0 V, T_A = 25 °C, CPU = 24 MHz, No USB/I^2C/SPI.	–	2.9	4.0	mA
$I_{DD12,3}$	Supply current, CPU = 12 MHz	Conditions are V_{DD} = 3.0 V, T_A = 25 °C, CPU = 12 MHz, No USB/I^2C/SPI.	–	1.7	2.6	mA
$I_{DD6,3}$	Supply current, CPU = 6 MHz	Conditions are V_{DD} = 3.0 V, T_A = 25 °C, CPU = 6 MHz, No USB/I^2C/SPI.	–	1.2	1.8	mA
$I_{SB1,3}$	Standby current with POR, LVD, and sleep timer	V_{DD} = 3.0 V, T_A = 25 °C, I/O regulator turned off.	–	1.1	1.5	µA
$I_{SB0,3}$	Deep sleep current	V_{DD} = 3.0 V, T_A = 25 °C, I/O regulator turned off.	–	0.1	–	µA
V_{DDUSB}	Operating voltage	USB activity, USB regulator enabled	4.35	–	5.25	V
$I_{DD24,5}$	Supply current, CPU = 24 MHz	Conditions are V_{DD} = 5.0 V, T_A = 25 °C, CPU = 24 MHz, IMO = 24 MHz USB Active, No I^2C/SPI.	–	7.1	–	mA
$I_{DD12,5}$	Supply current, CPU = 12 MHz	Conditions are V_{DD} = 5.0 V, T_A = 25 °C, CPU = 12 MHz, IMO = 24 MHz USB Active, No I^2C/SPI.	–	6.2	–	mA
$I_{DD6,5}$	Supply current, CPU = 6 MHz	Conditions are V_{DD} = 5.0 V, T_A = 25 °C, CPU = 6 MHz, IMO = 24 MHz USB Active, No I^2C/SPI	–	5.8	–	mA
$I_{SB1,5}$	Standby current with POR, LVD, and sleep timer	V_{DD} = 5.0 V, T_A = 25 °C, I/O regulator turned off.	–	1.1	–	µA
$I_{SB0,5}$	Deep sleep current	V_{DD} = 5.0 V, T_A = 25 °C, I/O regulator turned off.	–	0.1	–	µA
V_{DDUSB}	Operating voltage	USB activity, USB regulator bypassed	3.15	3.3	3.60	V

Notes
10. Higher storage temperatures reduce data retention time. Recommended storage temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 85 °C degrade reliability.
11. The temperature rise from ambient to junction is package specific. See Package Handling on page 31. The user must limit the power consumption to comply with this requirement.

DC General Purpose I/O Specifications

Table 9 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and package specific temperature range. Typical parameters apply to 5 V and 3.3 V at 25 °C. These are for design guidance only.

Table 9. 3.0 V and 5.5 V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{PU}	Pull-up resistor		4	5.6	8	kΩ
V_{OH1}	High output voltage Port 2 or 3 pins	$I_{OH} \leq 10$ µA, maximum of 10 mA source current in all I/Os.	$V_{DD} - 0.2$	–	–	V
V_{OH2}	High output voltage Port 2 or 3 Pins	I_{OH} = 1 mA, maximum of 20 mA source current in all I/Os.	$V_{DD} - 0.9$	–	–	V
V_{OH3}	High output voltage Port 0 or 1 pins with LDO regulator disabled	$I_{OH} < 10$ µA, maximum of 10 mA source current in all I/Os.	$V_{DD} - 0.2$	–	–	V
V_{OH4}	High output voltage Port 0 or 1 pins with LDO regulator disabled	I_{OH} = 5 mA, maximum of 20 mA source current in all I/Os.	$V_{DD} - 0.9$	–	–	V
V_{OH5}	High output voltage Port 1 pins with LDO regulator enabled for 3 V Out	$I_{OH} < 10$ µA, $V_{DD} > 3.1$ V, maximum of 4 I/Os all sourcing 5 mA	2.85	3.00	3.3	V
V_{OH6}	High output voltage Port 1 pins with LDO regulator enabled for 3 V out	I_{OH} = 5 mA, $V_{DD} > 3.1$ V, maximum of 20 mA source current in all I/Os	2.20	–	–	V
V_{OH7}	High output voltage Port 1 pins with LDO enabled for 2.5 V out	$I_{OH} < 10$ µA, $V_{DD} > 3.0$ V, maximum of 20 mA source current in all I/Os	2.35	2.50	2.75	V
V_{OH8}	High output voltage Port 1 pins with LDO enabled for 2.5 V out	I_{OH} = 2 mA, $V_{DD} > 3.0$ V, maximum of 20 mA source current in all I/Os	1.90	–	–	V
V_{OH9}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	$I_{OH} < 10$ µA, $V_{DD} > 3.0$ V, maximum of 20 mA source current in all I/Os	1.60	1.80	2.1	V
V_{OH10}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	I_{OH} = 1 mA, $V_{DD} > 3.0$ V, maximum of 20 mA source current in all I/Os	1.20	–	–	V
V_{OL}	Low output voltage	I_{OL} = 25 mA, $V_{DD} > 3.3$ V, maximum of 60 mA sink current on even port pins (for example, P0[2] and P1[4]) and 60 mA sink current on odd port pins (for example, P0[3] and P1[5]).	–	–	0.75	V
V_{IL}	Input low voltage		–	–	0.8	V
V_{IH}	Input high voltage		2.0	–	–	V
V_H	Input hysteresis voltage		–	80	–	mV
I_{IL}	Input leakage (absolute value)		–	0.001	1	µA
C_{PIN}	Pin capacitance	Package and pin dependent. Temp = 25 °C.	0.5	1.7	5	pF

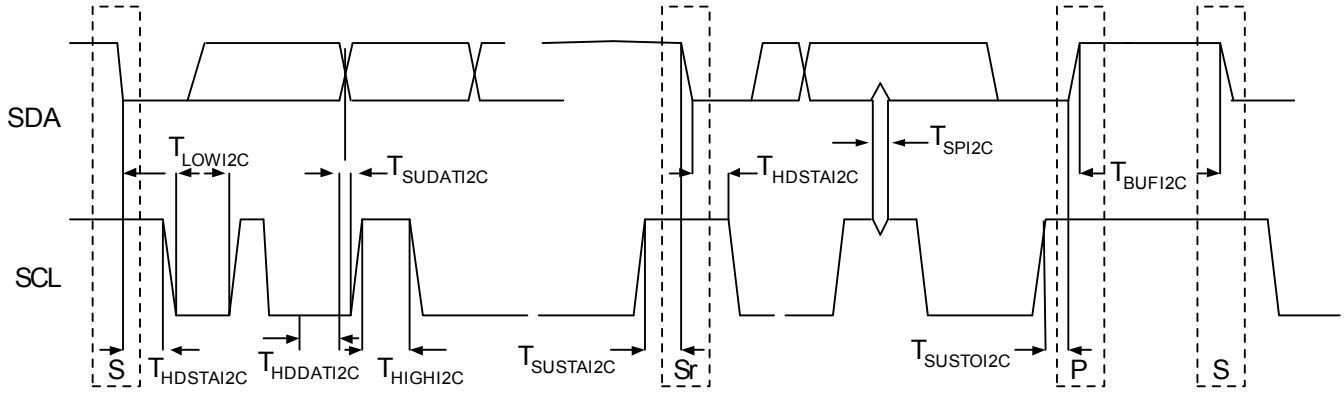
AC I²C Specifications

Table 18 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 18. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
F_{SCLI2C}	SCL clock frequency	0	100	0	400	kHz
$T_{HDSTAI2C}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4.0	–	0.6	–	µs
T_{LOWI2C}	LOW period of the SCL clock	4.7	–	1.3	–	µs
$T_{HIGHI2C}$	HIGH period of the SCL clock	4.0	–	0.6	–	µs
$T_{SUSTAI2C}$	Setup time for a repeated START condition	4.7	–	0.6	–	µs
$T_{HDDATI2C}$	Data hold time	0	–	0	–	µs
$T_{SUDATI2C}$	Data setup time	250	–	100[20]	–	ns
$T_{SUSTOI2C}$	Setup time for STOP condition	4.0	–	0.6	–	µs
T_{BUFI2C}	Bus free time between a STOP and START condition	4.7	–	1.3	–	µs
T_{SPI2C}	Pulse width of spikes are suppressed by the input filter	–	–	0	50	ns

Figure 13. Definition of Timing for Fast/Standard Mode on the I²C Bus



Note

20. A Fast mode I²C bus device can be used in a standard mode I²C bus system, but the requirement $t_{SUDAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SUDAT} = 1000 + 250 = 1250$ ns (according to the standard mode I²C bus specification) before the SCL line is released.

Table 19. SPI Master AC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{SCLK}	SCLK clock frequency		–	–	6	MHz
DC	SCLK duty cycle		–	50	–	%
T_{SETUP}	MISO to SCLK setup time		60	–	–	ns
T_{HOLD}	SCLK to MISO hold time		40	–	–	ns
T_{OUT_VAL}	SCLK to MOSI valid time		–	–	40	ns
T_{OUT_H}	SCLK to MOSI hold time		40	–	–	ns

Figure 14. SPI Master Mode 0 and 2

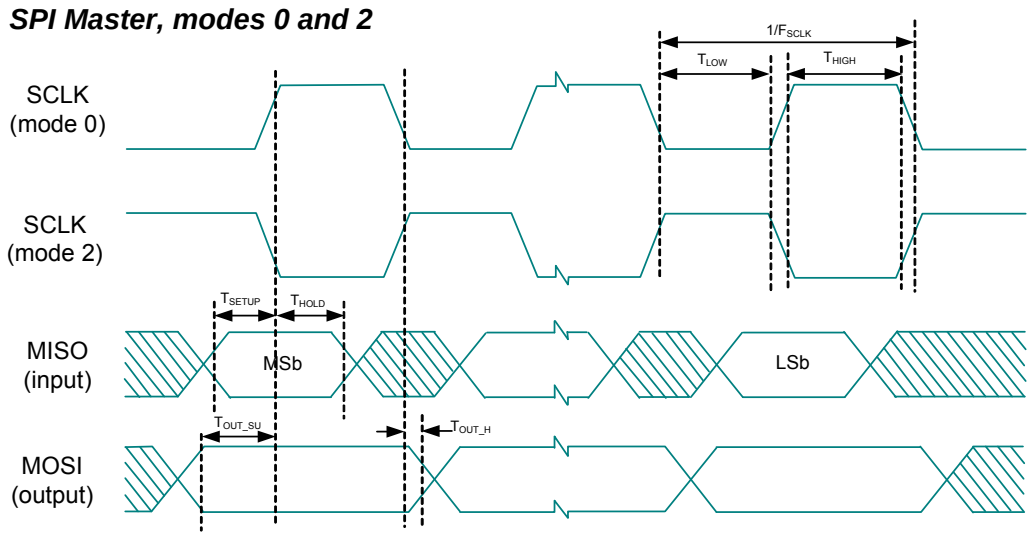


Figure 15. SPI Master Mode 1 and 3

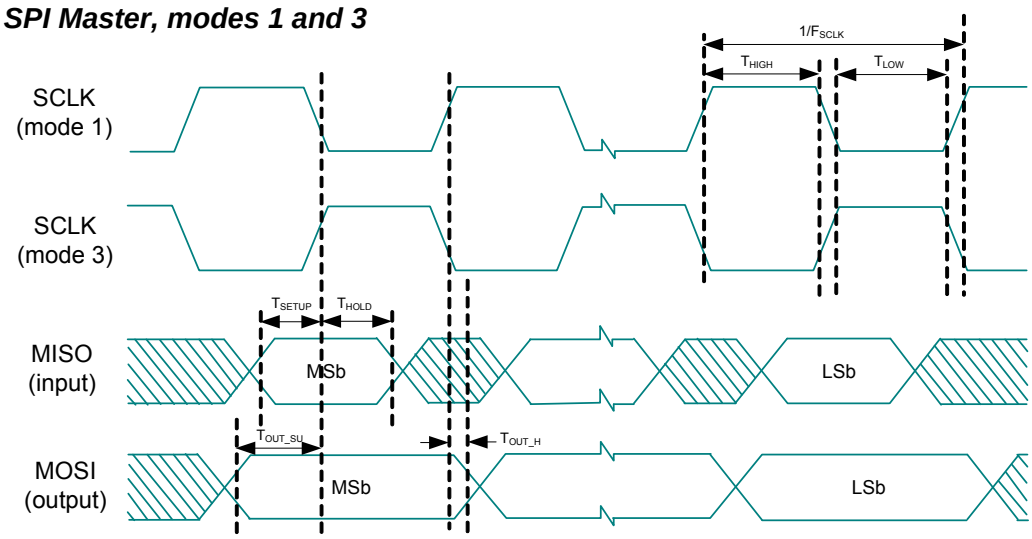
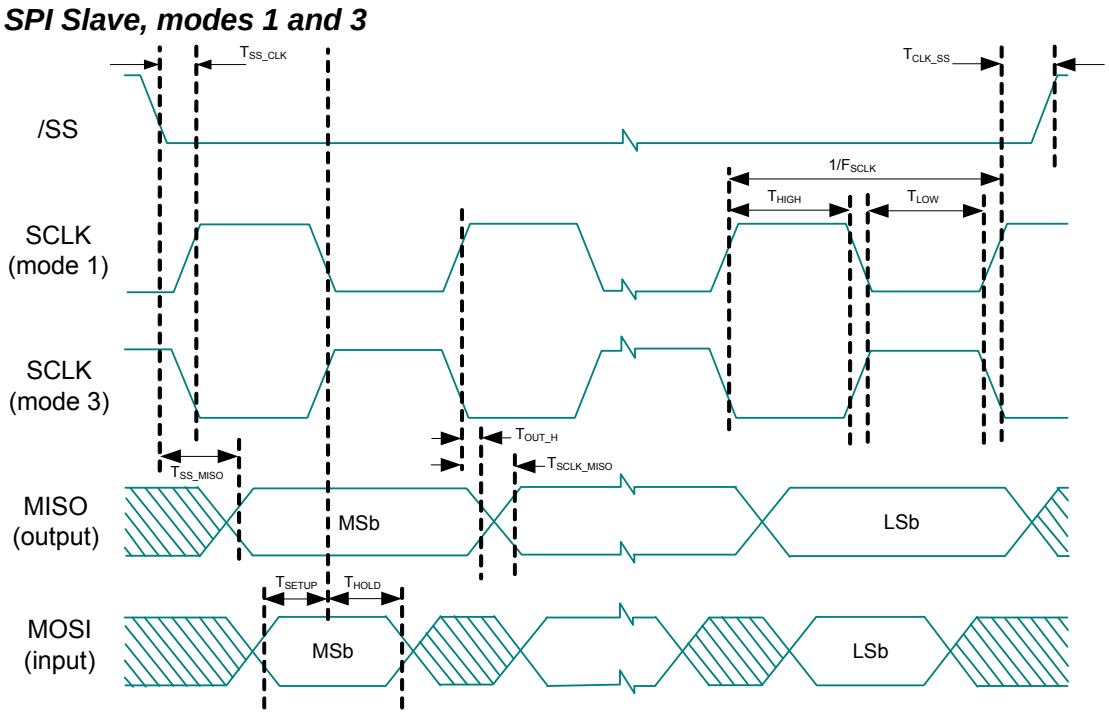


Figure 17. SPI Slave Mode 1 and 3



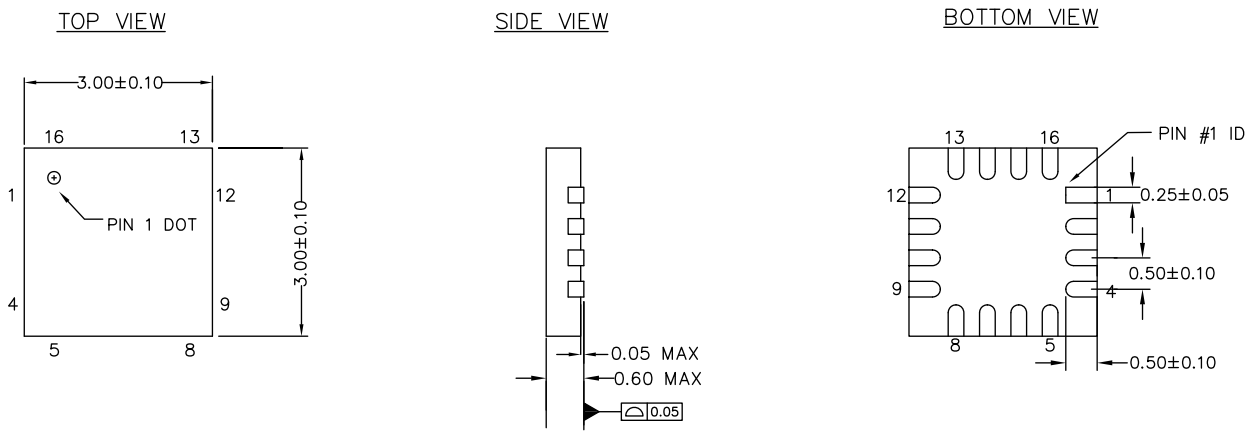
Package Diagrams

This section illustrates the packaging specifications for the enCoRe V USB device, along with the thermal impedances for each package.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the enCoRe V emulation tools and their dimensions, refer to the development kit.

Packaging Dimensions

Figure 18. 16-pin Chip On Lead (3 × 3 × 0.6 mm) LG16A/LD16A (Sawn) Package Outline, 001-09116



NOTES
1. REFERENCE JEDEC # MO−220
2. ALL DIMENSIONS ARE IN MILLIMETERS

001-09116 *J

Acronyms

Acronym	Description
API	Application Programming Interface
CPU	Central Processing Unit
GPIO	General Purpose I/O
ICE	In-Circuit Emulator
ILO	Internal Low speed Oscillator
IMO	Internal Main Oscillator
I/O	Input/Output
LSb	Least Significant Bit
LVD	Low Voltage Detect
MSb	Most Significant Bit
POR	Power On Reset
PPOR	Precision Power On Reset
PSoC	Programmable System-on-Chip
SLIMO	Slow IMO
SRAM	Static Random Access Memory

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
dB	decibel
fF	femtofarad
Hz	hertz
KB	1024 bytes
Kbit	1024 bits
kHz	kilohertz
kΩ	kilohm
MHz	megahertz
MΩ	megaohm
µA	microampere
µF	microfarad
µH	microhenry
µs	microsecond
µV	microvolt
µVrms	microvolts root-mean-square
µW	microwatt
mA	milliampere
ms	milli-second
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
W	ohm
pA	picoampere
pF	picofarad
pp	peak-to-peak
ppm	parts per million
ps	picosecond
sps	samples per second
σ	sigma: one standard deviation
V	volt

Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, ‘01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’, ‘b’, or ‘0x’ are decimal.

Errata

This section describes the errata for the enCoRe V – CY7C643xx. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability.

Contact your local Cypress Sales Representative if you have questions.

CY7C643xx Errata Summary

The following Errata item applies to the **CY7C643xx** data sheets.

1. Latch up susceptibility when maximum I/O sink current exceeded

■PROBLEM DEFINITION

P1[3], P1[6], and P1[7] pins are susceptible to latch up when the I/O sink current exceeds 25 mA per pin on these pins.

■PARAMETERS AFFECTED

LU – Latch up current. Per JESD78A, the maximum allowable latch up current per pin is 100 mA. Cypress internal specification is 200 mA latch up current limit.

■TRIGGER CONDITIONS

Latch up occurs when both the following conditions are met:

A. The offending I/O is externally connected to a voltage higher than the I/O high state, causing a current to flow into the pin that exceeds 25 mA.

B. A Port1 I/O (P1[1], P1[4], and P1[5] respectively) adjacent to the offending I/O is connected to a voltage lower than the I/O low state. This causes a signal that drops below Vss (signal undershoot) and a current greater than 200 mA to flow out of the pin.

■SCOPE OF IMPACT

The trigger conditions outlined in this item exceed the maximum ratings specified in the CY7C643xx data sheets.

■WORKAROUND

Add a series resistor > 300 Ω to P1[3], P1[6], and P1[7] pins to restrict current to within latch up limits.

■FIX STATUS

This issue will be corrected in the next new silicon revision.

2. Does not meet USB 2.0 specification for D+ and D- rise/fall matching when supply voltage is under 3.3 V

■PROBLEM DEFINITION

Rising to falling rate matching of the USB D+ and D- lines has a corner case at lower supply voltages, such as those under 3.3 V.

■PARAMETERS AFFECTED

Rising to falling rate matching of the USB data lines.

■TRIGGER CONDITION(S)

Operating the VCC supply voltage at the low end of the chip's specification (under 3.3 V) may cause a mismatch in the rising to falling rate.

■SCOPE OF IMPACT

This condition does not affect USB communications but could cause corner case issues with USB lines' rise/fall matching specification. Signal integrity tests were run using the Cypress development kit and excellent eye was observed with supply voltage of 3.15 V.

Document History Page

Document Title: CY7C6431x/CY7C6434x/CY7C6435x, enCoRe™ V Full Speed USB Controller Document Number: 001-12394				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	626256	TYJ	See ECN	New data sheet.
*A	735718	TYJ / ARI	See ECN	Filled in TBDs, added new block diagram, and corrected some values. Part numbers updated as per new specifications.
*B	1120404	ARI	See ECN	Corrected the block diagram and Figure 3, which is the 16-pin enCoRe V device. Corrected the description to pin 29 on Table 2, the Typ/Max values for I_{SB0} on the DC chip-level specifications, the current value for the latch-up current in the Electrical Characteristics section, and corrected the 16 QFN package information in the Thermal Impedance table. Corrected some of the bulleted items on the first page. Added DC Characteristics–USB Interface table. Added AC Characteristics–USB Data Timings table. Added AC Characteristics–USB Driver table. Corrected Flash Write Endurance minimum value in the DC Programming Specifications table. Corrected the Flash Erase Time max value and the Flash Block Write Time max value in the AC Programming Specifications table. Implemented new latest template. Include parameters: Vcrs, Rpu (USB, active), Rpu (USB suspend), Tfdeop, Tfeopr2, Tfeopt, Tfst. Added register map tables. Corrected a value in the DC Chip-Level Specifications table.
*C	1241024	TYJ / ARI	See ECN	Corrected Idd values in Table 6 - DC Chip-Level Specifications.
*D	1639963	AESA	See ECN	Post to www.cypress.com
*E	2138889	TYJ / PYRS	See ECN	Updated Ordering Code table: - Ordering code changed for 32-QFN package: From -32LKXC to -32LTXC - Added a new package type – “LTXC” for 48-QFN - Included Tape and Reel ordering code for 32-QFN and 48-QFN packages Changed active current values at 24, 12 and 6MHz in table “DC Chip-Level Specifications” - IDD24: 2.15 to 3.1mA - IDD12: 1.45 to 2.0mA - IDD6: 1.1 to 1.5mA Added information on using P1[0] and P1[1] as the I2C interface during POR or reset events

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Document Title: CY7C6431x/CY7C6434x/CY7C6435x, enCoRe™ V Full Speed USB Controller Document Number: 001-12394				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*F	2583853	TYJ / PYRS / HMT	10/10/08	Converted from Preliminary to Final Added operating voltage ranges with USB ADC resolution changed from 10-bit to 8-bit Rephrased battery monitoring clause in page 1 to include “with external components” Included ADC specifications table Included Voh7, Voh8, Voh9, Voh10 specs Flash data retention – condition added to Note [11] Input leakage spec changed to 25 nA max Under AC Char, Frequency accuracy of ILO corrected GPIO rise time for ports 0,1 and ports 2,3 made common AC Programming specifications updated Included AC Programming cycle timing diagram AC SPI specification updated Spec change for 32-QFN package Input Leakage Current maximum value changed to 1 μA Updated V_{OHV} parameter in Table 13 Updated thermal impedances for the packages Update Development Tools, add Designing with PSoC Designer. Edit, fix links and table format. Update TMs.
*G	2653717	DVJA / PYRS	02/04/09	Updated Features, Functional Overview, Development Tools, and Designing with PSoC Designer sections with edits. Removed ‘GUI - graphical user interface’ from Document Conventions acronym table. Removed ‘O - Only a read/write register or bits’ in Table 4 Edited Table 8: removed 10-bit resolution information and corrected units column. Added package handling section Added 8K part ‘CY7C64343-32LQXC’ to Ordering Information.
*H	2714694	DVJA / AESA	06/04/2009	Updated Block Diagram. Added Full Speed USB, 10-bit ADC, SPI, and I2C Slave sections. ADC Resolution changed from 8-bit to 10-bit Updated Table 9 DC Chip Level Specs Updated Table10 DC Char - USB Interface Updated Table 12 DC POR and LDV Specs Changed operating temperature from Commercial to Industrial Changed Temperature Range to Industrial: –40 to 85°C Figure 9: Changed minimum CPU Frequency from 750 kHz to 5.7 MHz Table 14: Removed “Maximum” from the F_{CPU} description Ordering Information: Replaced ‘C’ with ‘I’ in all part numbers to denote Industrial Temp Range
*I	2764460	DVJA / AESA	09/16/2009	Changed Table 12: ADC Specs Added F_{32K2} (Untrimmed) spec to Table 16: AC Chip level Specs Changed T_{RAMP} spec to SR_{POWER_UP} in Table 16: AC Chip Level Specs Added Table 27: Typical Package Capacitance on Crystal Pins
*J	2811903	DVJA	11/20/2009	Added USB-IF TID number in Features on page 1. Added Note 5 on page 18. Changed V_{IHP} in Table 12 on page 22.

Document History Page *(continued)*

Document Title: CY7C6431x/CY7C6434x/CY7C6435x, enCoRe™ V Full Speed USB Controller Document Number: 001-12394				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*K	2874274	KKU / PYRS	02/05/10	On page 4, changed the input voltage range from '0 V to 1.3 V' to '0 V to V_{REFADC}'. Added note for Operating Voltage in Table 6. Updated Register Map. Added SPI slave and master mode diagrams; in Table 19, changed T_{OUT_HIGH} parameter to T_{OUT_H} and modified description; in Table 20, updated T_{SS_CLK} and T_{CLK_SS} min values to $2/F_{SCLK}$ and changed description of T_{SS_MISO}. Added Vdd_{USB} parameter in Table 6. Updated package diagrams.
*L	3028310	XUT	09/13/2010	Removed HPOR bit reference from DC POR and LVD Specifications Updated Development Tools and Designing with PSoC Designer. Added Ordering Code Definitions Moved Acronyms and Document Conventions to end of document.
*M	3048308	NXZ	10/06/2010	Updated Features section as furnished in the CDT 74890 Updated datasheet as per new template All footnotes updated sequentially
*N	3557631	CSAI	03/21/2012	Updated Getting Started. Updated Package Diagrams. Updated in new template.
*O	3912957	NXZ	03/06/2013	Updated Functional Overview (Updated The enCoRe V Core (Updated contents in the section), updated Full-Speed USB (Updated contents in the section)). Updated Register Mapping Tables (Updated Table 3 (Replaced "EC0_ENBUS" with "ECO_ENBUS" and replaced "EC0_TRIM" with "ECO_TRIM")). Updated Package Diagrams: spec 001-09116 – Changed revision from *F to *H. spec 001-42168 – Changed revision from *D to *E. spec 001-13191 – Changed revision from *F to *G.
*P	3979449	ANKC	04/23/2013	Added Errata.
*Q	4074443	ANKC	07/23/2013	Added Errata footnotes (Note 8, 19). Updated Electrical Specifications: Updated Absolute Maximum Ratings: Added Note 8 and referred the same note in LU parameter. Updated AC Electrical Characteristics Updated AC Chip Level Specifications: Added Note 19 and referred the same note in TR parameter in Table 14. Updated to new template.
*R	4197134	ANKC	11/20/2013	Updated Package Diagrams: spec 001-09116 – Changed revision from *H to *I. Completing Sunset Review.