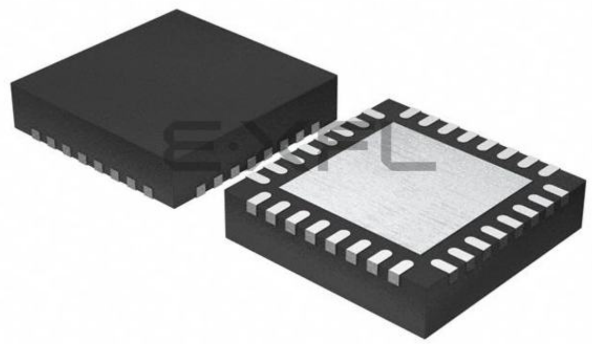

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Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	USB Microcontroller
Core Processor	M8C
Program Memory Type	FLASH (16kB)
Controller Series	CY7C643xx
RAM Size	1K x 8
Interface	I²C, SPI, USB
Number of I/O	25
Voltage - Supply	3V ~ 5.5V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy7c64345-32lqxc

Contents

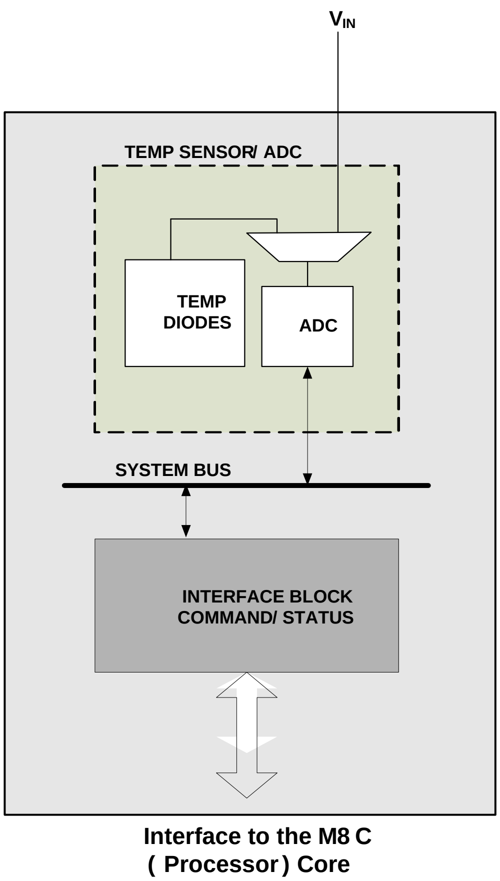
Firmware is required to handle various parts of the USB interface. The SIE issues interrupts after key USB events to direct firmware to appropriate tasks:

- Fill and empty the USB data buffers in USB SRAM.
- Enable PMA channels appropriately.
- Coordinate enumeration by decoding USB device requests.
- Suspend and resume coordination.
- Verify and select data toggle values.

10-bit ADC

The ADC on enCoRe V device is an independent block with a state machine interface to control accesses to the block. The ADC is housed together with the temperature sensor core and can be connected to this or the Analog mux bus. As a default operation, the ADC is connected to the temperature sensor diodes to give digital values of the temperature.

Figure 2. ADC System Performance Block Diagram



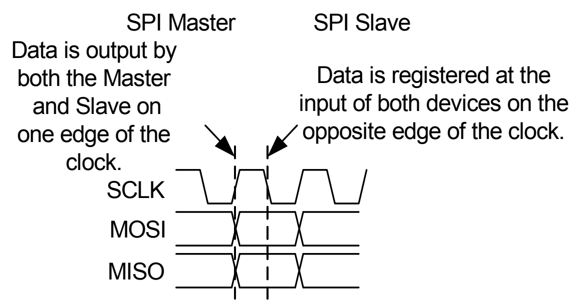
The ADC User Module contains an integrator block and one comparator with positive and negative input set by the MUXes. The input to the integrator stage comes from the analog global input mux or the temperature sensor with an input voltage range of 0 V to V_{REFADC}.

In the ADC only configuration (the ADC MUX selects the Analog mux bus, not the default temperature sensor connection), an external voltage can be connected to the input of the modulator for voltage conversion. The ADC is run for a number of cycles set by the timer, depending upon the desired resolution of the ADC. A counter counts the number of trips by the comparator, which is proportional to the input voltage. The Temp Sensor block clock speed is 36 MHz and is divided down to 1 to 12 MHz for ADC operation.

SPI

The serial peripheral interconnect (SPI) 3-wire protocol uses both edges of the clock to enable synchronous communication without the need for stringent setup and hold requirements.

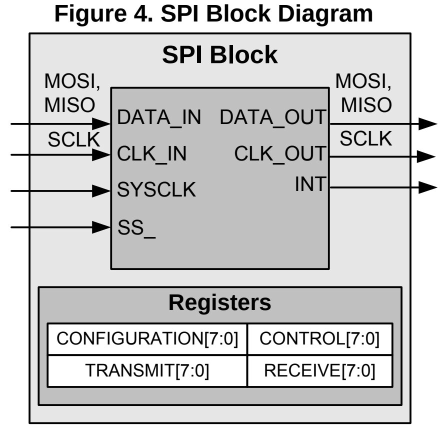
Figure 3. Basic SPI Configuration



A device can be a master or slave. A master outputs clock and data to the slave device and inputs slave data. A slave device inputs clock and data from the master device and outputs data for input to the master. Together, the master and slave are essentially a circular Shift register, where the master generates the clocking and initiates data transfers.

A basic data transfer occurs when the master sends eight bits of data, along with eight clocks. In any transfer, both master and slave transmit and receive simultaneously. If the master only sends data, the received data from the slave is ignored. If the master wishes to receive data from the slave, the master must send dummy bytes to generate the clocking for the slave to send data back.

Figure 4. SPI Block Diagram



SPI configuration register (SPI_CFG) sets master/slave functionality, clock speed, and interrupt select. SPI control register (SPI_CR) provides four control bits and four status bits for device interfacing and synchronization.

The SPIM hardware has no support for driving the Slave Select (SS_) signal. The behavior and use of this signal is dependent on the application and enCoRe V device and, if required, must be implemented in firmware.

There is an additional data input in the SPIS, Slave Select (SS_), which is an active low signal. SS_ must be asserted to enable the SPIS to receive and transmit. SS_ has two high level functions:

- To allow for the selection of a given slave in a multi-slave environment.
- To provide additional clocking for TX data queuing in SPI modes 0 and 1.

I^2C Slave

The I^2C slave enhanced communications block is a serial-to-parallel processor, designed to interface the enCoRe V device to a two-wire I^2C serial communications bus. To eliminate the need for excessive CPU intervention and overhead, the block provides I^2C-specific support for status detection and generation of framing bits. By default, the I^2C slave enhanced module is firmware compatible with the previous generation of I^2C slave functionality. However, this module provides new features that are configurable to implement significant flexibility for both internal and external interfacing. The basic I^2C features include:

- Slave, transmitter, and receiver operation.
- Byte processing for low CPU overhead.
- Interrupt or polling CPU interface.
- Support for clock rates of up to 400 kHz.
- 7- or 10-bit addressing (through firmware support).
- SMBus operation (through firmware support).

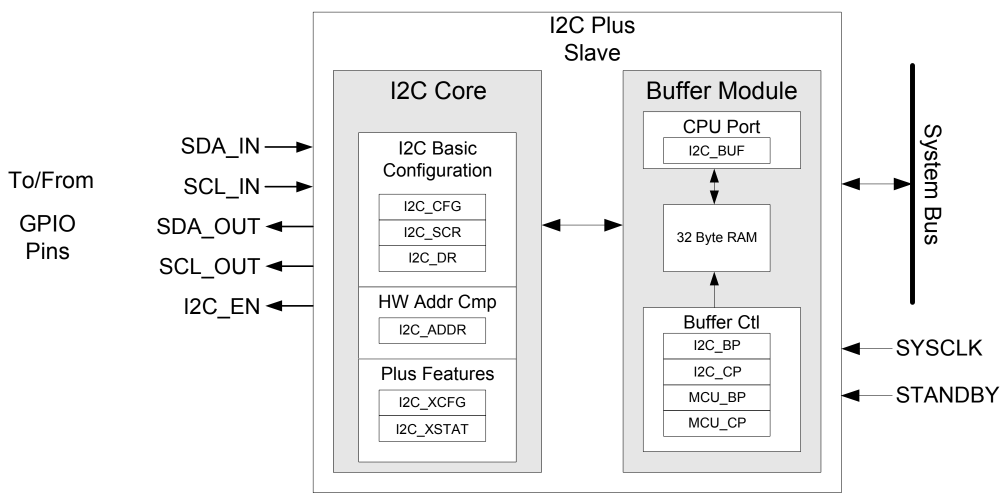
Enhanced features of the I^2C Slave Enhanced Module include:

- Support for 7-bit hardware address compare.
- Flexible data buffering schemes.
- A “no bus stalling” operating mode.
- A low power bus monitoring mode.

The I^2C block controls the data (SDA) and the clock (SCL) to the external I^2C interface through direct connections to two dedicated GPIO pins. When I^2C is enabled, these GPIO pins are not available for general purpose use. The enCoRe V CPU firmware interacts with the block through I/O register reads and writes, and firmware synchronization is implemented through polling and/or interrupts.

In the default operating mode, which is firmware compatible with previous versions of I^2C slave modules, the I^2C bus is stalled upon every received address or byte, and the CPU is required to read the data or supply data as required before the I^2C bus continues. However, this I^2C Slave Enhanced module provides new data buffering capability as an enhanced feature. In the EZI^{2}C buffering mode, the I^2C slave interface appears as a 32-byte RAM buffer to the external I^2C master. Using a simple predefined protocol, the master controls the read and write pointers into the RAM. When this method is enabled, the slave never stalls the bus. In this protocol, the data available in the RAM (this is managed by the CPU) is valid.

Figure 5. I^2C Block Diagram



Development Tools

PSoC Designer™ is the revolutionary Integrated Design Environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
  - Hardware and software I^2C slaves and masters
  - Full-speed USB 2.0
  - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are analog-to-digital converters (ADCs), digital-to-analog converters (DACs), amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this allows you to use more than 100 percent of PSoC's resources for a given application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows you to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer.

In-Circuit Emulator

A low-cost, high-functionality In-Circuit Emulator (ICE) is available for development support. This hardware can program single devices.

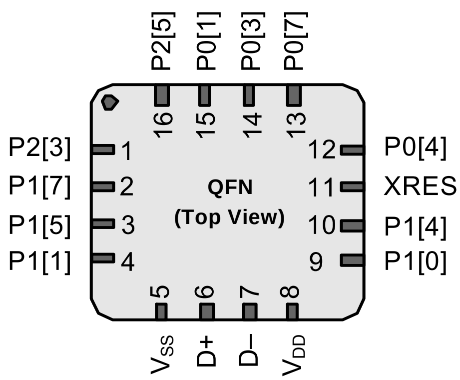
The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24-MHz) operation.

Pin Information

The enCoRe V USB device is available in a variety of packages which are listed and illustrated in the subsequent tables.

16-pin part pinout

Figure 6. CY7C64315/CY7C64316 16-pin enCoRe V USB Device



Pin Definitions

16-pin part pinout (QFN)

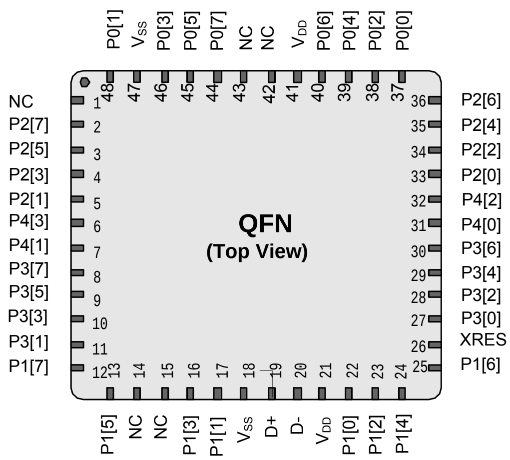
Pin No.	Type	Name	Description
1	I/O	P2[3]	Digital I/O, crystal input (Xin)
2	I/OHR	P1[7]	Digital I/O, SPI SS, I^2C SCL
3	I/OHR	P1[5]	Digital I/O, SPI MISO, I^2C SDA
4	I/OHR	P1[1][1, 2]	Digital I/O, ISSP CLK, I^2C SCL, SPI MOSI
5	Power	V_{SS}	Ground connection
6	USB line	D+	USB PHY
7	USB line	D–	USB PHY
8	Power	V_{DD}	Supply
9	I/OHR	P1[0][1, 2]	Digital I/O, ISSP DATA, I^2C SDA, SPI CLK
10	I/OHR	P1[4]	Digital I/O, optional external clock input (EXTCLK)
11	Input	XRES	Active high external reset with internal pull-down
12	I/OH	P0[4]	Digital I/O
13	I/OH	P0[7]	Digital I/O
14	I/OH	P0[3]	Digital I/O
15	I/OH	P0[1]	Digital I/O
16	I/O	P2[5]	Digital I/O, crystal output (Xout)

LEGEND I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output

Notes
1. During power up or reset event, device P1[0] and P1[1] may disturb the I^2C bus. Use alternate pins if issues are encountered.
2. These are the in-system serial programming (ISSP) pins that are not High Z at power on reset (POR).

48-pin Part Pinout

Figure 8. CY7C64355/CY7C64356 48-pin enCoRe V USB Device



Pin Definitions

48-pin Part Pinout (QFN)

Pin No.	Type	Pin Name	Description
1	NC	NC	No connection
2	I/O	P2[7]	Digital I/O
3	I/O	P2[5]	Digital I/O, crystal out (Xout)
4	I/O	P2[3]	Digital I/O, crystal in (Xin)
5	I/O	P2[1]	Digital I/O
6	I/O	P4[3]	Digital I/O
7	I/O	P4[1]	Digital I/O
8	I/O	P3[7]	Digital I/O
9	I/O	P3[5]	Digital I/O
10	I/O	P3[3]	Digital I/O
11	I/O	P3[1]	Digital I/O
12	I/OHR	P1[7]	Digital I/O, I^2C SCL, SPI SS
13	I/OHR	P1[5]	Digital I/O, I^2C SDA, SPI MISO
14	NC	NC	No connection
15	NC	NC	No connection
16	I/OHR	P1[3]	Digital I/O, SPI CLK
17	I/OHR	P1[1][5, 6]	Digital I/O, ISSP CLK, I^2C SCL, SPI MOSI
18	Power	V_{SS}	Supply ground
19	I/O	D+	USB
20	I/O	D–	USB
21	Power	V_{DD}	Supply voltage
22	I/OHR	P1[0][5, 6]	Digital I/O, ISSP DATA, I^2C SDA, SPI CLK
23	I/OHR	P1[2]	Digital I/O

Notes

5. During power up or reset event, device P1[0] and P1[1] may disturb the I^2C bus. Use alternate pins if issues are encountered.
6. These are the in-system serial programming (ISSP) pins that are not High Z at power on reset (POR).

Register Reference

The section discusses the registers of the enCoRe V device. It lists all the registers in mapping tables, in address order.

Register Conventions

The register conventions specific to this section are listed in the following table.

Table 1. Register Conventions

Convention	Description
R	Read register or bits
W	Write register or bits
L	Logical register or bits
C	Clearable register or bits
#	Access is bit specific

Register Mapping Tables

The enCoRe V device has a total register address space of 512 bytes. The register space is also referred to as I/O space and is broken into two parts: Bank 0 (user space) and Bank 1 (configuration space). The XIO bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XIO bit is set, the user is said to be in the “extended” address space or the “configuration” registers.

Table 2. Register Map Bank 0 Table: User Space

Name	Addr (0, Hex)	Access	Name	Addr (0, Hex)	Access	Name	Addr (0, Hex)	Access	Name	Addr (0, Hex)	Access
PRT0DR	00	RW	EP1_CNT0	40	#		80			C0	
PRT0IE	01	RW	EP1_CNT1	41	RW		81			C1	
	02		EP2_CNT0	42	#		82			C2	
	03		EP2_CNT1	43	RW		83			C3	
PRT1DR	04	RW	EP3_CNT0	44	#		84			C4	
PRT1IE	05	RW	EP3_CNT1	45	RW		85			C5	
	06		EP4_CNT0	46	#		86			C6	
	07		EP4_CNT1	47	RW		87			C7	
PRT2DR	08	RW	EP5_CNT0	48	#		88		I2C_XCFG	C8	RW
PRT2IE	09	RW	EP5_CNT1	49	RW		89		I2C_XSTAT	C9	R
	0A		EP6_CNT0	4A	#		8A		I2C_ADDR	CA	RW
	0B		EP6_CNT1	4B	RW		8B		I2C_BP	CB	R
PRT3DR	0C	RW	EP7_CNT0	4C	#		8C		I2C_CP	CC	R
PRT3IE	0D	RW	EP7_CNT1	4D	RW		8D		CPU_BP	CD	RW
	0E		EP8_CNT0	4E	#		8E		CPU_CP	CE	R
	0F		EP8_CNT1	4F	RW		8F		I2C_BUF	CF	RW
PRT4DR	10	RW		50			90		CUR_PP	D0	RW
PRT4IE	11	RW		51			91		STK_PP	D1	RW
	12			52			92			D2	
	13			53			93		IDX_PP	D3	RW
	14			54			94		MVR_PP	D4	RW
	15			55			95		MVW_PP	D5	RW
	16			56			96		I2C_CFG	D6	RW
	17			57			97		I2C_SCR	D7	#
	18		PMA0_DR	58	RW		98		I2C_DR	D8	RW
	19		PMA1_DR	59	RW		99			D9	
	1A		PMA2_DR	5A	RW		9A		INT_CLR0	DA	RW
	1B		PMA3_DR	5B	RW		9B		INT_CLR1	DB	RW
	1C		PMA4_DR	5C	RW		9C		INT_CLR2	DC	RW
	1D		PMA5_DR	5D	RW		9D			DD	
	1E		PMA6_DR	5E	RW		9E		INT_MSK2	DE	RW
	1F		PMA7_DR	5F	RW		9F		INT_MSK1	DF	RW
	20			60			A0		INT_MSK0	E0	RW
	21			61			A1		INT_SW_EN	E1	RW
	22			62			A2		INT_VC	E2	RC
	23			63			A3		RES_WDT	E3	W
	24		PMA8_DR	64	RW		A4			E4	
	25		PMA9_DR	65	RW		A5			E5	
	26		PMA10_DR	66	RW		A6			E6	
	27		PMA11_DR	67	RW		A7			E7	
	28		PMA12_DR	68	RW		A8			E8	
SPI_TXR	29	W	PMA13_DR	69	RW		A9			E9	
SPI_RXR	2A	R	PMA14_DR	6A	RW		AA			EA	
SPI_CR	2B	#	PMA15_DR	6B	RW		AB			EB	
	2C		TMP_DR0	6C	RW		AC			EC	
	2D		TMP_DR1	6D	RW		AD			ED	
	2E		TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
	30			70		PT0_CFG	B0	RW		F0	
USB_SOF0	31	R		71		PT0_DATA1	B1	RW		F1	
USB_SOF1	32	R		72		PT0_DATA0	B2	RW		F2	
USB_CR0	33	RW		73		PT1_CFG	B3	RW		F3	
USBIO_CR0	34	#		74		PT1_DATA1	B4	RW		F4	
USBIO_CR1	35	#		75		PT1_DATA0	B5	RW		F5	
EP0_CR	36	#		76		PT2_CFG	B6	RW		F6	
EP0_CNT0	37	#		77		PT2_DATA1	B7	RW	CPU_F	F7	RL
EP0_DR0	38	RW		78		PT2_DATA0	B8	RW		F8	
EP0_DR1	39	RW		79			B9			F9	
EP0_DR2	3A	RW		7A			BA			FA	
EP0_DR3	3B	RW		7B			BB			FB	
EP0_DR4	3C	RW		7C			BC			FC	
EP0_DR5	3D	RW		7D			BD			FD	
EP0_DR6	3E	RW		7E			BE		CPU_SCR1	FE	#
EP0_DR7	3F	RW		7F			BF		CPU_SCR0	FF	#

Gray fields are reserved; do not access these fields. # Access is bit specific.

DC Electrical Characteristics

DC Chip Level Specifications

Table 6 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 6. DC Chip Level Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{DD}	Operating voltage [7, 9]	No USB activity.	3.0	–	5.5	V
$I_{DD24,3}$	Supply current, CPU = 24 MHz	Conditions are V_{DD} = 3.0 V, T_A = 25 °C, CPU = 24 MHz, No USB/I^2C/SPI.	–	2.9	4.0	mA
$I_{DD12,3}$	Supply current, CPU = 12 MHz	Conditions are V_{DD} = 3.0 V, T_A = 25 °C, CPU = 12 MHz, No USB/I^2C/SPI.	–	1.7	2.6	mA
$I_{DD6,3}$	Supply current, CPU = 6 MHz	Conditions are V_{DD} = 3.0 V, T_A = 25 °C, CPU = 6 MHz, No USB/I^2C/SPI.	–	1.2	1.8	mA
$I_{SB1,3}$	Standby current with POR, LVD, and sleep timer	V_{DD} = 3.0 V, T_A = 25 °C, I/O regulator turned off.	–	1.1	1.5	µA
$I_{SB0,3}$	Deep sleep current	V_{DD} = 3.0 V, T_A = 25 °C, I/O regulator turned off.	–	0.1	–	µA
V_{DDUSB}	Operating voltage	USB activity, USB regulator enabled	4.35	–	5.25	V
$I_{DD24,5}$	Supply current, CPU = 24 MHz	Conditions are V_{DD} = 5.0 V, T_A = 25 °C, CPU = 24 MHz, IMO = 24 MHz USB Active, No I^2C/SPI.	–	7.1	–	mA
$I_{DD12,5}$	Supply current, CPU = 12 MHz	Conditions are V_{DD} = 5.0 V, T_A = 25 °C, CPU = 12 MHz, IMO = 24 MHz USB Active, No I^2C/SPI.	–	6.2	–	mA
$I_{DD6,5}$	Supply current, CPU = 6 MHz	Conditions are V_{DD} = 5.0 V, T_A = 25 °C, CPU = 6 MHz, IMO = 24 MHz USB Active, No I^2C/SPI	–	5.8	–	mA
$I_{SB1,5}$	Standby current with POR, LVD, and sleep timer	V_{DD} = 5.0 V, T_A = 25 °C, I/O regulator turned off.	–	1.1	–	µA
$I_{SB0,5}$	Deep sleep current	V_{DD} = 5.0 V, T_A = 25 °C, I/O regulator turned off.	–	0.1	–	µA
V_{DDUSB}	Operating voltage	USB activity, USB regulator bypassed	3.15	3.3	3.60	V

Notes
10. Higher storage temperatures reduce data retention time. Recommended storage temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 85 °C degrade reliability.
11. The temperature rise from ambient to junction is package specific. See Package Handling on page 31. The user must limit the power consumption to comply with this requirement.

Table 7. DC Characteristics – USB Interface

Symbol	Description	Conditions	Min	Typ	Max	Units
Rusbi	USB D+ pull-up resistance	With idle bus	0.900	–	1.575	kΩ
Rusba	USB D+ pull-up resistance	While receiving traffic	1.425	–	3.090	kΩ
Vohusb	Static output high		2.8	–	3.6	V
Volusb	Static output low		–	–	0.3	V
Vdi	Differential input sensitivity		0.2	–	–	V
Vcm	Differential input common mode range		0.8	–	2.5	V
Vse	Single-ended receiver threshold		0.8	–	2.0	V
Cin	Transceiver capacitance			–	50	pF
Iio	High Z state data Line Leakage	On D+ or D– line	–10	–	+10	μA
Rps2	PS/2 Pull Up Resistance		3	5	7	kΩ
Rext	External USB Series Resistor	In series with each USB pin	21.78	22.0	22.22	Ω

ADC Electrical Specifications

Table 8. ADC User Module Electrical Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
Input						
V_{IN}	Input voltage range		0	–	VREFADC	V
C_{IIN}	Input capacitance		–	–	5	pF
R_{IN}	Input resistance	Equivalent switched cap input resistance for 8-, 9-, or 10-bit resolution	1/(500fF* Data Clock)	1/(400fF* Data Clock)	1/(300fF* Data Clock)	Ω
Reference						
V_{REFADC}	ADC reference voltage		1.14	–	1.26	V
Conversion Rate						
F_{CLK}	Data clock	Source is chip's internal main oscillator. See AC Chip-Level Specifications for accuracy	2.25	–	6	MHz
S8	8-bit sample rate	Data Clock set to 6 MHz. Sample Rate = 0.001/ (2^Resolution/Data Clock)	–	23.4375	–	ksps
S10	10-bit sample rate	Data Clock set to 6 MHz. Sample Rate = 0.001/ (2^Resolution/Data Clock)	–	5.859	–	ksps
DC Accuracy						
RES	Resolution	Can be set to 8-, 9-, or 10-bit	8	–	10	bits
DNL	Differential nonlinearity		–1	–	+2	LSB
INL	Integral nonlinearity		–2	–	+2	LSB
E_{Offset}	Offset error	8-bit resolution	0	3.2	19.2	LSB
		10-bit resolution	0	12.8	76.8	LSB
E_{gain}	Gain error	For any resolution	–5	–	+5	%FSR
Power						
I_{ADC}	Operating current		–	2.1	2.6	mA
PSRR	Power supply rejection ratio	PSRR (V_{DD} > 3.0 V)	–	24	–	dB
		PSRR (V_{DD} < 3.0 V)	–	30	–	dB

DC General Purpose I/O Specifications

Table 9 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and package specific temperature range. Typical parameters apply to 5 V and 3.3 V at 25 °C. These are for design guidance only.

Table 9. 3.0 V and 5.5 V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{PU}	Pull-up resistor		4	5.6	8	kΩ
V_{OH1}	High output voltage Port 2 or 3 pins	$I_{OH} \leq 10$ µA, maximum of 10 mA source current in all I/Os.	$V_{DD} - 0.2$	–	–	V
V_{OH2}	High output voltage Port 2 or 3 Pins	I_{OH} = 1 mA, maximum of 20 mA source current in all I/Os.	$V_{DD} - 0.9$	–	–	V
V_{OH3}	High output voltage Port 0 or 1 pins with LDO regulator disabled	I_{OH} < 10 µA, maximum of 10 mA source current in all I/Os.	$V_{DD} - 0.2$	–	–	V
V_{OH4}	High output voltage Port 0 or 1 pins with LDO regulator disabled	I_{OH} = 5 mA, maximum of 20 mA source current in all I/Os.	$V_{DD} - 0.9$	–	–	V
V_{OH5}	High output voltage Port 1 pins with LDO regulator enabled for 3 V Out	I_{OH} < 10 µA, V_{DD} > 3.1 V, maximum of 4 I/Os all sourcing 5 mA	2.85	3.00	3.3	V
V_{OH6}	High output voltage Port 1 pins with LDO regulator enabled for 3 V out	I_{OH} = 5 mA, V_{DD} > 3.1 V, maximum of 20 mA source current in all I/Os	2.20	–	–	V
V_{OH7}	High output voltage Port 1 pins with LDO enabled for 2.5 V out	I_{OH} < 10 µA, V_{DD} > 3.0 V, maximum of 20 mA source current in all I/Os	2.35	2.50	2.75	V
V_{OH8}	High output voltage Port 1 pins with LDO enabled for 2.5 V out	I_{OH} = 2 mA, V_{DD} > 3.0 V, maximum of 20 mA source current in all I/Os	1.90	–	–	V
V_{OH9}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	I_{OH} < 10 µA, V_{DD} > 3.0 V, maximum of 20 mA source current in all I/Os	1.60	1.80	2.1	V
V_{OH10}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	I_{OH} = 1 mA, V_{DD} > 3.0 V, maximum of 20 mA source current in all I/Os	1.20	–	–	V
V_{OL}	Low output voltage	I_{OL} = 25 mA, V_{DD} > 3.3 V, maximum of 60 mA sink current on even port pins (for example, P0[2] and P1[4]) and 60 mA sink current on odd port pins (for example, P0[3] and P1[5]).	–	–	0.75	V
V_{IL}	Input low voltage		–	–	0.8	V
V_{IH}	Input high voltage		2.0	–	–	V
V_H	Input hysteresis voltage		–	80	–	mV
I_{IL}	Input leakage (absolute value)		–	0.001	1	µA
C_{PIN}	Pin capacitance	Package and pin dependent. Temp = 25 °C.	0.5	1.7	5	pF

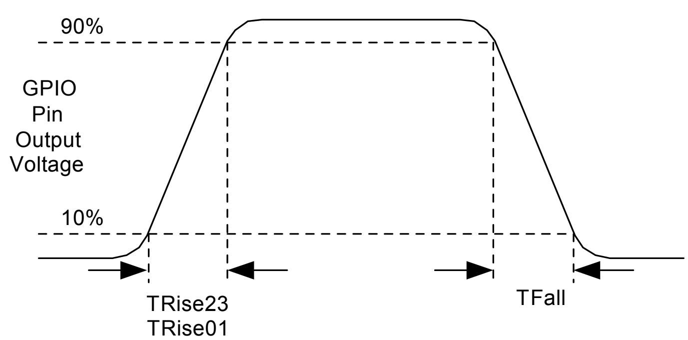
AC General Purpose I/O Specifications

Table 15 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 15. AC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{GPIO}	GPIO operating frequency	Normal strong mode, Ports 0, 1	–	–	12	MHz
TRise23	Rise time, strong mode Ports 2, 3	V_{DD} = 3.0 to 3.6 V, 10% - 90%	15	–	80	ns
TRise01	Rise time, strong mode Ports 0, 1	V_{DD} = 3.0 to 3.6 V, 10% - 90%	10	–	50	ns
TFall	Fall time, strong mode All Ports	V_{DD} = 3.0 to 3.6 V, 10% - 90%	10	–	50	ns

Figure 11. GPIO Timing Diagram



AC External Clock Specifications

Table 16 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 16. AC External Clock Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{OSCEXT}	Frequency		0.750	–	25.2	MHz
–	High period		20.6	–	5300	ns
–	Low period		20.6	–	–	ns
–	Power-up IMO to switch		150	–	–	µs

Table 19. SPI Master AC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{SCLK}	SCLK clock frequency		–	–	6	MHz
DC	SCLK duty cycle		–	50	–	%
T_{SETUP}	MISO to SCLK setup time		60	–	–	ns
T_{HOLD}	SCLK to MISO hold time		40	–	–	ns
T_{OUT_VAL}	SCLK to MOSI valid time		–	–	40	ns
T_{OUT_H}	SCLK to MOSI hold time		40	–	–	ns

Figure 14. SPI Master Mode 0 and 2

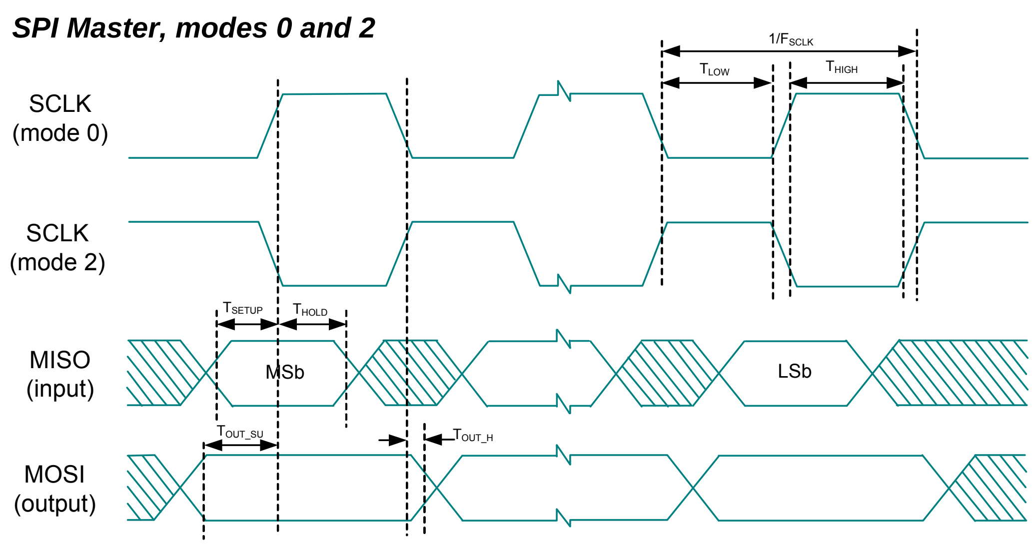


Figure 15. SPI Master Mode 1 and 3

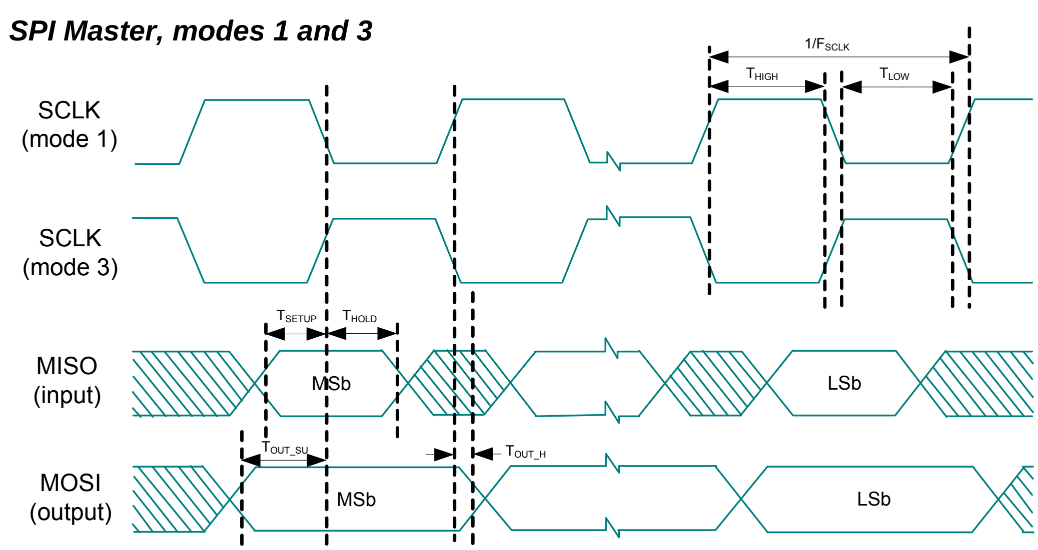


Table 20. SPI Slave AC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{SCLK}	SCLK clock frequency		0.0469	–	12	MHz
T_{LOW}	SCLK low time		41.67	–	–	ns
T_{HIGH}	SCLK high time		41.67	–	–	ns
T_{SETUP}	MOSI to SCLK setup time		30	–	–	ns
T_{HOLD}	SCLK to MOSI hold time		50	–	–	ns
T_{SS_MISO}	SS low to MISO valid		–	–	153	ns
T_{SCLK_MISO}	SCLK to MISO valid		–	–	125	ns
T_{SS_HIGH}	SS high time		50	–	–	ns
T_{SS_CLK}	Time from SS low to first SCLK		$2/F_{SCLK}$	–	–	ns
T_{CLK_SS}	Time from last SCLK to SS high		$2/F_{SCLK}$	–	–	ns

Figure 16. SPI Slave Mode 0 and 2

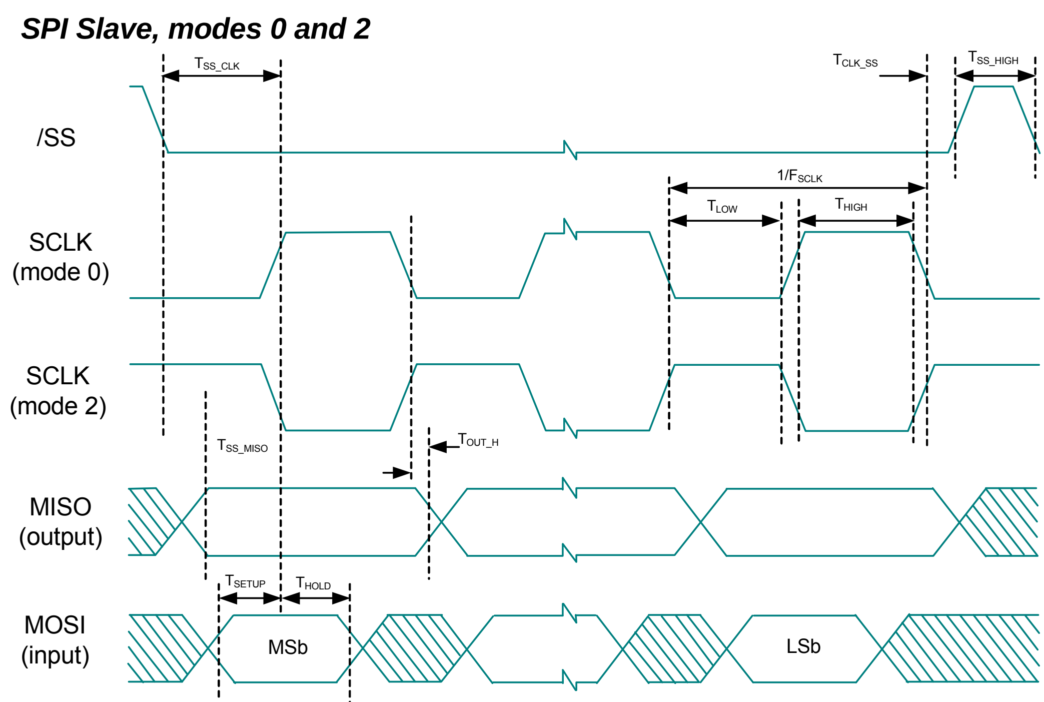
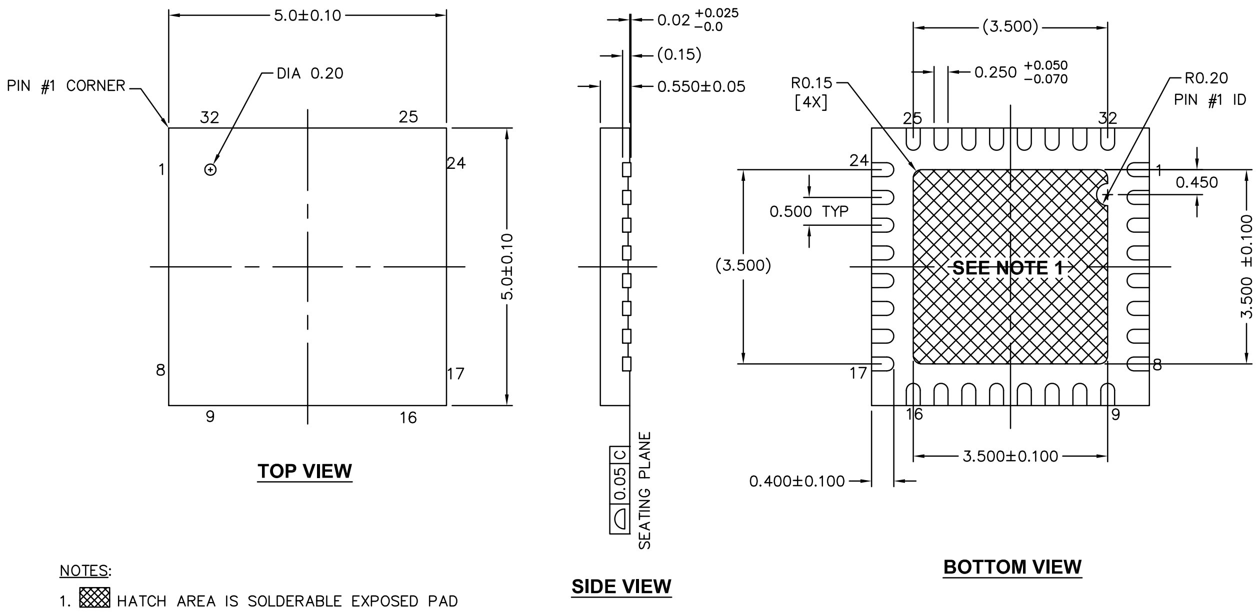


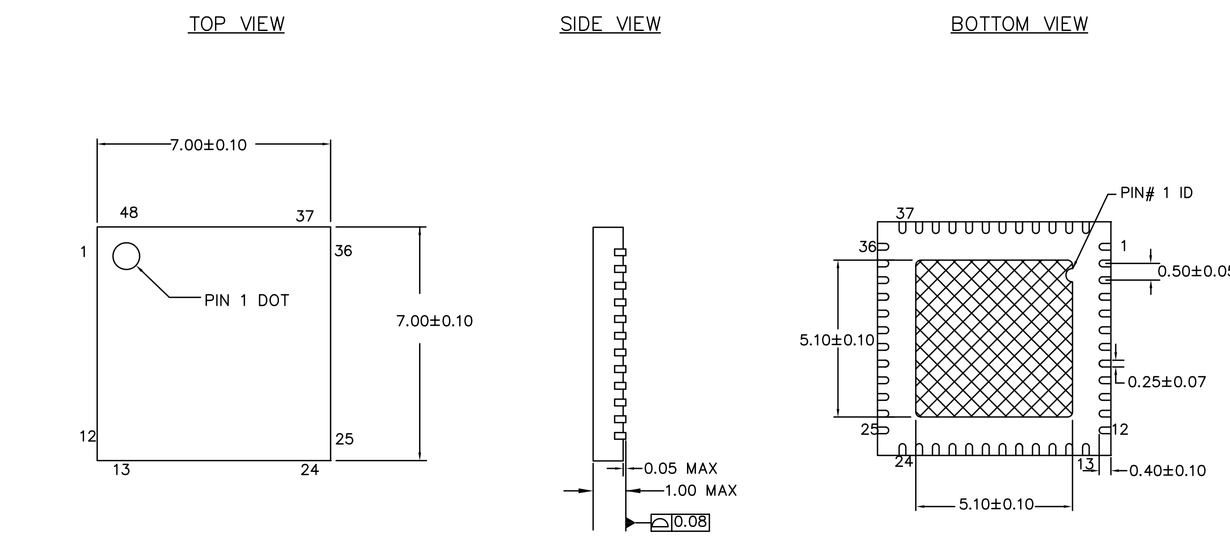
Figure 19. 32-pin QFN (5 × 5 × 0.55 mm) LQ32 3.5 × 3.5 E-Pad (Sawn) Package Outline, 001-42168



NOTES:
1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO–248
3. PACKAGE WEIGHT: 0.0388g
4. DIMENSIONS ARE IN MILLIMETERS

001-42168 *E

Figure 20. 48-pin QFN (7 × 7 × 1.00 mm) LT48A 5.1 × 5.1 E-Pad (Sawn) Package Outline, 001-13191



NOTES:
1. HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO–220
3. PACKAGE WEIGHT: 13 ± 1 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13191 *H

Ordering Information

Table 25. Ordering Code - Commercial Parts

Ordering Code	Package Information	Flash (KB)	SRAM (KB)	No. of GPIOs	Target Applications
CY7C64315-16LKXC	16-pin QFN (3 × 3 mm)	16	1	11	Mid-tier Full-Speed USB dongle, Remote Control Host Module, Various
CY7C64315-16LKXCT	16-pin QFN (Tape and Reel), (3 × 3 mm)	16	1	11	Mid-tier Full-Speed USB dongle, Remote Control Host Module, Various
CY7C64316-16LKXC	16-pin QFN (3 × 3 mm)	32	2	11	Feature-rich Full-Speed USB dongle, Remote Control Host Module, Various
CY7C64316-16LKXCT	16-pin QFN (Tape and Reel), (3 × 3 mm)	32	2	11	Feature-rich Full-Speed USB dongle, Remote Control Host Module, Various
CY7C64343-32LQXC	32-pin QFN (5 × 5 mm)	8	1	25	Full-Speed USB mouse, Various
CY7C64343-32LQXCT	32-pin QFN (Tape and Reel), (5 × 5 mm)	8	1	25	Full-Speed USB mouse, Various
CY7C64345-32LQXC	32-pin QFN (5 × 5 mm)	16	1	25	Full-Speed USB mouse, Various
CY7C64345-32LQXCT	32-pin QFN (Tape and Reel), (5 × 5 mm)	16	1	25	Full-Speed USB mouse, Various
CY7C64346-32LQXCT	32-pin QFN (Tape and Reel), (5 × 5 mm)	32	1	25	Full-Speed USB keyboard, Various
CY7C64355-48LTXC	48-pin QFN (7 × 7 mm)	16	1	36	Full-Speed USB keyboard, Various
CY7C64355-48LTXCT	48-pin QFN (Tape and Reel), (7 × 7 mm)	16	1	36	Full-Speed USB keyboard, Various
CY7C64356-48LTXC	48-pin QFN (7 × 7 mm)	32	2	36	Feature-rich Full-Speed USB keyboard, Various
CY7C64356-48LTXCT	48-pin QFN (Tape and Reel), (7 × 7 mm)	32	2	36	Feature-rich Full-Speed USB keyboard, Various

Table 26. Ordering Code - Industrial Parts

Ordering Code	Package Information	Flash (KB)	SRAM (KB)	No. of GPIOs	Target Applications
CY7C64315-16LKXI	16-pin QFN, Industrial (3 × 3 mm)	16	1	11	Mid-tier Full-Speed USB dongle, Remote Control Host Module, Various
CY7C64315-16LKXIT	16-pin QFN, Industrial (Tape and Reel), (3 × 3 mm)	16	1	11	Mid-tier Full-Speed USB dongle, Remote Control Host Module, Various

Errata

This section describes the errata for the enCoRe V – CY7C643xx. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability.

Contact your local Cypress Sales Representative if you have questions.

CY7C643xx Errata Summary

The following Errata item applies to the **CY7C643xx** data sheets.

1. Latch up susceptibility when maximum I/O sink current exceeded

- **PROBLEM DEFINITION**

  P1[3], P1[6], and P1[7] pins are susceptible to latch up when the I/O sink current exceeds 25 mA per pin on these pins.

- **PARAMETERS AFFECTED**

  LU – Latch up current. Per JESD78A, the maximum allowable latch up current per pin is 100 mA. Cypress internal specification is 200 mA latch up current limit.

- **TRIGGER CONDITIONS**

  Latch up occurs when both the following conditions are met:

  A. The offending I/O is externally connected to a voltage higher than the I/O high state, causing a current to flow into the pin that exceeds 25 mA.

  B. A Port1 I/O (P1[1], P1[4], and P1[5] respectively) adjacent to the offending I/O is connected to a voltage lower than the I/O low state. This causes a signal that drops below Vss (signal undershoot) and a current greater than 200 mA to flow out of the pin.

- **SCOPE OF IMPACT**

  The trigger conditions outlined in this item exceed the maximum ratings specified in the CY7C643xx data sheets.

- **WORKAROUND**

  Add a series resistor > 300 Ω to P1[3], P1[6], and P1[7] pins to restrict current to within latch up limits.

- **FIX STATUS**

  This issue will be corrected in the next new silicon revision.

2. Does not meet USB 2.0 specification for D+ and D- rise/fall matching when supply voltage is under 3.3 V

- **PROBLEM DEFINITION**

  Rising to falling rate matching of the USB D+ and D- lines has a corner case at lower supply voltages, such as those under 3.3 V.

- **PARAMETERS AFFECTED**

  Rising to falling rate matching of the USB data lines.

- **TRIGGER CONDITION(S)**

  Operating the VCC supply voltage at the low end of the chip's specification (under 3.3 V) may cause a mismatch in the rising to falling rate.

- **SCOPE OF IMPACT**

  This condition does not affect USB communications but could cause corner case issues with USB lines' rise/fall matching specification. Signal integrity tests were run using the Cypress development kit and excellent eye was observed with supply voltage of 3.15 V.

Document History Page

Document Title: CY7C6431x/CY7C6434x/CY7C6435x, enCoRe™ V Full Speed USB Controller Document Number: 001-12394				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	626256	TYJ	See ECN	New data sheet.
*A	735718	TYJ / ARI	See ECN	Filled in TBDs, added new block diagram, and corrected some values. Part numbers updated as per new specifications.
*B	1120404	ARI	See ECN	Corrected the block diagram and Figure 3, which is the 16-pin enCoRe V device. Corrected the description to pin 29 on Table 2, the Typ/Max values for I_{SB0} on the DC chip-level specifications, the current value for the latch-up current in the Electrical Characteristics section, and corrected the 16 QFN package information in the Thermal Impedance table. Corrected some of the bulleted items on the first page. Added DC Characteristics–USB Interface table. Added AC Characteristics–USB Data Timings table. Added AC Characteristics–USB Driver table. Corrected Flash Write Endurance minimum value in the DC Programming Specifications table. Corrected the Flash Erase Time max value and the Flash Block Write Time max value in the AC Programming Specifications table. Implemented new latest template. Include parameters: Vcrs, Rpu (USB, active), Rpu (USB suspend), Tfdeop, Tfeopr2, Tfeopt, Tfst. Added register map tables. Corrected a value in the DC Chip-Level Specifications table.
*C	1241024	TYJ / ARI	See ECN	Corrected Idd values in Table 6 - DC Chip-Level Specifications.
*D	1639963	AESA	See ECN	Post to www.cypress.com
*E	2138889	TYJ / PYRS	See ECN	Updated Ordering Code table: - Ordering code changed for 32-QFN package: From -32LKXC to -32LTXC - Added a new package type – “LTXC” for 48-QFN - Included Tape and Reel ordering code for 32-QFN and 48-QFN packages Changed active current values at 24, 12 and 6MHz in table “DC Chip-Level Specifications” - IDD24: 2.15 to 3.1mA - IDD12: 1.45 to 2.0mA - IDD6: 1.1 to 1.5mA Added information on using P1[0] and P1[1] as the I2C interface during POR or reset events

Document History Page *(continued)*

Document Title: CY7C6431x/CY7C6434x/CY7C6435x, enCoRe™ V Full Speed USB Controller Document Number: 001-12394				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*F	2583853	TYJ / PYRS / HMT	10/10/08	Converted from Preliminary to Final Added operating voltage ranges with USB ADC resolution changed from 10-bit to 8-bit Rephrased battery monitoring clause in page 1 to include “with external components” Included ADC specifications table Included Voh7, Voh8, Voh9, Voh10 specs Flash data retention – condition added to Note [11] Input leakage spec changed to 25 nA max Under AC Char, Frequency accuracy of ILO corrected GPIO rise time for ports 0,1 and ports 2,3 made common AC Programming specifications updated Included AC Programming cycle timing diagram AC SPI specification updated Spec change for 32-QFN package Input Leakage Current maximum value changed to 1 μA Updated V_{OHV} parameter in Table 13 Updated thermal impedances for the packages Update Development Tools, add Designing with PSoC Designer. Edit, fix links and table format. Update TMs.
*G	2653717	DVJA / PYRS	02/04/09	Updated Features, Functional Overview, Development Tools, and Designing with PSoC Designer sections with edits. Removed ‘GUI - graphical user interface’ from Document Conventions acronym table. Removed ‘O - Only a read/write register or bits’ in Table 4 Edited Table 8: removed 10-bit resolution information and corrected units column. Added package handling section Added 8K part ‘CY7C64343-32LQXC’ to Ordering Information.
*H	2714694	DVJA / AESA	06/04/2009	Updated Block Diagram. Added Full Speed USB, 10-bit ADC, SPI, and I2C Slave sections. ADC Resolution changed from 8-bit to 10-bit Updated Table 9 DC Chip Level Specs Updated Table10 DC Char - USB Interface Updated Table 12 DC POR and LDV Specs Changed operating temperature from Commercial to Industrial Changed Temperature Range to Industrial: –40 to 85°C Figure 9: Changed minimum CPU Frequency from 750 kHz to 5.7 MHz Table 14: Removed “Maximum” from the F_{CPU} description Ordering Information: Replaced ‘C’ with ‘I’ in all part numbers to denote Industrial Temp Range
*I	2764460	DVJA / AESA	09/16/2009	Changed Table 12: ADC Specs Added F_{32K2} (Untrimmed) spec to Table 16: AC Chip level Specs Changed T_{RAMP} spec to SR_{POWER_UP} in Table 16: AC Chip Level Specs Added Table 27: Typical Package Capacitance on Crystal Pins
*J	2811903	DVJA	11/20/2009	Added USB-IF TID number in Features on page 1. Added Note 5 on page 18. Changed V_{IHP} in Table 12 on page 22.

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