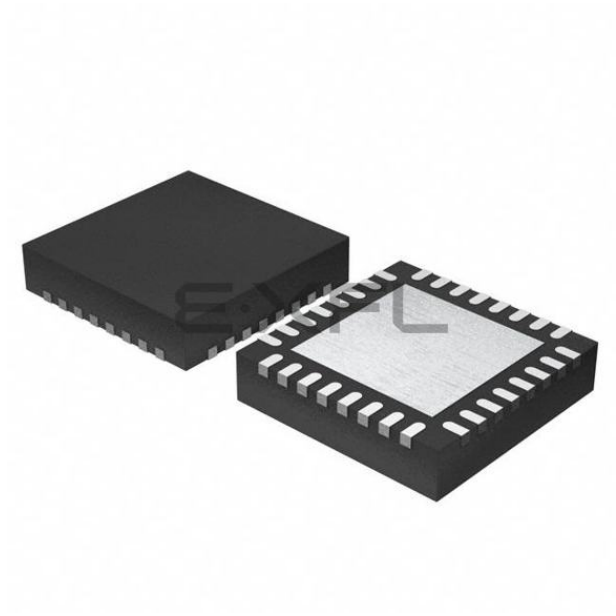

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Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	-
Core Processor	-
Program Memory Type	-
Controller Series	-
RAM Size	-
Interface	USB
Number of I/O	-
Voltage - Supply	3V ~ 5.5V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy7c64346-32lqxct

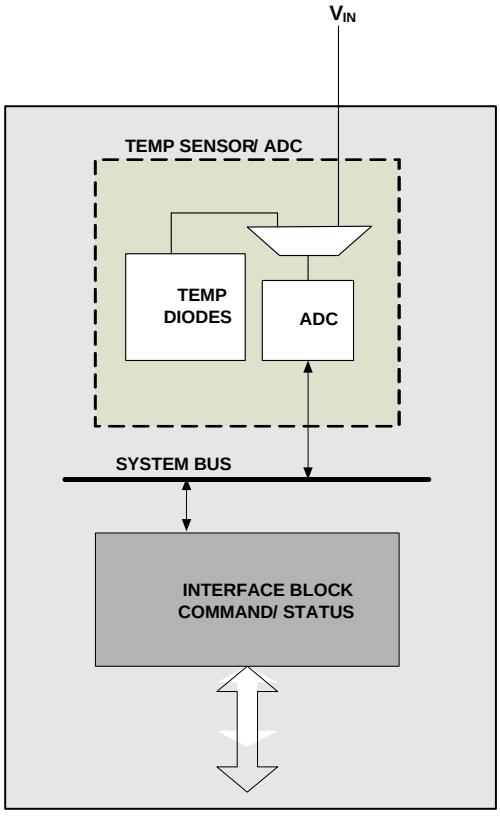
Firmware is required to handle various parts of the USB interface. The SIE issues interrupts after key USB events to direct firmware to appropriate tasks:

- Fill and empty the USB data buffers in USB SRAM.
- Enable PMA channels appropriately.
- Coordinate enumeration by decoding USB device requests.
- Suspend and resume coordination.
- Verify and select data toggle values.

10-bit ADC

The ADC on enCoRe V device is an independent block with a state machine interface to control accesses to the block. The ADC is housed together with the temperature sensor core and can be connected to this or the Analog mux bus. As a default operation, the ADC is connected to the temperature sensor diodes to give digital values of the temperature.

Figure 2. ADC System Performance Block Diagram



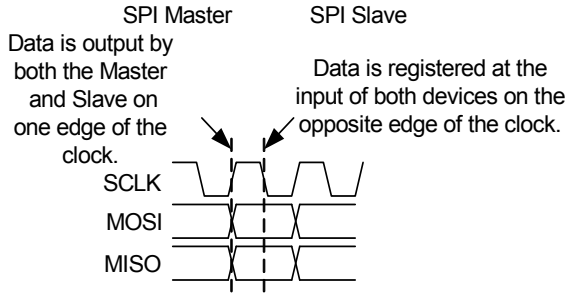
The ADC User Module contains an integrator block and one comparator with positive and negative input set by the MUXes. The input to the integrator stage comes from the analog global input mux or the temperature sensor with an input voltage range of 0 V to V_{REFADC}.

In the ADC only configuration (the ADC MUX selects the Analog mux bus, not the default temperature sensor connection), an external voltage can be connected to the input of the modulator for voltage conversion. The ADC is run for a number of cycles set by the timer, depending upon the desired resolution of the ADC. A counter counts the number of trips by the comparator, which is proportional to the input voltage. The Temp Sensor block clock speed is 36 MHz and is divided down to 1 to 12 MHz for ADC operation.

SPI

The serial peripheral interconnect (SPI) 3-wire protocol uses both edges of the clock to enable synchronous communication without the need for stringent setup and hold requirements.

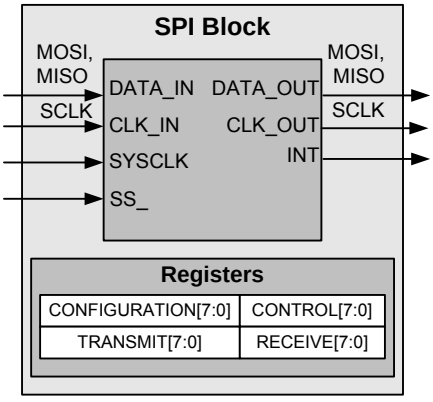
Figure 3. Basic SPI Configuration



A device can be a master or slave. A master outputs clock and data to the slave device and inputs slave data. A slave device inputs clock and data from the master device and outputs data for input to the master. Together, the master and slave are essentially a circular Shift register, where the master generates the clocking and initiates data transfers.

A basic data transfer occurs when the master sends eight bits of data, along with eight clocks. In any transfer, both master and slave transmit and receive simultaneously. If the master only sends data, the received data from the slave is ignored. If the master wishes to receive data from the slave, the master must send dummy bytes to generate the clocking for the slave to send data back.

Figure 4. SPI Block Diagram



Additional System Resources

System resources, some of which have been previously listed, provide additional capability useful to complete systems. Additional resources include low voltage detection and power on reset. The following statements describe the merits of each system resource.

- Low voltage detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR (power on reset) circuit eliminates the need for a system supervisor.
- The 5 V maximum input, 1.8, 2.5, or 3 V selectable output, LDO regulator provides regulation for I/Os. A register controlled bypass mode enables the user to disable the LDO.
- Standard Cypress PSoC IDE tools are available for debugging the enCoRe V family of parts.

Getting Started

The quickest path to understanding the enCoRe V silicon is by reading this data sheet and using the PSoC Designer Integrated Development Environment (IDE). This datasheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications. For in-depth information, along with detailed programming information, see the *enCoRe™ V CY7C643xx, enCoRe™ V LV CY7C604xx Technical Reference Manual (TRM)* for this PSoC device.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device data sheets on the web at http://www.cypress.com.

Application Notes

Application notes are an excellent introduction to the wide variety of possible PSoC designs and are available at http://www.cypress.com.

Development Kits

PSoC development kits are available online from Cypress at http://www.cypress.com and through a growing number of regional and global distributors, including Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops) is available online at http://www.cypress.com. The training covers a wide variety of topics and skill levels to assist you in your designs.

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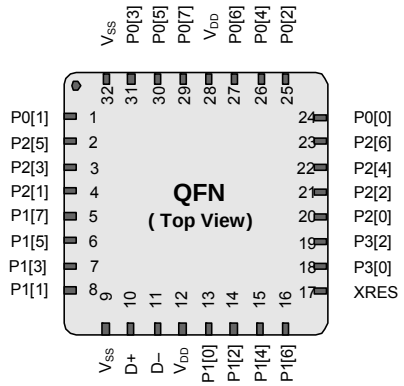
For assistance with technical issues, search KnowledgeBase articles and forums at http://www.cypress.com. If you cannot find an answer to your question, call technical support at 1-800-541-4736.

32-pin part pinout

Figure 7. CY7C64343/CY7C64345/CY7C64346 32-pin enCoRe V USB Device



Pin Definitions

32-pin part pinout (QFN)

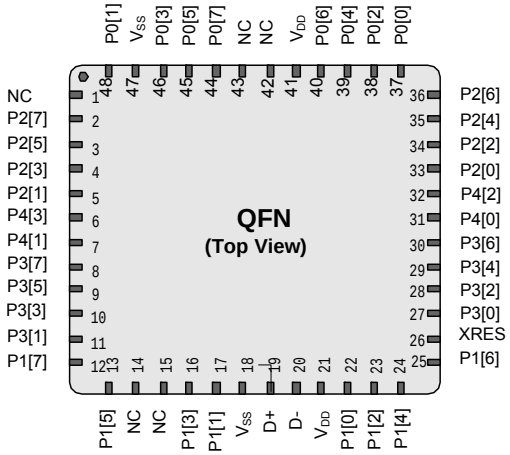
Pin No.	Type	Name	Description
1	I/OH	P0[1]	Digital I/O
2	I/O	P2[5]	Digital I/O, crystal output (Xout)
3	I/O	P2[3]	Digital I/O, crystal Input (Xin)
4	I/O	P2[1]	Digital I/O
5	I/OHR	P1[7]	Digital I/O, I^2C SCL, SPI SS
6	I/OHR	P1[5]	Digital I/O, I^2C SDA, SPI MISO
7	I/OHR	P1[3]	Digital I/O, SPI CLK
8	I/OHR	P1[1][3, 4]	Digital I/O, ISSP CLK, I^2C SCL, SPI MOSI
9	Power	V_{SS}	Ground
10	I/O	D+	USB PHY
11	I/O	D–	USB PHY
12	Power	V_{DD}	Supply voltage
13	I/OHR	P1[0][3, 4]	Digital I/O, ISSP DATA, I^2C SDA, SPI CLK
14	I/OHR	P1[2]	Digital I/O
15	I/OHR	P1[4]	Digital I/O, optional external clock input (EXTCLK)
16	I/OHR	P1[6]	Digital I/O
17	Reset	XRES	Active high external reset with internal pull down
18	I/O	P3[0]	Digital I/O
19	I/O	P3[2]	Digital I/O
20	I/O	P2[0]	Digital I/O
21	I/O	P2[2]	Digital I/O
22	I/O	P2[4]	Digital I/O
23	I/O	P2[6]	Digital I/O
24	I/OH	P0[0]	Digital I/O
25	I/OH	P0[2]	Digital I/O
26	I/OH	P0[4]	Digital I/O
27	I/OH	P0[6]	Digital I/O
28	Power	V_{DD}	Supply voltage
29	I/OH	P0[7]	Digital I/O
30	I/OH	P0[5]	Digital I/O
31	I/OH	P0[3]	Digital I/O
32	Power	V_{SS}	Ground
CP	Power	V_{SS}	Ensure the center pad is connected to ground

LEGEND I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output

Notes
3. During power up or reset event, device P1[0] and P1[1] may disturb the I^2C bus. Use alternate pins if issues are encountered.
4. These are the in-system serial programming (ISSP) pins that are not High Z at power on reset (POR).

48-pin Part Pinout

Figure 8. CY7C64355/CY7C64356 48-pin enCoRe V USB Device



Pin Definitions

48-pin Part Pinout (QFN)

Pin No.	Type	Pin Name	Description
1	NC	NC	No connection
2	I/O	P2[7]	Digital I/O
3	I/O	P2[5]	Digital I/O, crystal out (Xout)
4	I/O	P2[3]	Digital I/O, crystal in (Xin)
5	I/O	P2[1]	Digital I/O
6	I/O	P4[3]	Digital I/O
7	I/O	P4[1]	Digital I/O
8	I/O	P3[7]	Digital I/O
9	I/O	P3[5]	Digital I/O
10	I/O	P3[3]	Digital I/O
11	I/O	P3[1]	Digital I/O
12	I/OHR	P1[7]	Digital I/O, I^2C SCL, SPI SS
13	I/OHR	P1[5]	Digital I/O, I^2C SDA, SPI MISO
14	NC	NC	No connection
15	NC	NC	No connection
16	I/OHR	P1[3]	Digital I/O, SPI CLK
17	I/OHR	P1[1][5, 6]	Digital I/O, ISSP CLK, I^2C SCL, SPI MOSI
18	Power	V_{SS}	Supply ground
19	I/O	D+	USB
20	I/O	D–	USB
21	Power	V_{DD}	Supply voltage
22	I/OHR	P1[0][5, 6]	Digital I/O, ISSP DATA, I^2C SDA, SPI CLK
23	I/OHR	P1[2]	Digital I/O

Notes
5. During power up or reset event, device P1[0] and P1[1] may disturb the I^2C bus. Use alternate pins if issues are encountered.
6. These are the in-system serial programming (ISSP) pins that are not High Z at power on reset (POR).

Pin Definitions

48-pin Part Pinout (QFN)

Pin No.	Type	Pin Name	Description
24	I/OHR	P1[4]	Digital I/O, optional external clock input (EXTCLK)
25	I/OHR	P1[6]	Digital I/O
26	XRES	Ext Reset	Active high external reset with internal pull down
27	I/O	P3[0]	Digital I/O
28	I/O	P3[2]	Digital I/O
29	I/O	P3[4]	Digital I/O
30	I/O	P3[6]	Digital I/O
31	I/O	P4[0]	Digital I/O
32	I/O	P4[2]	Digital I/O
33	I/O	P2[0]	Digital I/O
34	I/O	P2[2]	Digital I/O
35	I/O	P2[4]	Digital I/O
36	I/O	P2[6]	Digital I/O
37	I/OH	P0[0]	Digital I/O
38	I/OH	P0[2]	Digital I/O
39	I/OH	P0[4]	Digital I/O
40	I/OH	P0[6]	Digital I/O
41	Power	V_{DD}	Supply voltage
42	NC	NC	No connection
43	NC	NC	No connection
44	I/OH	P0[7]	Digital I/O
45	I/OH	P0[5]	Digital I/O
46	I/OH	P0[3]	Digital I/O
47	Power	V_{SS}	Supply ground
48	I/OH	P0[1]	Digital I/O
CP	Power	V_{SS}	Ensure the center pad is connected to ground

LEGEND I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output

Register Reference

The section discusses the registers of the enCoRe V device. It lists all the registers in mapping tables, in address order.

Register Conventions

The register conventions specific to this section are listed in the following table.

Table 1. Register Conventions

Convention	Description
R	Read register or bits
W	Write register or bits
L	Logical register or bits
C	Clearable register or bits
#	Access is bit specific

Register Mapping Tables

The enCoRe V device has a total register address space of 512 bytes. The register space is also referred to as I/O space and is broken into two parts: Bank 0 (user space) and Bank 1 (configuration space). The XIO bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XIO bit is set, the user is said to be in the “extended” address space or the “configuration” registers.

Table 3. Register Map Bank 1 Table: Configuration Space

Name	Addr (1, Hex)	Access	Name	Addr (1, Hex)	Access	Name	Addr (1, Hex)	Access	Name	Addr (1, Hex)	Access
PRT0DM0	00	RW	PMA4_RA	40	RW		80			C0	
PRT0DM1	01	RW	PMA5_RA	41	RW		81			C1	
	02		PMA6_RA	42	RW		82			C2	
	03		PMA7_RA	43	RW		83			C3	
PRT1DM0	04	RW	PMA8_WA	44	RW		84			C4	
PRT1DM1	05	RW	PMA9_WA	45	RW		85			C5	
	06		PMA10_WA	46	RW		86			C6	
	07		PMA11_WA	47	RW		87			C7	
PRT2DM0	08	RW	PMA12_WA	48	RW		88			C8	
PRT2DM1	09	RW	PMA13_WA	49	RW		89			C9	
	0A		PMA14_WA	4A	RW		8A			CA	
	0B		PMA15_WA	4B	RW		8B			CB	
PRT3DM0	0C	RW	PMA8_RA	4C	RW		8C			CC	
PRT3DM1	0D	RW	PMA9_RA	4D	RW		8D			CD	
	0E		PMA10_RA	4E	RW		8E			CE	
	0F		PMA11_RA	4F	RW		8F			CF	
PRT4DM0	10	RW	PMA12_RA	50	RW		90			D0	
PRT4DM1	11	RW	PMA13_RA	51	RW		91			D1	
	12		PMA14_RA	52	RW		92		ECO_ENBUS	D2	RW
	13		PMA15_RA	53	RW		93		ECO_TRIM	D3	RW
	14		EP1_CR0	54	#		94			D4	
	15		EP2_CR0	55	#		95			D5	
	16		EP3_CR0	56	#		96			D6	
	17		EP4_CR0	57	#		97			D7	
	18		EP5_CR0	58	#		98		MUX_CR0	D8	RW
	19		EP6_CRO	59	#		99		MUX_CR1	D9	RW
	1A		EP7_CR0	5A	#		9A		MUX_CR2	DA	RW
	1B		EP8_CR0	5B	#		9B		MUX_CR3	DB	RW
	1C			5C			9C		IO_CFG1	DC	RW
	1D			5D			9D		OUT_P1	DD	RW
	1E			5E			9E		IO_CFG2	DE	RW
	1F			5F			9F		MUX_CR4	DF	RW
	20			60			A0		OSC_CR0	E0	RW
	21			61			A1		ECO_CFG	E1	#
	22			62			A2		OSC_CR2	E2	RW
	23			63			A3		VLT_CR	E3	RW
	24			64			A4		VLT_CMP	E4	R
	25			65			A5			E5	
	26			66			A6			E6	
	27			67			A7			E7	
	28			68			A8		IMO_TR	E8	W
SPI_CFG	29	RW		69			A9		ILO_TR	E9	W
	2A			6A			AA			EA	
	2B			6B			AB		SLP_CFG	EB	RW
	2C		TMP_DR0	6C	RW		AC		SLP_CFG2	EC	RW
	2D		TMP_DR1	6D	RW		AD		SLP_CFG3	ED	RW
	2E		TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
USB_CR1	30	#		70			B0			F0	
	31			71			B1			F1	
	32			72			B2			F2	
	33			73			B3			F3	
PMA0_WA	34	RW		74			B4			F4	
PMA1_WA	35	RW		75			B5			F5	
PMA2_WA	36	RW		76			B6			F6	
PMA3_WA	37	RW		77			B7		CPU_F	F7	RL
PMA4_WA	38	RW		78			B8			F8	
PMA5_WA	39	RW		79			B9			F9	
PMA6_WA	3A	RW		7A			BA		IMO_TR1	FA	RW
PMA7_WA	3B	RW		7B			BB			FB	
PMA0_RA	3C	RW		7C			BC			FC	
PMA1_RA	3D	RW		7D		USB_MISC_CR	BD	RW		FD	
PMA2_RA	3E	RW		7E			BE			FE	
PMA3_RA	3F	RW		7F			BF			FF	

Gray fields are reserved; do not access these fields. # Access is bit specific.

Electrical Specifications

This section presents the DC and AC electrical specifications of the enCoRe V USB devices. For the most up-to-date electrical specifications, verify that you have the most recent data sheet available by visiting the company web site at http://www.cypress.com

Figure 9. Voltage versus CPU Frequency

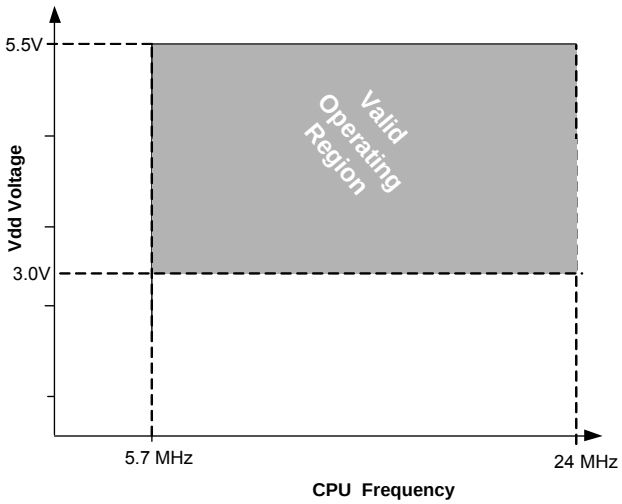
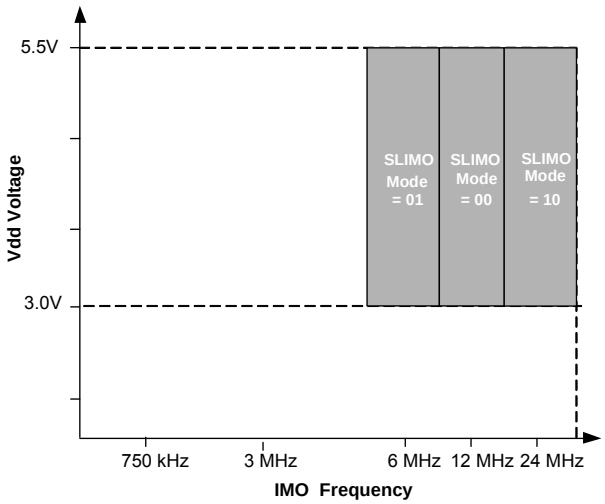


Figure 10. IMO Frequency Trim Options



DC Electrical Characteristics

DC Chip Level Specifications

Table 6 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 6. DC Chip Level Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{DD}	Operating voltage [7, 9]	No USB activity.	3.0	–	5.5	V
$I_{DD24,3}$	Supply current, CPU = 24 MHz	Conditions are V_{DD} = 3.0 V, T_A = 25 °C, CPU = 24 MHz, No USB/I^2C/SPI.	–	2.9	4.0	mA
$I_{DD12,3}$	Supply current, CPU = 12 MHz	Conditions are V_{DD} = 3.0 V, T_A = 25 °C, CPU = 12 MHz, No USB/I^2C/SPI.	–	1.7	2.6	mA
$I_{DD6,3}$	Supply current, CPU = 6 MHz	Conditions are V_{DD} = 3.0 V, T_A = 25 °C, CPU = 6 MHz, No USB/I^2C/SPI.	–	1.2	1.8	mA
$I_{SB1,3}$	Standby current with POR, LVD, and sleep timer	V_{DD} = 3.0 V, T_A = 25 °C, I/O regulator turned off.	–	1.1	1.5	µA
$I_{SB0,3}$	Deep sleep current	V_{DD} = 3.0 V, T_A = 25 °C, I/O regulator turned off.	–	0.1	–	µA
V_{DDUSB}	Operating voltage	USB activity, USB regulator enabled	4.35	–	5.25	V
$I_{DD24,5}$	Supply current, CPU = 24 MHz	Conditions are V_{DD} = 5.0 V, T_A = 25 °C, CPU = 24 MHz, IMO = 24 MHz USB Active, No I^2C/SPI.	–	7.1	–	mA
$I_{DD12,5}$	Supply current, CPU = 12 MHz	Conditions are V_{DD} = 5.0 V, T_A = 25 °C, CPU = 12 MHz, IMO = 24 MHz USB Active, No I^2C/SPI.	–	6.2	–	mA
$I_{DD6,5}$	Supply current, CPU = 6 MHz	Conditions are V_{DD} = 5.0 V, T_A = 25 °C, CPU = 6 MHz, IMO = 24 MHz USB Active, No I^2C/SPI	–	5.8	–	mA
$I_{SB1,5}$	Standby current with POR, LVD, and sleep timer	V_{DD} = 5.0 V, T_A = 25 °C, I/O regulator turned off.	–	1.1	–	µA
$I_{SB0,5}$	Deep sleep current	V_{DD} = 5.0 V, T_A = 25 °C, I/O regulator turned off.	–	0.1	–	µA
V_{DDUSB}	Operating voltage	USB activity, USB regulator bypassed	3.15	3.3	3.60	V

Notes
10. Higher storage temperatures reduce data retention time. Recommended storage temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 85 °C degrade reliability.
11. The temperature rise from ambient to junction is package specific. See Package Handling on page 31. The user must limit the power consumption to comply with this requirement.

DC General Purpose I/O Specifications

Table 9 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and package specific temperature range. Typical parameters apply to 5 V and 3.3 V at 25 °C. These are for design guidance only.

Table 9. 3.0 V and 5.5 V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{PU}	Pull-up resistor		4	5.6	8	kΩ
V_{OH1}	High output voltage Port 2 or 3 pins	$I_{OH} \leq 10$ µA, maximum of 10 mA source current in all I/Os.	$V_{DD} - 0.2$	–	–	V
V_{OH2}	High output voltage Port 2 or 3 Pins	I_{OH} = 1 mA, maximum of 20 mA source current in all I/Os.	$V_{DD} - 0.9$	–	–	V
V_{OH3}	High output voltage Port 0 or 1 pins with LDO regulator disabled	$I_{OH} < 10$ µA, maximum of 10 mA source current in all I/Os.	$V_{DD} - 0.2$	–	–	V
V_{OH4}	High output voltage Port 0 or 1 pins with LDO regulator disabled	I_{OH} = 5 mA, maximum of 20 mA source current in all I/Os.	$V_{DD} - 0.9$	–	–	V
V_{OH5}	High output voltage Port 1 pins with LDO regulator enabled for 3 V Out	$I_{OH} < 10$ µA, $V_{DD} > 3.1$ V, maximum of 4 I/Os all sourcing 5 mA	2.85	3.00	3.3	V
V_{OH6}	High output voltage Port 1 pins with LDO regulator enabled for 3 V out	I_{OH} = 5 mA, $V_{DD} > 3.1$ V, maximum of 20 mA source current in all I/Os	2.20	–	–	V
V_{OH7}	High output voltage Port 1 pins with LDO enabled for 2.5 V out	$I_{OH} < 10$ µA, $V_{DD} > 3.0$ V, maximum of 20 mA source current in all I/Os	2.35	2.50	2.75	V
V_{OH8}	High output voltage Port 1 pins with LDO enabled for 2.5 V out	I_{OH} = 2 mA, $V_{DD} > 3.0$ V, maximum of 20 mA source current in all I/Os	1.90	–	–	V
V_{OH9}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	$I_{OH} < 10$ µA, $V_{DD} > 3.0$ V, maximum of 20 mA source current in all I/Os	1.60	1.80	2.1	V
V_{OH10}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	I_{OH} = 1 mA, $V_{DD} > 3.0$ V, maximum of 20 mA source current in all I/Os	1.20	–	–	V
V_{OL}	Low output voltage	I_{OL} = 25 mA, $V_{DD} > 3.3$ V, maximum of 60 mA sink current on even port pins (for example, P0[2] and P1[4]) and 60 mA sink current on odd port pins (for example, P0[3] and P1[5]).	–	–	0.75	V
V_{IL}	Input low voltage		–	–	0.8	V
V_{IH}	Input high voltage		2.0	–	–	V
V_H	Input hysteresis voltage		–	80	–	mV
I_{IL}	Input leakage (absolute value)		–	0.001	1	µA
C_{PIN}	Pin capacitance	Package and pin dependent. Temp = 25 °C.	0.5	1.7	5	pF

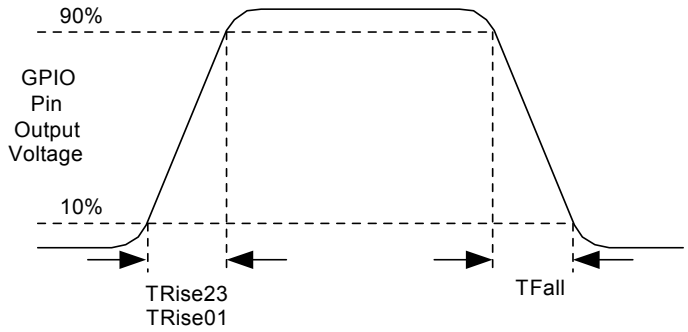
AC General Purpose I/O Specifications

Table 15 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 15. AC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{GPIO}	GPIO operating frequency	Normal strong mode, Ports 0, 1	–	–	12	MHz
TRise23	Rise time, strong mode Ports 2, 3	V_{DD} = 3.0 to 3.6 V, 10% - 90%	15	–	80	ns
TRise01	Rise time, strong mode Ports 0, 1	V_{DD} = 3.0 to 3.6 V, 10% - 90%	10	–	50	ns
TFall	Fall time, strong mode All Ports	V_{DD} = 3.0 to 3.6 V, 10% - 90%	10	–	50	ns

Figure 11. GPIO Timing Diagram



AC External Clock Specifications

Table 16 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 16. AC External Clock Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{OSCEXT}	Frequency		0.750	–	25.2	MHz
–	High period		20.6	–	5300	ns
–	Low period		20.6	–	–	ns
–	Power-up IMO to switch		150	–	–	µs

Table 19. SPI Master AC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{SCLK}	SCLK clock frequency		–	–	6	MHz
DC	SCLK duty cycle		–	50	–	%
T_{SETUP}	MISO to SCLK setup time		60	–	–	ns
T_{HOLD}	SCLK to MISO hold time		40	–	–	ns
T_{OUT_VAL}	SCLK to MOSI valid time		–	–	40	ns
T_{OUT_H}	SCLK to MOSI hold time		40	–	–	ns

Figure 14. SPI Master Mode 0 and 2

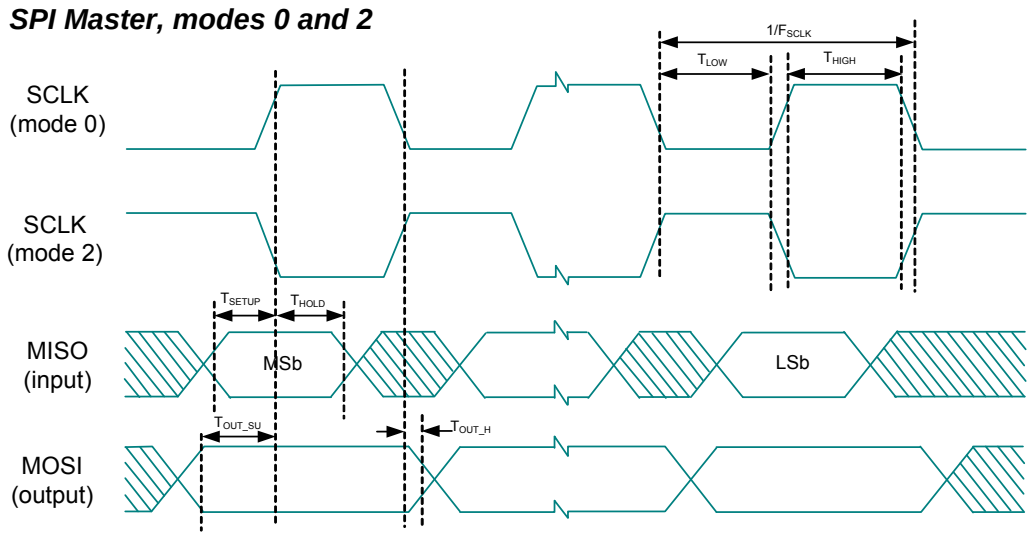


Figure 15. SPI Master Mode 1 and 3

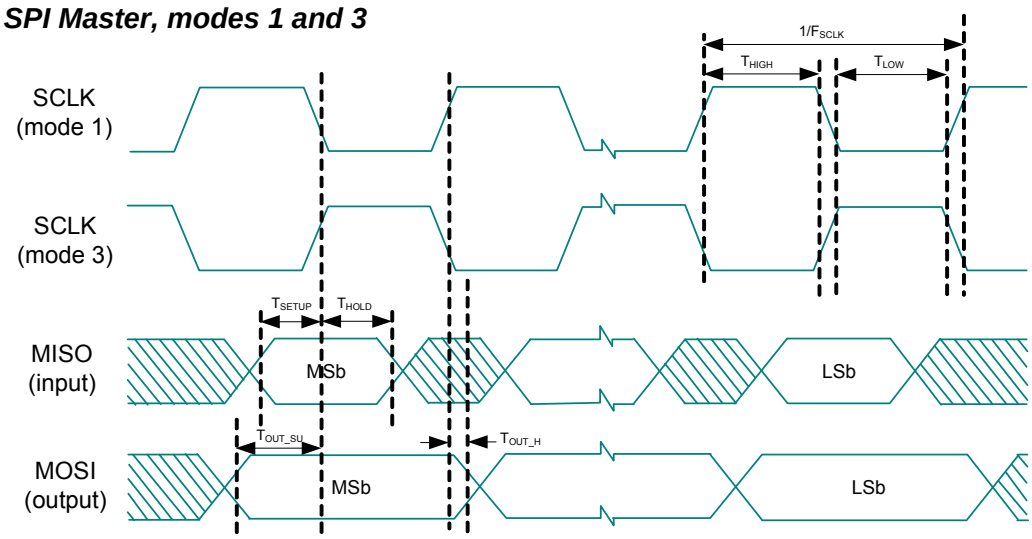
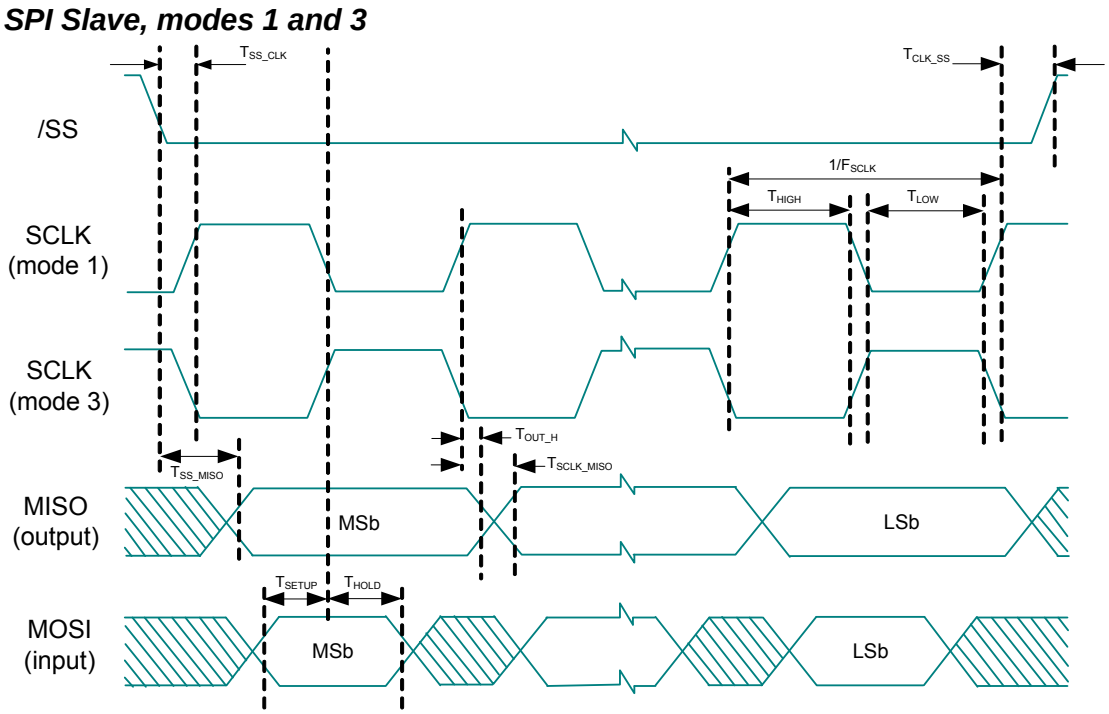


Figure 17. SPI Slave Mode 1 and 3



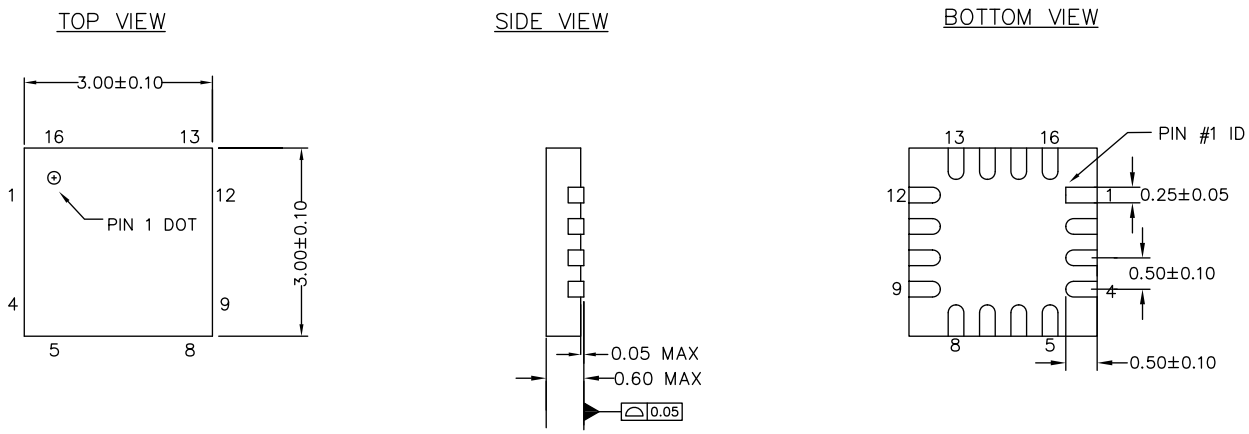
Package Diagrams

This section illustrates the packaging specifications for the enCoRe V USB device, along with the thermal impedances for each package.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the enCoRe V emulation tools and their dimensions, refer to the development kit.

Packaging Dimensions

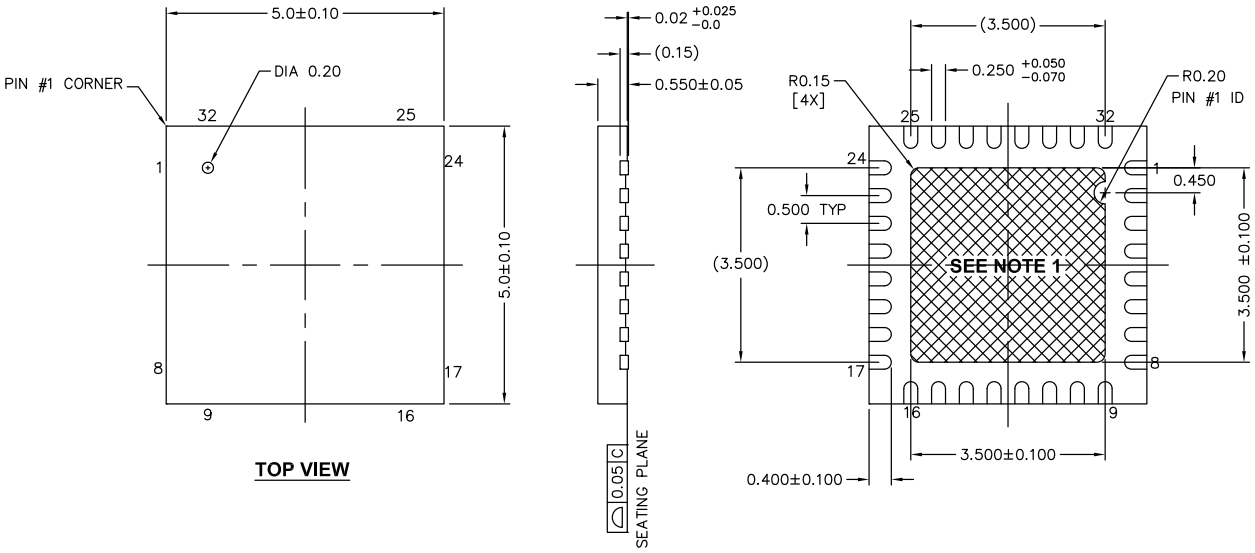
Figure 18. 16-pin Chip On Lead (3 × 3 × 0.6 mm) LG16A/LD16A (Sawn) Package Outline, 001-09116



NOTES
1. REFERENCE JEDEC # MO−220
2. ALL DIMENSIONS ARE IN MILLIMETERS

001-09116 *J

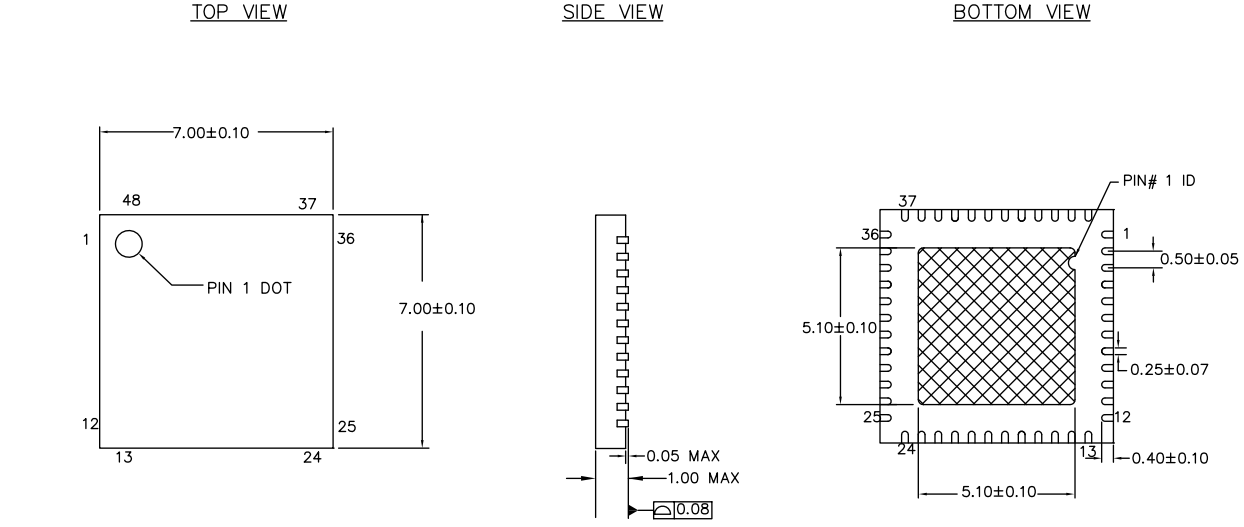
Figure 19. 32-pin QFN (5 × 5 × 0.55 mm) LQ32 3.5 × 3.5 E-Pad (Sawn) Package Outline, 001-42168



NOTES:
1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO−248
3. PACKAGE WEIGHT: 0.0388g
4. DIMENSIONS ARE IN MILLIMETERS

001-42168 *E

Figure 20. 48-pin QFN (7 × 7 × 1.00 mm) LT48A 5.1 × 5.1 E-Pad (Sawn) Package Outline, 001-13191



NOTES:
1. HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO−220
3. PACKAGE WEIGHT: 13 ± 1 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13191 *H

Package Handling

Some IC packages require baking before they are soldered onto a PCB to remove moisture that may have been absorbed after leaving the factory. A label on the package has details about the actual bake temperature and the minimum bake time to remove this moisture. The maximum bake time is the aggregate time that the parts exposed to the bake temperature. Exceeding this exposure may degrade device reliability.

Table 21. Package Handling

Parameter	Description	Minimum	Typical	Maximum	Unit
TBAKETEMP	Bake temperature	–	125	See package label	°C
TBAKETIME	Bake time	See package label	–	72	hours

Thermal Impedances

Table 22. Thermal Impedances per Package

Package	Typical θ_{JA} [21]
16-pin QFN	32.69 °C / W
32-pin QFN [22]	19.51 °C / W
48-pin QFN [22]	17.68 °C / W

Capacitance on Crystal Pins

Table 23. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
32-pin QFN	3.2 pF
48-pin QFN	3.3 pF

Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Table 24. Solder Reflow Peak Temperature

Package	Minimum Peak Temperature [23]	Maximum Peak Temperature
16-pin QFN	240 °C	260 °C
32-pin QFN	240 °C	260 °C
48-pin QFN	240 °C	260 °C

Notes
21. $T_J = T_A$ + Power x θ_{JA}.
22. To achieve the thermal impedance specified for the package, solder the center thermal pad to the PCB ground plane.
23. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5 °C with Sn-Pb or 245 ± 5 °C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

Ordering Code Definitions

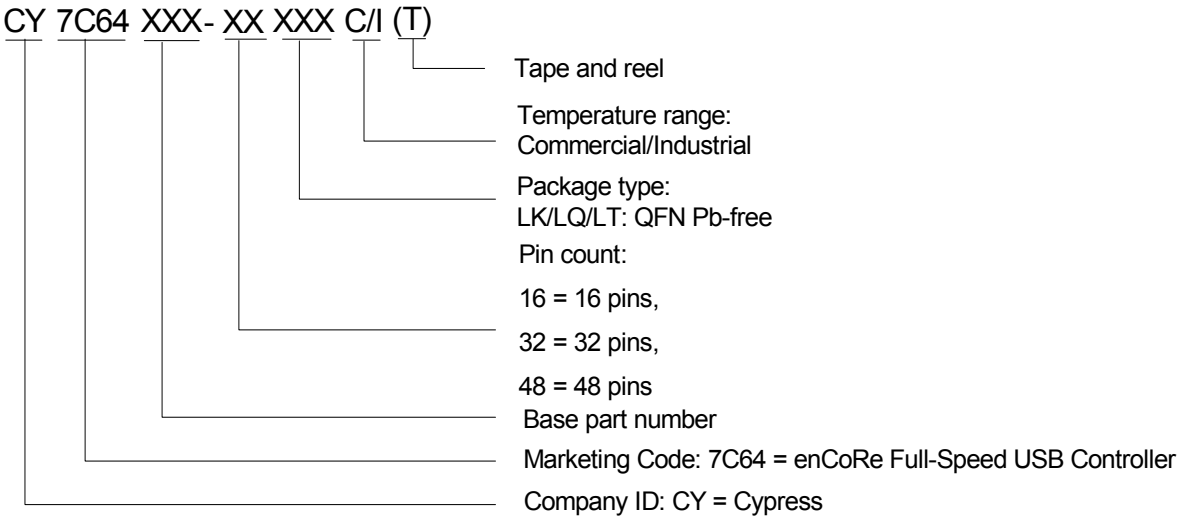
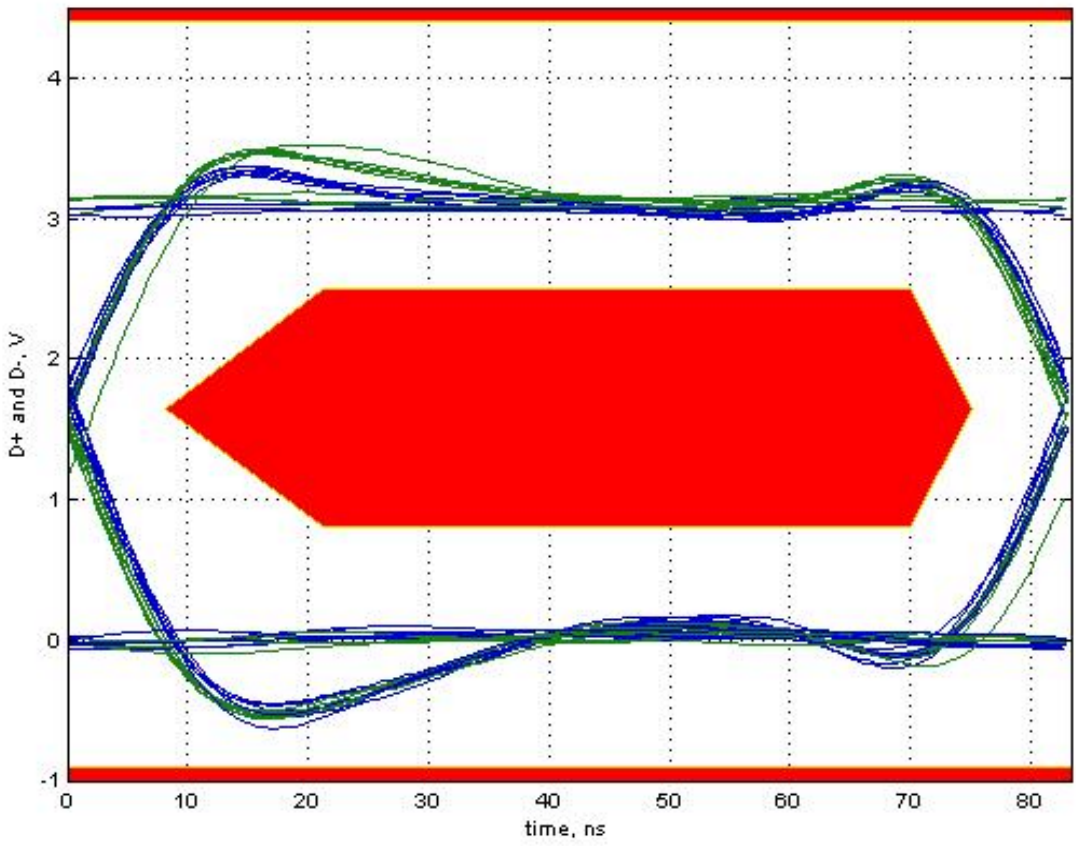


Figure 21. Eye Diagram



■WORKAROUND

Avoid the trigger condition by using lower tolerance voltage regulators.

■FIX STATUS

This issue will not be corrected in the next new silicon revision.

Document History Page

Document Title: CY7C6431x/CY7C6434x/CY7C6435x, enCoRe™ V Full Speed USB Controller Document Number: 001-12394				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	626256	TYJ	See ECN	New data sheet.
*A	735718	TYJ / ARI	See ECN	Filled in TBDs, added new block diagram, and corrected some values. Part numbers updated as per new specifications.
*B	1120404	ARI	See ECN	Corrected the block diagram and Figure 3, which is the 16-pin enCoRe V device. Corrected the description to pin 29 on Table 2, the Typ/Max values for I_{SB0} on the DC chip-level specifications, the current value for the latch-up current in the Electrical Characteristics section, and corrected the 16 QFN package information in the Thermal Impedance table. Corrected some of the bulleted items on the first page. Added DC Characteristics–USB Interface table. Added AC Characteristics–USB Data Timings table. Added AC Characteristics–USB Driver table. Corrected Flash Write Endurance minimum value in the DC Programming Specifications table. Corrected the Flash Erase Time max value and the Flash Block Write Time max value in the AC Programming Specifications table. Implemented new latest template. Include parameters: Vcrs, Rpu (USB, active), Rpu (USB suspend), Tfdeop, Tfeopr2, Tfeopt, Tfst. Added register map tables. Corrected a value in the DC Chip-Level Specifications table.
*C	1241024	TYJ / ARI	See ECN	Corrected Idd values in Table 6 - DC Chip-Level Specifications.
*D	1639963	AESA	See ECN	Post to www.cypress.com
*E	2138889	TYJ / PYRS	See ECN	Updated Ordering Code table: - Ordering code changed for 32-QFN package: From -32LKXC to -32LTXC - Added a new package type – “LTXC” for 48-QFN - Included Tape and Reel ordering code for 32-QFN and 48-QFN packages Changed active current values at 24, 12 and 6MHz in table “DC Chip-Level Specifications” - IDD24: 2.15 to 3.1mA - IDD12: 1.45 to 2.0mA - IDD6: 1.1 to 1.5mA Added information on using P1[0] and P1[1] as the I2C interface during POR or reset events

Document History Page *(continued)*

Document Title: CY7C6431x/CY7C6434x/CY7C6435x, enCoRe™ V Full Speed USB Controller Document Number: 001-12394				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*F	2583853	TYJ / PYRS / HMT	10/10/08	Converted from Preliminary to Final Added operating voltage ranges with USB ADC resolution changed from 10-bit to 8-bit Rephrased battery monitoring clause in page 1 to include “with external components” Included ADC specifications table Included Voh7, Voh8, Voh9, Voh10 specs Flash data retention – condition added to Note [11] Input leakage spec changed to 25 nA max Under AC Char, Frequency accuracy of ILO corrected GPIO rise time for ports 0,1 and ports 2,3 made common AC Programming specifications updated Included AC Programming cycle timing diagram AC SPI specification updated Spec change for 32-QFN package Input Leakage Current maximum value changed to 1 μA Updated V_{OHV} parameter in Table 13 Updated thermal impedances for the packages Update Development Tools, add Designing with PSoC Designer. Edit, fix links and table format. Update TMs.
*G	2653717	DVJA / PYRS	02/04/09	Updated Features, Functional Overview, Development Tools, and Designing with PSoC Designer sections with edits. Removed ‘GUI - graphical user interface’ from Document Conventions acronym table. Removed ‘O - Only a read/write register or bits’ in Table 4 Edited Table 8: removed 10-bit resolution information and corrected units column. Added package handling section Added 8K part ‘CY7C64343-32LQXC’ to Ordering Information.
*H	2714694	DVJA / AESA	06/04/2009	Updated Block Diagram. Added Full Speed USB, 10-bit ADC, SPI, and I2C Slave sections. ADC Resolution changed from 8-bit to 10-bit Updated Table 9 DC Chip Level Specs Updated Table10 DC Char - USB Interface Updated Table 12 DC POR and LDV Specs Changed operating temperature from Commercial to Industrial Changed Temperature Range to Industrial: –40 to 85°C Figure 9: Changed minimum CPU Frequency from 750 kHz to 5.7 MHz Table 14: Removed “Maximum” from the F_{CPU} description Ordering Information: Replaced ‘C’ with ‘I’ in all part numbers to denote Industrial Temp Range
*I	2764460	DVJA / AESA	09/16/2009	Changed Table 12: ADC Specs Added F_{32K2} (Untrimmed) spec to Table 16: AC Chip level Specs Changed T_{RAMP} spec to SR_{POWER_UP} in Table 16: AC Chip Level Specs Added Table 27: Typical Package Capacitance on Crystal Pins
*J	2811903	DVJA	11/20/2009	Added USB-IF TID number in Features on page 1. Added Note 5 on page 18. Changed V_{IHP} in Table 12 on page 22.