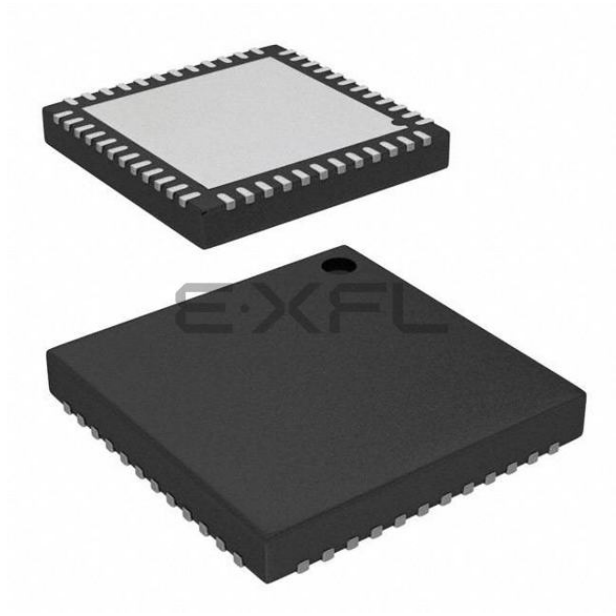

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Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	USB Microcontroller
Core Processor	M8C
Program Memory Type	FLASH (16kB)
Controller Series	CY7C643xx
RAM Size	1K x 8
Interface	I²C, SPI, USB
Number of I/O	36
Voltage - Supply	3V ~ 5.5V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy7c64355-48ltxct

Contents

Functional Overview

The enCoRe V family of devices are designed to replace multiple traditional full-speed USB microcontroller system components with one, low cost single-chip programmable component. Communication peripherals (I^2C/SPI), a fast CPU, Flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The architecture for this device family, as illustrated in the enCoRe V Block Diagram on page 1, consists of two main areas: the CPU core and the system resources. Depending on the enCoRe V package, up to 36 GPIO are also included.

This product is an enhanced version of Cypress's successful full speed-USB peripheral controllers. Enhancements include faster CPU at lower voltage operation, lower current consumption, twice the RAM and Flash, hot-swappable I/Os, I^2C hardware address recognition, new very low current sleep mode, and new package options.

The enCoRe V Core

The enCoRe V Core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and IMO and ILO. The CPU core, called the M8C, is a powerful processor with speeds up to 24 MHz. The M8C is a four-MIPS, 8-bit Harvard architecture microprocessor.

During USB operation, the CPU speed can be set to any setting. Be aware that USB throughput decreases with a decrease in CPU speed. For maximum throughput, the CPU clock should be made equal to the system clock. The system clock must be 24 MHz for USB operation.

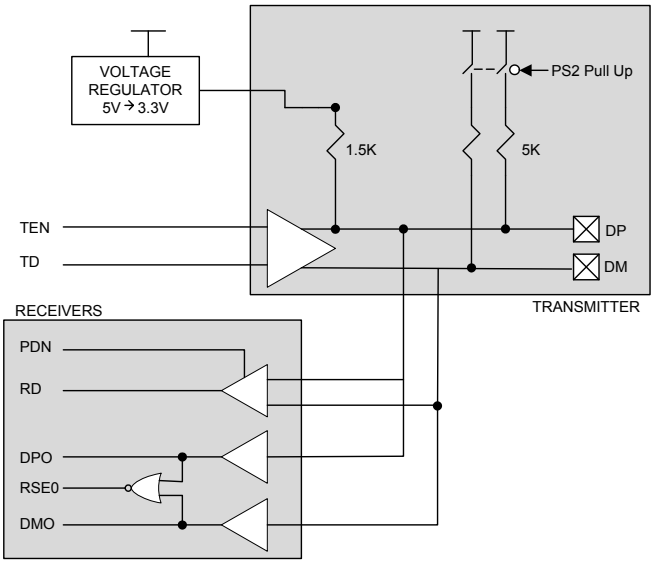
System resources provide additional capability, such as a configurable I^2C slave and SPI master-slave communication interface and various system resets supported by the M8C.

Full-Speed USB

The enCoRe V USB system resource adheres to the USB 2.0 Specification for full speed devices operating at 12 Mb/second with one upstream port and one USB address. enCoRe V USB consists of these components:

- Serial interface engine (SIE) block.
- PSoC memory arbiter (PMA) block.
- 512 bytes of dedicated SRAM.
- A full-speed USB Transceiver with internal regulator and two dedicated USB pins.

Figure 1. USB Transceiver Regulator



At the enCoRe V system level, the full-speed USB system resource interfaces to the rest of the enCoRe V by way of the M8C's register access instructions and to the outside world by way of the two USB pins. The SIE supports nine endpoints including a bidirectional control endpoint (endpoint 0) and eight unidirectional data endpoints (endpoints 1 to 8). The unidirectional data endpoints are individually configurable as either IN or OUT.

Low value series resistors R_{EXT} (22 Ω) must be added externally to the D+ and D– lines to meet the driving impedance requirement for full-speed USB.

The USB Serial Interface Engine (SIE) allows the enCoRe V device to communicate with the USB host at full speed data rates (12 Mb/s). The SIE simplifies the interface to USB traffic by automatically handling the following USB processing tasks without firmware intervention:

- Translates the encoded received data and formats the data to be transmitted on the bus.
- Generates and checks cyclical redundancy checks (CRCs). Incoming packets failing checksum verification are ignored.
- Checks addresses. Ignores all transactions not addressed to the device.
- Sends appropriate ACK/NAK/Stall handshakes.
- Identifies token type (SETUP, IN, OUT) and sets the appropriate token bit once a valid token in received.
- Identifies Start-of-Frame (SOF) and saves the frame count.
- Sends data to or retrieves data from the USB SRAM, by way of the PSoC Memory Arbiter (PMA).

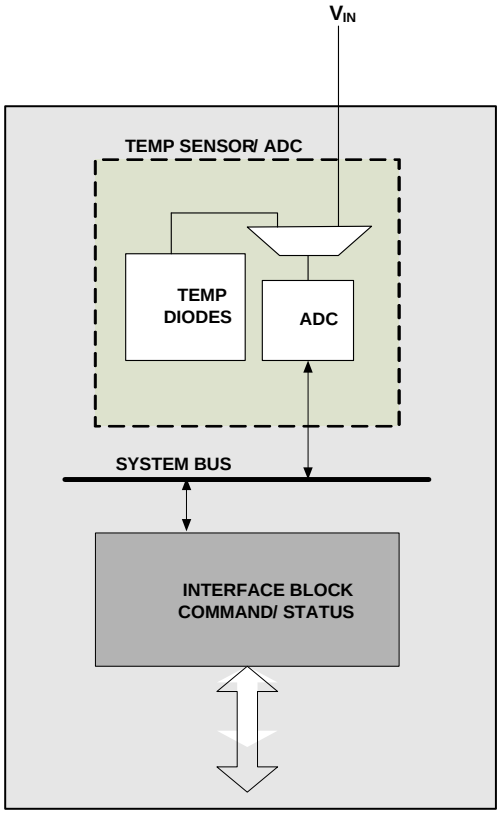
Firmware is required to handle various parts of the USB interface. The SIE issues interrupts after key USB events to direct firmware to appropriate tasks:

- Fill and empty the USB data buffers in USB SRAM.
- Enable PMA channels appropriately.
- Coordinate enumeration by decoding USB device requests.
- Suspend and resume coordination.
- Verify and select data toggle values.

10-bit ADC

The ADC on enCoRe V device is an independent block with a state machine interface to control accesses to the block. The ADC is housed together with the temperature sensor core and can be connected to this or the Analog mux bus. As a default operation, the ADC is connected to the temperature sensor diodes to give digital values of the temperature.

Figure 2. ADC System Performance Block Diagram



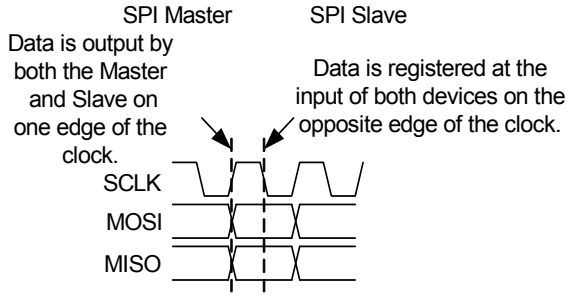
The ADC User Module contains an integrator block and one comparator with positive and negative input set by the MUXes. The input to the integrator stage comes from the analog global input mux or the temperature sensor with an input voltage range of 0 V to V_{REFADC}.

In the ADC only configuration (the ADC MUX selects the Analog mux bus, not the default temperature sensor connection), an external voltage can be connected to the input of the modulator for voltage conversion. The ADC is run for a number of cycles set by the timer, depending upon the desired resolution of the ADC. A counter counts the number of trips by the comparator, which is proportional to the input voltage. The Temp Sensor block clock speed is 36 MHz and is divided down to 1 to 12 MHz for ADC operation.

SPI

The serial peripheral interconnect (SPI) 3-wire protocol uses both edges of the clock to enable synchronous communication without the need for stringent setup and hold requirements.

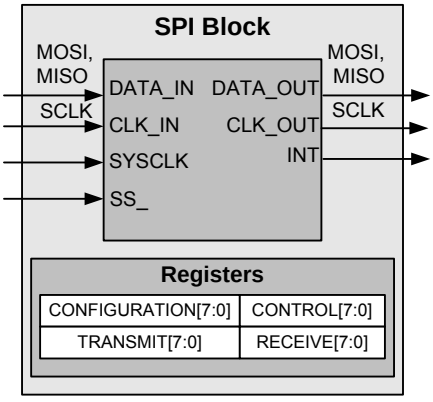
Figure 3. Basic SPI Configuration



A device can be a master or slave. A master outputs clock and data to the slave device and inputs slave data. A slave device inputs clock and data from the master device and outputs data for input to the master. Together, the master and slave are essentially a circular Shift register, where the master generates the clocking and initiates data transfers.

A basic data transfer occurs when the master sends eight bits of data, along with eight clocks. In any transfer, both master and slave transmit and receive simultaneously. If the master only sends data, the received data from the slave is ignored. If the master wishes to receive data from the slave, the master must send dummy bytes to generate the clocking for the slave to send data back.

Figure 4. SPI Block Diagram



Additional System Resources

System resources, some of which have been previously listed, provide additional capability useful to complete systems. Additional resources include low voltage detection and power on reset. The following statements describe the merits of each system resource.

- Low voltage detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR (power on reset) circuit eliminates the need for a system supervisor.
- The 5 V maximum input, 1.8, 2.5, or 3 V selectable output, LDO regulator provides regulation for I/Os. A register controlled bypass mode enables the user to disable the LDO.
- Standard Cypress PSoC IDE tools are available for debugging the enCoRe V family of parts.

Getting Started

The quickest path to understanding the enCoRe V silicon is by reading this data sheet and using the PSoC Designer Integrated Development Environment (IDE). This datasheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications. For in-depth information, along with detailed programming information, see the *enCoRe™ V CY7C643xx, enCoRe™ V LV CY7C604xx Technical Reference Manual (TRM)* for this PSoC device.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device data sheets on the web at http://www.cypress.com.

Application Notes

Application notes are an excellent introduction to the wide variety of possible PSoC designs and are available at http://www.cypress.com.

Development Kits

PSoC development kits are available online from Cypress at http://www.cypress.com and through a growing number of regional and global distributors, including Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops) is available online at http://www.cypress.com. The training covers a wide variety of topics and skill levels to assist you in your designs.

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Register Reference

The section discusses the registers of the enCoRe V device. It lists all the registers in mapping tables, in address order.

Register Conventions

The register conventions specific to this section are listed in the following table.

Table 1. Register Conventions

Convention	Description
R	Read register or bits
W	Write register or bits
L	Logical register or bits
C	Clearable register or bits
#	Access is bit specific

Register Mapping Tables

The enCoRe V device has a total register address space of 512 bytes. The register space is also referred to as I/O space and is broken into two parts: Bank 0 (user space) and Bank 1 (configuration space). The XIO bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XIO bit is set, the user is said to be in the “extended” address space or the “configuration” registers.

Table 2. Register Map Bank 0 Table: User Space

Name	Addr (0, Hex)	Access	Name	Addr (0, Hex)	Access	Name	Addr (0, Hex)	Access	Name	Addr (0, Hex)	Access
PRT0DR	00	RW	EP1_CNT0	40	#		80			C0	
PRT0IE	01	RW	EP1_CNT1	41	RW		81			C1	
	02		EP2_CNT0	42	#		82			C2	
	03		EP2_CNT1	43	RW		83			C3	
PRT1DR	04	RW	EP3_CNT0	44	#		84			C4	
PRT1IE	05	RW	EP3_CNT1	45	RW		85			C5	
	06		EP4_CNT0	46	#		86			C6	
	07		EP4_CNT1	47	RW		87			C7	
PRT2DR	08	RW	EP5_CNT0	48	#		88		I2C_XCFG	C8	RW
PRT2IE	09	RW	EP5_CNT1	49	RW		89		I2C_XSTAT	C9	R
	0A		EP6_CNT0	4A	#		8A		I2C_ADDR	CA	RW
	0B		EP6_CNT1	4B	RW		8B		I2C_BP	CB	R
PRT3DR	0C	RW	EP7_CNT0	4C	#		8C		I2C_CP	CC	R
PRT3IE	0D	RW	EP7_CNT1	4D	RW		8D		CPU_BP	CD	RW
	0E		EP8_CNT0	4E	#		8E		CPU_CP	CE	R
	0F		EP8_CNT1	4F	RW		8F		I2C_BUF	CF	RW
PRT4DR	10	RW		50			90		CUR_PP	D0	RW
PRT4IE	11	RW		51			91		STK_PP	D1	RW
	12			52			92			D2	
	13			53			93		IDX_PP	D3	RW
	14			54			94		MVR_PP	D4	RW
	15			55			95		MVW_PP	D5	RW
	16			56			96		I2C_CFG	D6	RW
	17			57			97		I2C_SCR	D7	#
	18		PMA0_DR	58	RW		98		I2C_DR	D8	RW
	19		PMA1_DR	59	RW		99			D9	
	1A		PMA2_DR	5A	RW		9A		INT_CLR0	DA	RW
	1B		PMA3_DR	5B	RW		9B		INT_CLR1	DB	RW
	1C		PMA4_DR	5C	RW		9C		INT_CLR2	DC	RW
	1D		PMA5_DR	5D	RW		9D			DD	
	1E		PMA6_DR	5E	RW		9E		INT_MSK2	DE	RW
	1F		PMA7_DR	5F	RW		9F		INT_MSK1	DF	RW
	20			60			A0		INT_MSK0	E0	RW
	21			61			A1		INT_SW_EN	E1	RW
	22			62			A2		INT_VC	E2	RC
	23			63			A3		RES_WDT	E3	W
	24		PMA8_DR	64	RW		A4			E4	
	25		PMA9_DR	65	RW		A5			E5	
	26		PMA10_DR	66	RW		A6			E6	
	27		PMA11_DR	67	RW		A7			E7	
	28		PMA12_DR	68	RW		A8			E8	
SPI_TXR	29	W	PMA13_DR	69	RW		A9			E9	
SPI_RXR	2A	R	PMA14_DR	6A	RW		AA			EA	
SPI_CR	2B	#	PMA15_DR	6B	RW		AB			EB	
	2C		TMP_DR0	6C	RW		AC			EC	
	2D		TMP_DR1	6D	RW		AD			ED	
	2E		TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
	30			70		PT0_CFG	B0	RW		F0	
USB_SOF0	31	R		71		PT0_DATA1	B1	RW		F1	
USB_SOF1	32	R		72		PT0_DATA0	B2	RW		F2	
USB_CR0	33	RW		73		PT1_CFG	B3	RW		F3	
USBIO_CR0	34	#		74		PT1_DATA1	B4	RW		F4	
USBIO_CR1	35	#		75		PT1_DATA0	B5	RW		F5	
EP0_CR	36	#		76		PT2_CFG	B6	RW		F6	
EP0_CNT0	37	#		77		PT2_DATA1	B7	RW	CPU_F	F7	RL
EP0_DR0	38	RW		78		PT2_DATA0	B8	RW		F8	
EP0_DR1	39	RW		79			B9			F9	
EP0_DR2	3A	RW		7A			BA			FA	
EP0_DR3	3B	RW		7B			BB			FB	
EP0_DR4	3C	RW		7C			BC			FC	
EP0_DR5	3D	RW		7D			BD			FD	
EP0_DR6	3E	RW		7E			BE		CPU_SCR1	FE	#
EP0_DR7	3F	RW		7F			BF		CPU_SCR0	FF	#

Gray fields are reserved; do not access these fields. # Access is bit specific.

Table 3. Register Map Bank 1 Table: Configuration Space

Name	Addr (1, Hex)	Access	Name	Addr (1, Hex)	Access	Name	Addr (1, Hex)	Access	Name	Addr (1, Hex)	Access
PRT0DM0	00	RW	PMA4_RA	40	RW		80			C0	
PRT0DM1	01	RW	PMA5_RA	41	RW		81			C1	
	02		PMA6_RA	42	RW		82			C2	
	03		PMA7_RA	43	RW		83			C3	
PRT1DM0	04	RW	PMA8_WA	44	RW		84			C4	
PRT1DM1	05	RW	PMA9_WA	45	RW		85			C5	
	06		PMA10_WA	46	RW		86			C6	
	07		PMA11_WA	47	RW		87			C7	
PRT2DM0	08	RW	PMA12_WA	48	RW		88			C8	
PRT2DM1	09	RW	PMA13_WA	49	RW		89			C9	
	0A		PMA14_WA	4A	RW		8A			CA	
	0B		PMA15_WA	4B	RW		8B			CB	
PRT3DM0	0C	RW	PMA8_RA	4C	RW		8C			CC	
PRT3DM1	0D	RW	PMA9_RA	4D	RW		8D			CD	
	0E		PMA10_RA	4E	RW		8E			CE	
	0F		PMA11_RA	4F	RW		8F			CF	
PRT4DM0	10	RW	PMA12_RA	50	RW		90			D0	
PRT4DM1	11	RW	PMA13_RA	51	RW		91			D1	
	12		PMA14_RA	52	RW		92		ECO_ENBUS	D2	RW
	13		PMA15_RA	53	RW		93		ECO_TRIM	D3	RW
	14		EP1_CR0	54	#		94			D4	
	15		EP2_CR0	55	#		95			D5	
	16		EP3_CR0	56	#		96			D6	
	17		EP4_CR0	57	#		97			D7	
	18		EP5_CR0	58	#		98		MUX_CR0	D8	RW
	19		EP6_CRO	59	#		99		MUX_CR1	D9	RW
	1A		EP7_CR0	5A	#		9A		MUX_CR2	DA	RW
	1B		EP8_CR0	5B	#		9B		MUX_CR3	DB	RW
	1C			5C			9C		IO_CFG1	DC	RW
	1D			5D			9D		OUT_P1	DD	RW
	1E			5E			9E		IO_CFG2	DE	RW
	1F			5F			9F		MUX_CR4	DF	RW
	20			60			A0		OSC_CR0	E0	RW
	21			61			A1		ECO_CFG	E1	#
	22			62			A2		OSC_CR2	E2	RW
	23			63			A3		VLT_CR	E3	RW
	24			64			A4		VLT_CMP	E4	R
	25			65			A5			E5	
	26			66			A6			E6	
	27			67			A7			E7	
	28			68			A8		IMO_TR	E8	W
SPI_CFG	29	RW		69			A9		ILO_TR	E9	W
	2A			6A			AA			EA	
	2B			6B			AB		SLP_CFG	EB	RW
	2C		TMP_DR0	6C	RW		AC		SLP_CFG2	EC	RW
	2D		TMP_DR1	6D	RW		AD		SLP_CFG3	ED	RW
	2E		TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
USB_CR1	30	#		70			B0			F0	
	31			71			B1			F1	
	32			72			B2			F2	
	33			73			B3			F3	
PMA0_WA	34	RW		74			B4			F4	
PMA1_WA	35	RW		75			B5			F5	
PMA2_WA	36	RW		76			B6			F6	
PMA3_WA	37	RW		77			B7		CPU_F	F7	RL
PMA4_WA	38	RW		78			B8			F8	
PMA5_WA	39	RW		79			B9			F9	
PMA6_WA	3A	RW		7A			BA		IMO_TR1	FA	RW
PMA7_WA	3B	RW		7B			BB			FB	
PMA0_RA	3C	RW		7C			BC			FC	
PMA1_RA	3D	RW		7D		USB_MISC_CR	BD	RW		FD	
PMA2_RA	3E	RW		7E			BE			FE	
PMA3_RA	3F	RW		7F			BF			FF	

Gray fields are reserved; do not access these fields. # Access is bit specific.

Electrical Specifications

This section presents the DC and AC electrical specifications of the enCoRe V USB devices. For the most up-to-date electrical specifications, verify that you have the most recent data sheet available by visiting the company web site at http://www.cypress.com

Figure 9. Voltage versus CPU Frequency

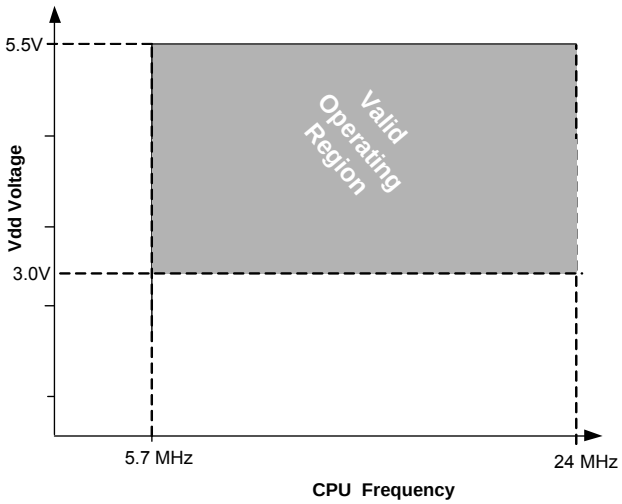
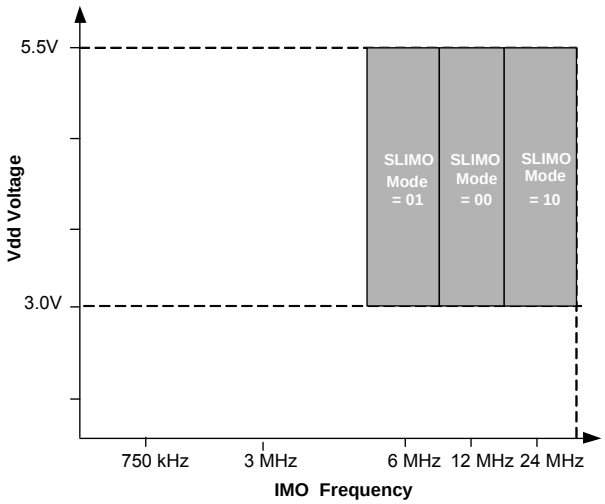


Figure 10. IMO Frequency Trim Options



Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 4. Absolute Maximum Ratings

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{STG}	Storage temperature[10]	Higher storage temperatures reduces data retention time. Recommended Storage Temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 85°C degrades reliability.	–55	+25	+125	°C
V_{DD}	Supply voltage relative to V_{SS}		–0.5	–	+6.0	V
V_{IO}	DC input voltage		V_{SS} – 0.5	–	V_{DD} + 0.5	V
V_{IOZ}	DC voltage applied to tristate		V_{SS} – 0.5	–	V_{DD} + 0.5	V
I_{MIO}	Maximum current into any port pin		–25	–	+50	mA
ESD	Electrostatic discharge voltage	Human body model ESD	2000	–	–	V
LU [8]	Latch up current	In accordance with JESD78 standard	–	–	200	mA

Operating Temperature

Table 5. Operating Temperature

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{AI}	Ambient industrial temperature		–40	–	+85	°C
T_{AC}	Ambient commercial temperature		0	–	+70	°C
T_{JI}	Operational industrial die temperature [11]	The temperature rise from ambient to junction is package specific. Refer the table Thermal Impedances per Package on page 31. The user must limit the power consumption to comply with this requirement.	–40	–	+100	°C
T_{JC}	Operational commercial die temperature	The temperature rise from ambient to junction is package specific. Refer the table Thermal Impedances per Package on page 31. The user must limit the power consumption to comply with this requirement.	0	–	+85	°C

Notes

7. When V_{DD} remains in the range from 1.71 V to 1.9 V for more than 50 µsec, the slew rate when moving from the 1.71 V to 1.9 V range to greater than 2 V must be slower than 1 V/500 µsec to avoid triggering POR. The only other restriction on slew rates for any other voltage range or transition is the SRPOWER_UP parameter.
8. Errata: For Port 1 pins P1[1], P1[4], and P1[5] 300 Ohm external resistor is needed to meet this spec. Refer to "Errata" on page 35 for more details.
9. If powering down in standby sleep mode, to properly detect and recover from a V_{DD} brown out condition any of the following actions must be taken:
   - Bring the device out of sleep before powering down.
   - Assure that V_{DD} falls below 100 mV before powering back up.
   - Set the No Buzz bit in the OSC_CR0 register to keep the voltage monitoring circuit powered during sleep.
   - Increase the buzz rate to assure that the falling edge of V_{DD} is captured. The rate is configured through the PSSDC bits in the SLP_CFG register. For the referenced registers, refer to the enCoRe V Technical Reference Manual. In deep sleep mode, additional low power voltage monitoring circuitry allows V_{DD} brown out conditions to be detected for edge rates slower than 1 V/ms.

DC General Purpose I/O Specifications

Table 9 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and package specific temperature range. Typical parameters apply to 5 V and 3.3 V at 25 °C. These are for design guidance only.

Table 9. 3.0 V and 5.5 V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{PU}	Pull-up resistor		4	5.6	8	kΩ
V_{OH1}	High output voltage Port 2 or 3 pins	$I_{OH} \leq 10$ µA, maximum of 10 mA source current in all I/Os.	$V_{DD} - 0.2$	–	–	V
V_{OH2}	High output voltage Port 2 or 3 Pins	I_{OH} = 1 mA, maximum of 20 mA source current in all I/Os.	$V_{DD} - 0.9$	–	–	V
V_{OH3}	High output voltage Port 0 or 1 pins with LDO regulator disabled	$I_{OH} < 10$ µA, maximum of 10 mA source current in all I/Os.	$V_{DD} - 0.2$	–	–	V
V_{OH4}	High output voltage Port 0 or 1 pins with LDO regulator disabled	I_{OH} = 5 mA, maximum of 20 mA source current in all I/Os.	$V_{DD} - 0.9$	–	–	V
V_{OH5}	High output voltage Port 1 pins with LDO regulator enabled for 3 V Out	$I_{OH} < 10$ µA, $V_{DD} > 3.1$ V, maximum of 4 I/Os all sourcing 5 mA	2.85	3.00	3.3	V
V_{OH6}	High output voltage Port 1 pins with LDO regulator enabled for 3 V out	I_{OH} = 5 mA, $V_{DD} > 3.1$ V, maximum of 20 mA source current in all I/Os	2.20	–	–	V
V_{OH7}	High output voltage Port 1 pins with LDO enabled for 2.5 V out	$I_{OH} < 10$ µA, $V_{DD} > 3.0$ V, maximum of 20 mA source current in all I/Os	2.35	2.50	2.75	V
V_{OH8}	High output voltage Port 1 pins with LDO enabled for 2.5 V out	I_{OH} = 2 mA, $V_{DD} > 3.0$ V, maximum of 20 mA source current in all I/Os	1.90	–	–	V
V_{OH9}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	$I_{OH} < 10$ µA, $V_{DD} > 3.0$ V, maximum of 20 mA source current in all I/Os	1.60	1.80	2.1	V
V_{OH10}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	I_{OH} = 1 mA, $V_{DD} > 3.0$ V, maximum of 20 mA source current in all I/Os	1.20	–	–	V
V_{OL}	Low output voltage	I_{OL} = 25 mA, $V_{DD} > 3.3$ V, maximum of 60 mA sink current on even port pins (for example, P0[2] and P1[4]) and 60 mA sink current on odd port pins (for example, P0[3] and P1[5]).	–	–	0.75	V
V_{IL}	Input low voltage		–	–	0.8	V
V_{IH}	Input high voltage		2.0	–	–	V
V_H	Input hysteresis voltage		–	80	–	mV
I_{IL}	Input leakage (absolute value)		–	0.001	1	µA
C_{PIN}	Pin capacitance	Package and pin dependent. Temp = 25 °C.	0.5	1.7	5	pF

DC POR and LVD Specifications

Table 10 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 10. DC POR and LVD Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{PPOR}	V_{DD} value for PPOR trip[12] PORLEV[1:0] = 10b		–	2.82	2.95	V
	V_{DD} value for LVD trip					
V_{LVD0}	VM[2:0] = 000b		–	–	–	V
V_{LVD1}	VM[2:0] = 001b		–	–	–	V
V_{LVD2}	VM[2:0] = 010b		2.85	2.92	2.99	V
V_{LVD3}	VM[2:0] = 011b		2.95	3.02	3.09	V
V_{LVD4}	VM[2:0] = 100b		3.06	3.13	3.20	V
V_{LVD5}	VM[2:0] = 101b		–-	–	–	V
V_{LVD6}	VM[2:0] = 110b		–	–	–	V
V_{LVD7}	VM[2:0] = 111b		4.62	4.73	4.83	V

DC Programming Specifications

Table 11 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 11. DC Programming Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
$V_{DDIWRITE}$	Supply voltage for flash write operations		1.71	–	5.25	V
I_{DDP}	Supply current during programming or verify		–	5	25	mA
V_{ILP}	Input low voltage during programming or verify	See appropriate DC General Purpose I/O Specifications table	–	–	V_{IL}	V
V_{IHP}	Input high voltage during programming or verify		1.71	–	$V_{DDIWRITE}$ + 0.3	V
I_{ILP}	Input current when applying Vilp to P1[0] or P1[1] during programming or verify[13]		–	–	0.2	mA
I_{IHP}	Input current when applying Vihp to P1[0] or P1[1] during programming or verify[13]		–	–	1.5	mA
V_{OLP}	Output low voltage during programming or verify		–	–	V_{SS} + 0.75	V
V_{OHP}	Output high voltage during programming or verify		$V_{DDIWRITE}$ – 0.9	–	$V_{DDIWRITE}$	V
$Flash_{ENPB}$	Flash write endurance[14]		50,000	–	–	Cycles
$Flash_{DR}$	Flash data retention[15]		10	20	–	Years

Notes
12. Always greater than 50 mV above V_{PPOR} (PORLEV = 10) for falling supply.
13. Driving internal pull down resistor.
14. Erase/write cycles per block.
15. Following maximum Flash write cycles at Tamb = 55 °C and Tj = 70 °C.

AC Programming Specifications

Table 17 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 17. AC Programming Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{RSCLK}	Rise time of SCLK		1	–	20	ns
T_{FSCLK}	Fall time of SCLK		1	–	20	ns
T_{SSCLK}	Data setup time to falling edge of SCLK		40	–	–	ns
T_{HSCLK}	Data hold time from falling edge of SCLK		40	–	–	ns
F_{SCLK}	Frequency of SCLK		0	–	8	MHz
T_{ERASEB}	Flash erase time (Block)		–	–	18	ms
T_{WRITE}	Flash block write time		–	–	25	ms
T_{DSCLK1}	Data out delay from falling edge of SCLK,	V_{DD} > 3.6 V	–	–	60	ns
T_{DSCLK2}	Data out delay from falling edge of SCLK	3.0 V < V_{DD} < 3.6 V	–	–	85	ns
T_{XRST3}	External reset pulse width after power-up	Required to enter programming mode when coming out of sleep	263	–	–	µs

Figure 12. Timing Diagram - AC Programming Cycle

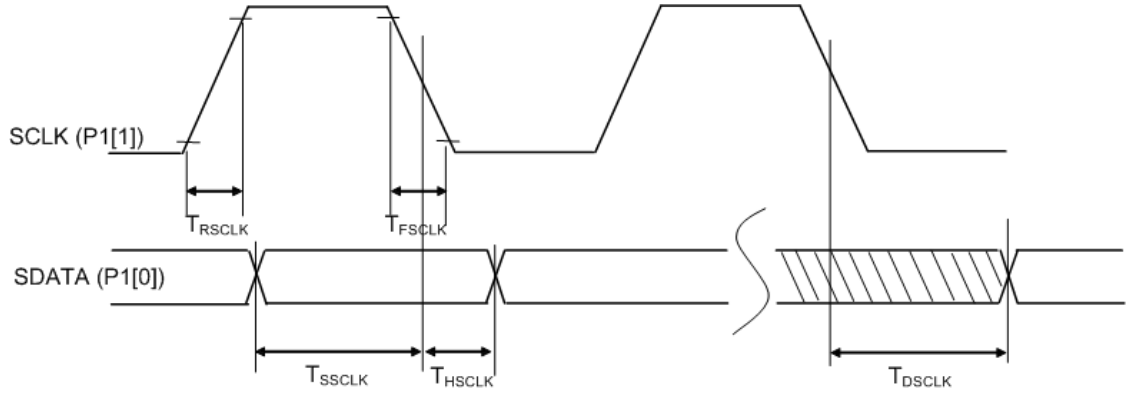


Table 19. SPI Master AC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{SCLK}	SCLK clock frequency		–	–	6	MHz
DC	SCLK duty cycle		–	50	–	%
T_{SETUP}	MISO to SCLK setup time		60	–	–	ns
T_{HOLD}	SCLK to MISO hold time		40	–	–	ns
T_{OUT_VAL}	SCLK to MOSI valid time		–	–	40	ns
T_{OUT_H}	SCLK to MOSI hold time		40	–	–	ns

Figure 14. SPI Master Mode 0 and 2

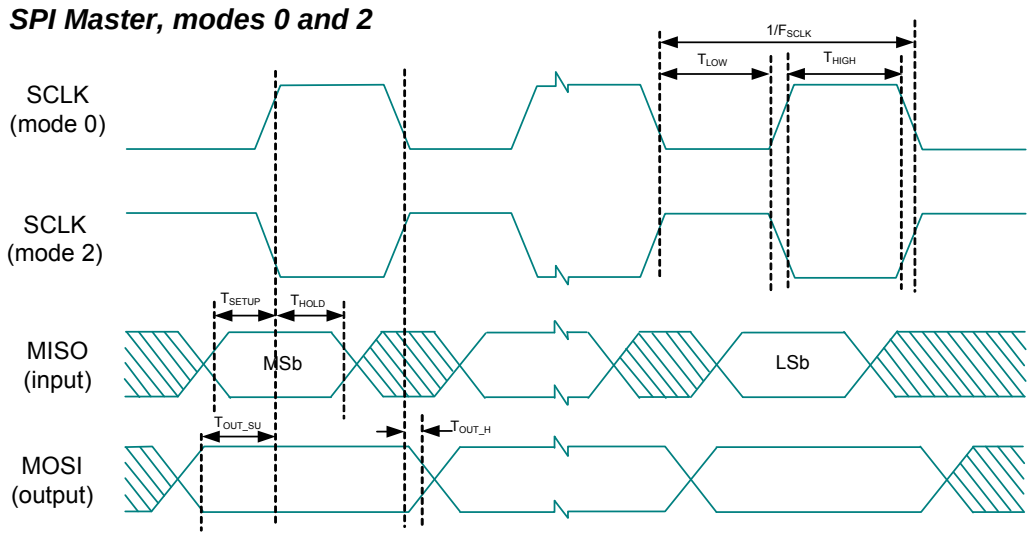
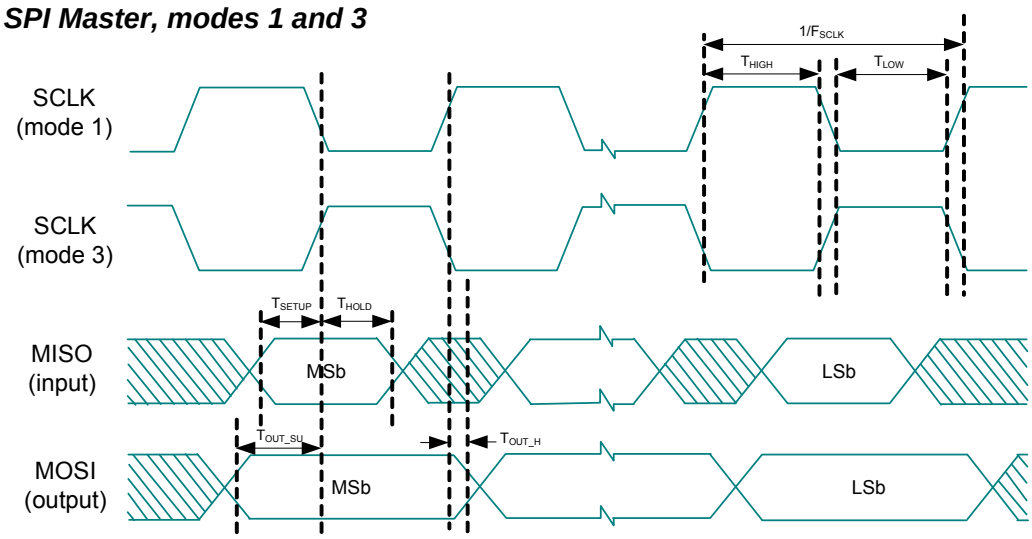


Figure 15. SPI Master Mode 1 and 3



Package Handling

Some IC packages require baking before they are soldered onto a PCB to remove moisture that may have been absorbed after leaving the factory. A label on the package has details about the actual bake temperature and the minimum bake time to remove this moisture. The maximum bake time is the aggregate time that the parts exposed to the bake temperature. Exceeding this exposure may degrade device reliability.

Table 21. Package Handling

Parameter	Description	Minimum	Typical	Maximum	Unit
TBAKETEMP	Bake temperature	–	125	See package label	°C
TBAKETIME	Bake time	See package label	–	72	hours

Thermal Impedances

Table 22. Thermal Impedances per Package

Package	Typical θ_{JA} [21]
16-pin QFN	32.69 °C / W
32-pin QFN [22]	19.51 °C / W
48-pin QFN [22]	17.68 °C / W

Capacitance on Crystal Pins

Table 23. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
32-pin QFN	3.2 pF
48-pin QFN	3.3 pF

Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Table 24. Solder Reflow Peak Temperature

Package	Minimum Peak Temperature [23]	Maximum Peak Temperature
16-pin QFN	240 °C	260 °C
32-pin QFN	240 °C	260 °C
48-pin QFN	240 °C	260 °C

Notes
21. $T_J = T_A$ + Power x θ_{JA}.
22. To achieve the thermal impedance specified for the package, solder the center thermal pad to the PCB ground plane.
23. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5 °C with Sn-Pb or 245 ± 5 °C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

Ordering Information

Table 25. Ordering Code - Commercial Parts

Ordering Code	Package Information	Flash (KB)	SRAM (KB)	No. of GPIOs	Target Applications
CY7C64315-16LKXC	16-pin QFN (3 × 3 mm)	16	1	11	Mid-tier Full-Speed USB dongle, Remote Control Host Module, Various
CY7C64315-16LKXCT	16-pin QFN (Tape and Reel), (3 × 3 mm)	16	1	11	Mid-tier Full-Speed USB dongle, Remote Control Host Module, Various
CY7C64316-16LKXC	16-pin QFN (3 × 3 mm)	32	2	11	Feature-rich Full-Speed USB dongle, Remote Control Host Module, Various
CY7C64316-16LKXCT	16-pin QFN (Tape and Reel), (3 × 3 mm)	32	2	11	Feature-rich Full-Speed USB dongle, Remote Control Host Module, Various
CY7C64343-32LQXC	32-pin QFN (5 × 5 mm)	8	1	25	Full-Speed USB mouse, Various
CY7C64343-32LQXCT	32-pin QFN (Tape and Reel), (5 × 5 mm)	8	1	25	Full-Speed USB mouse, Various
CY7C64345-32LQXC	32-pin QFN (5 × 5 mm)	16	1	25	Full-Speed USB mouse, Various
CY7C64345-32LQXCT	32-pin QFN (Tape and Reel), (5 × 5 mm)	16	1	25	Full-Speed USB mouse, Various
CY7C64346-32LQXCT	32-pin QFN (Tape and Reel), (5 × 5 mm)	32	1	25	Full-Speed USB keyboard, Various
CY7C64355-48LTXC	48-pin QFN (7 × 7 mm)	16	1	36	Full-Speed USB keyboard, Various
CY7C64355-48LTXCT	48-pin QFN (Tape and Reel), (7 × 7 mm)	16	1	36	Full-Speed USB keyboard, Various
CY7C64356-48LTXC	48-pin QFN (7 × 7 mm)	32	2	36	Feature-rich Full-Speed USB keyboard, Various
CY7C64356-48LTXCT	48-pin QFN (Tape and Reel), (7 × 7 mm)	32	2	36	Feature-rich Full-Speed USB keyboard, Various

Table 26. Ordering Code - Industrial Parts

Ordering Code	Package Information	Flash (KB)	SRAM (KB)	No. of GPIOs	Target Applications
CY7C64315-16LKXI	16-pin QFN, Industrial (3 × 3 mm)	16	1	11	Mid-tier Full-Speed USB dongle, Remote Control Host Module, Various
CY7C64315-16LKXIT	16-pin QFN, Industrial (Tape and Reel), (3 × 3 mm)	16	1	11	Mid-tier Full-Speed USB dongle, Remote Control Host Module, Various

Errata

This section describes the errata for the enCoRe V – CY7C643xx. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability.

Contact your local Cypress Sales Representative if you have questions.

CY7C643xx Errata Summary

The following Errata item applies to the **CY7C643xx** data sheets.

1. Latch up susceptibility when maximum I/O sink current exceeded

■PROBLEM DEFINITION

P1[3], P1[6], and P1[7] pins are susceptible to latch up when the I/O sink current exceeds 25 mA per pin on these pins.

■PARAMETERS AFFECTED

LU – Latch up current. Per JESD78A, the maximum allowable latch up current per pin is 100 mA. Cypress internal specification is 200 mA latch up current limit.

■TRIGGER CONDITIONS

Latch up occurs when both the following conditions are met:

A. The offending I/O is externally connected to a voltage higher than the I/O high state, causing a current to flow into the pin that exceeds 25 mA.

B. A Port1 I/O (P1[1], P1[4], and P1[5] respectively) adjacent to the offending I/O is connected to a voltage lower than the I/O low state. This causes a signal that drops below Vss (signal undershoot) and a current greater than 200 mA to flow out of the pin.

■SCOPE OF IMPACT

The trigger conditions outlined in this item exceed the maximum ratings specified in the CY7C643xx data sheets.

■WORKAROUND

Add a series resistor > 300 Ω to P1[3], P1[6], and P1[7] pins to restrict current to within latch up limits.

■FIX STATUS

This issue will be corrected in the next new silicon revision.

2. Does not meet USB 2.0 specification for D+ and D- rise/fall matching when supply voltage is under 3.3 V

■PROBLEM DEFINITION

Rising to falling rate matching of the USB D+ and D- lines has a corner case at lower supply voltages, such as those under 3.3 V.

■PARAMETERS AFFECTED

Rising to falling rate matching of the USB data lines.

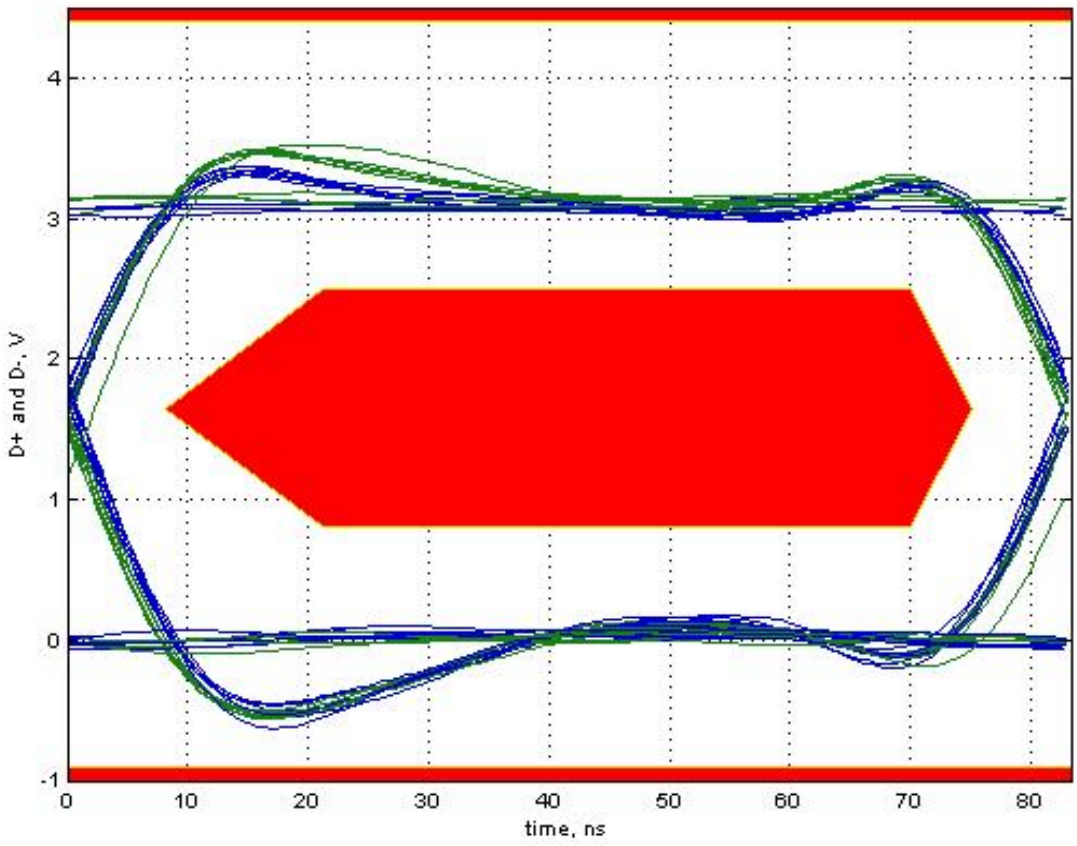
■TRIGGER CONDITION(S)

Operating the VCC supply voltage at the low end of the chip's specification (under 3.3 V) may cause a mismatch in the rising to falling rate.

■SCOPE OF IMPACT

This condition does not affect USB communications but could cause corner case issues with USB lines' rise/fall matching specification. Signal integrity tests were run using the Cypress development kit and excellent eye was observed with supply voltage of 3.15 V.

Figure 21. Eye Diagram



■WORKAROUND

Avoid the trigger condition by using lower tolerance voltage regulators.

■FIX STATUS

This issue will not be corrected in the next new silicon revision.

Document History Page *(continued)*

Document Title: CY7C6431x/CY7C6434x/CY7C6435x, enCoRe™ V Full Speed USB Controller Document Number: 001-12394				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*F	2583853	TYJ / PYRS / HMT	10/10/08	Converted from Preliminary to Final Added operating voltage ranges with USB ADC resolution changed from 10-bit to 8-bit Rephrased battery monitoring clause in page 1 to include “with external components” Included ADC specifications table Included Voh7, Voh8, Voh9, Voh10 specs Flash data retention – condition added to Note [11] Input leakage spec changed to 25 nA max Under AC Char, Frequency accuracy of ILO corrected GPIO rise time for ports 0,1 and ports 2,3 made common AC Programming specifications updated Included AC Programming cycle timing diagram AC SPI specification updated Spec change for 32-QFN package Input Leakage Current maximum value changed to 1 μA Updated V_{OHV} parameter in Table 13 Updated thermal impedances for the packages Update Development Tools, add Designing with PSoC Designer. Edit, fix links and table format. Update TMs.
*G	2653717	DVJA / PYRS	02/04/09	Updated Features, Functional Overview, Development Tools, and Designing with PSoC Designer sections with edits. Removed ‘GUI - graphical user interface’ from Document Conventions acronym table. Removed ‘O - Only a read/write register or bits’ in Table 4 Edited Table 8: removed 10-bit resolution information and corrected units column. Added package handling section Added 8K part ‘CY7C64343-32LQXC’ to Ordering Information.
*H	2714694	DVJA / AESA	06/04/2009	Updated Block Diagram. Added Full Speed USB, 10-bit ADC, SPI, and I2C Slave sections. ADC Resolution changed from 8-bit to 10-bit Updated Table 9 DC Chip Level Specs Updated Table10 DC Char - USB Interface Updated Table 12 DC POR and LDV Specs Changed operating temperature from Commercial to Industrial Changed Temperature Range to Industrial: –40 to 85°C Figure 9: Changed minimum CPU Frequency from 750 kHz to 5.7 MHz Table 14: Removed “Maximum” from the F_{CPU} description Ordering Information: Replaced ‘C’ with ‘I’ in all part numbers to denote Industrial Temp Range
*I	2764460	DVJA / AESA	09/16/2009	Changed Table 12: ADC Specs Added F_{32K2} (Untrimmed) spec to Table 16: AC Chip level Specs Changed T_{RAMP} spec to SR_{POWER_UP} in Table 16: AC Chip Level Specs Added Table 27: Typical Package Capacitance on Crystal Pins
*J	2811903	DVJA	11/20/2009	Added USB-IF TID number in Features on page 1. Added Note 5 on page 18. Changed V_{IHP} in Table 12 on page 22.

Document History Page *(continued)*

Document Title: CY7C6431x/CY7C6434x/CY7C6435x, enCoRe™ V Full Speed USB Controller Document Number: 001-12394				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*S	4578605	GINS	12/11/2014	Updated Pin Information: Updated 32-pin part pinout: Updated Figure 7 (No change in figure, included CY7C64346 in figure caption). Updated Package Diagrams: spec 001-09116 – Changed revision from *I to *J. Updated Ordering Information: Updated Table 25: Updated part numbers.
*T	5548557	ANKC	12/12/2016	Updated Cypress Logo, Sales Page and Disclaimer. Updated Figure 20 (spec 001-13191 *G to *H) in Package Diagrams. Removed the following obsolete part numbers (Table 26) in Ordering Information: CY7C64343-32LQXI, CY7C64343-32LQXIT, CY7C64345-32LQXI, CY7C64345-32LQXIT, CY7C64356-48LTXI, CY7C64356-48LTXIT.

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