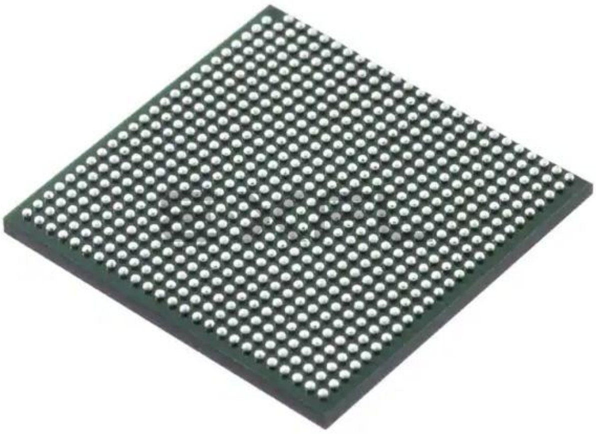

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-A9 |
| Number of Cores/Bus Width | 4 Core, 32-Bit |
| Speed | 800MHz |
| Co-Processors/DSP | Multimedia; NEON™ SIMD |
| RAM Controllers | LPDDR2, DDR3L, DDR3 |
| Graphics Acceleration | Yes |
| Display & Interface Controllers | HDMI, Keypad, LCD, LVDS, MIPI/DSI, Parallel |
| Ethernet | 10/100/1000Mbps (1) |
| SATA | SATA 3Gbps (1) |
| USB | USB 2.0 + PHY (3), USB 2.0 OTG + PHY (1) |
| Voltage - I/O | 1.8V, 2.5V, 2.8V, 3.3V |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Security Features | ARM TZ, A-HAB, CAAM, CSU, SJC, SNVS |
| Package / Case | 624-FBGA, FCBGA |
| Supplier Device Package | 624-FCBGA (21x21) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6qp7cvt8ab |

The i.MX 6DualPlus/6QuadPlus processors offers numerous advanced features, such as:

- Multilevel memory system—The multilevel memory system of each processor is based on the L1 instruction and data caches, L2 cache, and internal and external memory. The processors support many types of external memory devices, including DDR3, DDR3L, LPDDR2, NOR Flash, PSRAM, cellular RAM, NAND Flash (MLC and SLC), OneNAND™, and managed NAND, including eMMC up to rev 4.4/4.41.
- Smart speed technology—The processors have power management throughout the device that enables the rich suite of multimedia features and peripherals to consume minimum power in both active and various low power modes. Smart speed technology enables the designer to deliver a feature-rich product, requiring levels of power far lower than industry expectations.
- Dynamic voltage and frequency scaling—The processors improve the power efficiency of devices by scaling the voltage and frequency to optimize performance.
- Multimedia powerhouse—The multimedia performance of each processor is enhanced by a multilevel cache system, Neon® MPE (Media Processor Engine) co-processor, a multi-standard hardware video codec, 2 autonomous and independent image processing units (IPU), and a programmable smart DMA (SDMA) controller.
- Powerful graphics acceleration—Each processor provides three independent, integrated graphics processing units: an OpenGL® ES 3.0 3D graphics accelerator with four shaders (up to 198 MTri/s and OpenCL support), 2D graphics accelerator, and dedicated OpenVG™ 1.1 accelerator.
- Interface flexibility—Each processor supports connections to a variety of interfaces: LCD controller for up to four displays (including parallel display, HDMI1.4, MIPI display, and LVDS display), dual CMOS sensor interface (parallel or through MIPI), high-speed USB on-the-go with PHY, high-speed USB host with PHY, multiple expansion card ports (high-speed MMC/SDIO host and other), 10/100/1000 Mbps Gigabit Ethernet controller, and a variety of other popular interfaces (such as UART, $I^2C$, and $I^2S$ serial audio, SATA-II, and PCIe-II).
- Advanced security—The processors deliver hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, secure boot, and secure software downloads. The security features are discussed in detail in the i.MX 6Dual/6Quad security reference manual (IMX6DQ6SDLSRM).
- Integrated power management—The processors integrate linear regulators and internally generate voltage levels for different domains. This significantly simplifies system power management structure.

## 1.1 Ordering Information

Table 1 shows examples of orderable part numbers covered by this data sheet. This table does not include all possible orderable part numbers. The latest part numbers are available on nxp.com/imx6series. If your desired part number is not listed in the table, or you have questions about available parts, see nxp.com/imx6series or contact your NXP representative.

**Table 1. Example Orderable Part Numbers**

| Part Number | Quad/Dual | CPU Options | Speed[1] | Temperature Grade | Package |
|---|---|---|---|---|---|
| MCIMX6DP7CVT8AA | i.MX 6DualPlus | VPU, GPU | 800 MHz | Industrial | 21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded) |
| MCIMX6DP7CVT8AB | i.MX 6DualPlus | VPU, GPU | 800 MHz | Industrial | 21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded) |
| MCIMX6QP7CVT8AA | i.MX 6QuadPlus | VPU, GPU | 800 MHz | Industrial | 21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded) |
| MCIMX6QP7CVT8AB | i.MX 6QuadPlus | VPU, GPU | 800 MHz | Industrial | 21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded) |

[1] For 800 MHz speed grade: If a 24 MHz input clock is used (required for USB), the maximum speed is limited to 792 MHz.

Figure 1 describes the part number nomenclature to identify the characteristics of the specific part number you have (for example, cores, frequency, temperature grade, fuse options, silicon revision). Figure 1 applies to the i.MX 6DualPlus/6QuadPlus.

The two characteristics that identify which data sheet a specific part applies to are the part number series field and the temperature grade (junction) field:

- The i.MX 6DualPlus/6QuadPlus Automotive Applications Processors data sheet (IMX6DQPAEC) covers parts listed for the “Plus” series and with “A” indicating automotive temperature.
- The i.MX 6DualPlus/6QuadPlus Applications Processors for Consumer Products data sheet (IMX6DQPCEC) covers parts listed with “D (Commercial temp)” or “E (Extended Commercial temp)”
- The i.MX 6DualPlus/6QuadPlus Applications Processors for Industrial Products data sheet (IMX6DQPIEC) covers parts listed with “C (Industrial temp)”

Ensure that you have the right data sheet for your specific part by checking the fields: Part # Series (DP/QP), temperature grade (junction) (A), and Frequency (8).

### 4.9.3.1 EIM Interface Pads Allocation

EIM supports 32-bit, 16-bit and 8-bit devices operating in address/data separate or multiplexed modes. Table 36 provides EIM interface pads allocation in different modes.

**Table 36. EIM Internal Module Multiplexing[1]**

| Setup | Non Multiplexed Address/Data Mode | | | | | | | Multiplexed Address/Data mode | |
|---|---|---|---|---|---|---|---|---|---|
| | 8 Bit | | | | 16 Bit | | 32 Bit | 16 Bit | 32 Bit |
| | MUM = 0, DSZ = 100 | MUM = 0, DSZ = 101 | MUM = 0, DSZ = 110 | MUM = 0, DSZ = 111 | MUM = 0, DSZ = 001 | MUM = 0, DSZ = 010 | MUM = 0, DSZ = 011 | MUM = 1, DSZ = 001 | MUM = 1, DSZ = 011 |
| EIM_ADDR [15:00] | EIM_AD [15:00] | EIM_AD [15:00] | EIM_AD [15:00] | EIM_AD [15:00] | EIM_AD [15:00] | EIM_AD [15:00] | EIM_AD [15:00] | EIM_AD [15:00] | EIM_AD [15:00] |
| EIM_ADDR [25:16] | EIM_ADDR [25:16] | EIM_ADDR [25:16] | EIM_ADDR [25:16] | EIM_ADDR [25:16] | EIM_ADDR [25:16] | EIM_ADDR [25:16] | EIM_ADDR [25:16] | EIM_ADDR [25:16] | EIM_DATA [09:00] |
| EIM_DATA [07:00], EIM_EB0_B | EIM_DATA [07:00] | — | — | — | EIM_DATA [07:00] | — | EIM_DATA [07:00] | EIM_AD [07:00] | EIM_AD [07:00] |
| EIM_DATA [15:08], EIM_EB1_B | — | EIM_DATA [15:08] | — | — | EIM_DATA [15:08] | — | EIM_DATA [15:08] | EIM_AD [15:08] | EIM_AD [15:08] |
| EIM_DATA [23:16], EIM_EB2_B | — | — | EIM_DATA [23:16] | — | — | EIM_DATA [23:16] | EIM_DATA [23:16] | — | EIM_DATA [07:00] |
| EIM_DATA [31:24], EIM_EB3_B | — | — | — | EIM_DATA [31:24] | — | EIM_DATA [31:24] | EIM_DATA [31:24] | — | EIM_DATA [15:08] |

[1] For more information on configuration ports mentioned in this table, see the i.MX 6DualPlus/6QuadPlus reference manual (IMX6DQPRM).

Figure 12 to Figure 15 provide few examples of basic EIM accesses to external memory devices with the timing parameters mentioned previously for specific control parameters settings.

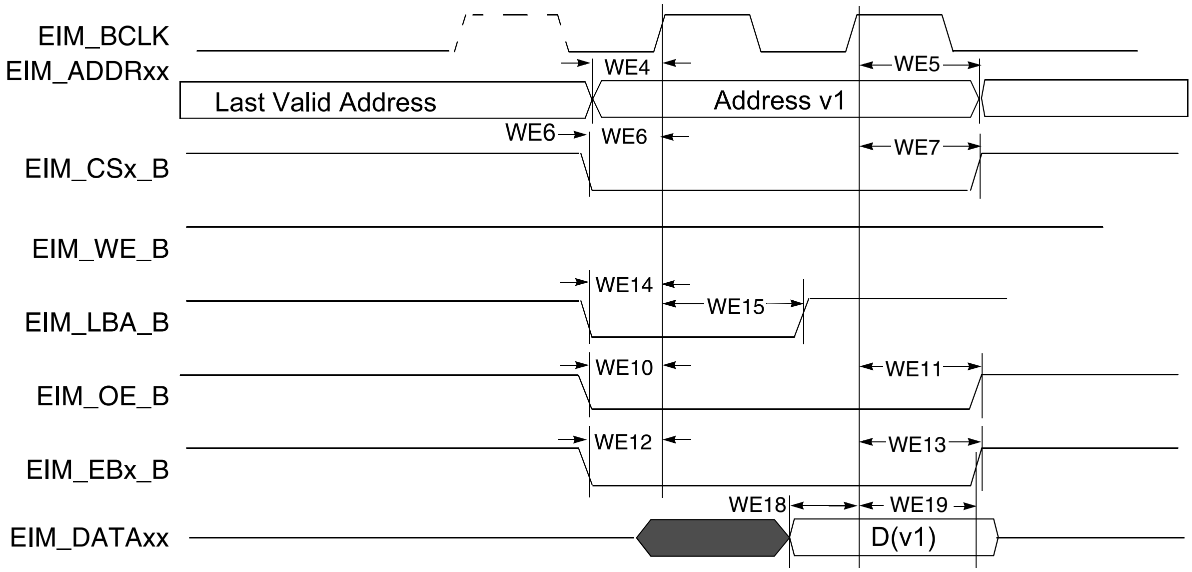



**Figure 12. Synchronous Memory Read Access, WSC=1**

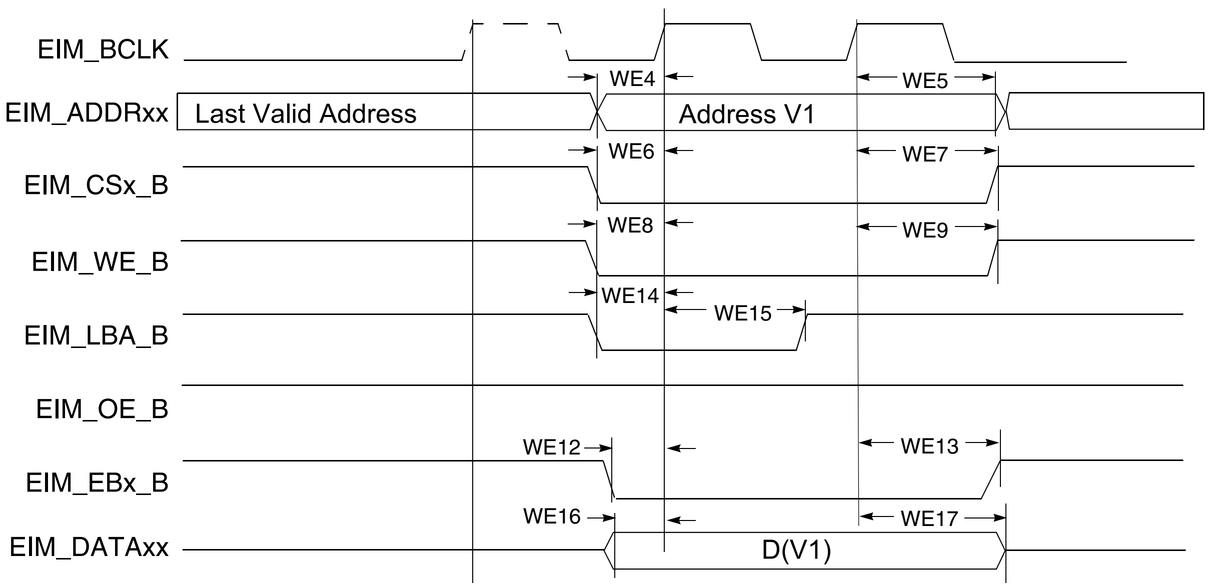



**Figure 13. Synchronous Memory, Write Access, WSC=1, WBEA=0 and WADVN=0**

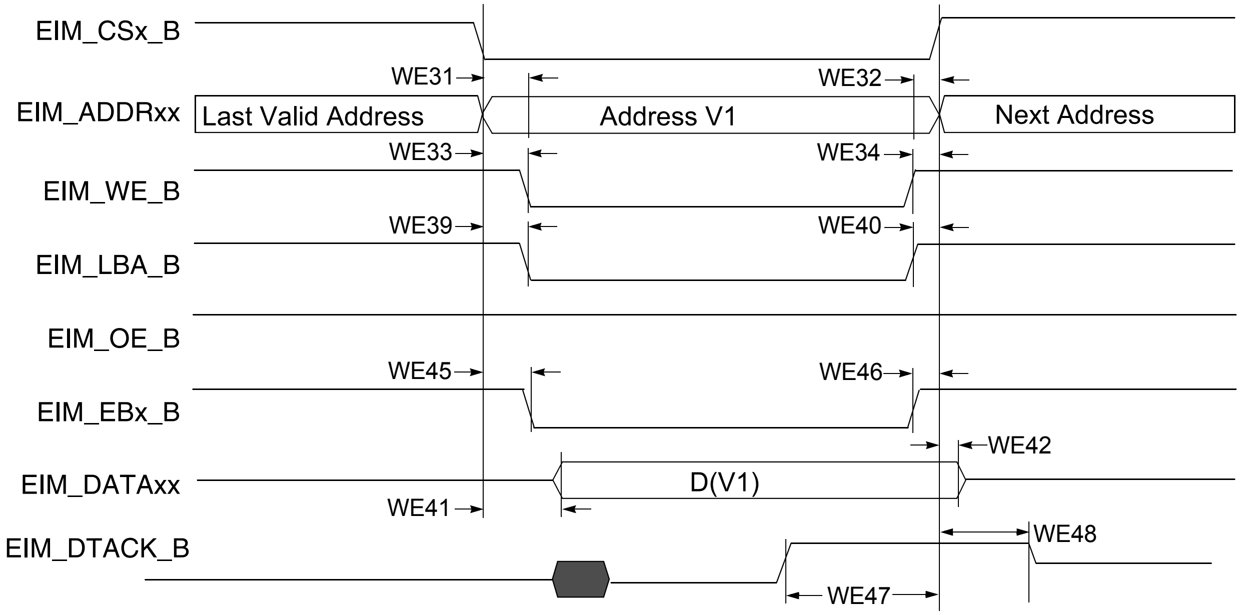



**Figure 21. DTACK Mode Write Access (DAP=0)**

**Table 38. EIM Asynchronous Timing Parameters Relative to Chip Select[1, 2]**

| Ref No. | Parameter | Determination by Synchronous measured parameters | Min | Max | Unit |
|---|---|---|---|---|---|
| WE31 | EIM_CSx_B valid to Address Valid | WE4-WE6-CSA×t | -3.5-CSA×t | 3.5-CSA×t | ns |
| WE32 | Address Invalid to EIM_CSx_B Invalid | WE7-WE5-CSN×t | -3.5-CSN×t | 3.5-CSN×t | ns |
| WE32A (muxed A/D) | EIM_CSx_B valid to Address Invalid | t+WE4-WE7+ (ADVN+ADVA+1-CSA)×t | t - 3.5+(ADVN+ADVA+1-CSA)×t | t + 3.5+(ADVN+ADVA+ 1-CSA)×t | ns |
| WE33 | EIM_CSx_B Valid to EIM_WE_B Valid | WE8-WE6+(WEA-WCSA)×t | -3.5+(WEA-WCSA)×t | 3.5+(WEA-WCSA)×t | ns |
| WE34 | EIM_WE_B Invalid to EIM_CSx_B Invalid | WE7-WE9+(WEN-WCSN)×t | -3.5+(WEN-WCSN)×t | 3.5+(WEN-WCSN)×t | ns |
| WE35 | EIM_CSx_B Valid to EIM_OE_B Valid | WE10- WE6+(OEA-RCSA)×t | -3.5+(OEA-RCSA)×t | 3.5+(OEA-RCSA)×t | ns |
| WE35A (muxed A/D) | EIM_CSx_B Valid to EIM_OE_B Valid | WE10-WE6+(OEA+RADVN+RADVA+ADH+1-RCSA)×t | -3.5+(OEA+RADVN+RADVA+ADH +1-RCSA)×t | 3.5+(OEA+RADVN+RADVA+ADH+1-RCSA)×t | ns |
| WE36 | EIM_OE_B Invalid to EIM_CSx_B Invalid | WE7-WE11+(OEN-RCSN)×t | -3.5+(OEN-RCSN)×t | 3.5+(OEN-RCSN)×t | ns |
| WE37 | EIM_CSx_B Valid to EIM_EBx_B Valid (Read access) | WE12-WE6+(RBEA-RCSA)× t | -3.5+(RBEA- RCSA)×t | 3.5+(RBEA - RCSA)×t | ns |
| WE38 | EIM_EBx_B Invalid to EIM_CSx_B Invalid (Read access) | WE7-WE13+(RBEN-RCSN)×t | -3.5+ (RBEN-RCSN)×t | 3.5+(RBEN-RCSN)×t | ns |
| WE39 | EIM_CSx_B Valid to EIM_LBA_B Valid | WE14-WE6+(ADVA-CSA)×t | -3.5+ (ADVA-CSA)×t | 3.5+(ADVA-CSA)×t | ns |

### 4.11.1 Asynchronous Mode AC Timing (ONFI 1.0 Compatible)

Asynchronous mode AC timings are provided as multiplications of the clock cycle and fixed delay. The Maximum I/O speed of GPMI in Asynchronous mode is about 50 MB/s. Figure 22 through Figure 25 depict the relative timing between GPMI signals at the module level for different operations under Asynchronous mode. Table 40 describes the timing parameters (NF1–NF17) that are shown in the figures.

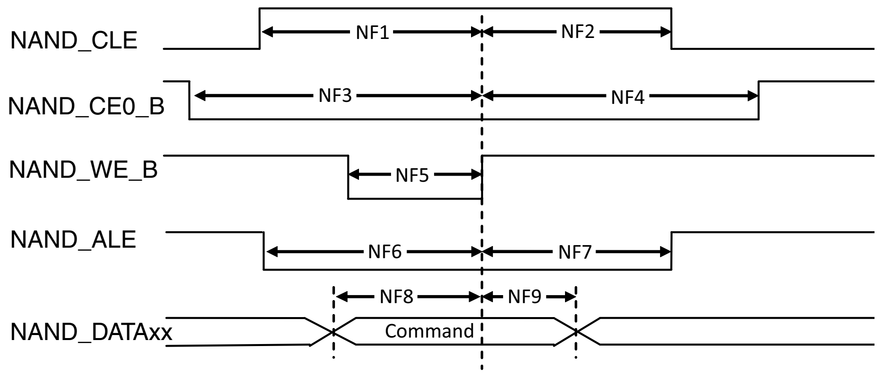



**Figure 22. Command Latch Cycle Timing Diagram**

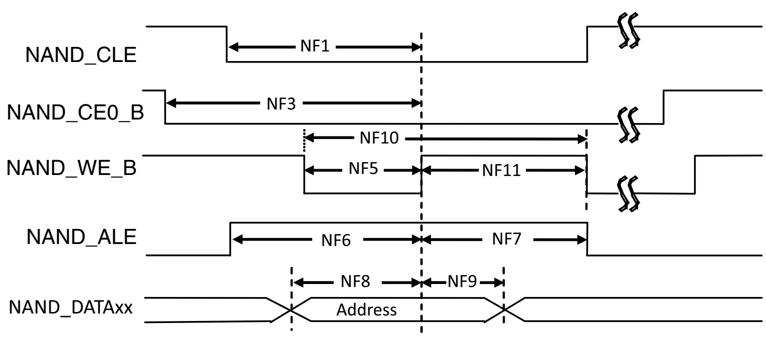



**Figure 23. Address Latch Cycle Timing Diagram**

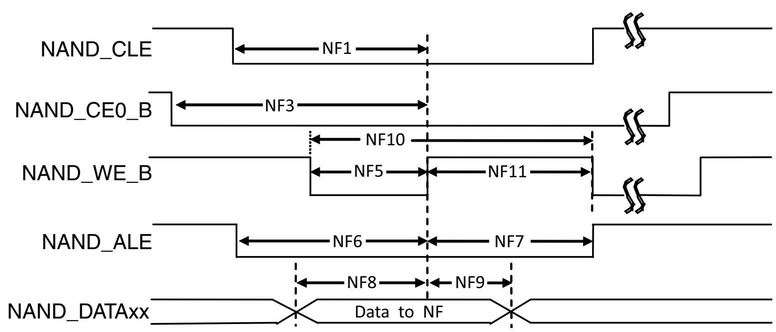



**Figure 24. Write Data Latch Cycle Timing Diagram**

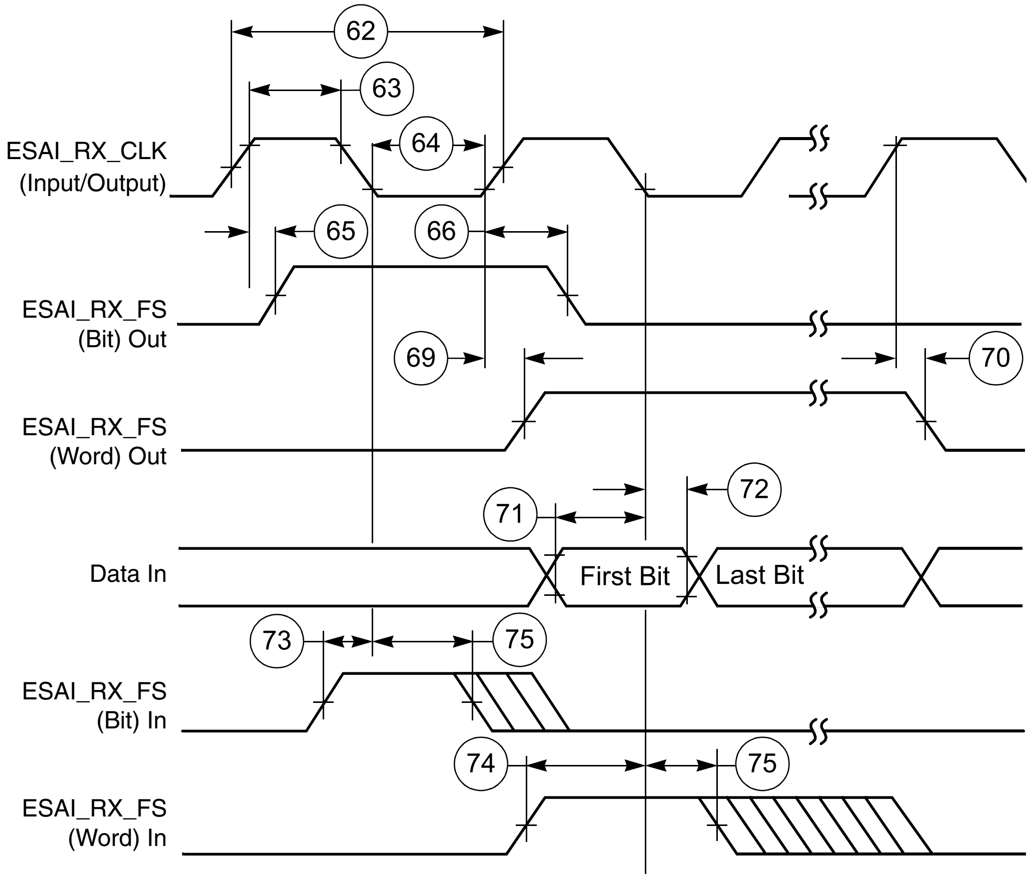



**Figure 36. ESAI Receiver Timing**

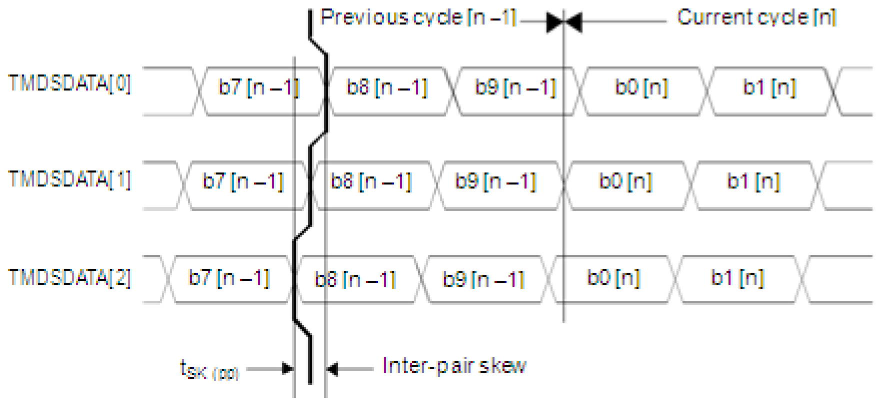



**Figure 54. Inter-Pair Skew Definition**

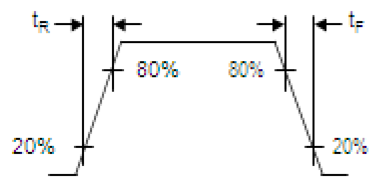



**Figure 55. TMDS Output Signals Rise and Fall Time Definition**

**Table 56. Switching Characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **TMDS Drivers Specifications** | | | | | | |
| — | Maximum serial data rate | — | — | — | 3.4 | Gbps |
| $F_{TMDSCLK}$ | TMDSCLK frequency | On TMDSCLKP/N outputs | 25 | — | 340 | MHz |
| $P_{TMDSCLK}$ | TMDSCLK period | RL = 50 Ω<br>See Figure 51. | 2.94 | — | 40 | ns |
| $t_{CDC}$ | TMDSCLK duty cycle | $t_{CDC} = t_{CPH} / P_{TMDSCLK}$<br>RL = 50 Ω<br>See Figure 51. | 40 | 50 | 60 | % |
| $t_{CPH}$ | TMDSCLK high time | RL = 50 Ω<br>See Figure 51. | 4 | 5 | 6 | UI |
| $t_{CPL}$ | TMDSCLK low time | RL = 50 Ω<br>See Figure 51. | 4 | 5 | 6 | UI |
| — | TMDSCLK jitter[1] | RL = 50 Ω | — | — | 0.25 | UI |
| $t_{SK(p)}$ | Intra-pair (pulse) skew | RL = 50 Ω<br>See Figure 53. | — | — | 0.15 | UI |
| $t_{SK(pp)}$ | Inter-pair skew | RL = 50 Ω<br>See Figure 54. | — | — | 1 | UI |
| $t_R$ | Differential output signal rise time | 20–80%<br>RL = 50 Ω<br>See Figure 55. | 75 | — | 0.4 UI | ps |

### 4.12.10.1 IPU Sensor Interface Signal Mapping

The IPU supports a number of sensor input formats. Table 58 defines the mapping of the Sensor Interface Pins used for various supported interface formats.

**Table 58. Camera Input Signal Cross Reference, Format, and Bits Per Cycle**

| Signal Name[1] | RGB565 8 bits 2 cycles | RGB565[2] 8 bits 3 cycles | RGB666[3] 8 bits 3 cycles | RGB888 8 bits 3 cycles | YCbCr[4] 8 bits 2 cycles | RGB565[5] 16 bits 1 cycle | YCbCr[6] 16 bits 1 cycle | YCbCr[7] 16 bits 1 cycle | YCbCr[8] 20 bits 1 cycle |
|---|---|---|---|---|---|---|---|---|---|
| IPUx_CSIx_ DATA00 | — | — | — | — | — | — | — | 0 | C[0] |
| IPUx_CSIx_ DATA01 | — | — | — | — | — | — | — | 0 | C[1] |
| IPUx_CSIx_ DATA02 | — | — | — | — | — | — | — | C[0] | C[2] |
| IPUx_CSIx_ DATA03 | — | — | — | — | — | — | — | C[1] | C[3] |
| IPUx_CSIx_ DATA04 | — | — | — | — | — | B[0] | C[0] | C[2] | C[4] |
| IPU2_CSIx_ DATA_05 | — | — | — | — | — | B[1] | C[1] | C[3] | C[5] |
| IPUx_CSIx_ DATA06 | — | — | — | — | — | B[2] | C[2] | C[4] | C[6] |
| IPUx_CSIx_ DATA07 | — | — | — | — | — | B[3] | C[3] | C[5] | C[7] |
| IPUx_CSIx_ DATA08 | — | — | — | — | — | B[4] | C[4] | C[6] | C[8] |
| IPUx_CSIx_ DATA09 | — | — | — | — | — | G[0] | C[5] | C[7] | C[9] |
| IPUx_CSIx_ DATA10 | — | — | — | — | — | G[1] | C[6] | 0 | Y[0] |
| IPUx_CSIx_ DATA11 | — | — | — | — | — | G[2] | C[7] | 0 | Y[1] |
| IPUx_CSIx_ DATA12 | B[0], G[3] | R[2],G[4],B[2] | R/G/B[4] | R/G/B[0] | Y/C[0] | G[3] | Y[0] | Y[0] | Y[2] |
| IPUx_CSIx_ DATA13 | B[1], G[4] | R[3],G[5],B[3] | R/G/B[5] | R/G/B[1] | Y/C[1] | G[4] | Y[1] | Y[1] | Y[3] |
| IPUx_CSIx_ DATA14 | B[2], G[5] | R[4],G[0],B[4] | R/G/B[0] | R/G/B[2] | Y/C[2] | G[5] | Y[2] | Y[2] | Y[4] |
| IPUx_CSIx_ DATA15 | B[3], R[0] | R[0],G[1],B[0] | R/G/B[1] | R/G/B[3] | Y/C[3] | R[0] | Y[3] | Y[3] | Y[5] |
| IPUx_CSIx_ DATA16 | B[4], R[1] | R[1],G[2],B[1] | R/G/B[2] | R/G/B[4] | Y/C[4] | R[1] | Y[4] | Y[4] | Y[6] |
| IPUx_CSIx_ DATA17 | G[0], R[2] | R[2],G[3],B[2] | R/G/B[3] | R/G/B[5] | Y/C[5] | R[2] | Y[5] | Y[5] | Y[7] |
| IPUx_CSIx_ DATA18 | G[1], R[3] | R[3],G[4],B[3] | R/G/B[4] | R/G/B[6] | Y/C[6] | R[3] | Y[6] | Y[6] | Y[8] |
| IPUx_CSIx_ DATA19 | G[2], R[4] | R[4],G[5],B[4] | R/G/B[5] | R/G/B[7] | Y/C[7] | R[4] | Y[7] | Y[7] | Y[9] |

[1] IPU2_CSIx stands for IPU2_CSI1 or IPU2_CSI2.

There are special physical outputs to provide synchronous controls:

- The ipp_disp_clk is a dedicated base synchronous signal that is used to generate a base display (component, pixel) clock for a display.
- The ipp_pin_1– ipp_pin_7 are general purpose synchronous pins, that can be used to provide HSYNC, VSYNC, DRDY or any else independent signal to a display.

The IPU has a system of internal binding counters for internal events (such as, HSYNC/VSYNC) calculation. The internal event (local start point) is synchronized with internal DI_CLK. A suitable control starts from the local start point with predefined UP and DOWN values to calculate control's changing points with half DI_CLK resolution. A full description of the counter system can be found in the IPU chapter of the i.MX 6DualPlus/6QuadPlus reference manual (IMX6DQPRM).

#### 4.12.10.5.2 Asynchronous Controls

The asynchronous control is a data-oriented signal that changes its value with an output data according to additional internal flags coming with the data.

There are special physical outputs to provide asynchronous controls, as follows:

- The ipp_d0_cs and ipp_d1_cs pins are dedicated to provide chip select signals to two displays.
- The ipp_pin_11– ipp_pin_17 are general purpose asynchronous pins, that can be used to provide WR. RD, RS or any other data-oriented signal to display.

**NOTE**

The IPU has independent signal generators for asynchronous signals toggling. When a DI decides to put a new asynchronous data on the bus, a new internal start (local start point) is generated. The signal generators calculate predefined UP and DOWN values to change pins states with half DI_CLK resolution.

### 4.12.10.6 Synchronous Interfaces to Standard Active Matrix TFT LCD Panels

#### 4.12.10.6.1 IPU Display Operating Signals

The IPU uses four control signals and data to operate a standard synchronous interface:

- IPP_DISP_CLK—Clock to display
- HSYNC—Horizontal synchronization
- VSYNC—Vertical synchronization
- DRDY—Active data

All synchronous display controls are generated on the base of an internally generated "local start point". The synchronous display controls can be placed on time axis with DI's offset, up and down parameters. The display access can be whole number of DI clock (Tdiclk) only. The IPP_DATA can not be moved relative to the local start point. The data bus of the synchronous interface is output direction only.

Table 61 shows timing characteristics of signals presented in Figure 61 and Figure 62.

**Table 61. Synchronous Display Interface Timing Characteristics (Pixel Level)**

| ID | Parameter | Symbol | Value | Description | Unit |
|---|---|---|---|---|---|
| IP5 | Display interface clock period | Tdicp | (see[1]) | Display interface clock IPP_DISP_CLK | ns |
| IP6 | Display pixel clock period | Tdpcp | DISP_CLK_PER_PIXEL × Tdicp | Time of translation of one pixel to display, DISP_CLK_PER_PIXEL—number of pixel components in one pixel (1.***n***).<br>The DISP_CLK_PER_PIXEL is virtual parameter to define display pixel clock period.<br>The DISP_CLK_PER_PIXEL is received by DC/DI one access division to ***n*** components. | ns |
| IP7 | Screen width time | Tsw | (SCREEN_WIDTH) × Tdicp | SCREEN_WIDTH—screen width in, interface clocks. horizontal blanking included.<br>The SCREEN_WIDTH should be built by suitable DI's counter[2]. | ns |
| IP8 | HSYNC width time | Thsw | (HSYNC_WIDTH) | HSYNC_WIDTH—Hsync width in DI_CLK with 0.5 DI_CLK resolution. Defined by DI's counter. | ns |
| IP9 | Horizontal blank interval 1 | Thbi1 | BGXP × Tdicp | BGXP—width of a horizontal blanking before a first active data in a line (in interface clocks). The BGXP should be built by suitable DI's counter. | ns |
| IP10 | Horizontal blank interval 2 | Thbi2 | (SCREEN_WIDTH – BGXP – FW) × Tdicp | Width a horizontal blanking after a last active data in a line (in interface clocks)<br>FW—with of active line in interface clocks. The FW should be built by suitable DI's counter. | ns |
| IP12 | Screen height | Tsh | (SCREEN_HEIGHT) × Tsw | SCREEN_HEIGHT— screen height in lines with blanking.<br>The SCREEN_HEIGHT is a distance between 2 VSYNCs.<br>The SCREEN_HEIGHT should be built by suitable DI's counter. | ns |
| IP13 | VSYNC width | Tvsw | VSYNC_WIDTH | VSYNC_WIDTH—Vsync width in DI_CLK with 0.5 DI_CLK resolution. Defined by DI's counter. | ns |
| IP14 | Vertical blank interval 1 | Tvbi1 | BGYP × Tsw | BGYP—width of first Vertical blanking interval in line. The BGYP should be built by suitable DI's counter. | ns |
| IP15 | Vertical blank interval 2 | Tvbi2 | (SCREEN_HEIGHT – BGYP – FH) × Tsw | Width of second vertical blanking interval in line. The FH should be built by suitable DI's counter. | ns |

**Table 61. Synchronous Display Interface Timing Characteristics (Pixel Level) (continued)**

| ID | Parameter | Symbol | Value | Description | Unit |
|---|---|---|---|---|---|
| IP5o | Offset of IPP_DISP_CLK | Todicp | DISP_CLK_OFFSET × Tdiclk | DISP_CLK_OFFSET—offset of IPP_DISP_CLK edges from local start point, in DI_CLK×2 (0.5 DI_CLK Resolution). Defined by DISP_CLK counter. | ns |
| IP13o | Offset of VSYNC | Tovs | VSYNC_OFFSET × Tdiclk | VSYNC_OFFSET—offset of Vsync edges from a local start point, when a Vsync should be active, in DI_CLK×2 (0.5 DI_CLK Resolution). The VSYNC_OFFSET should be built by suitable DI's counter. | ns |
| IP8o | Offset of HSYNC | Tohs | HSYNC_OFFSET × Tdiclk | HSYNC_OFFSET—offset of Hsync edges from a local start point, when a Hsync should be active, in DI_CLK×2 (0.5 DI_CLK Resolution). The HSYNC_OFFSET should be built by suitable DI's counter. | ns |
| IP9o | Offset of DRDY | Todrdy | DRDY_OFFSET × Tdiclk | DRDY_OFFSET—offset of DRDY edges from a suitable local start point, when a corresponding data has been set on the bus, in DI_CLK×2 (0.5 DI_CLK Resolution). The DRDY_OFFSET should be built by suitable DI's counter. | ns |

[1] Display interface clock period immediate value.

$$\mathrm{Tdicp} = \begin{cases} T_{\mathrm{diclk}} \times \dfrac{\mathrm{DISP\_CLK\_PERIOD}}{\mathrm{DI\_CLK\_PERIOD}}, & \text{for integer } \dfrac{\mathrm{DISP\_CLK\_PERIOD}}{\mathrm{DI\_CLK\_PERIOD}} \\ T_{\mathrm{diclk}}\left(\mathrm{floor}\left[\dfrac{\mathrm{DISP\_CLK\_PERIOD}}{\mathrm{DI\_CLK\_PERIOD}}\right] + 0.5 \pm 0.5\right), & \text{for fractional } \dfrac{\mathrm{DISP\_CLK\_PERIOD}}{\mathrm{DI\_CLK\_PERIOD}} \end{cases}$$

DISP_CLK_PERIOD—number of DI_CLK per one Tdicp. Resolution 1/16 of DI_CLK.
DI_CLK_PERIOD—relation of between programing clock frequency and current system clock frequency
Display interface clock period average value.

$$\bar{T}\mathrm{dicp} = T_{\mathrm{diclk}} \times \frac{\mathrm{DISP\_CLK\_PERIOD}}{\mathrm{DI\_CLK\_PERIOD}}$$

[2] DI's counter can define offset, period and UP/DOWN characteristic of output signal according to programed parameters of the counter. Same of parameters in the table are not defined by DI's registers directly (by name), but can be generated by corresponding DI's counter. The SCREEN_WIDTH is an input value for DI's HSYNC generation counter. The distance between HSYNCs is a SCREEN_WIDTH.

The maximum accuracy of UP/DOWN edge of controls is:

$$\mathrm{Accuracy} = (0.5 \times T_{\mathrm{diclk}}) \pm 0.62\mathrm{ns}$$

The maximum accuracy of UP/DOWN edge of IPP_DISP_DATA is:

$$\mathrm{Accuracy} = T_{\mathrm{diclk}} \pm 0.62\mathrm{ns}$$

The DISP_CLK_PERIOD, DI_CLK_PERIOD parameters are register-controlled.

### 4.12.16 SATA PHY Parameters

This section describes SATA PHY electrical specifications.

#### 4.12.16.1 Transmitter and Receiver Characteristics

The SATA PHY meets or exceeds the electrical compliance requirements defined in the SATA specifications.

**NOTE**

The tables in the following sections indicate any exceptions to the SATA specification or aspects of the SATA PHY that exceed the standard, as well as provide information about parameters not defined in the standard.

The following subsections provide values obtained from a combination of simulations and silicon characterization.

##### 4.12.16.1.1 SATA PHY Transmitter Characteristics

Table 68 provides specifications for SATA PHY transmitter characteristics.

**Table 68. SATA PHY Transmitter Characteristics**

| Parameters | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Transmit common mode voltage | $V_{CTM}$ | 0.4 | — | 0.6 | V |
| Transmitter pre-emphasis accuracy (measured change in de-emphasized bit) | — | –0.5 | — | 0.5 | dB |

##### 4.12.16.1.2 SATA PHY Receiver Characteristics

Table 69 provides specifications for SATA PHY receiver characteristics.

**Table 69. SATA PHY Receiver Characteristics**

| Parameters | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Minimum Rx eye height (differential peak-to-peak) | $V_{MIN\_RX\_EYE\_HEIGHT}$ | 175 | — | — | mV |
| Tolerance | PPM | –400 | — | 400 | ppm |

#### 4.12.16.2 SATA_REXT Reference Resistor Connection

The impedance calibration process requires connection of reference resistor 191 Ω. 1% precision resistor on SATA_REXT pad to ground.

Resistor calibration consists of learning which state of the internal Resistor Calibration register causes an internal, digitally trimmed calibration resistor to best match the impedance applied to the SATA_REXT pin. The calibration register value is then supplied to all Tx and Rx termination resistors.

During the calibration process (for a few tens of microseconds), up to 0.3 mW can be dissipated in the external SATA_REXT resistor. At other times, no power is dissipated by the SATA_REXT resistor.

**Table 70. JTAG Timing (continued)**

| ID | Parameter[1,2] | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| SJ9 | JTAG_TMS, JTAG_TDI data hold time | 25 | — | ns |
| SJ10 | JTAG_TCK low to JTAG_TDO data valid | — | 44 | ns |
| SJ11 | JTAG_TCK low to JTAG_TDO high impedance | — | 44 | ns |
| SJ12 | JTAG_TRST_B assert time | 100 | — | ns |
| SJ13 | JTAG_TRST_B set-up time to JTAG_TCK low | 40 | — | ns |

1 $T_{DC}$ = target frequency of SJC
2 $V_M$ = mid-point voltage

### 4.12.18 SPDIF Timing Parameters

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

Table 71 and Figure 84 and Figure 85 show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SPDIF_SR_CLK) for SPDIF in Rx mode and the timing of the modulating Tx clock (SPDIF_ST_CLK) for SPDIF in Tx mode.

**Table 71. SPDIF Timing Parameters**

| Parameter | Symbol | Timing Parameter Range | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| SPDIF_IN Skew: asynchronous inputs, no specs apply | — | — | 0.7 | ns |
| SPDIF_OUT output (Load = 50pf)<br>• Skew<br>• Transition rising<br>• Transition falling | <br>—<br>—<br>— | <br>—<br>—<br>— | <br>1.5<br>24.2<br>31.3 | ns |
| SPDIF_OUT output (Load = 30pf)<br>• Skew<br>• Transition rising<br>• Transition falling | <br>—<br>—<br>— | <br>—<br>—<br>— | <br>1.5<br>13.6<br>18.0 | ns |
| Modulating Rx clock (SPDIF_SR_CLK) period | srckp | 40.0 | — | ns |
| SPDIF_SR_CLK high period | srckph | 16.0 | — | ns |
| SPDIF_SR_CLK low period | srckpl | 16.0 | — | ns |
| Modulating Tx clock (SPDIF_ST_CLK) period | stclkp | 40.0 | — | ns |
| SPDIF_ST_CLK high period | stclkph | 16.0 | — | ns |
| SPDIF_ST_CLK low period | stclkpl | 16.0 | — | ns |

### 4.12.19.2 SSI Receiver Timing with Internal Clock

Figure 87 depicts the SSI receiver internal clock timing and Table 74 lists the timing parameters for the receiver timing with the internal clock.

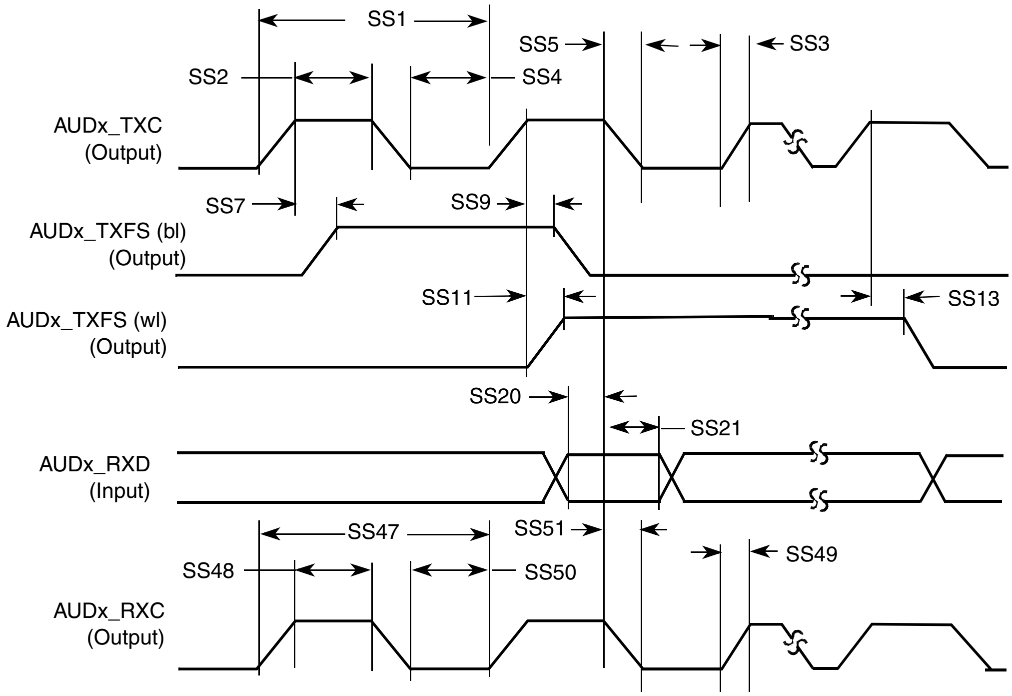



**Figure 87. SSI Receiver Internal Clock Timing Diagram**

**Table 74. SSI Receiver Timing with Internal Clock**

| ID | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| Internal Clock Operation | | | | |
| SS1 | AUDx_TXC/AUDx_RXC clock period | 81.4 | — | ns |
| SS2 | AUDx_TXC/AUDx_RXC clock high period | 36.0 | — | ns |
| SS3 | AUDx_TXC/AUDx_RXC clock rise time | — | 6.0 | ns |
| SS4 | AUDx_TXC/AUDx_RXC clock low period | 36.0 | — | ns |
| SS5 | AUDx_TXC/AUDx_RXC clock fall time | — | 6.0 | ns |
| SS7 | AUDx_RXC high to AUDx_TXFS (bl) high | — | 15.0 | ns |
| SS9 | AUDx_RXC high to AUDx_TXFS (bl) low | — | 15.0 | ns |
| SS11 | AUDx_RXC high to AUDx_TXFS (wl) high | — | 15.0 | ns |
| SS13 | AUDx_RXC high to AUDx_TXFS (wl) low | — | 15.0 | ns |
| SS20 | AUDx_RXD setup time before AUDx_RXC low | 10.0 | — | ns |
| SS21 | AUDx_RXD hold time after AUDx_RXC low | 0.0 | — | ns |

## 4.12.21 USB HSIC Timings

This section describes the electrical information of the USB HSIC port.

**NOTE**

HSIC is a DDR signal. The following timing specification is for both rising and falling edges.

### 4.12.21.1 Transmit Timing

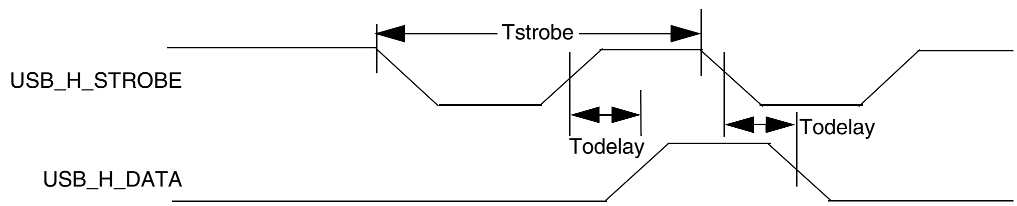



**Figure 94. USB HSIC Transmit Waveform**

**Table 82. USB HSIC Transmit Parameters**

| Name | Parameter | Min | Max | Unit | Comment |
|---|---|---|---|---|---|
| Tstrobe | strobe period | 4.166 | 4.167 | ns | — |
| Todelay | data output delay time | 550 | 1350 | ps | Measured at 50% point |
| Tslew | strobe/data rising/falling time | 0.7 | 2 | V/ns | Averaged from 30% – 70% points |

### 4.12.21.2 Receive Timing

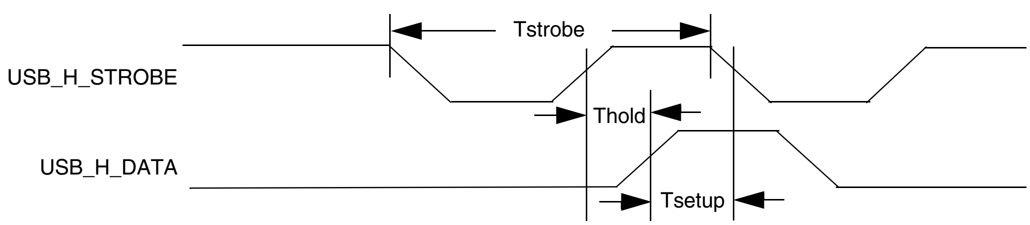



**Figure 95. USB HSIC Receive Waveform**

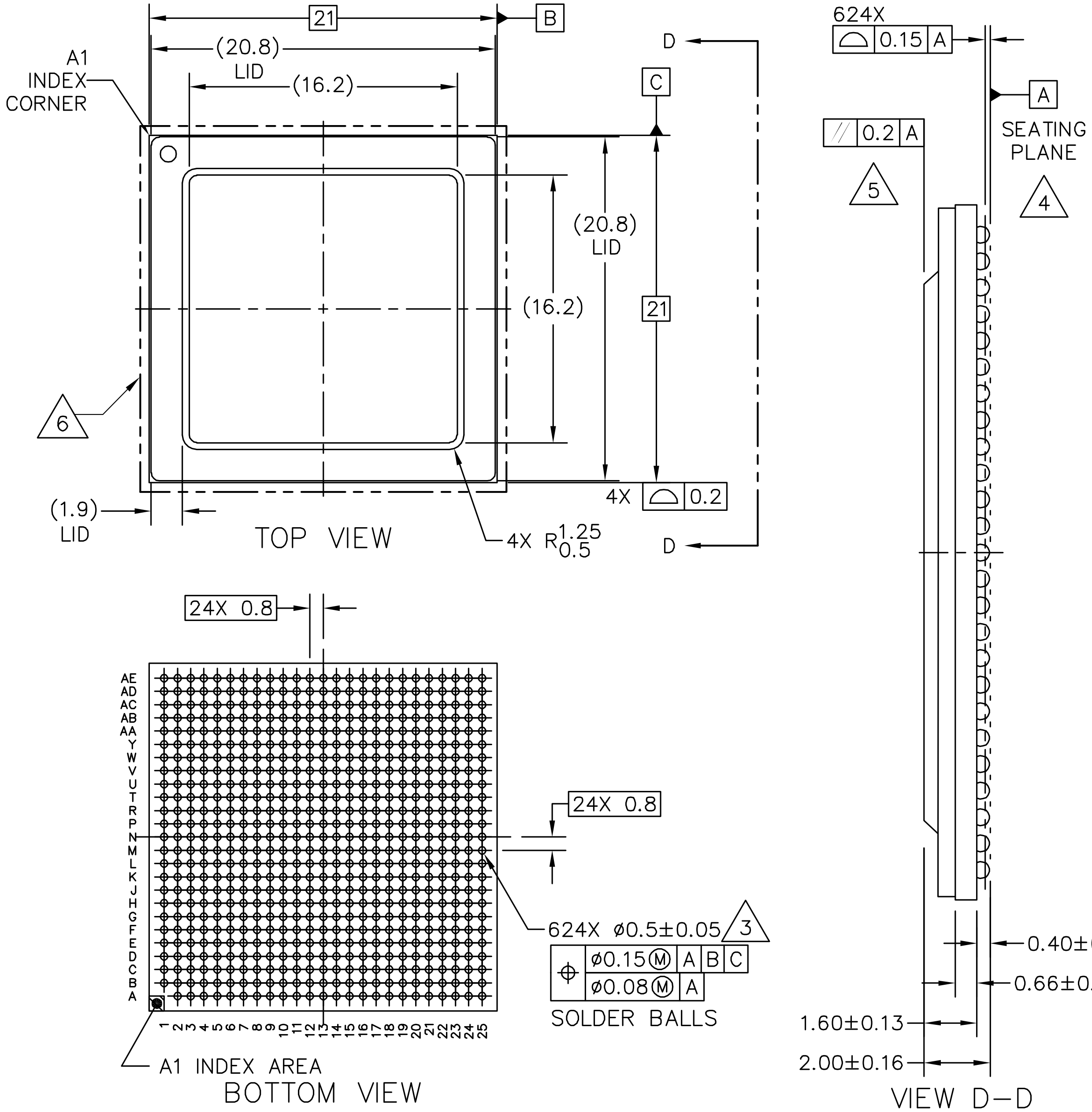
**Table 83. USB HSIC Receive Parameters[1]**

| Name | Parameter | Min | Max | Unit | Comment |
|---|---|---|---|---|---|
| Tstrobe | strobe period | 4.166 | 4.167 | ns | — |
| Thold | data hold time | 300 | — | ps | Measured at 50% point |
| Tsetup | data setup time | 365 | — | ps | Measured at 50% point |
| Tslew | strobe/data rising/falling time | 0.7 | 2 | V/ns | Averaged from 30% – 70% points |

1 The timings in the table are guaranteed when:
—AC I/O voltage is between 0.9x to 1x of the I/O supply
—DDR_SEL configuration bits of the I/O are set to (10)b

### 6.2.1.1 21 x 21 mm Lidded Package

Figure 96 and Figure 97 show the top, bottom, and side views of the 21 × 21 mm lidded package.




| © NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED | MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE |
|---|---|---|
| TITLE: 624 I/O FC PBGA, 21 X 21 X 2 PKG, 0.8 MM PITCH, STAMPED LID | DOCUMENT NO: 98ASA00330D | REV: E |
| | STANDARD: NON–JEDEC | |
| | SOT1643–1 | 07 JAN 2016 |

**Figure 96. 21 x 21 mm Lidded Package Top, Bottom, and Side Views (Sheet 1 of 2)**

**Table 86. 21 x 21 mm Supplies Contact Assignment (continued)**

| Supply Rail Name | Ball(s) Position(s) | Remark |
|---|---|---|
| VDDHIGH_CAP | H10, J10 | Secondary supply for the 2.5 V domain (internal regulator output—requires capacitor if internal regulator is used) |
| VDDHIGH_IN | H9, J9 | Primary supply for the 2.5 V regulator |
| VDDPU_CAP | H17, J17, K17, L17, M17, N17, P17 | Secondary supply for the VPU and GPU (internal regulator output—requires capacitor if internal regulator is used) |
| VDDSOC_CAP | R10, T10, T13, T14, U10, U13, U14 | Secondary supply for the SoC and PU (internal regulator output—requires capacitor if internal regulator is used) |
| VDDSOC_IN | H16, J16, K16, L16, M16, N16, P16, R16, T16, U16 | Primary supply for the SoC and PU regulators |
| VDDUSB_CAP | F9 | Secondary supply for the 3 V domain (internal regulator output—requires capacitor if internal regulator is used) |
| ZQPAD | AE17 | Connect ZQPAD to an external 240Ω 1% resistor to GND. This is a reference used during DRAM output buffer driver calibration. |

## 6.2.3 21 x 21 mm Functional Contact Assignments

Table 87 displays an alpha-sorted list of the signal assignments including power rails. The table also includes out of reset pad state.

**Table 87. 21 x 21 mm Functional Contact Assignments**

| Ball Name | Ball | Power Group | Ball Type | Out of Reset Condition[1] | | | |
|---|---|---|---|---|---|---|---|
| | | | | Default Mode (Reset Mode) | Default Function (Signal Name) | Input/Output | Value[2] |
| BOOT_MODE0 | C12 | VDD_SNVS_IN | GPIO | ALT0 | SRC_BOOT_MODE0 | Input | PD (100K) |
| BOOT_MODE1 | F12 | VDD_SNVS_IN | GPIO | ALT0 | SRC_BOOT_MODE1 | Input | PD (100K) |
| CLK1_N | C7 | VDD_HIGH_CAP | — | — | CLK1_N | — | — |
| CLK1_P | D7 | VDD_HIGH_CAP | — | — | CLK1_P | — | — |
| CLK2_N | C5 | VDD_HIGH_CAP | — | — | CLK2_N | — | — |
| CLK2_P | D5 | VDD_HIGH_CAP | — | — | CLK2_P | — | — |
| CSI_CLK0M | F4 | NVCC_MIPI | — | — | CSI_CLK_N | — | — |
| CSI_CLK0P | F3 | NVCC_MIPI | — | — | CSI_CLK_P | — | — |
| CSI_D0M | E4 | NVCC_MIPI | — | — | CSI_DATA0_N | — | — |
| CSI_D0P | E3 | NVCC_MIPI | — | — | CSI_DATA0_P | — | — |
| CSI_D1M | D1 | NVCC_MIPI | — | — | CSI_DATA1_N | — | — |

**Table 87. 21 x 21 mm Functional Contact Assignments (continued)**

| Ball Name | Ball | Power Group | Ball Type | Out of Reset Condition[1] | | | |
|---|---|---|---|---|---|---|---|
| | | | | Default Mode (Reset Mode) | Default Function (Signal Name) | Input/Output | Value[2] |
| DISP0_DAT14 | U25 | NVCC_LCD | GPIO | ALT5 | GPIO5_IO08 | Input | PU (100K) |
| DISP0_DAT15 | T22 | NVCC_LCD | GPIO | ALT5 | GPIO5_IO09 | Input | PU (100K) |
| DISP0_DAT16 | T21 | NVCC_LCD | GPIO | ALT5 | GPIO5_IO10 | Input | PU (100K) |
| DISP0_DAT17 | U24 | NVCC_LCD | GPIO | ALT5 | GPIO5_IO11 | Input | PU (100K) |
| DISP0_DAT18 | V25 | NVCC_LCD | GPIO | ALT5 | GPIO5_IO12 | Input | PU (100K) |
| DISP0_DAT19 | U23 | NVCC_LCD | GPIO | ALT5 | GPIO5_IO13 | Input | PU (100K) |
| DISP0_DAT2 | P23 | NVCC_LCD | GPIO | ALT5 | GPIO4_IO23 | Input | PU (100K) |
| DISP0_DAT20 | U22 | NVCC_LCD | GPIO | ALT5 | GPIO5_IO14 | Input | PU (100K) |
| DISP0_DAT21 | T20 | NVCC_LCD | GPIO | ALT5 | GPIO5_IO15 | Input | PU (100K) |
| DISP0_DAT22 | V24 | NVCC_LCD | GPIO | ALT5 | GPIO5_IO16 | Input | PU (100K) |
| DISP0_DAT23 | W24 | NVCC_LCD | GPIO | ALT5 | GPIO5_IO17 | Input | PU (100K) |
| DISP0_DAT3 | P21 | NVCC_LCD | GPIO | ALT5 | GPIO4_IO24 | Input | PU (100K) |
| DISP0_DAT4 | P20 | NVCC_LCD | GPIO | ALT5 | GPIO4_IO25 | Input | PU (100K) |
| DISP0_DAT5 | R25 | NVCC_LCD | GPIO | ALT5 | GPIO4_IO26 | Input | PU (100K) |
| DISP0_DAT6 | R23 | NVCC_LCD | GPIO | ALT5 | GPIO4_IO27 | Input | PU (100K) |
| DISP0_DAT7 | R24 | NVCC_LCD | GPIO | ALT5 | GPIO4_IO28 | Input | PU (100K) |
| DISP0_DAT8 | R22 | NVCC_LCD | GPIO | ALT5 | GPIO4_IO29 | Input | PU (100K) |
| DISP0_DAT9 | T25 | NVCC_LCD | GPIO | ALT5 | GPIO4_IO30 | Input | PU (100K) |
| DRAM_A0 | AC14 | NVCC_DRAM | DDR | ALT0 | DRAM_ADDR00 | Output | 0 |
| DRAM_A1 | AB14 | NVCC_DRAM | DDR | ALT0 | DRAM_ADDR01 | Output | 0 |
| DRAM_A10 | AA15 | NVCC_DRAM | DDR | ALT0 | DRAM_ADDR10 | Output | 0 |
| DRAM_A11 | AC12 | NVCC_DRAM | DDR | ALT0 | DRAM_ADDR11 | Output | 0 |
| DRAM_A12 | AD12 | NVCC_DRAM | DDR | ALT0 | DRAM_ADDR12 | Output | 0 |
| DRAM_A13 | AC17 | NVCC_DRAM | DDR | ALT0 | DRAM_ADDR13 | Output | 0 |
| DRAM_A14 | AA12 | NVCC_DRAM | DDR | ALT0 | DRAM_ADDR14 | Output | 0 |
| DRAM_A15 | Y12 | NVCC_DRAM | DDR | ALT0 | DRAM_ADDR15 | Output | 0 |
| DRAM_A2 | AA14 | NVCC_DRAM | DDR | ALT0 | DRAM_ADDR02 | Output | 0 |
| DRAM_A3 | Y14 | NVCC_DRAM | DDR | ALT0 | DRAM_ADDR03 | Output | 0 |
| DRAM_A4 | W14 | NVCC_DRAM | DDR | ALT0 | DRAM_ADDR04 | Output | 0 |
| DRAM_A5 | AE13 | NVCC_DRAM | DDR | ALT0 | DRAM_ADDR05 | Output | 0 |
| DRAM_A6 | AC13 | NVCC_DRAM | DDR | ALT0 | DRAM_ADDR06 | Output | 0 |
| DRAM_A7 | Y13 | NVCC_DRAM | DDR | ALT0 | DRAM_ADDR07 | Output | 0 |
| DRAM_A8 | AB13 | NVCC_DRAM | DDR | ALT0 | DRAM_ADDR08 | Output | 0 |
| DRAM_A9 | AE12 | NVCC_DRAM | DDR | ALT0 | DRAM_ADDR09 | Output | 0 |
| DRAM_CAS | AE16 | NVCC_DRAM | DDR | ALT0 | DRAM_CAS_B | Output | 0 |
| DRAM_CS0 | Y16 | NVCC_DRAM | DDR | ALT0 | DRAM_CS0_B | Output | 0 |

Table 87. 21 x 21 mm Functional Contact Assignments (continued)

| Ball Name | Ball | Power Group | Ball Type | Out of Reset Condition[1] | | | |
|---|---|---|---|---|---|---|---|
| | | | | Default Mode (Reset Mode) | Default Function (Signal Name) | Input/Output | Value[2] |
| LVDS0_TX1_P | U3 | NVCC_LVDS_2P5 | LVDS | ALT0 | LVDS0_TX1_P | Input | Keeper |
| LVDS0_TX2_N | V2 | NVCC_LVDS_2P5 | LVDS | — | LVDS0_TX2_N | — | — |
| LVDS0_TX2_P | V1 | NVCC_LVDS_2P5 | LVDS | ALT0 | LVDS0_TX2_P | Input | Keeper |
| LVDS0_TX3_N | W2 | NVCC_LVDS_2P5 | LVDS | — | LVDS0_TX3_N | — | — |
| LVDS0_TX3_P | W1 | NVCC_LVDS_2P5 | LVDS | ALT0 | LVDS0_TX3_P | Input | Keeper |
| LVDS1_CLK_N | Y3 | NVCC_LVDS_2P5 | LVDS | — | LVDS1_CLK_N | — | — |
| LVDS1_CLK_P | Y4 | NVCC_LVDS_2P5 | LVDS | ALT0 | LVDS1_CLK_P | Input | Keeper |
| LVDS1_TX0_N | Y1 | NVCC_LVDS_2P5 | LVDS | — | LVDS1_TX0_N | — | — |
| LVDS1_TX0_P | Y2 | NVCC_LVDS_2P5 | LVDS | ALT0 | LVDS1_TX0_P | Input | Keeper |
| LVDS1_TX1_N | AA2 | NVCC_LVDS_2P5 | LVDS | — | LVDS1_TX1_N | — | — |
| LVDS1_TX1_P | AA1 | NVCC_LVDS_2P5 | LVDS | ALT0 | LVDS1_TX1_P | Input | Keeper |
| LVDS1_TX2_N | AB1 | NVCC_LVDS_2P5 | LVDS | — | LVDS1_TX2_N | — | — |
| LVDS1_TX2_P | AB2 | NVCC_LVDS_2P5 | LVDS | ALT0 | LVDS1_TX2_P | Input | Keeper |
| LVDS1_TX3_N | AA3 | NVCC_LVDS_2P5 | LVDS | — | LVDS1_TX3_N | — | — |
| LVDS1_TX3_P | AA4 | NVCC_LVDS_2P5 | LVDS | ALT0 | LVDS1_TX3_P | Input | Keeper |
| NANDF_ALE | A16 | NVCC_NANDF | GPIO | ALT5 | GPIO6_IO08 | Input | PU (100K) |
| NANDF_CLE | C15 | NVCC_NANDF | GPIO | ALT5 | GPIO6_IO07 | Input | PU (100K) |
| NANDF_CS0 | F15 | NVCC_NANDF | GPIO | ALT5 | GPIO6_IO11 | Input | PU (100K) |
| NANDF_CS1 | C16 | NVCC_NANDF | GPIO | ALT5 | GPIO6_IO14 | Input | PU (100K) |
| NANDF_CS2 | A17 | NVCC_NANDF | GPIO | ALT5 | GPIO6_IO15 | Input | PU (100K) |
| NANDF_CS3 | D16 | NVCC_NANDF | GPIO | ALT5 | GPIO6_IO16 | Input | PU (100K) |
| NANDF_D0 | A18 | NVCC_NANDF | GPIO | ALT5 | GPIO2_IO00 | Input | PU (100K) |
| NANDF_D1 | C17 | NVCC_NANDF | GPIO | ALT5 | GPIO2_IO01 | Input | PU (100K) |
| NANDF_D2 | F16 | NVCC_NANDF | GPIO | ALT5 | GPIO2_IO02 | Input | PU (100K) |
| NANDF_D3 | D17 | NVCC_NANDF | GPIO | ALT5 | GPIO2_IO03 | Input | PU (100K) |
| NANDF_D4 | A19 | NVCC_NANDF | GPIO | ALT5 | GPIO2_IO04 | Input | PU (100K) |
| NANDF_D5 | B18 | NVCC_NANDF | GPIO | ALT5 | GPIO2_IO05 | Input | PU (100K) |
| NANDF_D6 | E17 | NVCC_NANDF | GPIO | ALT5 | GPIO2_IO06 | Input | PU (100K) |
| NANDF_D7 | C18 | NVCC_NANDF | GPIO | ALT5 | GPIO2_IO07 | Input | PU (100K) |
| NANDF_RB0 | B16 | NVCC_NANDF | GPIO | ALT5 | GPIO6_IO10 | Input | PU (100K) |
| NANDF_WP_B | E15 | NVCC_NANDF | GPIO | ALT5 | GPIO6_IO09 | Input | PU (100K) |
| ONOFF | D12 | VDD_SNVS_IN | GPIO | — | SRC_ONOFF | Input | PU (100K) |
| PCIE_RXM | B1 | PCIE_VPH | — | — | PCIE_RX_N | — | — |
| PCIE_RXP | B2 | PCIE_VPH | — | — | PCIE_RX_P | — | — |
| PCIE_TXM | A3 | PCIE_VPH | — | — | PCIE_TX_N | — | — |
| PCIE_TXP | B3 | PCIE_VPH | — | — | PCIE_TX_P | — | — |