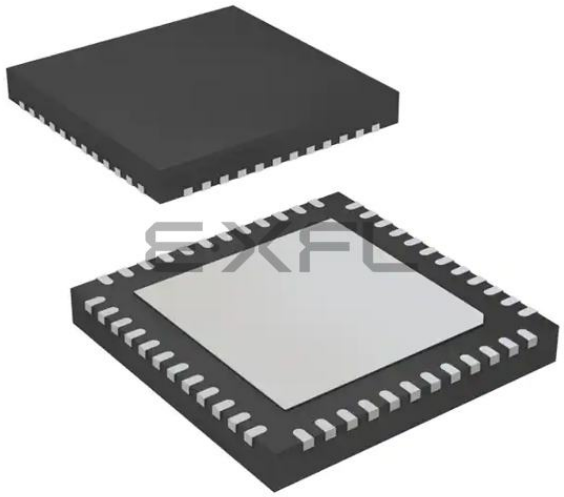

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MSP430 CPUXV2
Core Size	16-Bit
Speed	25MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	37
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-VQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/texas-instruments/msp430f5244irgzt

2.1.1 LOW-VOLTAGE ICSP PROGRAMMING

In Low-Voltage ICSP mode, the PIC18F1XK50/PIC18LF1XK50 devices can be programmed using a single VDD source in the operating range. The MCLR/VPP/RA3 does not have to be brought to a different voltage, but can instead be left at the normal operating voltage. Refer to **Section 8.1 "AC/DC Characteristics Timing Requirements for Program/Verify Test Mode"** for additional hardware parameters.

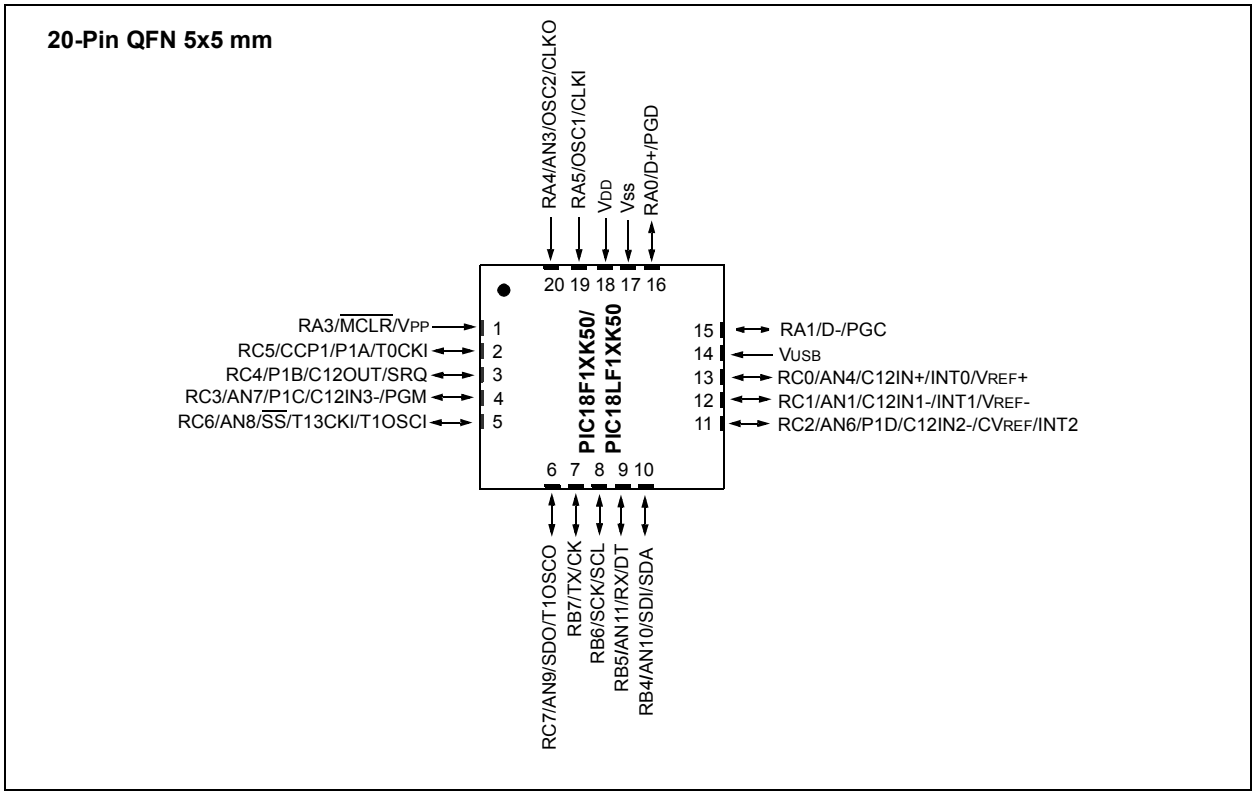
2.1.1.1 Single-Supply ICSP Programming

The LVP bit in Configuration register, CONFIG4L, enables single-supply (low-voltage) ICSP programming. The LVP bit defaults to a '1' (enabled) from the factory.

If Single-Supply Programming mode is not used, the LVP bit can be programmed to a '0' and RC3/PGM becomes a digital I/O pin. However, the LVP bit may only be programmed by entering the High-Voltage ICSP mode, where MCLR/VPP/RA3 is raised to VIHH. Once the LVP bit is programmed to a '0', only the High-Voltage ICSP mode is available and only the High-Voltage ICSP mode can be used to program the device.

Note 1:	The High-Voltage ICSP mode is always available, regardless of the state of the LVP bit, by applying VIHH to the MCLR/VPP/RA3 pin.
2:	While in Low-Voltage ICSP mode, the RC3 pin can no longer be used as a general purpose I/O.

FIGURE 2-5: 20-PIN QFN PIN DIAGRAMS FOR PIC18F1XK50 AND PIC18LF1XK50



3.0 MEMORY MAPS

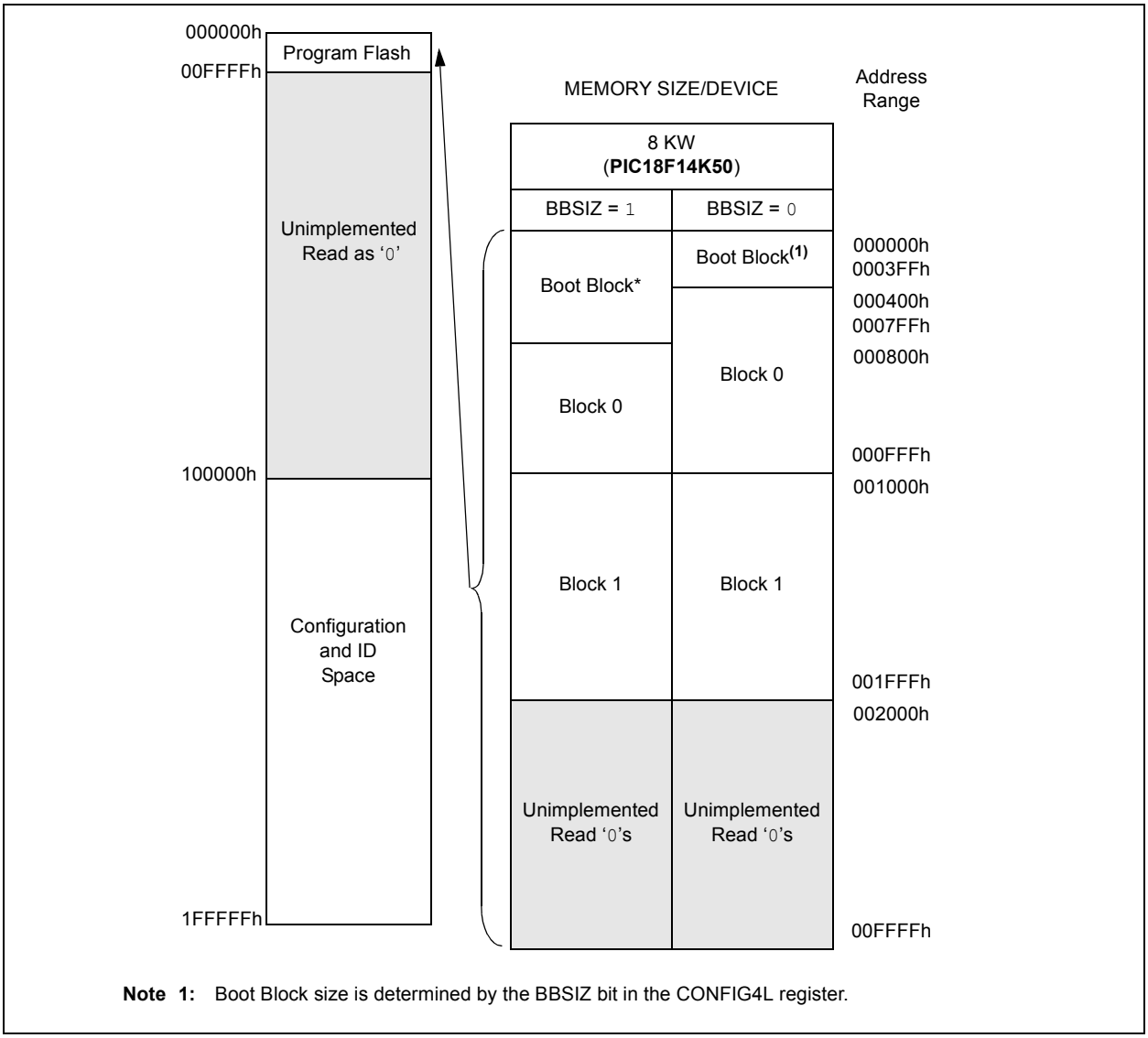
For the PIC18F14K50/PIC18LF14K50 device, the program Flash space extends from 0000h to 03FFFh (16 Kbytes) in two 8-Kbyte blocks. For the PIC18F13K50/PIC18LF13K50 device, the program Flash space extends from 0000h to 01FFFh (8 Kbytes) in two 4-Kbyte blocks.

For the PIC18F14K50/PIC18LF14K50 addresses 0000h through 0FFFh, however, define a “Boot Block” region that is treated separately from Block 0. For the PIC18F13K50/PIC18LF13K50 addresses 0000h through 07FFh, define the “Boot Block” region. All of these blocks define code protection boundaries within the program Flash space. The size of the Boot Block in the PIC18F14K50/PIC18LF14K50 devices can be configured as 2K, or 4 Kbyte (see Figure 3-1). The size of the Boot Block in the PIC18F13K50/PIC18LF13K50 devices can be configured as 1K, or 2 Kbytes, as illustrated in Figure 3-1. This is done through the BBSIZ bit in the Configuration register, CONFIG4L. It is important to note that increasing the size of the Boot Block decreases the size of the Block 0.

TABLE 3-1: IMPLEMENTATION OF PROGRAM FLASH

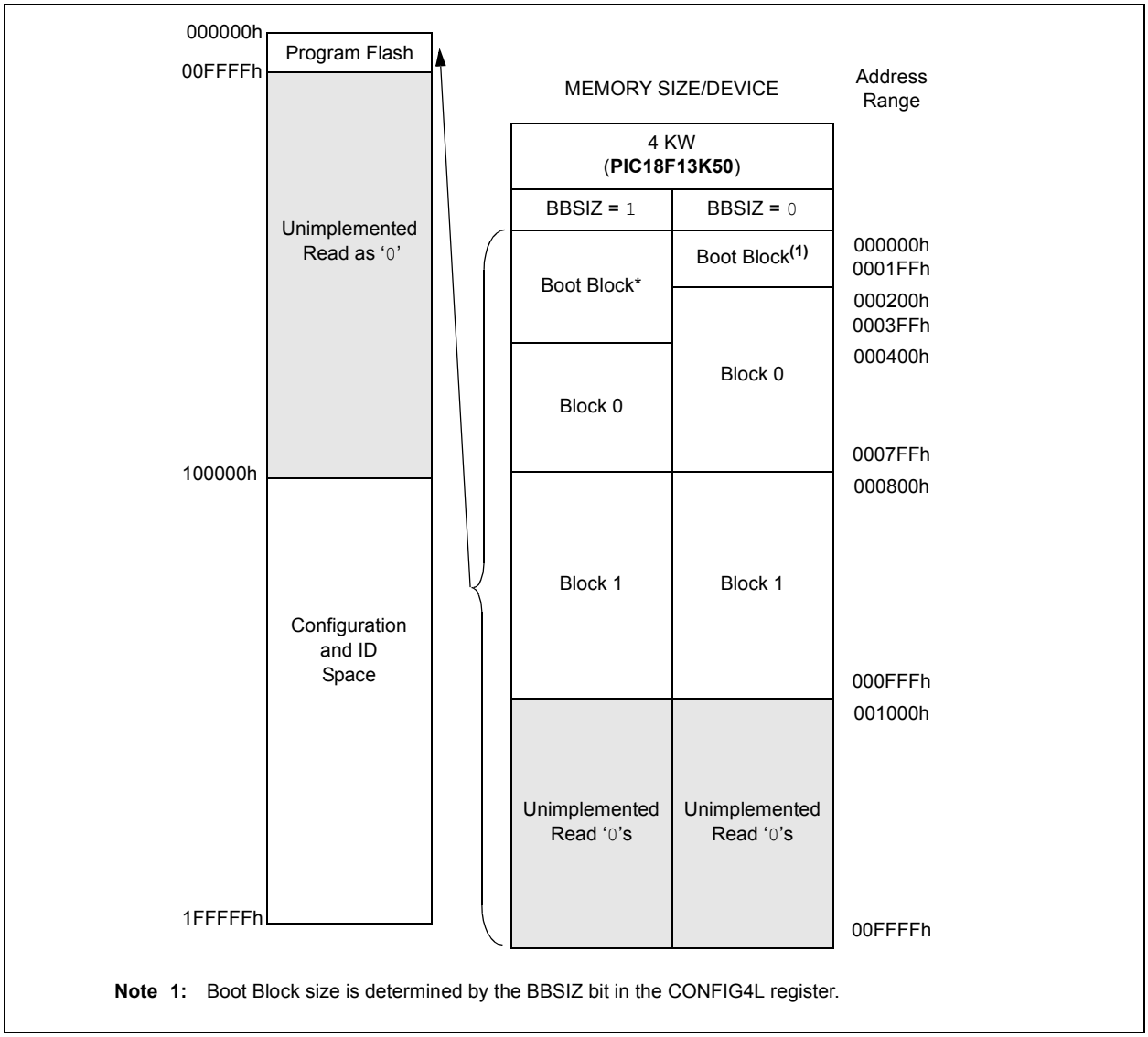
Device	Program Flash Size (Words)
PIC18F13K50/ PIC18LF13K50	000000h-000FFFh (4K)
PIC18F14K50/ PIC18LF14K50	000000h-001FFFh (8K)

FIGURE 3-1: MEMORY MAP AND THE PROGRAM FLASH SPACE FOR PIC18F14K50/ PIC18LF14K50 DEVICES



Note 1: Boot Block size is determined by the BBSIZ bit in the CONFIG4L register.

FIGURE 3-2: MEMORY MAP AND THE PROGRAM FLASH SPACE FOR PIC18F13K50/ PIC18LF13K50 DEVICES



Note 1: Boot Block size is determined by the BBSIZ bit in the CONFIG4L register.

In addition to the program Flash space, there are three blocks in the Configuration and ID space that are accessible to the user through table reads and table writes. Their locations in the memory map are shown in Figure 3-3.

Users may store identification information (ID) in eight ID registers. These ID registers are mapped in addresses 200000h through 200007h. The ID locations read out normally, even after code protection is applied.

Locations 300000h through 30000Dh are reserved for the Configuration bits. These bits select various device options and are described in **Section 6.0 "Configuration Word"**. These Configuration bits read out normally, even after code protection.

Locations 3FFFFEh and 3FFFFFh are reserved for the device ID bits. These bits may be used by the programmer to identify what device type is being programmed, and are described in **Section 6.0 "Configuration Word"**. These device ID bits read out normally, even after code protection.

3.1 Memory Address Pointer

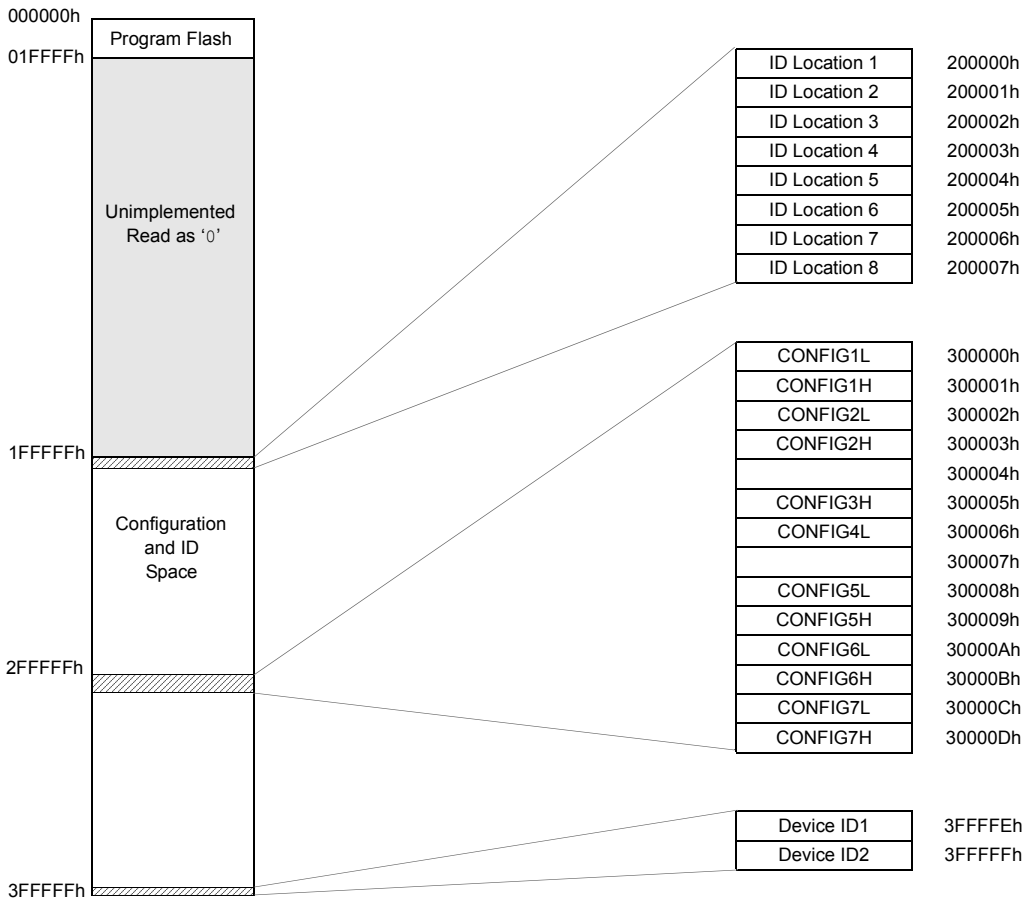
Memory in the address space, 0000000h to 3FFFFFh, is addressed via the Table Pointer register, which is comprised of three Pointer registers:

- TBLPTRU, at RAM address 0FF8h
- TBLPTRH, at RAM address 0FF7h
- TBLPTRL, at RAM address 0FF6h

TBLPTRU	TBLPTRH	TBLPTRL
Addr[21:16]	Addr[15:8]	Addr[7:0]

The 4-bit command, '0000' (core instruction), is used to load the Table Pointer prior to using any read or write operations.

FIGURE 3-3: CONFIGURATION AND ID LOCATIONS FOR PIC18F1XK50/PIC18LF1XK50 DEVICES

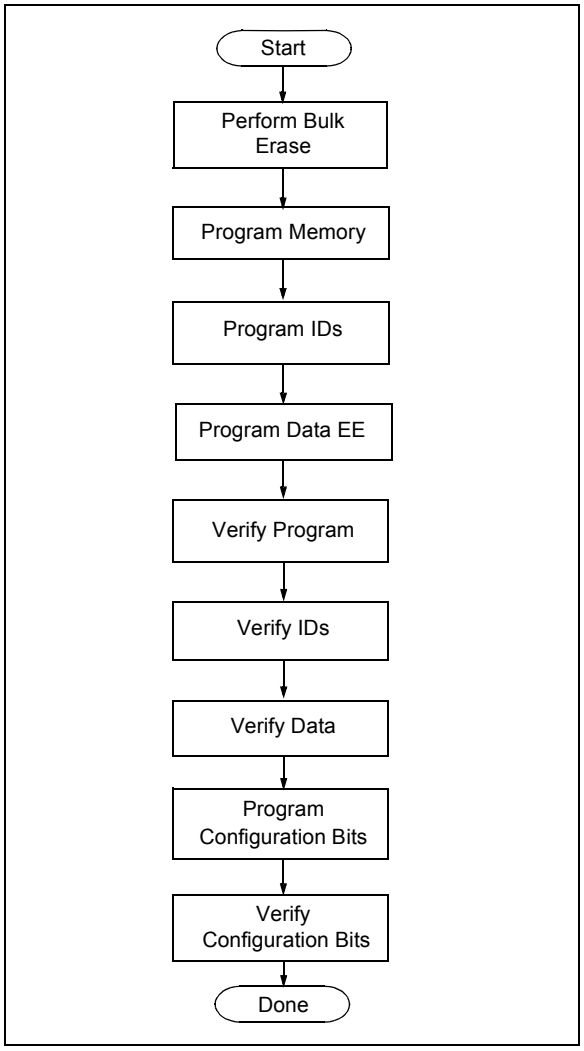


Note: Sizes of memory areas are not to scale.

3.2 High-Level Overview of the Programming Process

Figure 3-4 shows the high-level overview of the programming process. First, a Bulk Erase is performed. Next, the program Flash, ID locations and data EEPROM are programmed. These memories are then verified to ensure that programming was successful. If no errors are detected, the Configuration bits are then programmed and verified.

FIGURE 3-4: HIGH-LEVEL PROGRAMMING FLOW

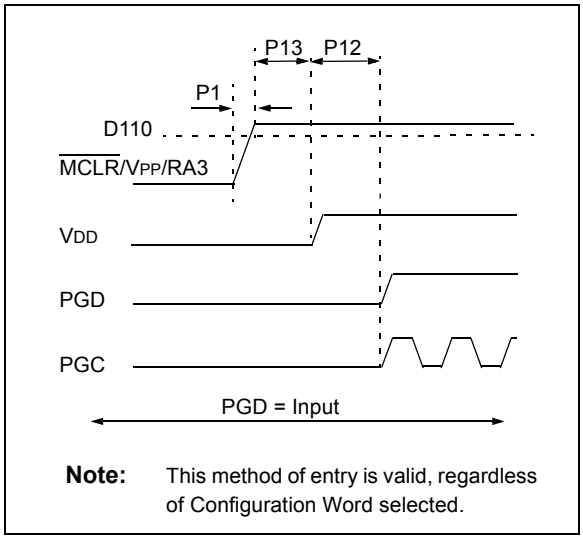


3.3 Entering and Exiting High-Voltage ICSP Program/Verify Mode

As shown in Figure 3-6, the High-Voltage ICSP Program/Verify mode is entered by holding PGC and PGD low and then raising $\overline{MCLR}/V_{PP}$/RA3 to V_{IHH} (high voltage). Once in this mode, the program Flash, data EEPROM, ID locations and Configuration bits can be accessed and programmed in serial fashion. Figure 3-7 shows the exit sequence.

The sequence that enters the device into the Program/Verify mode places all unused I/Os in the high-impedance state.

FIGURE 3-5: V_{PP}-FIRST PROGRAM/ VERIFY MODE ENTRY



Note: This method of entry is valid, regardless of Configuration Word selected.

FIGURE 3-6: V_{DD}-FIRST PROGRAM/ VERIFY MODE ENTRY

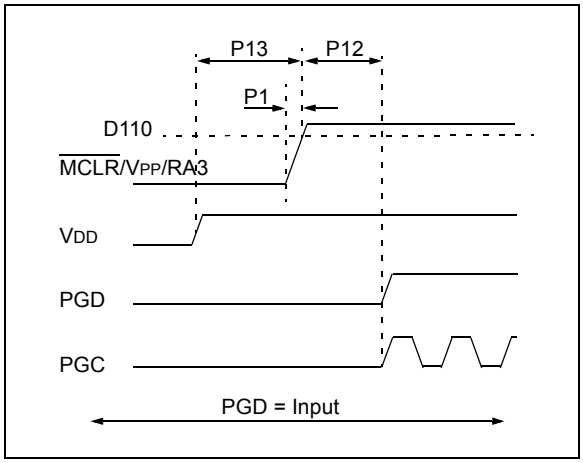
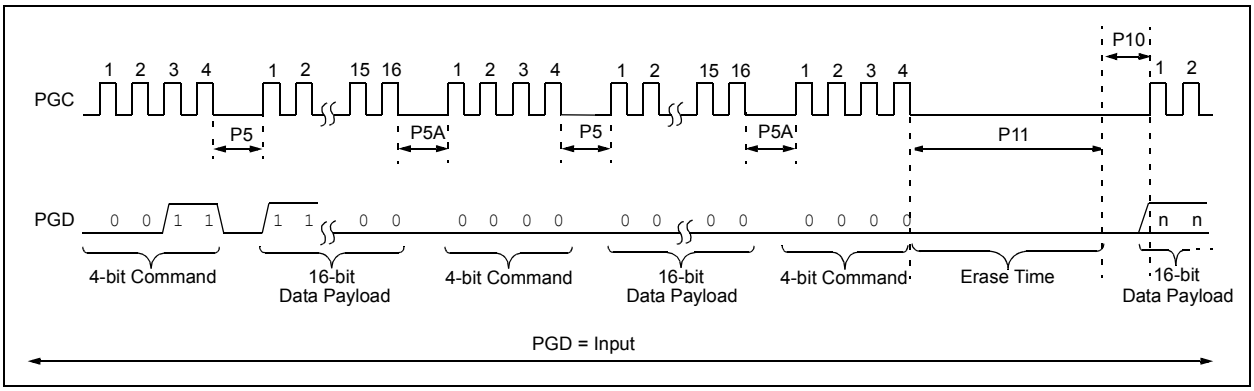


FIGURE 4-2: BULK ERASE TIMING DIAGRAM



4.1.2 LOW-VOLTAGE ICSP BULK ERASE

When using low-voltage ICSP, the part must be supplied by the voltage specified in parameter D111 if a Bulk Erase is to be executed. All other Bulk Erase details, as described above, apply.

If it is determined that a program memory erase must be performed at a supply voltage below the Bulk Erase limit, refer to the erase methodology described in **Section 4.1.3 "ICSP Row Erase"** and **Section 4.2.1 "Modifying Program Flash"**.

If it is determined that a data EEPROM erase must be performed at a supply voltage below the Bulk Erase limit, follow the methodology described in **Section 4.3 "Data EEPROM Programming"** and write '1's to the array.

4.1.3 ICSP ROW ERASE

Regardless of whether high or low-voltage ICSP is used, it is possible to erase one row (64 bytes of data), provided the block is not code or write-protected. Rows are located at static boundaries, beginning at program memory address 000000h, extending to the internal program memory limit (see **Section 3.0 "Memory Maps"**).

The Row Erase duration is self-timed. After the WR bit in EECON1 is set, two NOPs are issued. Erase starts upon the 4th PGC of the second NOP. It ends when the WR bit is cleared by hardware.

The code sequence to Row Erase a PIC18F1XK50/PIC18LF1XK50 device is shown in Table 4-3. The flow-chart shown in Figure 4-3 depicts the logic necessary to completely erase the PIC18F1XK50/PIC18LF1XK50 devices. The timing diagram for Row Erase is identical to the data EEPROM write timing, shown in Figure 4-7.

Note 1:	The TBLPTR register can point at any byte within the row intended for erase.
2:	ICSP row erase of the User ID locations is also possible using the technique described in **Section 4.1.3 "ICSP Row Erase"**. The address argument used should be 0x200000. A row erase of the User ID locations is required when V_{DD} is below the Bulk Erase threshold.

TABLE 4-3: ERASE PROGRAM FLASH CODE SEQUENCE

4-bit Command	Data Payload	Core Instruction
Step 1: Direct access to program Flash and enable writes.		
0000	8E A6	BSF EECON1, EEPGD
0000	9C A6	BCF EECON1, CFGS
0000	84 A6	BSF EECON1, WREN
Step 2: Point to first row in program Flash.		
0000	6A F8	CLRF TBLPTRU
0000	6A F7	CLRF TBLPTRH
0000	6A F6	CLRF TBLPTRL
Step 3: Enable erase and erase single row.		
0000	88 A6	BSF EECON1, FREE
0000	82 A6	BSF EECON1, WR
0000	00 00	NOP
0000	00 00	NOP Erase starts on the 4th clock of this instruction
Step 4: Poll WR bit. Repeat until bit is clear.		
0000	50 A6	MOVF EECON1, W, 0
0000	6E F5	MOVWF TABLAT
0000	00 00	NOP
0010	<MSB><LSB>	Shift out data(1)
Step 5: Hold PGC low for time P10.		
Step 6: Repeat step 3 with Address Pointer incremented by 64 until all rows are erased.		
Step 7: Disable writes.		
0000	94 A6	BCF EECON1, WREN

Note 1: See Figure 5-4 for details on shift out data timing.

FIGURE 4-3: SINGLE ROW ERASE PROGRAM FLASH FLOW

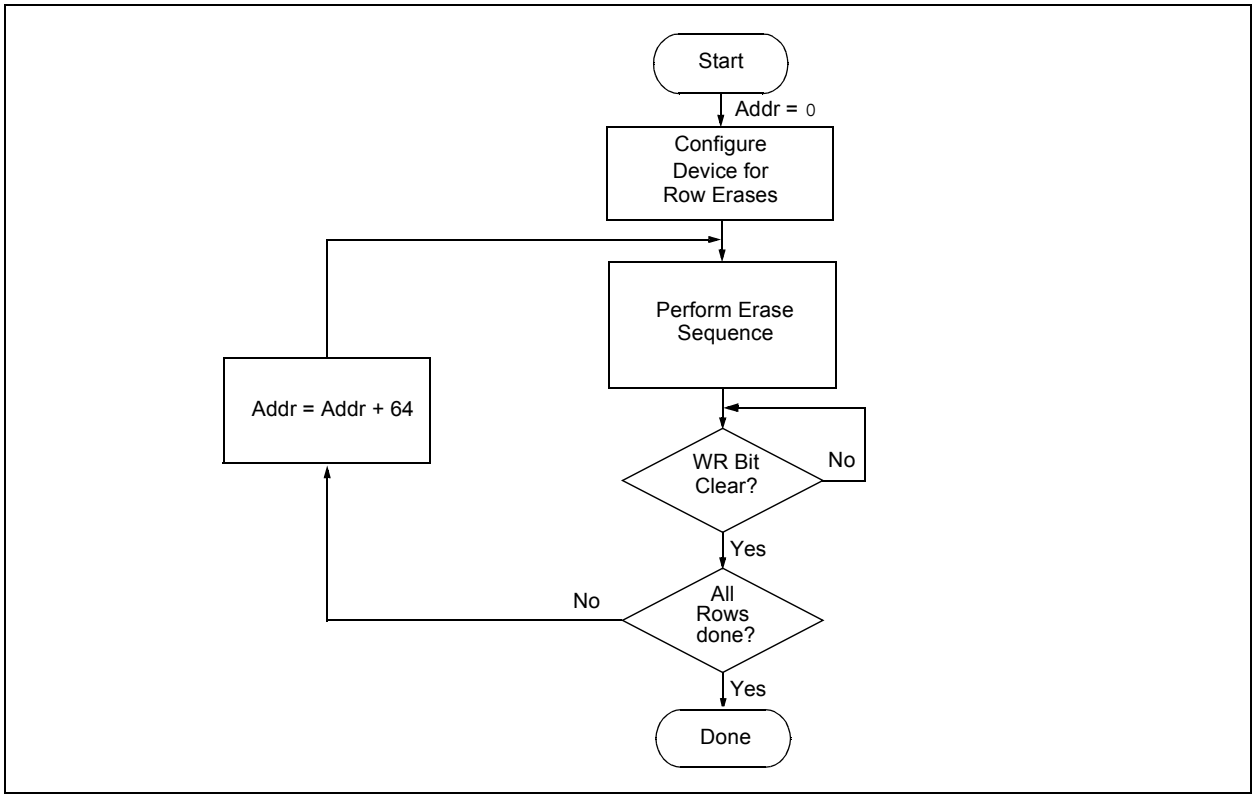


FIGURE 4-4: PROGRAM FLASH FLOW

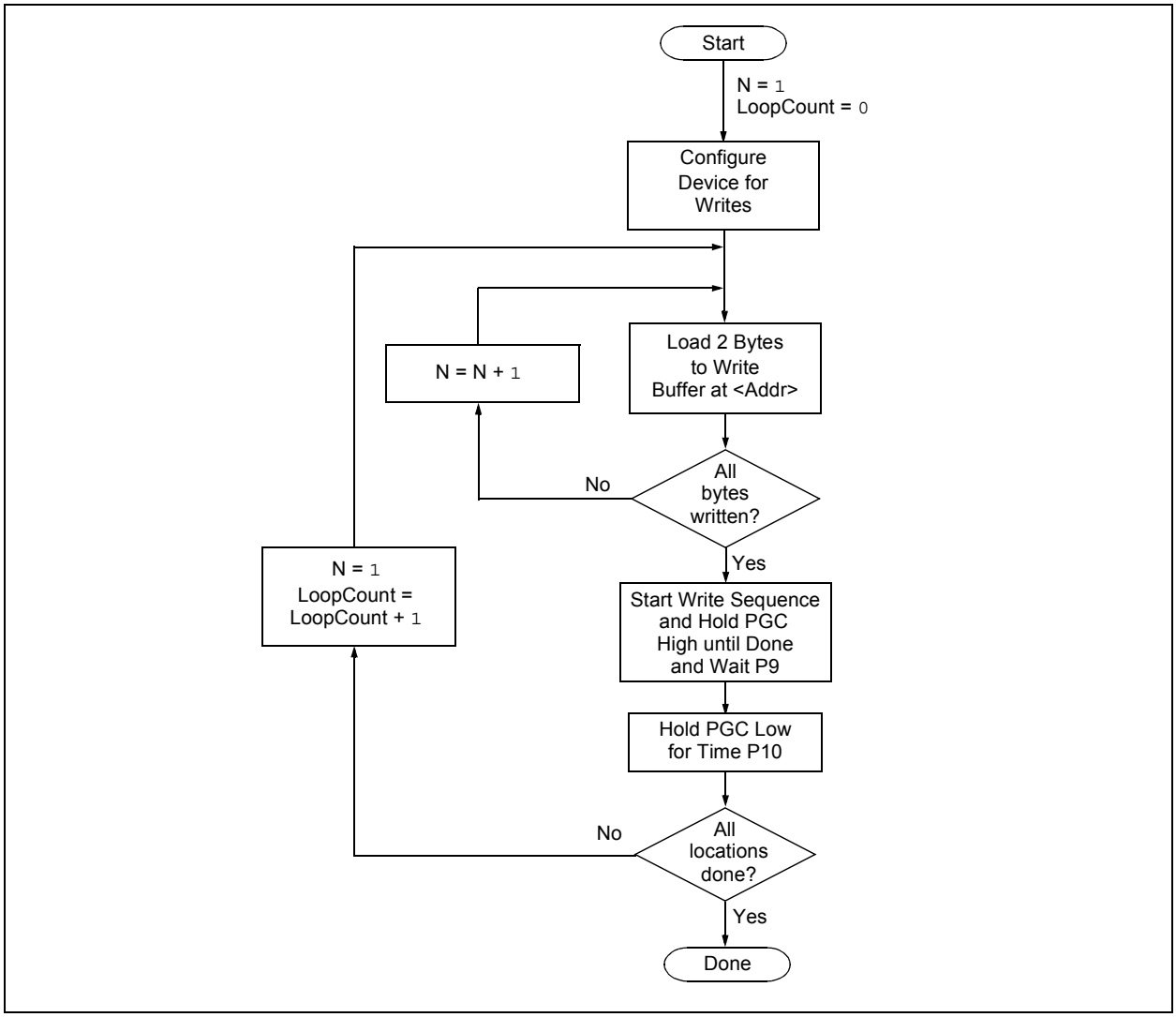
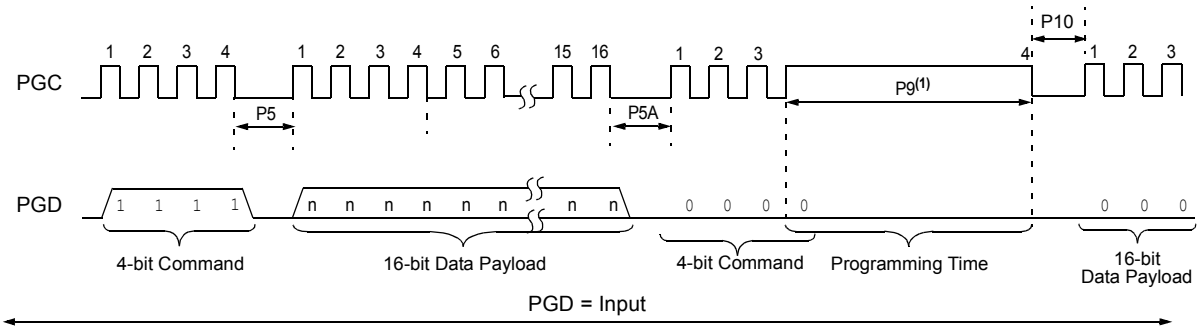


FIGURE 4-5: TABLE WRITE AND START PROGRAMMING INSTRUCTION TIMING DIAGRAM (1111)



Note 1: Use P9A for Configuration Word programming.

4.2.1 MODIFYING PROGRAM FLASH

The previous programming example assumed that the device has been Bulk Erased prior to programming (see **Section 4.1.1 "High-Voltage ICSP Bulk Erase"**). It may be the case, however, that the user wishes to modify only a section of an already programmed device.

The appropriate number of bytes required for the erase buffer must be read out of program Flash (as described in **Section 5.2 "Verify Program Flash and ID Locations"**) and buffered. Modifications can be made on this buffer. Then, the block of program Flash that was read out must be erased and rewritten with the modified data.

The WREN bit must be set if the WR bit in EECON1 is used to initiate a write sequence.

TABLE 4-6: MODIFYING PROGRAM FLASH

4-bit Command	Data Payload	Core Instruction
Step 1: Direct access to program Flash.		
0000	8E A6	BSF EECON1, EEPGD
0000	9C A6	BCF EECON1, CFGS
Step 2: Read program Flash into buffer (**Section 5.1 "Read Program Flash, ID Locations and Configuration Bits"**).		
Step 3: Set the Table Pointer for the block to be erased.		
0000	0E <Addr[21:16]>	MOVLW <Addr[21:16]>
0000	6E F8	MOVWF TBLPTRU
0000	0E <Addr[8:15]>	MOVLW <Addr[8:15]>
0000	6E F7	MOVWF TBLPTRH
0000	0E <Addr[7:0]>	MOVLW <Addr[7:0]>
0000	6E F6	MOVWF TBLPTRL
Step 4: Enable memory writes and setup an erase.		
0000	84 A6	BSF EECON1, WREN
0000	88 A6	BSF EECON1, FREE
Step 5: Initiate erase.		
0000	88 A6	BSF EECON1, FREE
0000	82 A6	BSF EECON1, WR
0000	00 00	NOP
0000	00 00	NOP Erase starts on the 4th clock of this instruction
Step 6: Poll WR bit. Repeat until bit is clear.		
0000	50 A6	MOVF EECON1, W, 0
0000	6E F5	MOVWF TABLAT
0000	00 00	NOP
0000	<MSB><LSB>	Shift out data(1)
Step 7: Load write buffer. The correct bytes will be selected based on the Table Pointer.		
0000	0E <Addr[21:16]>	MOVLW <Addr[21:16]>
0000	6E F8	MOVWF TBLPTRU
0000	0E <Addr[8:15]>	MOVLW <Addr[8:15]>
0000	6E F7	MOVWF TBLPTRH
0000	0E <Addr[7:0]>	MOVLW <Addr[7:0]>
0000	6E F6	MOVWF TBLPTRL
1101	<MSB><LSB>	Write 2 bytes and post-increment address by 2.
•	•	
•	•	Repeat as many times as necessary to fill the write buffer
•	•	Write 2 bytes and start programming.
1111	<MSB><LSB>	NOP - hold PGC high for time P9 and low for time P10.
0000	00 00	
To continue modifying data, repeat Steps 2 through 6, where the Address Pointer is incremented by the appropriate number of bytes (see Table 4-4) at each iteration of the loop. The write cycle must be repeated enough times to completely rewrite the contents of the erase buffer.		
Step 8: Disable writes.		
0000	94 A6	BCF EECON1, WREN

4.3 Data EEPROM Programming

Data EEPROM is accessed one byte at a time via an Address Pointer (register pair EEADRH:EEADR) and a data latch (EEDATA). Data EEPROM is written by loading EEADRH:EEADR with the desired memory location, EEDATA, with the data to be written and initiating a memory write by appropriately configuring the EECON1 register. A byte write automatically erases the location and writes the new data (erase-before-write).

When using the EECON1 register to perform a data EEPROM write, both the EEPGD and CFGS bits must be cleared (EECON1<7:6> = 00). The WREN bit must be set (EECON1<2> = 1) to enable writes of any sort and this must be done prior to initiating a write sequence. The write sequence is initiated by setting the WR bit (EECON1<1> = 1).

The write begins on the falling edge of the 24th PGC after the WR bit is set. It ends when the WR bit is cleared by hardware.

After the programming sequence terminates, PGC must be held low for the time specified by parameter P10 to allow high-voltage discharge of the memory array.

FIGURE 4-6: PROGRAM DATA FLOW

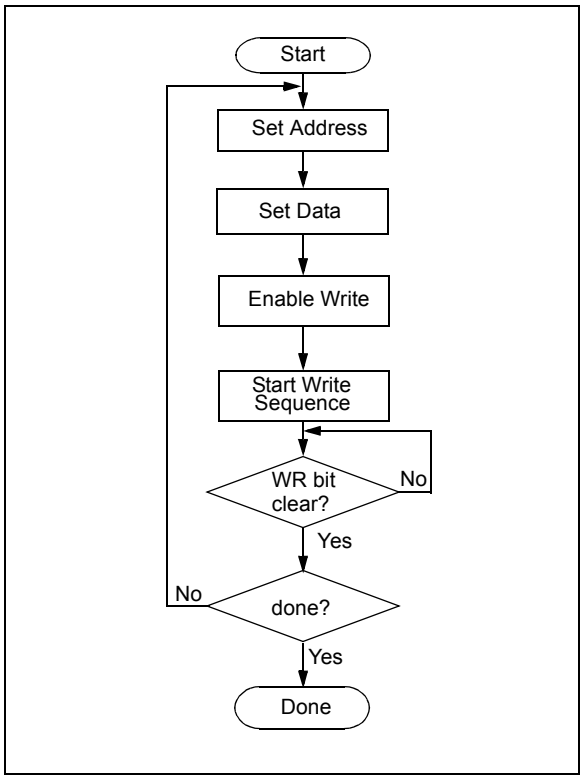
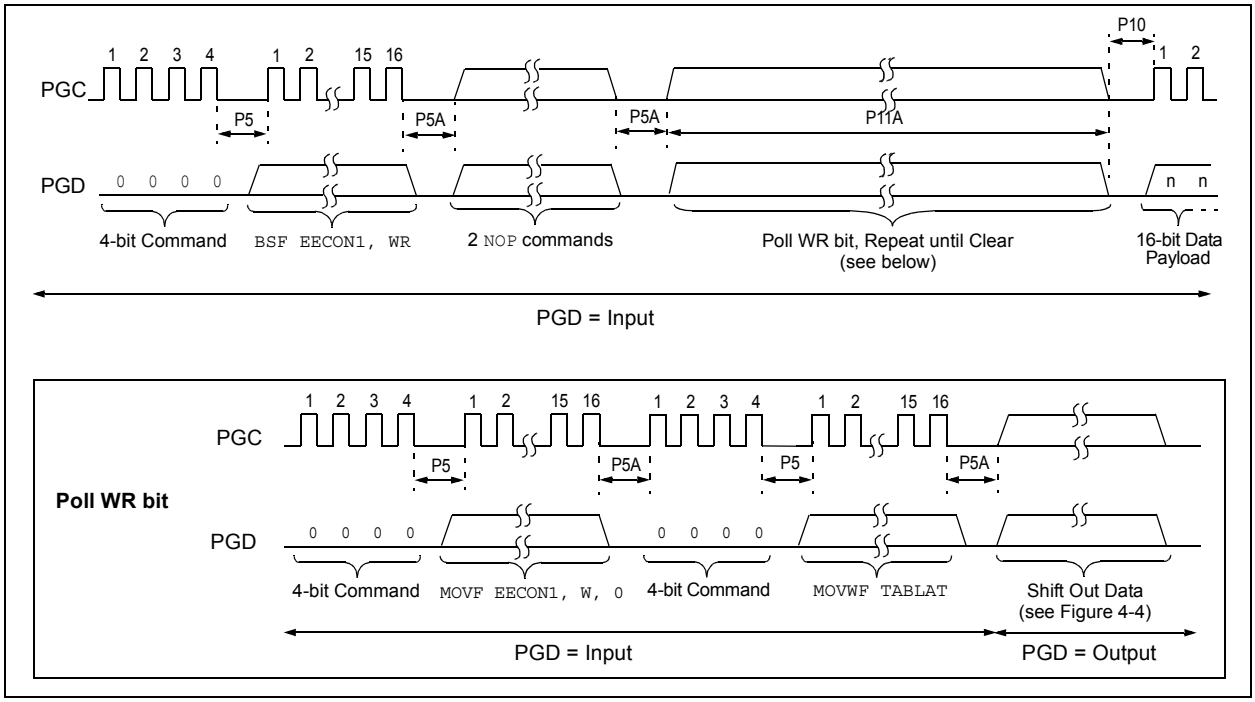


FIGURE 4-7: DATA EEPROM WRITE TIMING DIAGRAM



5.0 READING THE DEVICE

5.1 Read Program Flash, ID Locations and Configuration Bits

Program Flash is accessed one byte at a time via the 4-bit command, '1001' (table read, post-increment). The contents of memory pointed to by the Table Pointer (TBLPTRU:TBLPTRH:TBLPTRL) are serially output on PGD.

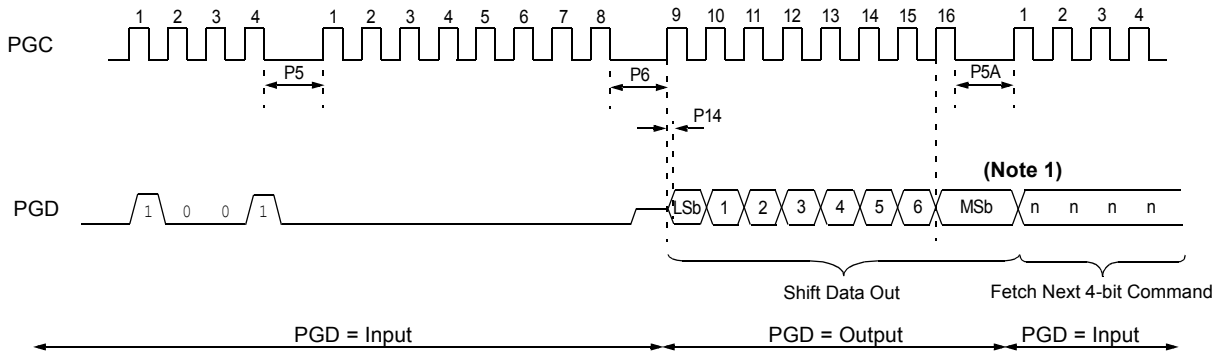
The 4-bit command is shifted in LSb first. The read is executed during the next 8 clocks, then shifted out on PGD during the last 8 clocks, LSb to MSb. A delay of P6 must be introduced after the falling edge of the 8th PGC of the operand to allow PGD to transition from an input to an output. During this time, PGC must be held low, as illustrated in Figure 5-1. This operation also increments the Table Pointer by one, pointing to the next byte in program Flash for the next read.

This technique will work to read any memory in the 000000h to 3FFFFFh address space, so it also applies to the reading of the ID and Configuration registers.

TABLE 5-1: READ PROGRAM FLASH SEQUENCE

4-bit Command	Data Payload	Core Instruction
Step 1: Set Table Pointer		
0000	0E <Addr[21:16]>	MOVLW Addr[21:16]
0000	6E F8	MOVWF TBLPTRU
0000	0E <Addr[15:8]>	MOVLW <Addr[15:8]>
0000	6E F7	MOVWF TBLPTRH
0000	0E <Addr[7:0]>	MOVLW <Addr[7:0]>
0000	6E F6	MOVWF TBLPTRL
Step 2: Read memory and then shift out on PGD, LSb to MSb		
1001	00 00	TBLRD *+

FIGURE 5-1: TABLE READ POST-INCREMENT INSTRUCTION TIMING DIAGRAM (1001)



Note 1: Magnification of the high-impedance delay between PGC and PGD is shown in Figure 5-5.

5.2 Verify Program Flash and ID Locations

The verify step involves reading back the program Flash space and comparing it against the copy held in the programmer's buffer. Memory reads occur a single byte at a time, so two bytes must be read to compare against the word in the programmer's buffer. Refer to **Section 5.1 "Read Program Flash, ID Locations and Configuration Bits"** for implementation details of reading program Flash.

The Table Pointer must be manually set to 200000h (base address of the ID locations) once the program Flash has been verified. The post-increment feature of the Table Read 4-bit command can not be used to increment the Table Pointer beyond the program Flash space. In a 64-Kbyte device, for example, a post-increment read of address FFFFh will wrap the Table Pointer back to 000000h, rather than point to unimplemented address, 010000h.

FIGURE 5-2: VERIFY PROGRAM FLASH FLOW

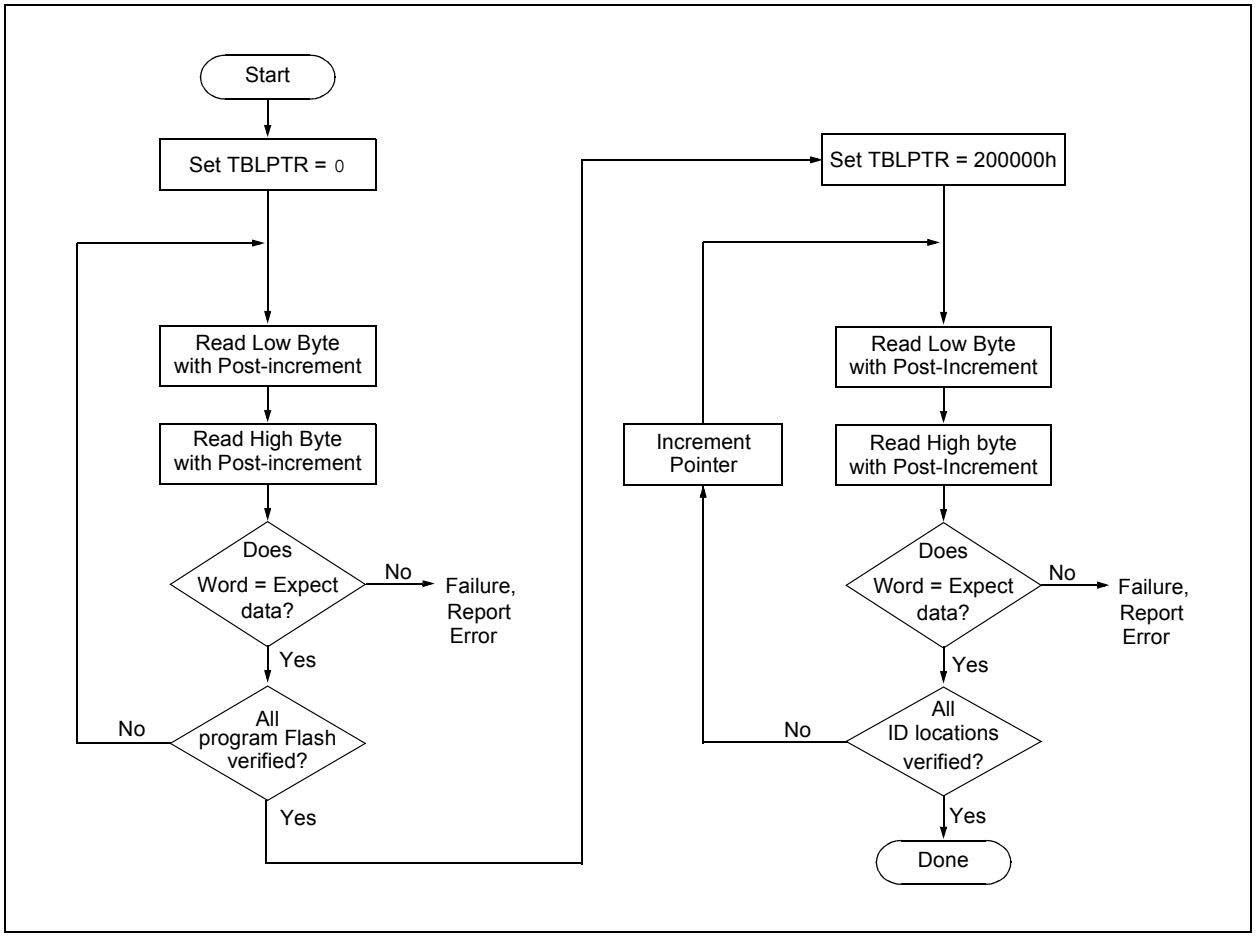


TABLE 6-3: PIC18F1XK50/PIC18LF1XK50 BIT DESCRIPTIONS (CONTINUED)

Bit Name	Configuration Words	Description
BOREN<1:0>	CONFIG2L	Brown-out Reset Enable bits 11 = Brown-out Reset enabled in hardware only (SBOREN is disabled) 10 = Brown-out Reset enabled in hardware only and disabled in Sleep mode SBOREN is disabled) 01 = Brown-out Reset enabled and controlled by software (SBOREN is enabled) 00 = Brown-out Reset disabled in hardware and software
$\overline{\text{PWRTEN}}$	CONFIG2L	Power-up Timer Enable bit 1 = PWRT disabled 0 = PWRT enabled
WDTPS<3:0>	CONFIG2H	Watchdog Timer Postscaler Select bits 1111 = 1:32,768 1110 = 1:16,384 1101 = 1:8,192 1100 = 1:4,096 1011 = 1:2,048 1010 = 1:1,024 1001 = 1:512 1000 = 1:256 0111 = 1:128 0110 = 1:64 0101 = 1:32 0100 = 1:16 0011 = 1:8 0010 = 1:4 0001 = 1:2 0000 = 1:1
WDTEN	CONFIG2H	Watchdog Timer Enable bit 1 = WDT enabled 0 = WDT disabled (control is placed on SWDTEN bit)
MCLRE	CONFIG3H	$\overline{\text{MCLR}}$ Pin Enable bit 1 = $\overline{\text{MCLR}}$ pin enabled, RA3 input pin disabled 0 = RA3 input pin enabled, $\overline{\text{MCLR}}$ pin disabled
HFOFST	CONFIG3H	HFINTOSC Fast Start 1 = HFINTOSC output is not delayed 0 = HFINTOSC output is delayed until oscillator is stable (IOFS = 1)
XINST	CONFIG4L	Extended Instruction Set Enable bit 1 = Instruction set extension and Indexed Addressing mode enabled 0 = Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
BBSIZ	CONFIG4L	Boot Block Size Select bit 1 = 2 kW Boot Block size for PIC18F14K50 (1 kW Boot Block size for PIC18F13K50) 0 = 1 kW Boot Block size for PIC18F14K50 (512 W Boot Block size for PIC18F13K50)
LVP	CONFIG4L	Low-Voltage Programming Enable bit 1 = Low-Voltage Programming enabled, RC3 is the PGM pin 0 = Low-Voltage Programming disabled, RC3 is an I/O pin

TABLE 7-1: CHECKSUM COMPUTATION

Device	Code-Protect BBSIZ = 0	Checksum	Blank Value	0xAA at 0 and Max Address
PIC18F14K50	None	SUM[0000:01FFF]+SUM[2000:3FFF]+ (CONFIG1L & 38h)+(CONFIG1H & FFh)+(CONFIG2L & 1Fh)+ (CONFIG2H & 1F)+(CONFIG3L & 00h)+(CONFIG3H & 88h)+ (CONFIG4L & 4Dh)+(CONFIG4H & 00h)+(CONFIG5L & 03h)+ (CONFIG5H & C0h)+(CONFIG6L & 03h)+(CONFIG6H & E0h)+ (CONFIG7L & 03h)+(CONFIG7H & 40h)	C2DB	C231
	Boot Block	SUM[0800:1FFF]+SUM[2000:3FFF]+ (CONFIG1L & 38h)+(CONFIG1H & FFh)+(CONFIG2L & 1Fh)+ (CONFIG2H & 1F)+(CONFIG3L & 00h)+ (CONFIG3H & 88h)+ (CONFIG4L & 4Dh)+(CONFIG4H & 00h)+(CONFIG5L & 03h)+ (CONFIG5H & C0h)+(CONFIG6L & 03h)+(CONFIG6H & E0h)+ (CONFIG7L & 03h)+(CONFIG7H & 40h)+SUM_ID	CAC1	CA58
	Boot/ Block 0	SUM[2000:3FFF]+ (CONFIG1L & 38h)+(CONFIG1H & FFh)+(CONFIG2L & 1Fh)+ (CONFIG2H & 1F)+(CONFIG3L & 00h)+(CONFIG3H & 88h)+ (CONFIG4L & 4Dh)+(CONFIG4H & 00h)+(CONFIG5L & 03h)+ (CONFIG5H & C0h)+(CONFIG6L & 03h)+(CONFIG6H & E0h)+ (CONFIG7L & 03h)+(CONFIG7H & 40h)+SUM_ID	E2C0	E257
	All	(CONFIG1L & 38h)+(CONFIG1H & FFh)+(CONFIG2L & 1Fh)+ (CONFIG2H & 1F)+(CONFIG3L & 00h)+(CONFIG3H & 88h)+ (CONFIG4L & 4Dh)+(CONFIG4H & 00h)+(CONFIG5L & 03h)+ (CONFIG5H & C0h)+(CONFIG6L & 03h)+(CONFIG6H & E0h)+ (CONFIG7L & 03h)+(CONFIG7H & 40h)+SUM_ID	02BE	02AA
PIC18F13K50	None	SUM[0000:0FFF]+SUM[1000:1FFF]+ (CONFIG1L & 38h)+(CONFIG1H & FFh)+(CONFIG2L & 1Fh)+ (CONFIG2H & 1F)+(CONFIG3L & 00h)+(CONFIG3H & 88h)+ (CONFIG4L & 4Dh)+(CONFIG4H & 00h)+(CONFIG5L & 03h)+ (CONFIG5H & C0h)+(CONFIG6L & 03h)+(CONFIG6H & E0h)+ (CONFIG7L & 03h)+(CONFIG7H & 40h)	E2DB	E231
	Boot Block	SUM[0400:0FFF]+SUM[1000:1FFF]+ (CONFIG1L & 38h)+(CONFIG1H & FFh)+(CONFIG2L & 1Fh)+ (CONFIG2H & 1F)+(CONFIG3L & 00h)+ (CONFIG3H & 88h)+ (CONFIG4L & 4Dh)+(CONFIG4H & 00h)+(CONFIG5L & 03h)+ (CONFIG5H & C0h)+(CONFIG6L & 03h)+(CONFIG6H & E0h)+ (CONFIG7L & 03h)+(CONFIG7H & 40h)+SUM_ID	E6C3	E65A
	Boot/ Block 0	SUM[1000:1FFF]+ (CONFIG1L & 38h)+(CONFIG1H & FFh)+(CONFIG2L & 1Fh)+ (CONFIG2H & 1F)+(CONFIG3L & 00h)+(CONFIG3H & 88h)+ (CONFIG4L & 4Dh)+(CONFIG4H & 00h)+(CONFIG5L & 03h)+ (CONFIG5H & C0h)+(CONFIG6L & 03h)+(CONFIG6H & E0h)+ (CONFIG7L & 03h)+(CONFIG7H & 40h)+SUM_ID	F2C2	F259
	All	(CONFIG1L & 38h)+(CONFIG1H & FFh)+(CONFIG2L & 1Fh)+ (CONFIG2H & 1F)+(CONFIG3L & 00h)+(CONFIG3H & 88h)+ (CONFIG4L & 4Dh)+(CONFIG4H & 00h)+(CONFIG5L & 03h)+ (CONFIG5H & C0h)+(CONFIG6L & 03h)+(CONFIG6H & E0h)+ (CONFIG7L & 03h)+(CONFIG7H & 40h)+SUM_ID	02C0	02AC

Legend:

Item		Description
CONFIGx	=	Configuration Word
SUM[a:b]	=	Sum of locations, a to b inclusive
SUM_ID	=	Byte-wise sum of lower four bits of all customer ID locations
+	=	Addition
&	=	Bit-wise AND

8.1 AC/DC Characteristics Timing Requirements for Program/Verify Test Mode

Standard Operating Conditions Operating Temperature: 25°C is recommended						
Param No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
D110	VIHH	High-Voltage Programming Voltage on MCLR/VPP/RA3	8	9	V	
D110A	VIHL	Low-Voltage Programming Voltage on MCLR/VPP/RA3	1.80	VDD	V	
D111	VDD	PIC18F1XK50 (includes Bulk Erase)	2.70	5.50	V	
		PIC18LF1XK50 (includes Bulk Erase)	2.70	3.60	V	
D112	IPP	Programming Current on MCLR/VPP/RA3	—	5	mA	
D113	IDDP	Supply Current During Programming	—	5	mA	
D031	VIL	Input Low Voltage	VSS	0.2 VDD	V	
D041	VIH	Input High Voltage	0.8 VDD	VDD	V	Except RA0 and RA1
D042	VIH	Input High Voltage on RA0 and RA1 pins only	0.8 VDD	VDD	V	VDD < 3.6V
D080	VOL	Output Low Voltage	—	0.6	V	IOL = 3.0 mA @ 2.7V
D090	VOH	Output High Voltage	VDD – 0.7	—	V	IOH = -2.0 mA @ 2.7V
D091	VOH	Output High Voltage on RA0 pin only	VUSB – 0.7 MIN	—	V	
D012	CIO	Capacitive Loading on I/O pin (PGD)	—	50	pF	To meet AC specifications
P1	TR	MCLR/VPP/RA3 Rise Time to enter Program/Verify mode	—	1.0	μs	**(Note 1)**
P2	TPGC	Serial Clock (PGC) Period	100	—	ns	VDD = 3.6V
			1	—	μs	VDD = 1.8V
P2A	TPGCL	Serial Clock (PGC) Low Time	40	—	ns	VDD = 3.6V
			400	—	ns	VDD = 1.8V
P2B	TPGCH	Serial Clock (PGC) High Time	40	—	ns	VDD = 3.6V
			400	—	ns	VDD = 1.8V
P3	TSET1	Input Data Setup Time to Serial Clock ↓	15	—	ns	
P4	THLD1	Input Data Hold Time from PGC ↓	15	—	ns	
P5	TDLY1	Delay between 4-bit Command and Command Operand	40	—	ns	
P5A	TDLY1A	Delay between 4-bit Command Operand and next 4-bit Command	40	—	ns	
P6	TDLY2	Delay between Last PGC ↓ of Command Byte to First PGC ↑ of Read of Data Word	20	—	ns	
P9	TDLY5	PGC High Time (minimum programming time)	1	—	ms	Externally Timed
P9A	TDLY5A	PGC High Time	5		ms	Configuration Word programming time
P10	TDLY6	PGC Low Time after Programming (high-voltage discharge time)	100	—	μs	
P11	TDLY7	Delay to allow Self-Timed Data Write or Bulk Erase to occur	5	—	ms	

Note 1: Do not allow excess time when transitioning MCLR between VIL and VIHH; this can cause spurious program executions to occur. The maximum transition time is:
1 TCY + TPWRT (if enabled) + 1024 TOSC (for LP, HS, HS/PLL and XT modes only) + 2 ms (for HS/PLL mode only) + 1.5 μs (for EC mode only) where TCY is the instruction cycle time, TPWRT is the Power-up Timer period and TOSC is the oscillator period. For specific values, refer to the Electrical Characteristics section of the device data sheet for the particular device.

REVISION HISTORY

Revision A (January 2008)

Original Programming Specification release.

Revision B (September 2008)

Updated to add VREG to Config 2L. Various minor edits.

Revision C (January 2009)

Updated to replace some data in Table 8.1. Various minor edits.

Revision D (04/2009)

Minor edits.

Revision E (05/2010)

Updated Table 3-1, Figure 3-1 and Figure 3-2.

NOTES:

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