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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	17
Program Memory Size	1KB (1K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	<a href="https://www.e-xfl.com/product-detail/zilog/z8f0130hh020sg">https://www.e-xfl.com/product-detail/zilog/z8f0130hh020sg</a>

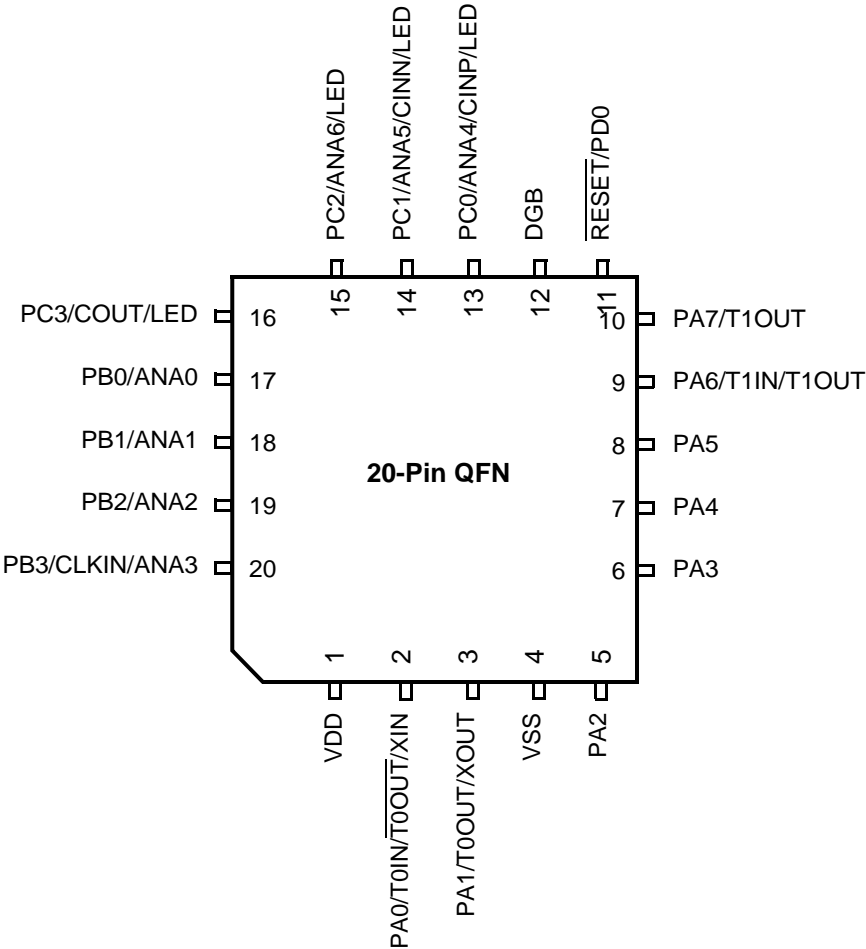


Figure 4. Z8F0830 Series in 20-Pin QFN Package

## Signal Descriptions

Table 4 describes the Z8 Encore! F0830 Series signals. See the [Pin Configurations](#) section on page 7 to determine the signals available for each specific package style.

**Table 4. Signal Descriptions**

Signal Mnemonic	I/O	Description
<b>General-Purpose I/O Ports A–D</b>		
PA[7:0]	I/O	Port A. These pins are used for general purpose I/O.
PB[7:0]	I/O	Port B. These pins are used for general purpose I/O. PB6 and PB7 are available only in those devices without an ADC.
PC[7:0]	I/O	Port C. These pins are used for general purpose I/O.
PD[0]	I/O	Port D. This pin is used for general purpose output only.
Note: PB6 and PB7 are only available in 28-pin packages without ADC. In 28-pin packages with ADC, they are replaced by $AV_{DD}$ and $AV_{SS}$ .		
<b>Timers</b>		
T0OUT/T1OUT	O	Timer output 0–1. These signals are the output from the timers.
$\overline{T0OUT}/\overline{T1OUT}$	O	Timer complement output 0–1. These signals are output from the timers in PWM DUAL OUTPUT Mode.
T0IN/T1IN	I	Timer Input 0–1. These signals are used as the capture, gating and counter inputs. The T0IN signal is multiplexed T0OUT signals.
<b>Comparator</b>		
CINP/CINN	I	Comparator inputs. These signals are the positive and negative inputs to the comparator.
COUT	O	Comparator output. This is the output of the comparator.
<b>Analog</b>		
ANA[7:0]	I	Analog port. These signals are used as inputs to the analog-to-digital converter (ADC).
$V_{REF}$	I/O	Analog-to-digital converter reference voltage input.
<b>Note:</b> When configuring ADC using external $V_{REF}$ , PB5 is used as $V_{REF}$ in 28-pin package.		
Note: The $AV_{DD}$ and $AV_{SS}$ signals are available only in the 28-pin packages with ADC. They are replaced by PB6 and PB7 on 28-pin packages without ADC.		

## Data Memory

The Z8 Encore! F0830 Series does not use the eZ8 CPU's 64KB data memory address space.

## Flash Information Area

Table 7 maps the Z8 Encore! F0830 Series Flash information area. The 128-byte information area is accessed, by setting bit 7 of the Flash Page Select Register to 1. When access is enabled, the Flash information area is mapped into program memory and overlays these 128 bytes at addresses FE00H to FE7FH. When information area access is enabled, all reads from these program memory addresses return information area data rather than program memory data. Access to the Flash information area is read-only.

**Table 7. Z8 Encore! F0830 Series Flash Memory Information Area Map**

<b>Program Memory Address (Hex)</b>	<b>Function</b>
FE00–FE3F	Zilog option bits
FE40–FE53	Part Number 20-character ASCII alphanumeric code Left-justified and filled with FH
FE54–FE5F	Reserved
FE60–FE7F	Reserved
FE80–FFFF	Reserved

## Interrupt Edge Select Register

The interrupt edge select (IRQES) register determines whether an interrupt is generated for the rising edge or falling edge on the selected GPIO Port A or Port D input pin. See Table 47.

**Table 47. Interrupt Edge Select Register (IRQES)**

Bit	7	6	5	4	3	2	1	0
Field	IES7	IES6	IES5	IES4	IES3	IES2	IES1	IES0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FCDH							

Bit	Description
[7]	<b>Interrupt Edge Select x</b>
IESx	0 = An interrupt request is generated on the falling edge of the PAX input or PDx. 1 = An interrupt request is generated on the rising edge of the PAX input or PDx.

Note: x indicates register bits in the address range 7–0.

6. Write to the Timer Control Register to enable the timer.
7. Counting begins on the first appropriate transition of the timer input signal. No interrupt is generated by the first edge.

In CAPTURE/COMPARE Mode, the elapsed time from timer start to capture event can be calculated using the following equation:

$$\text{Capture Elapsed Time (s)} = \frac{(\text{Capture Value} - \text{Start Value}) \times \text{Prescale}}{\text{System Clock Frequency (Hz)}}$$

## Reading the Timer Count Values

The current count value in the timers can be read while counting (enabled). This capability has no effect on Timer operation. When the timer is enabled and the Timer High Byte Register is read, the contents of the timer low byte register are placed in a holding register. A subsequent read from the timer low byte register returns the value in the holding register. This operation allows accurate reads of the full 16-bit timer count value when enabled. When the timers are not enabled, a read from the timer low byte register returns the actual value in the counter.

## Timer Pin Signal Operation

Timer output is a GPIO port pin alternate function. The timer output is toggled every time the counter is reloaded.

The timer input can be used as a selectable counting source. It shares the same pin as the complementary timer output. When selected by the GPIO alternate function registers, this pin functions as a timer input in all modes except for the DUAL PWM OUTPUT Mode. For this mode, no timer input is available.

# Comparator

The Z8 Encore! F0830 Series devices feature a general purpose comparator that compares two analog input signals. A GPIO (CINP) pin provides the positive comparator input. The negative input (CINN) can be taken from either an external GPIO pin or from an internal reference. The output is available as an interrupt source or can be routed to an external pin using the GPIO multiplex. The comparator includes the following features:

- Positive input is connected to a GPIO pin
- Negative input can be connected to either a GPIO pin or a programmable internal reference
- Output can be either an interrupt source or an output to an external pin

## Operation

One of the comparator inputs can be connected to an internal reference that is a user-selectable reference and is user-programmable with 200mV resolution.

The comparator can be powered down to save supply current. For details, see the [Power Control Register 0](#) section on page 31.

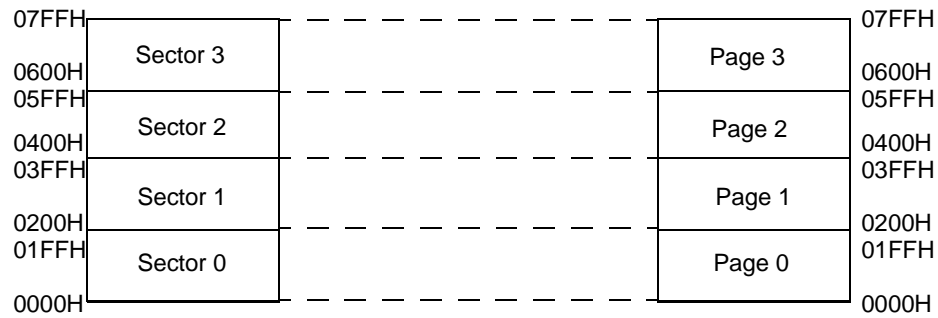
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**! Caution:** As a result of the propagation delay of the comparator, Zilog does not recommend enabling the comparator without first disabling interrupts and waiting for the comparator output to settle. This delay prevents spurious interrupts after comparator enabling.

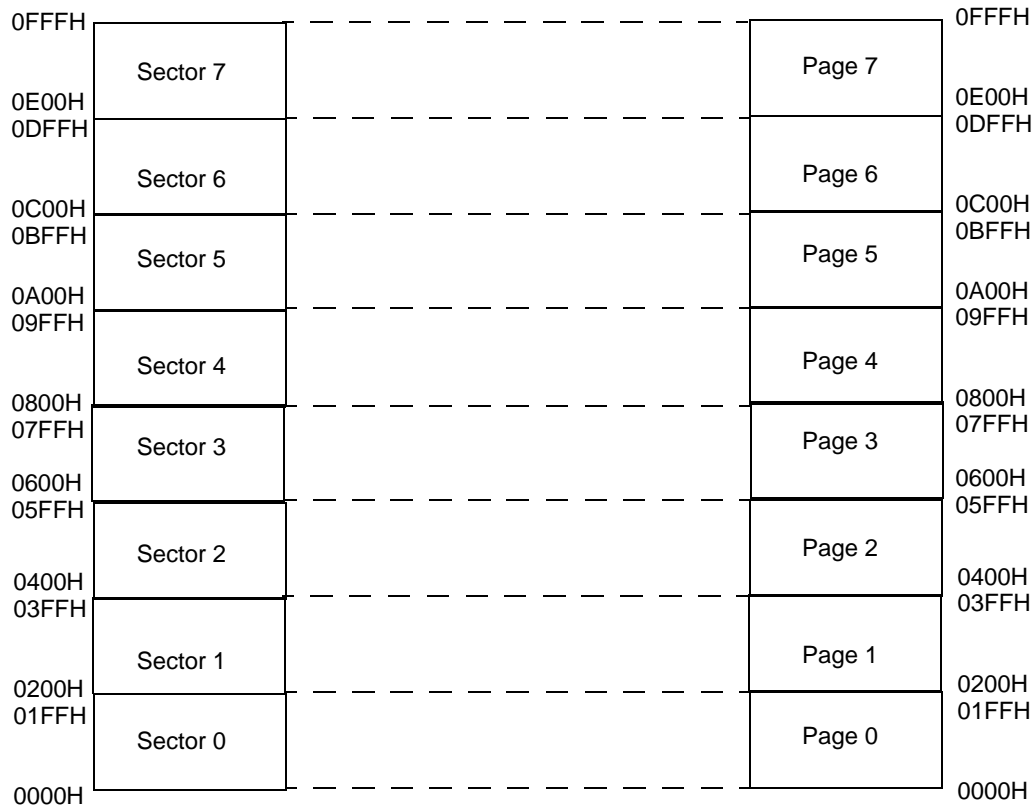
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The following example shows how to safely enable the comparator:

```
di
ld cmp0,r0; load some new configuration
nop
nop      ; wait for output to settle
clr irq0 ; clear any spurious interrupts pending
ei
```



**Figure 15. 2K Flash with NVDS**



**Figure 16. 4K Flash with NVDS**



## Flash Page Select Register

The Flash Page Select Register shares address space with the Flash Sector Protect Register. Unless the Flash Controller is locked and written with 5EH, any writes to this address will target the Flash Page Select Register.

The register selects one of the eight available Flash memory pages to be programmed or erased. Each Flash page contains 512-bytes of Flash memory. During a page erase operation, all Flash memory containing addresses with the most significant 7-bits within FPS[6:0] are chosen for program/erase operations.

**Table 74. Flash Page Select Register (FPS)**

Bit	7	6	5	4	3	2	1	0
Field	INFO_EN	PAGE						
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FF9H							

Bit	Description
[7] INFO_EN	<b>Information Area Enable</b> 0 = Information area is not selected. 1 = Information area is selected. The information area is mapped into the program memory address space at addresses FE00H through FFFFH.
[6:0] PAGE	<b>Page Select</b> This 7-bit field identifies the Flash memory page for page erase and page unlocking. Program memory address[15:9] = PAGE[6:0]. For Z8F04xx and Z8F02xx devices, the upper four bits must always be 0. For Z8F01xx devices, the upper five bits must always be 0.

Bit	Description (Continued)
[3] VBO_AO	<b>Voltage Brown-Out Protection Always On</b> 0 = Voltage Brown-Out protection is disabled in STOP Mode to reduce total power consumption. 1 = Voltage Brown-Out protection is always enabled, even during STOP Mode. This setting is the default setting for unprogrammed (erased) Flash.
[2] FRP	<b>Flash Read Protect</b> 0 = User program code is inaccessible. Limited control features are available through the On-Chip Debugger. 1 = User program code is accessible. All On-Chip Debugger commands are enabled. This is the default setting for unprogrammed (erased) Flash.
[1]	<b>Reserved</b> This bit is reserved and must be programmed to 1.
[0] FWP	<b>Flash Write Protect</b> This option bit provides Flash program memory protection. 0 = Programming and erasure disabled for all Flash program memory. Programming, page erase and mass erase through user code is disabled. Mass erase is available using the On-Chip Debugger. 1 = Programming, page erase and mass erase are enabled for all Flash program memory.

**Table 82. Flash Options Bits at Program Memory Address 0001H**

Bit	7	6	5	4	3	2	1	0
Field	VBO_RES	Reserved		XTLDIS	Reserved			
RESET	U	U	U	U	U	U	U	U
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	Program Memory 0001H							
Note: U = Unchanged by Reset. R/W = Read/Write.								

Bit	Description
[7] VBO_RES	<b>Voltage Brown-Out reset</b> 1 = VBO detection causes a system reset. This setting is the default setting for unprogrammed (erased) Flash.
[6:5]	<b>Reserved</b> These bits are reserved and must be programmed to 11.

## Byte Write

To write a byte to the NVDS array, the user code must first push the address, then the data byte onto the stack. The user code issues a `CALL` instruction to the address of the Byte Write routine (`0x20B3`). At the return from the subroutine, the write status byte resides in working register R0. The bit fields of this status byte are defined in Table 91. Additionally, user code should pop the address and data bytes off the stack.

The write routine uses 16 bytes of stack space in addition to the two bytes of address and data pushed by the user code. Sufficient memory must be available for this stack usage.

Because of the Flash memory architecture, NVDS writes exhibit a nonuniform execution time. In general, a write takes 136 $\mu$ s (assuming a 20MHz system clock). For every 200 writes, however, a maintenance operation is necessary. In this rare occurrence, the write takes up to 58ms to complete. Slower system clock speeds result in proportionally higher execution times.

NVDS byte writes to invalid addresses (those exceeding the NVDS array size) have no effect. Illegal write operations have a 7 $\mu$ s execution time.

**Table 91. Write Status Byte**

Bit	7	6	5	4	3	2	1	0
Field	Reserved					FE	IGADDR	WE
Default Value	0	0	0	0	0	0	0	0

Bit	Description
[7:3]	<b>Reserved</b> These bits are reserved and must be programmed to 00000.
[2] FE	<b>Flash Error</b> If a Flash error is detected, this bit is set to 1.
[1] IGADDR	<b>Illegal Address</b> When an NVDS byte writes to invalid addresses occur (those exceeding the NVDS array size), this bit is set to 1.
[0] WE	<b>Write Error</b> A failure occurs during data writes to Flash. When writing data into a certain address, a read-back operation is performed. If the read-back value is not the same as the value written, this bit is set to 1.

```
DBG ← 0AH
DBG ← Program Memory Address[15:8]
DBG ← Program Memory Address[7:0]
DBG ← Size[15:8]
DBG ← Size[7:0]
DBG ← 1-65536 data bytes
```

**Read Program Memory (0BH).** The read program memory command, reads data from program memory. This command is equivalent to the LDC and LDCI instructions. Data can be read 1–65536 bytes at a time (65536 bytes can be read by setting size to 0). If the device is not in DEBUG Mode or if the Flash read protect option bit is enabled, this command returns FFH for the data.

```
DBG ← 0BH
DBG ← Program Memory Address[15:8]
DBG ← Program Memory Address[7:0]
DBG ← Size[15:8]
DBG ← Size[7:0]
DBG → 1-65536 data bytes
```

**Write Data Memory (0CH).** The write data memory command, writes data to data memory. This command is equivalent to the LDE and LDEI instructions. Data can be written 1–65536 bytes at a time (65536 bytes can be written by setting size to 0). If the device is not in DEBUG Mode or if the flash read protect option bit is enabled, the data is discarded.

```
DBG ← 0CH
DBG ← Data Memory Address[15:8]
DBG ← Data Memory Address[7:0]
DBG ← Size[15:8]
DBG ← Size[7:0]
DBG ← 1-65536 data bytes
```

**Read Data Memory (0DH).** The read data memory command, reads from data memory. This command is equivalent to the LDE and LDEI instructions. Data can be read from 1 to 65536 bytes at a time (65536 bytes can be read by setting size to 0). If the device is not in DEBUG Mode, this command returns FFH for the data.

```
DBG ← 0DH
DBG ← Data Memory Address[15:8]
DBG ← Data Memory Address[7:0]
DBG ← Size[15:8]
DBG ← Size[7:0]
DBG → 1-65536 data bytes
```

**Read Program Memory CRC (0EH).** The read program memory CRC command, computes and returns the cyclic redundancy check (CRC) of program memory using the 16-bit CRC-CCITT polynomial. If the device is not in DEBUG Mode, this command returns FFFFH for the CRC value. Unlike the other OCD read commands, there is a delay from issuing of the command until the OCD returns the data. The OCD reads program memory, calculates the CRC value and returns the result. The delay is a function of program mem-

Table 113. eZ8 CPU Instruction Summary (Continued)

Assembly Mnemonic	Symbolic Operation	Address Mode		Op Code(s) (Hex)	Flags						Fetch Cycles	Instr. Cycles
		dst	src		C	Z	S	V	D	H		
DJNZ dst, RA	$\text{dst} \leftarrow \text{dst} - 1$ if $\text{dst} \neq 0$ $\text{PC} \leftarrow \text{PC} + X$	r		0A–FA	–	–	–	–	–	–	2	3
EI	$\text{IRQCTL}[7] \leftarrow 1$			9F	–	–	–	–	–	–	1	2
HALT	HALT Mode			7F	–	–	–	–	–	–	1	2
INC dst	$\text{dst} \leftarrow \text{dst} + 1$	R		20	–	*	*	–	–	–	2	2
		IR		21							2	3
		r		0E–FE							1	2
INCW dst	$\text{dst} \leftarrow \text{dst} + 1$	RR		A0	–	*	*	*	–	–	2	5
		IRR		A1							2	6
IRET	$\text{FLAGS} \leftarrow @\text{SP}$ $\text{SP} \leftarrow \text{SP} + 1$ $\text{PC} \leftarrow @\text{SP}$ $\text{SP} \leftarrow \text{SP} + 2$ $\text{IRQCTL}[7] \leftarrow 1$			BF	*	*	*	*	*	*	1	5
JP dst	$\text{PC} \leftarrow \text{dst}$	DA		8D	–	–	–	–	–	–	3	2
		IRR		C4							2	3
JP cc, dst	if cc is true $\text{PC} \leftarrow \text{dst}$	DA		0D–FD	–	–	–	–	–	–	3	2
JR dst	$\text{PC} \leftarrow \text{PC} + X$	DA		8B	–	–	–	–	–	–	2	2
JR cc, dst	if cc is true $\text{PC} \leftarrow \text{PC} + X$	DA		0B–FB	–	–	–	–	–	–	2	2

Note: Flags Notation:

\* = Value is a function of the result of the operation.

– = Unaffected.

X = Undefined.

0 = Reset to 0.

1 = Set to 1.

Table 113. eZ8 CPU Instruction Summary (Continued)

Assembly Mnemonic	Symbolic Operation	Address Mode		Op Code(s) (Hex)	Flags						Fetch Cycles	Instr. Cycles
		dst	src		C	Z	S	V	D	H		
TM dst, src	dst AND src	r	r	72	–	*	*	0	–	–	2	3
		r	lr	73							2	4
		R	R	74							3	3
		R	IR	75							3	4
		R	IM	76							3	3
		IR	IM	77							3	4
TMX dst, src	dst AND src	ER	ER	78	–	*	*	0	–	–	4	3
		ER	IM	79							4	3
TRAP Vector	SP ← SP – 2 @SP ← PC SP ← SP – 1 @SP ← FLAGS PC ← @Vector		Vec- tor	F2	–	–	–	–	–	–	2	6
WDT				5F	–	–	–	–	–	–	1	2
XOR dst, src	dst ← dst XOR src	r	r	B2	–	*	*	0	–	–	2	3
		r	lr	B3							2	4
		R	R	B4							3	3
		R	IR	B5							3	4
		R	IM	B6							3	3
		IR	IM	B7							3	4
XORX dst, src	dst ← dst XOR src	ER	ER	B8	–	*	*	0	–	–	4	3
		ER	IM	B9							4	3

Note: Flags Notation:

\* = Value is a function of the result of the operation.

– = Unaffected.

X = Undefined.

0 = Reset to 0.

1 = Set to 1.

## General Purpose I/O Port Input Data Sample Timing

Figure 33 displays timing of the GPIO port input sampling. The input value on a GPIO port pin is sampled on the rising edge of the system clock. The port value is available to the eZ8 CPU on the second rising clock edge following the change of the port value.

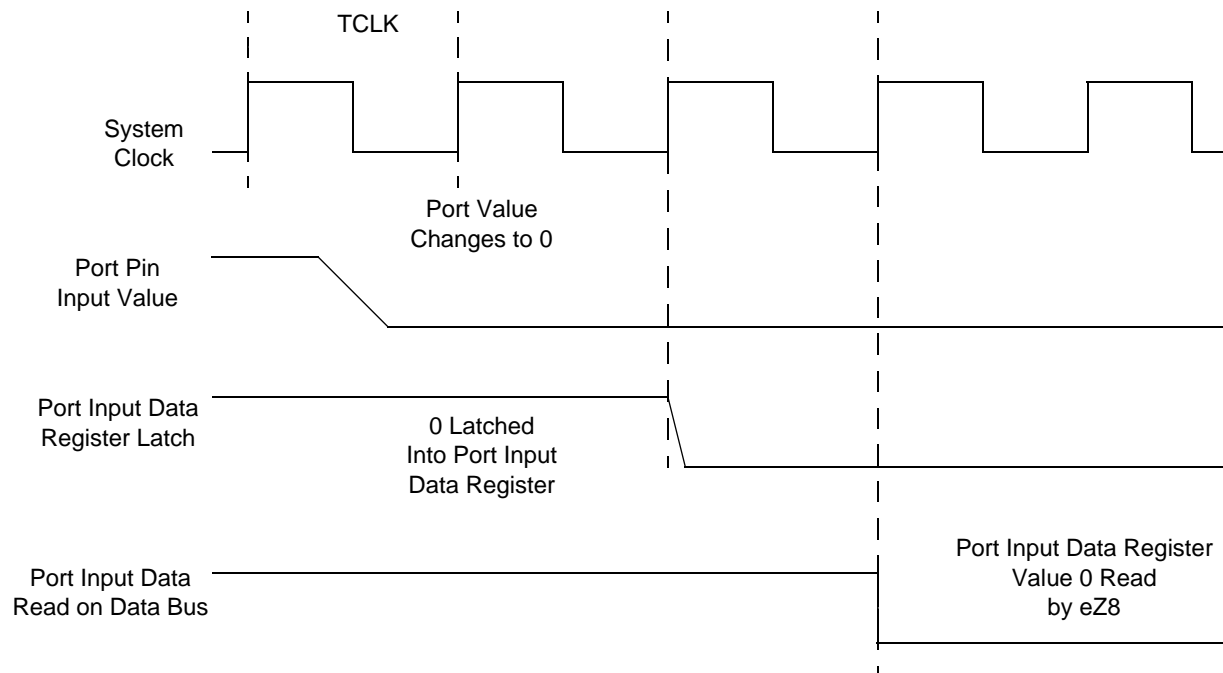


Figure 33. Port Input Sample Timing

Table 124. GPIO Port Input Timing

Parameter	Abbreviation	Delay (ns)	
		Minimum	Maximum
$T_{S\_PORT}$	Port Input Transition to $X_{IN}$ Rise Setup Time (not pictured)	5	–
$T_{H\_PORT}$	$X_{IN}$ Rise to Port Input Transition Hold Time (not pictured)	0	–
$T_{SMR}$	GPIO port pin pulse width to ensure Stop Mode Recovery (for GPIO port pins enabled as SMR sources)	1 $\mu$ s	

General Purpose I/O Port Output Timing

Figure 34 and Table 125 provide timing information for the GPIO port pins.

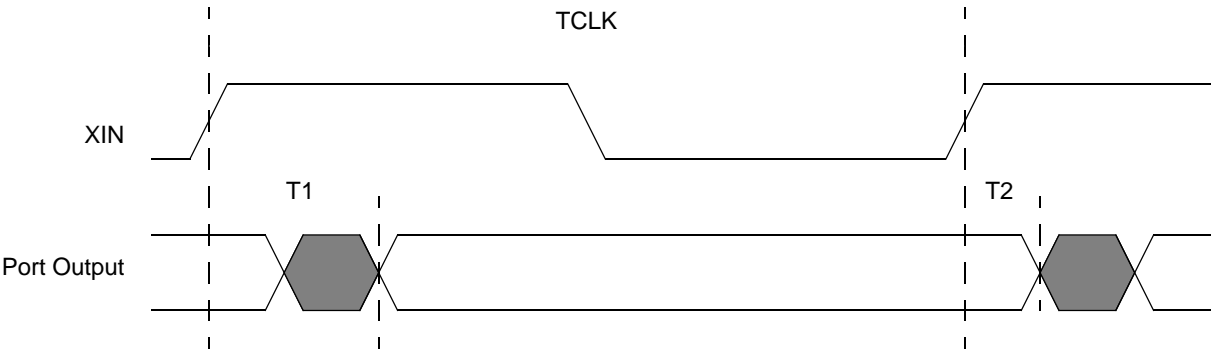


Figure 34. GPIO Port Output Timing

Table 125. GPIO Port Output Timing

Parameter	Abbreviation	Delay (ns)	
		Minimum	Maximum
GPIO Port Pins			
T <sub>1</sub>	XIN Rise to Port Output Valid Delay	–	15
T <sub>2</sub>	XIN Rise to Port Output Hold Time	2	–



**Table 128. Z8 Encore! XP F0830 Series Ordering Matrix**

Part Number	Flash	RAM	NVDS	ADC Channels	Description
Z8F0131PJ020SG	1KB	256	Yes	0	PDIP 28-pin
Z8F0131QJ020SG	1KB	256	Yes	0	QFN 28-pin
<b>Extended Temperature: –40°C to 105°C</b>					
Z8F0130SH020EG	1KB	256	Yes	7	SOIC 20-pin
Z8F0130HH020EG	1KB	256	Yes	7	SSOP 20-pin
Z8F0130PH020EG	1KB	256	Yes	7	PDIP 20-pin
Z8F0130QH020EG	1KB	256	Yes	7	QFN 20-pin
Z8F0131SH020EG	1KB	256	Yes	0	SOIC 20-pin
Z8F0131HH020EG	1KB	256	Yes	0	SSOP 20-pin
Z8F0131PH020EG	1KB	256	Yes	0	PDIP 20-pin
Z8F0131QH020EG	1KB	256	Yes	0	QFN 20-pin
Z8F0130SJ020EG	1KB	256	Yes	8	SOIC 28-pin
Z8F0130HJ020EG	1KB	256	Yes	8	SSOP 28-pin
Z8F0130PJ020EG	1KB	256	Yes	8	PDIP 28-pin
Z8F0130QJ020EG	1KB	256	Yes	8	QFN 28-pin
Z8F0131SJ020EG	1KB	256	Yes	0	SOIC 28-pin
Z8F0131HJ020EG	1KB	256	Yes	0	SSOP 28-pin
Z8F0131PJ020EG	1KB	256	Yes	0	PDIP 28-pin
Z8F0131QJ020EG	1KB	256	Yes	0	QFN 28-pin
ZUSBSC00100ZACG					USB Smart Cable Accessory Kit
ZUSBOPTSC01ZACG					Opto-Isolated USB Smart Cable Accessory Kit

## Part Number Suffix Designations

Zilog part numbers consist of a number of components, as indicated in the following example.

**Example.** Part number Z8F0830SH020SG is an 8-bit 20MHz Flash MCU with 8KB Program Memory and equipped with ADC and NVDS in a 20-pin SOIC package, operating within a 0°C to +70°C temperature range and built using lead-free solder.

Table 129 lists the pin count by package.

**Table 129. Package and Pin Count Description**

<b>Package</b>	<b>Pin Count</b>	
	<b>20</b>	<b>28</b>
PDIP	√	√
QFN	√	√
SOIC	√	√
SSOP	√	√

### Hex Address: F71

This address range is reserved.

### Hex Address: F72

Table 147. ADC Data High Byte Register (ADCD\_H)

Bit	7	6	5	4	3	2	1	0
Field	ADCDH							
RESET	X							
R/W	R							
Address	F72H							

Bit	Description
[7:0]	<b>ADC High Byte</b> 00h–FFh = The last conversion output is held in the data registers until the next ADC conversion is completed.

### Hex Address: F73

Table 148. ADC Data Low Bits Register (ADCD\_L)

Bit	7	6	5	4	3	2	1	0
Field	ADCDL		Reserved					
RESET	X		X					
R/W	R		R					
Address	F73H							

Bit Position	Description
[7:6]	<b>ADC Low Bits</b> 00–11b = These bits are the two least significant bits of the 10-bit ADC output. These bits are undefined after a reset. The low bits are latched into this register whenever the ADC Data High Byte Register is read.
[5:0]	<b>Reserved</b> These bits are reserved and must be programmed to 000000.

**Hex Address: F83**

**Table 153. LED Drive Level High Register (LEDLVLH)**

Bit	7	6	5	4	3	2	1	0
Field	LEDLVLH[7:0]							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F83H							

**Hex Address: F84**

**Table 154. LED Drive Level Low Register (LEDLVLL)**

Bit	7	6	5	4	3	2	1	0
Field	LEDLVLL[7:0]							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F84H							

**Hex Address: F85**

This address range is reserved.

## Oscillator Control

For more information about the Oscillator Control registers, see the [Oscillator Control Register Definitions](#) section on page 154.

**Hex Address: F86**

**Table 155. Oscillator Control Register (OSCCTL)**

Bit	7	6	5	4	3	2	1	0
Field	INTEN	XTLEN	WDTEN	POFEN	WDFEN	SCKSEL		
RESET	1	0	1	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F86H							

- reload high and low byte registers 85
- timer control register definitions 83
- timer output signal operation 82
- timers 0-3
  - control registers 87, 88
  - high and low byte registers 83, 86
- TM 167
- TMX 167
- TRAP 169

## **V**

- vector 165
- voltage brown-out reset (VBR) 24
- voltage measurement timing diagram 100

## **W**

- watch-dog timer
  - approximate time-out delay 92
  - approximate time-out delays 92, 106, 134, 151, 161
  - CNTL 24
  - control register 95, 154
  - electrical characteristics and timing 194
  - interrupt in normal operation 93
  - interrupt in stop mode 93
  - operation 92, 106, 134, 151, 161
  - refresh 93
  - reload unlock sequence 94
  - reload upper, high and low registers 96
  - reset 25
  - reset in normal operation 94
  - reset in Stop mode 94
  - time-out response 93
- watchdog timer
  - refresh 168
- WDTCTL register 29, 95, 107, 154, 217, 218, 226
- WDTH register 96, 227
- WDTL register 97, 227
- working register 164
- working register pair 165
- WTDU register 96, 227

## **X**

- X 165
- XOR 169
- XORX 169

## **Z**

- Z8 Encore!
  - block diagram 3
  - features 1
  - part selection guide 2