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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	23
Program Memory Size	1KB (1K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f0130sj020eg

List of Tables

The analog supply pins (AV_{DD} and AV_{SS}) are also not available on these parts and are replaced by PB6 and PB7.

At reset, by default, all pins of Port A, B and C are in Input state. The alternate functionality is also disabled, so the pins function as general purpose input ports until programmed otherwise. At power-up, the Port D0 pin defaults to the $\overline{\text{RESET}}$ Alternate function.

The pin configurations listed are preliminary and subject to change based on manufacturing limitations.

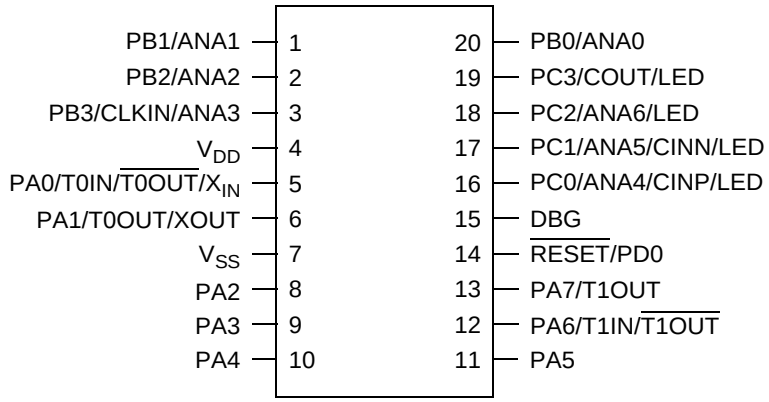

Figure 2. Z8F0830 Series in 20-Pin SOIC, SSOP, PDIP Package

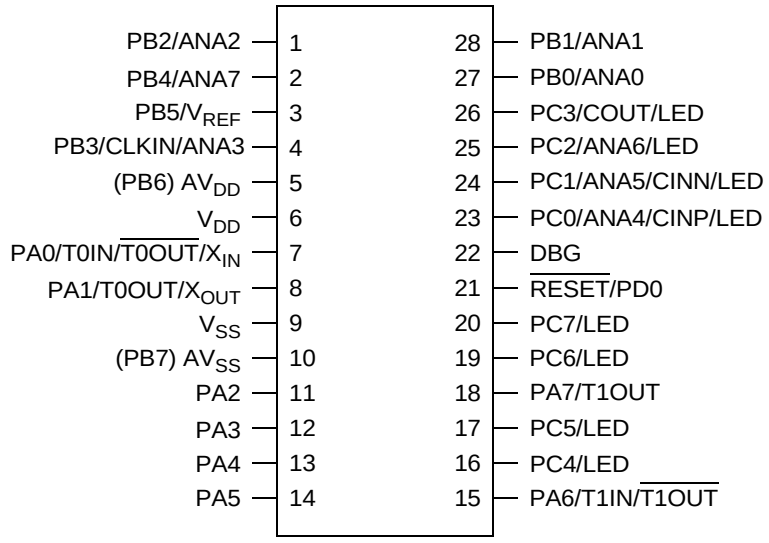

Figure 3. Z8F0830 Series in 28-Pin SOIC, SSOP, PDIP Package

Table 8. Register File Address Map (Continued)

Address (Hex)	Register Description	Mnemonic	Reset (Hex)	Page No.
Analog-to-Digital Converter (ADC, cont'd)				
F73	ADC data low bits	ADCD_L	XX	103
F74	ADC sample settling time	ADCSST	0F	104
F75	ADC sample time	ADCST	3F	105
F76	Reserved	—	XX	
F77–F7F	Reserved	—	XX	
Low Power Control				
F80	Power control 0	PWRCTL0	88	32
F81	Reserved	—	XX	
LED Controller				
F82	LED drive enable	LEDEN	00	51
F83	LED drive level high	LEDLVLH	00	51
F84	LED drive level low	LEDLVLL	00	52
F85	Reserved	—	XX	
Oscillator Control				
F86	Oscillator control	OSCCTL	A0	154
F87–F8F	Reserved	—	XX	
Comparator 0				
F90	Comparator 0 control	CMP0	14	107
F91–FBF	Reserved	—	XX	
Interrupt Controller				
FC0	Interrupt request 0	IRQ0	00	58
FC1	IRQ0 enable high bit	IRQ0ENH	00	61
FC2	IRQ0 enable low Bit	IRQ0ENL	00	61
FC3	Interrupt request 1	IRQ1	00	59
FC4	IRQ1 enable high bit	IRQ1ENH	00	62
FC5	IRQ1 enable low bit	IRQ1ENL	00	63
FC6	Interrupt request 2	IRQ2	00	60
FC7	IRQ2 enable high bit	IRQ2ENH	00	64
FC8	IRQ2 enable low bit	IRQ2ENL	00	64
FC9–FCC	Reserved	—	XX	
FCD	Interrupt edge select	IRQES	00	66

Note: XX = Undefined.

GPIO Interrupts

Many of the GPIO port pins can be used as interrupt sources. Some port pins can be configured to generate an interrupt request on either the rising edge or falling edge of the input pin signal. Other port pin interrupt sources, generate an interrupt when any edge occurs (both rising and falling). See the Interrupt Controller chapter on page 53 for more information about interrupts using the GPIO pins.

GPIO Control Register Definitions

Four registers for each port provide access to GPIO control, input data and output data; Table 17 lists these port registers. Use the Port A–D Address and Control registers together to provide access to subregisters for port configuration and control.

Table 17. GPIO Port Registers and Subregisters

Port Register Mnemonic	Port Register Name
P*x*ADDR	Port A–D Address Register (selects subregisters)
P*x*CTL	Port A–D Control Register (provides access to subregisters)
P*x*IN	Port A–D Input Data Register
P*x*OUT	Port A–D Output Data Register
Port Subregister Mnemonic	**Port Register Name**
P*x*DD	Data Direction
P*x*AF	Alternate Function
P*x*OC	Output Control (open-drain)
P*x*HDE	High Drive Enable
P*x*SMRE	Stop Mode Recovery Source Enable
P*x*PUE	Pull-Up Enable
PxAFS1	Alternate Function Set 1
PxAFS2	Alternate Function Set 2

Port A–D Alternate Function Set 2 Subregisters

The Port A–D Alternate Function Set 2 Subregister, shown in Table 28, is accessed through the Port A–D Control Register by writing 08H to the Port A–D Address Register. The Alternate Function Set 2 subregisters select the alternate function available at a port pin. Alternate functions selected by setting or clearing bits in this register are defined in Table 16 in the GPIO Alternate Functions section on page 34.

Note: Alternate function selection on the port pins must also be enabled, as described in the Port A–D Alternate Function Subregisters section on page 42.

Table 28. Port A–D Alternate Function Set 2 Subregisters (PxAFS2)

Bit	7	6	5	4	3	2	1	0
Field	PAFS27	PAFS26	PAFS25	PAFS24	PAFS23	PAFS22	PAFS21	PAFS20
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	If 08H in Port A–D Address Register, accessible through the Port A–D Control Register							

Bit	Description
[7:0] PAFS2x	**Port Alternate Function Set 2** 0 = The Port Alternate function is selected, as defined in Table 16 in the GPIO Alternate Functions section on page 34. 1 = The Port Alternate function is selected, as defined in Table 16 in the GPIO Alternate Functions section on page 34.

Note: x indicates the specific GPIO port pin number (7–0).

Table 43. IRQ1 Enable Low Bit Register (IRQ1ENL)

Bit	7	6	5	4	3	2	1	0
Field	PA7ENL	PA6CENL	PA5ENL	PA4ENL	PA3ENL	PA2ENL	PA1ENL	PA0ENL
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FC5H							

Bit	Description
[7] PA7ENL	**Port A Bit[7] Interrupt Request Enable Low Bit**
[6] PA6CENL	**Port A Bit[7] or Comparator Interrupt Request Enable Low Bit**
[5:0] PA*x*ENL	**Port A Bit[*x*] Interrupt Request Enable Low Bit** See the interrupt port select register for selection of either Port A or Port D as the interrupt source.

Note: *x* indicates register bits in the address range 5–0.

IRQ2 Enable High and Low Bit Registers

Table 44 describes the priority control for IRQ2. The IRQ2 Enable High and Low Bit registers, shown in Tables 45 and 46, form a priority-encoded enabling service for interrupts in the Interrupt Request 2 Register. Priority is generated by setting the bits in each register.

Table 44. IRQ2 Enable and Priority Encoding

IRQ2ENH[*x*]	IRQ2ENL[*x*]	Priority	Description
0	0	Disabled	Disabled
0	1	Level 1	Low
1	0	Level 2	Nominal
1	1	Level 3	High

Note: *x* indicates register bits in the address range 7–0.

Timers

The Z8 Encore! F0830 Series products contain up to two 16-bit reloadable timers that can be used for timing, event counting or generation of pulse width modulated (PWM) signals. The timers feature include:

- 16-bit reload counter
- Programmable prescaler with prescale values ranging from 1 to 128
- PWM output generation
- Capture and compare capability
- External input pin for timer input, clock gating or capture signal. External input pin signal frequency is limited to a maximum of one-fourth the system clock frequency
- Timer output pin
- Timer interrupt

Architecture

Figure 10 displays the architecture of the timers.

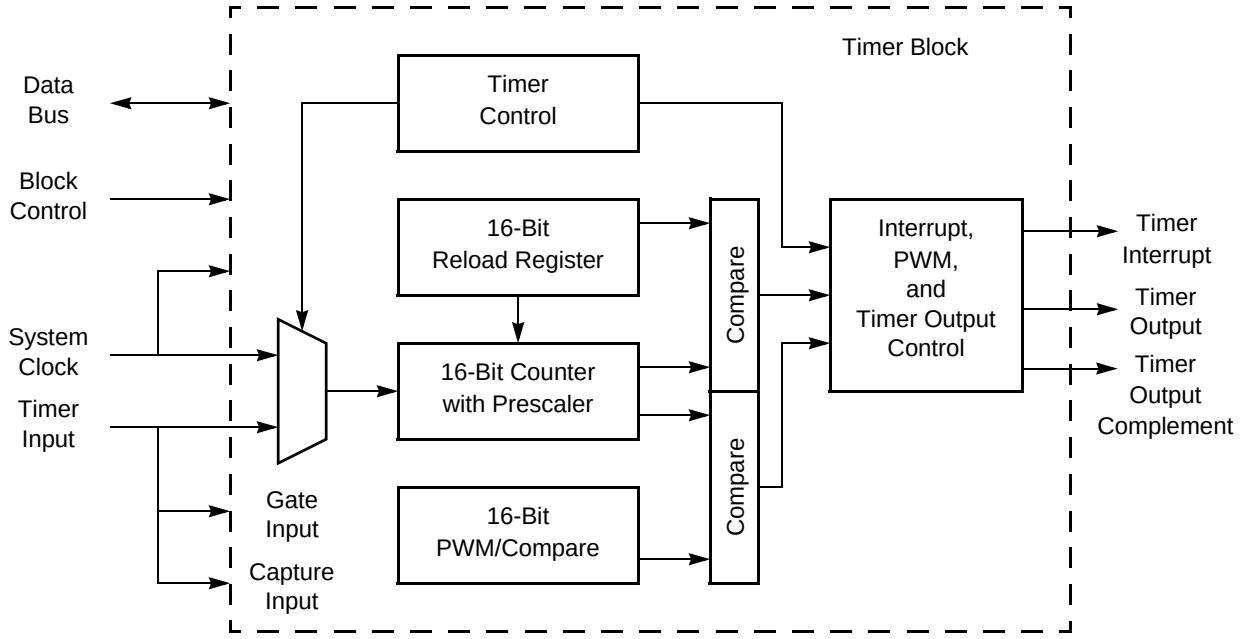

Figure 10. Timer Block Diagram

Operation

The timers are 16-bit up-counters. Minimum time-out delay is set by loading the value 0001H into the Timer Reload High and Low Byte registers and setting the prescale value to 1. Maximum time-out delay is set by loading the value 0000H into the Timer Reload High and Low Byte registers and setting the prescale value to 128. If the Timer reaches FFFFH, the timer resets back to 0000H and continues counting.

Timer Operating Modes

The timers can be configured to operate in the following modes:

ONE-SHOT Mode

In ONE-SHOT Mode, the timer counts up to the 16-bit reload value stored in the Timer Reload High and Low Byte registers. The timer input is the system clock. Upon reaching the reload value, the timer generates an interrupt and the count value in the Timer High and Low Byte registers is reset to 0001H. The timer is automatically disabled and stops counting.

Additionally, if the timer output alternate function is enabled, the timer output pin changes state for one system clock cycle (from Low to High or from High to Low) upon timer

4. Enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers.
5. If using the timer output function, configure the associated GPIO port pin for the timer output alternate function.
6. Write to the Timer Control Register to enable the timer and initiate counting.

In COMPARE Mode, the system clock always provides the timer input. The compare time can be calculated by the following equation:

$$\text{Compare Mode Time (s)} = \frac{(\text{Compare Value} - \text{Start Value}) \times \text{Prescale}}{\text{System Clock Frequency (Hz)}}$$

GATED Mode

In GATED Mode, the timer counts only when the timer input signal is in its active state (asserted), as determined by the TPOL bit in the Timer Control Register. When the timer input signal is asserted, counting begins. A timer interrupt is generated when the timer input signal is deasserted or a timer reload occurs. To determine whether the timer input signal deassertion generated the interrupt, read the associated GPIO input value and compare to the value stored in the TPOL bit.

The timer counts up to the 16-bit reload value stored in the Timer Reload High and Low Byte registers. The timer input is the system clock. Upon reaching the reload value, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to `0001H` and counting resumes (assuming the timer input signal remains asserted). Additionally, if the timer output alternate function is enabled, the timer output pin changes state (from Low to High or from High to Low) at timer reset.

Observe the following steps for configuring a timer for GATED Mode and for initiating the count:

1. Write to the Timer Control Register to:
   - Disable the timer
   - Configure the timer for GATED Mode
   - Set the prescale value
2. Write to the Timer High and Low Byte registers to set the starting count value. Writing these registers only affects the first pass in GATED Mode. After the first timer reset in GATED Mode, counting always begins at the reset value of `0001H`.
3. Write to the Timer Reload High and Low Byte registers to set the reload value.
4. Enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers. By default, the timer interrupt is generated for both input deasser-

Flash Operation Timing Using the Flash Frequency Registers

Before performing either a Program or Erase operation on Flash memory, the user must first configure the Flash Frequency High and Low Byte registers. The Flash frequency registers allow programming and erasing of the Flash with system clock frequencies ranging from 10kHz to 20MHz.

The Flash Frequency High and Low Byte registers combine to form a 16-bit value, FFREQ, to control the timing for Flash Program and Erase operations. The 16-bit binary Flash frequency value must contain the system clock frequency (in kHz). This value is calculated using the following equation:

$$FFREQ[15:0] = \frac{\text{System Clock Frequency (Hz)}}{1000}$$

Caution: Flash programming and erasure are not supported for system clock frequencies below 10kHz or above 20MHz. The Flash Frequency High and Low Byte registers must be loaded with the correct value to ensure operation of the Z8 Encore! F0830 Series devices.

Flash Code Protection Against External Access

The user code contained within Flash memory can be protected against external access by using the On-Chip Debugger. Programming the FRP Flash option bit prevents reading of the user code using the On-Chip Debugger. For more information, see the Flash Option Bits chapter on page 124 and the On-Chip Debugger chapter on page 139.

Flash Code Protection Against Accidental Program and Erasure

The Z8 Encore! F0830 Series provides several levels of protection against accidental program and erasure of the Flash memory contents. This protection is provided by a combination of the Flash option bits, the register locking mechanism, the page select redundancy and the sector level protection control of the Flash Controller.

Flash Code Protection Using the Flash Option Bits

The FHSWP and FWP Flash option bits combine to provide three levels of Flash program memory protection, as listed in Table 71. See the Flash Option Bits chapter on page 124 for more information.

Table 71. Flash Code Protection using the Flash Option Bits

FHSWP	FWP	Flash Code Protection Description
0	0	Programming and erasing disabled for all Flash program memory. In user code programming, page erase and mass erase are all disabled. Mass erase is available through the On-Chip Debugger.
0 or 1	1	Programming, page erase and mass erase are enabled for all of the Flash program memory.

At reset, the Flash Controller is locked to prevent accidental program or erasure of Flash memory. To program or erase Flash memory, first write the target page to the page select register. Unlock the Flash Controller by making two consecutive writes to the Flash Control Register with the values 73H and 8CH, sequentially. The page select register must be rewritten with the same page previously stored there. If the two page select writes do not match, the controller reverts to a Locked state. If the two writes match, the selected page becomes active. See Figure 19 for details.

After unlocking a specific page, you can enable either page program or erase. Writing the value 95H causes a page erase only if the active page resides in a sector that is not protected. Any other value written to the Flash Control Register locks the Flash Controller. Mass erase is not allowed in the user code, but is allowed through the debug port.

After unlocking a specific page, the user can also write to any byte on that page. After a byte is written, the page remains unlocked, allowing for subsequent writes to other bytes on the same page. Further writes to the Flash Control Register causes the active page to revert to a Locked state.

Sector Based Flash Protection

The final protection mechanism is implemented on a per-sector basis. The Flash memories of Z8 Encore! devices are divided into maximum number of eight sectors. A sector is one-eighth of the total size of Flash memory, unless this value is smaller than the page size, in which case the sector and page sizes are equal. On Z8 Encore! F0830 Series devices, the sector size is varied according to the Z8 Encore! F0830 Series Flash Memory Configuration shown in Table 69 on page 108 and in Figures 14 through 18, which follow the table

The Flash Sector Protect Register can be configured to prevent sectors from being programmed or erased. After a sector is protected, it cannot be unprotected by user code. The Flash Sector Protect Register is cleared after reset and any previously written protection values is lost. User code must write this register in their initialization routine if they want to enable sector protection.

The Flash Sector Protect Register shares its Register File address with the Page Select Register. The Flash Sector Protect Register is accessed by writing the Flash Control Register with 5EH. After the Flash Sector Protect Register is selected, it can be accessed at the Page Select Register address. When user code writes the Flash Sector Protect Register,

Note: The bit values used in Table 85 are set at the factory; no calibration is required.

Table 86. Trim Option Bits at 0002H (TIPO)

Bit	7	6	5	4	3	2	1	0
Field	IPO_TRIM							
RESET	U							
R/W	R/W							
Address	Information Page Memory 0022H							

Note: U = Unchanged by Reset. R/W = Read/Write.

Bit	Description
[7:0] IPO_TRIM	**Internal Precision Oscillator Trim Byte** Contains trimming bits for the Internal Precision Oscillator.

Note: The bit values used in Table 86 are set at the factory; no calibration is required.

Table 87. Trim Option Bits at 0003H (TVBO)

Bit	7	6	5	4	3	2	1	0
Field	Reserved				Reserved	VBO_TRIM		
RESET	U				U	1	0	0
R/W	R/W				R/W	R/W		
Address	Information Page Memory 0023H							

Note: U = Unchanged by Reset. R/W = Read/Write.

Bit	Description
[7:3]	**Reserved** These bits are reserved and must be programmed to 11111.
[2] VBO_TRIM	**VBO Trim Values** Contains factory-trimmed values for the oscillator and the VBO.

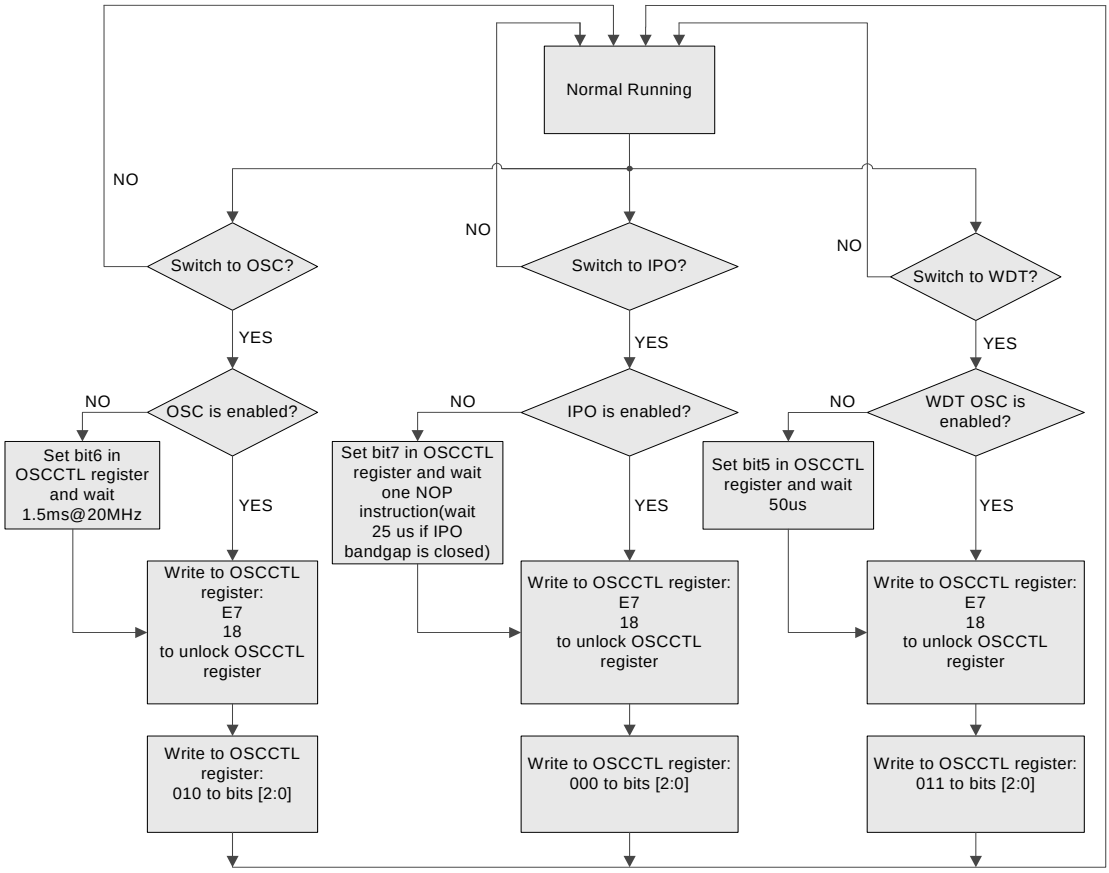

Figure 24. Oscillator Control Clock Switching Flow Chart

Table 116. DC Characteristics (Continued)

		T_A = 0°C to +70°C			T_A = –40°C to +105°C				
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
I_{LED}	Controlled Current Drive				1.5	3	4.5	mA	See GPIO section on LED description
					2.8	7	10.5	mA	
					7.8	13	19.5	mA	
					12	20	30	mA	
C_{PAD}	GPIO Port Pad Capacitance				–	8.0[2]	–	pF	TBD
C_{XIN}	XIN Pad Capacitance				–	8.0[2]	–	pF	TBD
C_{XOUT}	XOUT Pad Capacitance				–	9.5[2]	–	pF	TBD
I_{PU}	Weak Pull-up Current				50	120	220	µA	V_{DD} = 2.7 - 3.6V
ICCH[3]	Supply Current in HALT Mode					TBD		mA	TBD
ICCS	Supply Current in STOP Mode			2			8	µA	Without Watchdog Timer running

Notes:
1. This condition excludes all pins that have on-chip pull-ups, when driven Low.
2. These values are provided for design guidance only and are not tested in production.
3. See Figure 31 for HALT Mode current.

AC Characteristics

The section provides information about the AC characteristics and timing. All AC timing information assumes a standard load of 50pF on all outputs.

Table 117. AC Characteristics

		V_{DD} = 2.7 to 3.6V T_A = 0°C to +70°C		V_{DD} = 2.7 to 3.6V T_A = –40°C to +105°C			
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**	**Conditions**
F_{SYSCLK}	System Clock Frequency			–	20.0	MHz	Read-only from Flash memory
				0.032768	20.0	MHz	Program or erasure of the Flash memory
F_{XTAL}	Crystal Oscillator Frequency			1.0	20.0	MHz	System clock frequencies below the crystal oscillator minimum require an external
F_{IPO}	Internal Precision Oscillator Frequency			0.032768	5.5296	MHz	Oscillator is **not** adjustable over the entire range. User may select Min or Max value only.
F_{IPO}	Internal Precision Oscillator Frequency			5.31	5.75	MHz	High speed with trimming
F_{IPO}	Internal Precision Oscillator Frequency			4.15	6.91	MHz	High speed without trimming
F_{IPO}	Internal Precision Oscillator Frequency			30.7	33.3	KHz	Low speed with trimming
F_{IPO}	Internal Precision Oscillator Frequency			24	40	KHz	Low speed without trimming
T_{XIN}	System Clock Period			50	–	ns	$T_{CLK} = 1/F_{sysclk}$
T_{XINH}	System Clock High Time			20	30	ns	T_{CLK} = 50 ns
T_{XINL}	System Clock Low Time			20	30	ns	T_{CLK} = 50 ns

Table 118. Power-On Reset and Voltage Brown-Out Electrical Characteristics and Timing

		T_A = 0°C to +70°C			T_A = –40°C to +105°C				
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Min**	**Typ[1]**	**Max**	**Units**	**Conditions**
T_{POR}	Power-On Reset Digital Delay				TBD	13	TBD	µs	66 Internal Precision Oscillator cycles
T_{POR}	Power-On Reset Digital Delay				TBD	8	TBD	ms	5000 Internal Precision Oscillator cycles
T_{SMR}	Stop Mode Recovery with crystal oscillator disabled				TBD	13	TBD	µs	66 Internal Precision Oscillator cycles
T_{SMR}	Stop Mode Recovery with crystal oscillator enabled				TBD	8	TBD	ms	5000 Internal Precision Oscillator cycles
T_{VBO}	Voltage Brown-Out Pulse Rejection Period				–	10	–	µs	$V_{DD} < V_{VBO}$ to generate a Reset.
T_{RAMP}	Time for V_{DD} to transition from V_{SS} to V_{POR} to ensure valid Reset				0.10	–	100	ms	

Note: [1]Data in the typical column is from characterization at 3.3V and 0°C. These values are provided for design guidance only and are not tested in production.

Hex Address: F09

Table 139. Timer 1 Low Byte Register (T1L)

Bit	7	6	5	4	3	2	1	0
Field	TL							
RESET	0	0	0	0	0	0	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F09H							

Hex Address: F0A

Table 140. Timer 1 Reload High Byte Register (T1RH)

Bit	7	6	5	4	3	2	1	0
Field	TRH							
RESET	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F0AH							

Hex Address: F0B

Table 141. Timer 1 Reload Low Byte Register (T1RL)

Bit	7	6	5	4	3	2	1	0
Field	TRL							
RESET	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F0BH							

Hex Address: F0C

Table 142. Timer 1 PWM High Byte Register (T1PWMH)

Bit	7	6	5	4	3	2	1	0
Field	PWMH							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F0CH							

GPIO Port A

For more information about the GPIO registers, see the GPIO Control Register Definitions section on page 39.

Hex Address: FD0

Table 169. Port A GPIO Address Register (PAADDR)

Bit	7	6	5	4	3	2	1	0
Field	PADDR[7:0]							
RESET	00H							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FD0H							

Hex Address: FD1

Table 170. Port A Control Registers (PACTL)

Bit	7	6	5	4	3	2	1	0
Field	PCTL							
RESET	00H							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FD1H							

Hex Address: FD2

Table 171. Port A Input Data Registers (PAIN)

Bit	7	6	5	4	3	2	1	0
Field	PIN7	PIN6	PIN5	PIN4	PIN3	PIN2	PIN1	PIN0
RESET	X	X	X	X	X	X	X	X
R/W	R	R	R	R	R	R	R	R
Address	FD2H							

Hex Address: FFB

Table 196. Flash Frequency Low Byte Register (FFREQL)

Bit	7	6	5	4	3	2	1	0
Field	FFREQL							
RESET	0							
R/W	R/W							
Address	FFBH							