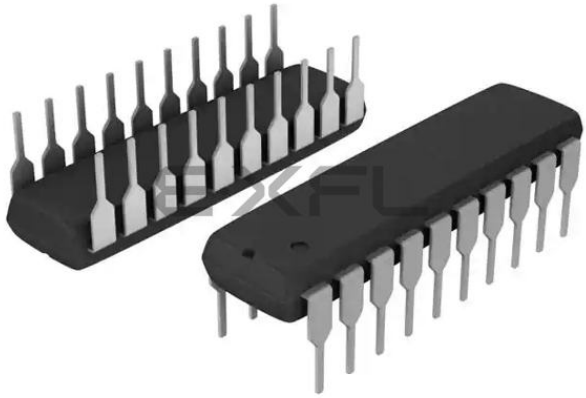

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	17
Program Memory Size	1KB (1K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f0131ph020eg

List of Tables

Block Diagram

Figure 1 displays a block diagram of the Z8 Encore! F0830 Series architecture.

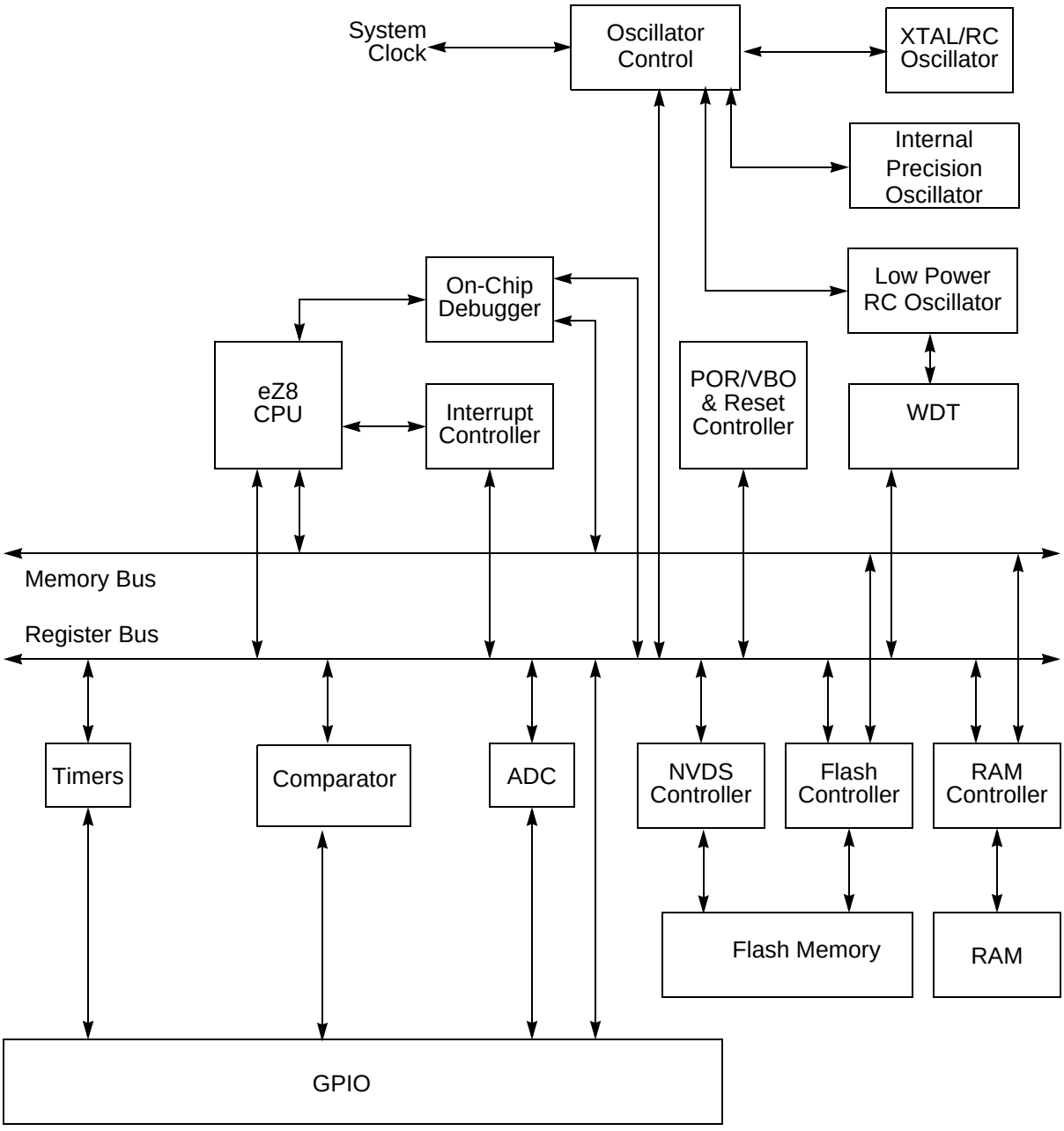

Figure 1. Z8 Encore! F0830 Series Block Diagram

Data Memory

The Z8 Encore! F0830 Series does not use the eZ8 CPU's 64KB data memory address space.

Flash Information Area

Table 7 maps the Z8 Encore! F0830 Series Flash information area. The 128-byte information area is accessed, by setting bit 7 of the Flash Page Select Register to 1. When access is enabled, the Flash information area is mapped into program memory and overlays these 128 bytes at addresses FE00H to FE7FH. When information area access is enabled, all reads from these program memory addresses return information area data rather than program memory data. Access to the Flash information area is read-only.

Table 7. Z8 Encore! F0830 Series Flash Memory Information Area Map

Program Memory Address (Hex)	Function
FE00–FE3F	Zilog option bits
FE40–FE53	Part Number 20-character ASCII alphanumeric code Left-justified and filled with FH
FE54–FE5F	Reserved
FE60–FE7F	Reserved
FE80–FFFF	Reserved

Port A–C Input Data Registers

Reading from the Port A–C Input Data registers, shown in Table 29, return the sampled values from the corresponding port pins. The Port A–C Input Data registers are read-only. The value returned for any unused ports is 0. Unused ports include those not included in the 8- and 28-pin packages, as well as those not included in the ADC-enabled 28-pin packages.

Table 29. Port A–C Input Data Registers (PxIN)

Bit	7	6	5	4	3	2	1	0
Field	PIN7	PIN6	PIN5	PIN4	PIN3	PIN2	PIN1	PIN0
RESET	X	X	X	X	X	X	X	X
R/W	R	R	R	R	R	R	R	R
Address	FD2H, FD6H, FDAH							

Bit	Description
[7:0] PxIN	**Port Input Data** Sampled data from the corresponding port pin input. 0 = Input data is logical 0 (Low). 1 = Input data is logical 1 (High).

Note: x indicates the specific GPIO port pin number (7–0).

- Writing 1 to the IRQE bit in the Interrupt Control Register

Interrupts are globally disabled by any of the following actions:

- Execution of a DI (disable interrupt) instruction
- eZ8 CPU acknowledgement of an interrupt service request from the Interrupt Controller
- Writing a 0 to the IRQE bit in the Interrupt Control Register
- Reset
- Execution of a trap instruction
- Illegal instruction Trap
- Primary oscillator fail trap
- Watchdog Oscillator fail trap

Interrupt Vectors and Priority

The Interrupt Controller supports three levels of interrupt priority. Level 3 is the highest priority, level 2 is the second highest priority and level 1 is the lowest priority. If all of the interrupts are enabled with identical interrupt priority (all as level 2 interrupts, for example), the interrupt priority is assigned from highest to lowest as specified in Table 34 on page 54. Level 3 interrupts are always assigned higher priority than level 2 interrupts and level 2 interrupts are assigned higher priority than level 1 interrupts. Within each interrupt priority level (level 1, level 2 or level 3), priority is assigned as specified in Table 34, above. Reset, Watchdog Timer interrupt (if enabled), primary oscillator fail trap, Watchdog Oscillator fail trap and illegal instruction trap always have highest (level 3) priority.

Interrupt Assertion

Interrupt sources assert their interrupt requests for only a single system clock period (single pulse). When the interrupt request is acknowledged by the eZ8 CPU, the corresponding bit in the interrupt request register is cleared. Writing 0 to the corresponding bit in the interrupt request register clears the interrupt request.

! **Caution:** Zilog recommends not using a coding style that clears bits in the Interrupt Request registers. All incoming interrupts received between execution of the first LDX command and the final LDX command are lost. See Example 1, which follows.

Example 1. A poor coding style that can result in lost interrupt requests:

Interrupt Request 0 Register

The Interrupt Request 0 (IRQ0) Register, shown in Table 35 stores the interrupt requests for both vectored and polled interrupts. When a request is sent to the Interrupt Controller, the corresponding bit in the IRQ0 Register becomes 1. If interrupts are globally enabled (vectored interrupts), the Interrupt Controller passes an interrupt request to the eZ8 CPU. If interrupts are globally disabled (polled interrupts), the eZ8 CPU can read the Interrupt Request 0 Register to determine if any interrupt requests are pending.

Table 35. Interrupt Request 0 Register (IRQ0)

Bit	7	6	5	4	3	2	1	0
Field	Reserved	T1I	T0I	Reserved				ADCI
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FC0H							

Bit	Description
[7]	**Reserved** This bit is reserved and must be programmed to 0.
[6] T1I	**Timer 1 Interrupt Request** 0 = No interrupt request is pending for timer 1. 1 = An interrupt request from timer 1 is awaiting service.
[5] T0I	**Timer 0 Interrupt Request** 0 = No interrupt request is pending for timer 0. 1 = An interrupt request from timer 0 is awaiting service.
[4:1]	**Reserved** These registers are reserved and must be programmed to 0000.
[0] ADCI	**ADC Interrupt Request** 0 = No interrupt request is pending for the analog-to-digital converter. 1 = An interrupt request from the analog-to-digital converter is awaiting service.

Interrupt Request 2 Register

The Interrupt Request 2 (IRQ2) Register, shown in Table 37, stores interrupt requests for both vectored and polled interrupts. When a request is sent to the Interrupt Controller, the corresponding bit in the IRQ2 Register becomes 1. If interrupts are globally enabled (vectored interrupts), the Interrupt Controller passes an interrupt request to the eZ8 CPU. If interrupts are globally disabled (polled interrupts), the eZ8 CPU can read the Interrupt Request 2 Register to determine if any interrupt requests are pending.

Table 37. Interrupt Request 2 Register (IRQ2)

Bit	7	6	5	4	3	2	1	0
Field	Reserved				PC3I	PC2I	PC1I	PC0I
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FC6H							

Bit	Description
[7:4]	**Reserved** These registers are reserved and must be programmed to 0000.
[3] PC*x*I	**Port C Pin *x* Interrupt Request** 0 = No interrupt request is pending for GPIO Port C pin *x*. 1 = An interrupt request from GPIO Port C pin *x* is awaiting service.

Note: x indicates the specific GPIO port pin number (3–0).

IRQ0 Enable High and Low Bit Registers

Table 38 lists the priority control values for IRQ0. The IRQ0 Enable High and Low Bit registers, shown in Tables 39 and 40, form a priority-encoded enabling service for interrupts in the Interrupt Request 0 Register. Priority is generated by setting the bits in each register.

Table 38. IRQ0 Enable and Priority Encoding

IRQ0ENH[*x*]	IRQ0ENL[*x*]	Priority	Description
0	0	Disabled	Disabled
0	1	Level 1	Low
1	0	Level 2	Nominal
1	1	Level 3	High

Note: *x* indicates the register bits in the range 7–0.

Observe the following steps for configuring a timer for PWM DUAL OUTPUT Mode and for initiating the PWM operation:

1. Write to the Timer Control Register to:
   - Disable the timer
   - Configure the timer for PWM DUAL OUTPUT Mode; setting the mode also involves writing to TMODEHI bit in the TxCTL1 Register
   - Set the prescale value
   - Set the initial logic level (High or Low) and PWM High/Low transition for the timer output alternate function
2. Write to the Timer High and Low Byte registers to set the starting count value (typically 0001H). This write only affects the first pass in PWM Mode. After the first timer reset in PWM Mode, counting always begins at the reset value of 0001H.
3. Write to the PWM High and Low Byte registers to set the PWM value.
4. Write to the PWM Control Register to set the PWM deadband delay value. The deadband delay must be less than the duration of the positive phase of the PWM signal (as defined by the PWM High and Low Byte registers). It must also be less than the duration of the negative phase of the PWM signal (as defined by the difference between the PWM registers and the Timer Reload registers).
5. Write to the Timer Reload High and Low Byte registers to set the reload value (PWM period). The reload value must be greater than the PWM value.
6. If appropriate, enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers.
7. Configure the associated GPIO port pin for the timer output and timer output complement alternate functions. The timer output complement function is shared with the timer input function for both timers. Setting the timer mode to DUAL PWM will automatically switch the function from timer-in to timer-out complement.
8. Write to the Timer Control Register to enable the timer and initiate counting.

The PWM period is represented by the following equation:

$$\text{PWM Period (s)} = \frac{\text{Reload Value} \times \text{Prescale}}{\text{System Clock Frequency (Hz)}}$$

If an initial starting value other than 0001H is loaded into the Timer High and Low Byte registers, the ONE-SHOT Mode equation determines the first PWM time-out period.

If TPOL is set to 0, the ratio of the PWM output high time to the total period is represented by:

$$\text{PWM Output High Time Ratio (\%)} = \frac{\text{Reload Value} - \text{PWM Value}}{\text{Reload Value}} \times 100$$

If TPOL is set to 1, the ratio of the PWM output high time to the total period is represented by:

$$\text{PWM Output High Time Ratio (\%)} = \frac{\text{PWM Value}}{\text{Reload Value}} \times 100$$

CAPTURE Mode

In CAPTURE Mode, the current timer count value is recorded when the appropriate external timer input transition occurs. The capture count value is written to the timer PWM High and Low Byte registers. The timer input is the system clock. The TPOL bit in the Timer Control Register determines if the capture occurs on a rising edge or a falling edge of the timer input signal.

When the capture event occurs, an interrupt is generated and the timer continues counting. The INPCAP bit in the TxCTL1 Register is set to indicate the timer interrupt because of an input capture event.

The timer continues counting up to the 16-bit reload value stored in the Timer Reload High and Low Byte registers. Upon reaching the reload value, the timer generates an interrupt and continues counting. The INPCAP bit in the TxCTL1 Register clears, indicating that the timer interrupt has not occurred because of an input capture event.

Observe the following steps for configuring a timer for CAPTURE Mode and initiating the count:

1. Write to the Timer Control Register to:
   - Disable the timer
   - Configure the timer for CAPTURE Mode
   - Set the prescale value
   - Set the capture edge (rising or falling) for the timer input
2. Write to the Timer High and Low Byte registers to set the starting count value (typically 0001H).
3. Write to the Timer Reload High and Low Byte registers to set the reload value.
4. Clear the timer PWM High and Low Byte registers to 0000H. Clearing these registers allows user software to determine if interrupts were generated either by a capture event or by a reload. If the PWM High and Low Byte registers still contain 0000H after the interrupt, the interrupt were generated by a reload.

Sample Time Register

The Sample Time Register, shown in Table 67, is used to program the length of active time for a sample after a conversion has begun by setting the START bit in the ADC Control Register. The number of system clock cycles required for the sample time varies from system to system, depending on the clock period used. The system designer should program this register to contain the number of system clocks required to meet a 1µs minimum sample time.

Table 67. Sample Time (ADCST)

Bit	7	6	5	4	3	2	1	0
Field	Reserved		ST					
RESET	0		1	1	1	1	1	1
R/W	R/W		R/W					
Address	F75H							

Bit	Description
[7:6]	**Reserved** These bits are reserved and must be programmed to 00.
[5:0] ST	0h–Fh = Sample-hold time in number of system clock periods to meet 1 µs minimum.

Flash information area is mapped into program memory and overlays the 128 bytes in the address range FE00H to FE7FH. When the information area access is enabled, all reads from these program memory addresses return the information area data rather than the program memory data. Access to the Flash information area is read-only.

The trim bits are handled differently than the other Zilog Flash option bits. The trim bits are the hybrid of the user option bits and the standard Zilog option bits. These trim bits must be user-accessible for reading at all times using external registers regardless of the state of bit 7 in the Flash Page Select Register. Writes to the trim space change the value of the Option Bit Holding Register but do not affect the Flash bits, which remain as read-only.

Table 70. Z8F083 Flash Memory Area Map

Program Memory Address (Hex)	Function
FE00–FE3F	Zilog option bits
FE40–FE53	Part number 20-character ASCII alphanumeric code Left justified and filled with FH
FE54–FE5F	Reserved
FE60–FE7F	Reserved

Operation

The Flash Controller programs and erases Flash memory. The Flash Controller provides the proper Flash controls and timing for byte programming, page erase and mass erase of Flash memory.

The Flash Controller contains several protection mechanisms to prevent accidental programming or erasure. These mechanism operate on the page, sector and full-memory levels.

The flowchart in Figure 19 display basic Flash Controller operation. The following subsections provide details about the various operations (Lock, Unlock, Byte Programming, Page Protect, Page Unprotect, Page Select Page Erase and Mass Erase) displayed in Figure 19.

Flash Operation Timing Using the Flash Frequency Registers

Before performing either a Program or Erase operation on Flash memory, the user must first configure the Flash Frequency High and Low Byte registers. The Flash frequency registers allow programming and erasing of the Flash with system clock frequencies ranging from 10kHz to 20MHz.

The Flash Frequency High and Low Byte registers combine to form a 16-bit value, FFREQ, to control the timing for Flash Program and Erase operations. The 16-bit binary Flash frequency value must contain the system clock frequency (in kHz). This value is calculated using the following equation:

$$FFREQ[15:0] = \frac{\text{System Clock Frequency (Hz)}}{1000}$$

Caution: Flash programming and erasure are not supported for system clock frequencies below 10kHz or above 20MHz. The Flash Frequency High and Low Byte registers must be loaded with the correct value to ensure operation of the Z8 Encore! F0830 Series devices.

Flash Code Protection Against External Access

The user code contained within Flash memory can be protected against external access by using the On-Chip Debugger. Programming the FRP Flash option bit prevents reading of the user code using the On-Chip Debugger. For more information, see the Flash Option Bits chapter on page 124 and the On-Chip Debugger chapter on page 139.

Flash Code Protection Against Accidental Program and Erasure

The Z8 Encore! F0830 Series provides several levels of protection against accidental program and erasure of the Flash memory contents. This protection is provided by a combination of the Flash option bits, the register locking mechanism, the page select redundancy and the sector level protection control of the Flash Controller.

Flash Code Protection Using the Flash Option Bits

The FHSWP and FWP Flash option bits combine to provide three levels of Flash program memory protection, as listed in Table 71. See the Flash Option Bits chapter on page 124 for more information.

Flash Page Select Register

The Flash Page Select Register shares address space with the Flash Sector Protect Register. Unless the Flash Controller is locked and written with 5EH, any writes to this address will target the Flash Page Select Register.

The register selects one of the eight available Flash memory pages to be programmed or erased. Each Flash page contains 512-bytes of Flash memory. During a page erase operation, all Flash memory containing addresses with the most significant 7-bits within FPS[6:0] are chosen for program/erase operations.

Table 74. Flash Page Select Register (FPS)

Bit	7	6	5	4	3	2	1	0
Field	INFO_EN	PAGE						
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FF9H							

Bit	Description
[7] INFO_EN	**Information Area Enable** 0 = Information area is not selected. 1 = Information area is selected. The information area is mapped into the program memory address space at addresses FE00H through FFFFH.
[6:0] PAGE	**Page Select** This 7-bit field identifies the Flash memory page for page erase and page unlocking. Program memory address[15:9] = PAGE[6:0]. For Z8F04xx and Z8F02xx devices, the upper four bits must always be 0. For Z8F01xx devices, the upper five bits must always be 0.

Table 83. Trim Bit Address Space

Address	Function
00h	ADC reference voltage
01h	ADC and comparator
02h	Internal Precision Oscillator
03h	Oscillator and VBO
06h	ClkFltr

Table 84. Trim Option Bits at 0000H (ADCREF)

Bit	7	6	5	4	3	2	1	0
Field	ADCREF_TRIM					Reserved		
RESET	U					U		
R/W	R/W					R/W		
Address	Information Page Memory 0020H							

Note: U = Unchanged by Reset. R/W = Read/Write.

Bit	Description
[7:3] ADCREF_TRIM	**ADC Reference Voltage Trim Byte** Contains trimming bits for ADC reference voltage.
[2:0]	**Reserved** These bits are reserved and must be programmed to 111.

Note: The bit values used in Table 84 are set at the factory; no calibration is required.

Table 85. Trim Option Bits at 0001H (TADC_COMP)

Bit	7	6	5	4	3	2	1	0
Field	Reserved							
RESET	U	U	U	U	U	U	U	U
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	Information Page Memory 0021H							

Note: U = Unchanged by Reset. R/W = Read/Write.

Bit	Description
[7:0]	**Reserved** Altering this register may result in incorrect device operation.

OCD Status Register

The OCD Status Register reports status information about the current state of the debugger and the system.

Table 97. OCD Status Register (OCDSTAT)

Bit	7	6	5	4	3	2	1	0
Field	DBG	HALT	FRPENB	Reserved				
RESET	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R

Bit	Description
[7] DBG	**Debug Status** 0 = NORMAL Mode. 1 = DEBUG Mode.
[6] HALT	**HALT Mode** 0 = Not in HALT Mode. 1 = In HALT Mode.
[5] FRPENB	**Flash Read Protect Option Bit Enable** 0 = FRP bit enabled, that allows disabling of many OCD commands. 1 = FRP bit has no effect.
[4:0]	**Reserved** These bits are reserved and must be programmed to 00000.

ister, the user code must wait at least 5000 IPO cycles for the crystal to stabilize. After this period, the crystal oscillator may be selected as the system clock.

Figure 25 displays a recommended configuration for connection with an external fundamental-mode, parallel-resonant crystal operating at 20 MHz. Recommended 20 MHz crystal specifications are provided in Table 100. Resistor R_1 is optional and limits total power dissipation by the crystal. Printed circuit board layout must add no more than 4 pF of stray capacitance to either the X_{IN} or X_{OUT} pins. If oscillation does not occur, reduce the values of capacitors C_1 and C_2 to decrease loading.

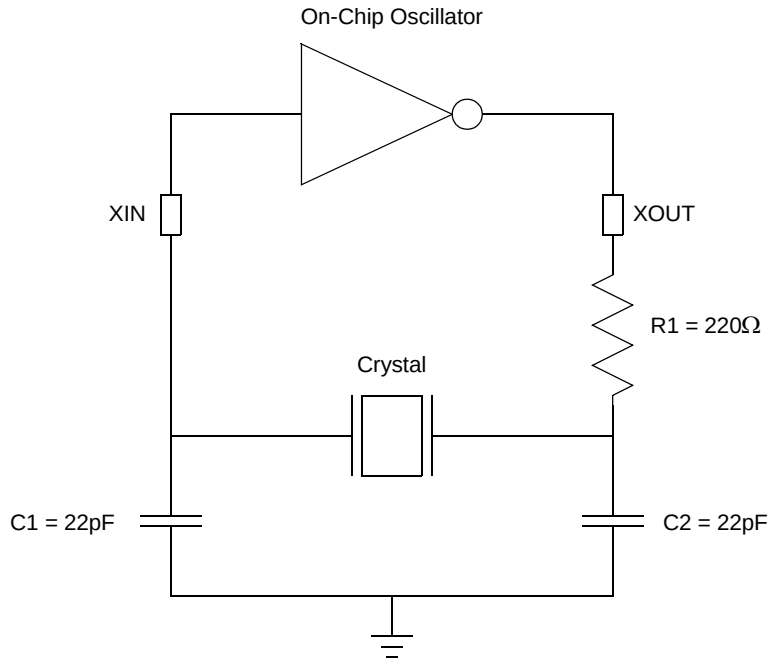

Figure 25. Recommended 20 MHz Crystal Oscillator Configuration

Table 100. Recommended Crystal Oscillator Specifications

Parameter	Value	Units	Comments
Frequency	20	MHz	
Resonance	Parallel		
Mode	Fundamental		
Series Resistance (R_S)	60	Ω	Maximum
Load Capacitance (C_L)	30	pF	Maximum
Shunt Capacitance (C_0)	7	pF	Maximum
Drive Level	1	mW	Maximum

Table 108. CPU Control Instructions

Mnemonic	Operands	Instruction
ATM	—	Atomic Execution
CCF	—	Complement Carry Flag
DI	—	Disable Interrupts
EI	—	Enable Interrupts
HALT	—	HALT Mode
NOP	—	No Operation
RCF	—	Reset Carry Flag
SCF	—	Set Carry Flag
SRP	src	Set Register Pointer
STOP	—	STOP Mode
WDT	—	Watchdog Timer Refresh

Table 109. Load Instructions

Mnemonic	Operands	Instruction
CLR	dst	Clear
LD	dst, src	Load
LDC	dst, src	Load Constant to/from Program Memory
LDCI	dst, src	Load Constant to/from Program Memory and Auto-Increment Addresses
LDE	dst, src	Load External Data to/from Data Memory
LDEI	dst, src	Load External Data to/from Data Memory and Auto-Increment Addresses
LDWX	dst, src	Load Word using Extended Addressing
LDX	dst, src	Load using Extended Addressing
LEA	dst, X(src)	Load Effective Address
POP	dst	Pop
POPX	dst	Pop using Extended Addressing
PUSH	src	Push
PUSHX	src	Push using Extended Addressing

Table 113. eZ8 CPU Instruction Summary (Continued)

Assembly Mnemonic	Symbolic Operation	Address Mode dst	Address Mode src	Op Code(s) (Hex)	Flags C	Z	S	V	D	H	Fetch Cycles	Instr. Cycles
CLR dst	dst ← 00H	R		B0	–	–	–	–	–	–	2	2
		IR		B1							2	3
COM dst	dst ← ~dst	R		60	–	*	*	0	–	–	2	2
		IR		61							2	3
CP dst, src	dst - src	r	r	A2	*	*	*	*	–	–	2	3
		r	Ir	A3							2	4
		R	R	A4							3	3
		R	IR	A5							3	4
		R	IM	A6							3	3
		IR	IM	A7							3	4
CPC dst, src	dst - src - C	r	r	1F A2	*	*	*	*	–	–	3	3
		r	Ir	1F A3							3	4
		R	R	1F A4							4	3
		R	IR	1F A5							4	4
		R	IM	1F A6							4	3
		IR	IM	1F A7							4	4
CPCX dst, src	dst - src - C	ER	ER	1F A8	*	*	*	*	–	–	5	3
		ER	IM	1F A9							5	3
CPX dst, src	dst - src	ER	ER	A8	*	*	*	*	–	–	4	3
		ER	IM	A9							4	3
DA dst	dst ← DA(dst)	R		40	*	*	*	X	–	–	2	2
		IR		41							2	3
DEC dst	dst ← dst - 1	R		30	–	*	*	*	–	–	2	2
		IR		31							2	3
DECW dst	dst ← dst - 1	RR		80	–	*	*	*	–	–	2	5
		IRR		81							2	6
DI	IRQCTL[7] ← 0			8F	–	–	–	–	–	–	1	2

Note: Flags Notation:
* = Value is a function of the result of the operation.
– = Unaffected.
X = Undefined.
0 = Reset to 0.
1 = Set to 1.

General Purpose I/O Port Output Timing

Figure 34 and Table 125 provide timing information for the GPIO port pins.

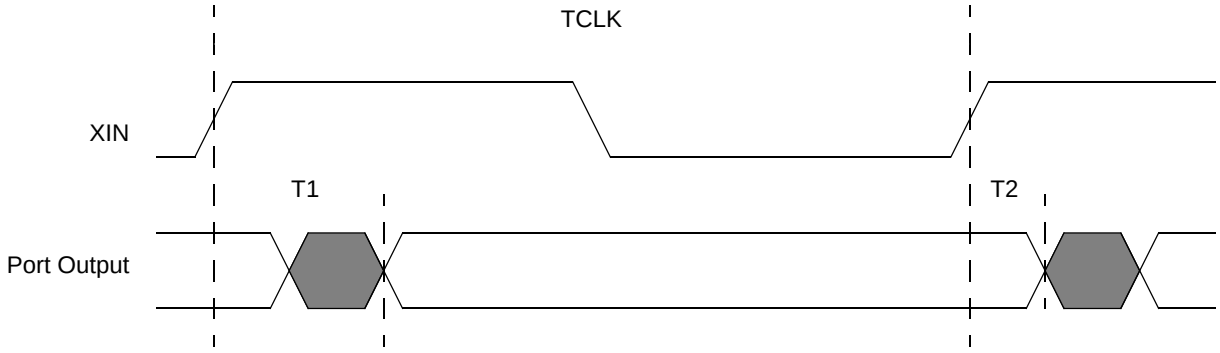

Figure 34. GPIO Port Output Timing

Table 125. GPIO Port Output Timing

		Delay (ns)	
Parameter	**Abbreviation**	**Minimum**	**Maximum**
GPIO Port Pins			
T_1	XIN Rise to Port Output Valid Delay	–	15
T_2	XIN Rise to Port Output Hold Time	2	–

Table 128. Z8 Encore! XP F0830 Series Ordering Matrix

Part Number	Flash	RAM	NVDS	ADC Channels	Description
Z8F0430QH020EG	4KB	256	Yes	7	QFN 20-pin
Z8F0431SH020EG	4KB	256	Yes	0	SOIC 20-pin
Z8F0431HH020EG	4KB	256	Yes	0	SSOP 20-pin
Z8F0431PH020EG	4KB	256	Yes	0	PDIP 20-pin
Z8F0431QH020EG	4KB	256	Yes	0	QFN 20-pin
Z8F0430SJ020EG	4KB	256	Yes	8	SOIC 28-pin
Z8F0430HJ020EG	4KB	256	Yes	8	SSOP 28-pin
Z8F0430PJ020EG	4KB	256	Yes	8	PDIP 28-pin
Z8F0430QJ020EG	4KB	256	Yes	8	QFN 28-pin
Z8F0431SJ020EG	4KB	256	Yes	0	SOIC 28-pin
Z8F0431HJ020EG	4KB	256	Yes	0	SSOP 28-pin
Z8F0431PJ020EG	4KB	256	Yes	0	PDIP 28-pin
Z8F0431QJ020EG	4KB	256	Yes	0	QFN 28-pin
Z8 Encore! F0830 with 2KB Flash					
Standard Temperature: 0°C to 70°C					
Z8F0230SH020SG	2KB	256	Yes	7	SOIC 20-pin
Z8F0230HH020SG	2KB	256	Yes	7	SSOP 20-pin
Z8F0230PH020SG	2KB	256	Yes	7	PDIP 20-pin
Z8F0230QH020SG	2KB	256	Yes	7	QFN 20-pin
Z8F0231SH020SG	2KB	256	Yes	0	SOIC 20-pin
Z8F0231HH020SG	2KB	256	Yes	0	SSOP 20-pin
Z8F0231PH020SG	2KB	256	Yes	0	PDIP 20-pin
Z8F0231QH020SG	2KB	256	Yes	0	QFN 20-pin
Z8F0230SJ020SG	2KB	256	Yes	8	SOIC 28-pin
Z8F0230HJ020SG	2KB	256	Yes	8	SSOP 28-pin
Z8F0230PJ020SG	2KB	256	Yes	8	PDIP 28-pin
Z8F0230QJ020SG	2KB	256	Yes	8	QFN 28-pin
Z8F0231SJ020SG	2KB	256	Yes	0	SOIC 28-pin
Z8F0231HJ020SG	2KB	256	Yes	0	SSOP 28-pin
Z8F0231PJ020SG	2KB	256	Yes	0	PDIP 28-pin
Z8F0231QJ020SG	2KB	256	Yes	0	QFN 28-pin