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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	23
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.173", 4.40mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f0230hj020sg

CPU and Peripheral Overview

The eZ8 CPU, Zilog's latest 8-bit CPU, meets the continuing demand for faster and more code-efficient microcontrollers. The eZ8 CPU executes a superset of the original Z8 instruction set. The eZ8 CPU features include:

- Direct register-to-register architecture allows each register to function as an accumulator, improving execution time and decreasing the required program memory
- Software stack allows much greater depth in subroutine calls and interrupts than hardware stacks
- Compatible with existing Z8 CPU code
- Expanded internal register file allows access up to 4KB
- New instructions improve execution efficiency for code developed using high-level programming languages, including C
- Pipelined instruction fetch and execution
- New instructions for improved performance including BIT, BSWAP, BTJ, CPC, LDC, LDCI, LEA, MULT and SRL
- New instructions support 12-bit linear addressing of the register file
- Up to 10 MIPS operation
- C Compiler-friendly
- 2 to 9 clock cycles per instruction

For more information about the eZ8 CPU, refer to the eZ8 CPU Core User Manual (UM0128), which is available for download on www.zilog.com.

General Purpose Input/Output

The Z8 Encore! F0830 Series features up to 25 port pins (Ports A–D) for general-purpose input/output (GPIO). The number of GPIO pins available is a function of package. Each pin is individually programmable.

Flash Controller

The Flash Controller programs and erases the Flash memory. It also supports protection against accidental programming and erasure.

Table 8. Register File Address Map (Continued)

Address (Hex)	Register Description	Mnemonic	Reset (Hex)	Page No.
Trim Bit Control				
FF6	Trim bit address	TRMADR	00	126
FF7	Trim data	TRMDR	XX	127
Flash Memory Controller				
FF8	Flash control	FCTL	00	119
FF8	Flash status	FSTAT	00	120
FF9	Flash page select	FPS	00	121
	Flash sector protect	FPROT	00	122
FFA	Flash programming frequency high byte	FFREQH	00	123
FFB	Flash programming frequency low byte	FFREQL	00	123
eZ8 CPU				
FFC	Flags	—	XX	Refer to the eZ8 CPU Core User Manual (UM0128)
FFD	Register pointer	RP	XX	
FFE	Stack pointer high byte	SPH	XX	
FFF	Stack pointer low byte	SPL	XX	

Note: XX = Undefined.

Table 9. Reset and Stop Mode Recovery Characteristics and Latency

	Reset Characteristics and Latency		
Reset Type	**Control Registers**	**eZ8 CPU**	**Reset Latency (Delay)**
System Reset	Reset (as applicable)	Reset	About 66 Internal Precision Oscillator Cycles
System Reset with Crystal Oscillator Enabled	Reset (as applicable)	Reset	About 5000 Internal Precision Oscillator Cycles
Stop Mode Recovery	Unaffected, except WDT_CTL and OSC_CTL registers	Reset	About 66 Internal Precision Oscillator cycles
Stop Mode Recovery with crystal oscillator enabled	Unaffected, except WDT_CTL and OSC_CTL registers	Reset	About 5000 Internal Precision Oscillator cycles

During a system RESET or Stop Mode Recovery, the Z8 Encore! F0830 Series device is held in reset for about 66 cycles of the Internal Precision Oscillator. If the crystal oscillator is enabled in the Flash option bits, the reset period is increased to about 5000 IPO cycles. When a reset occurs because of a low voltage condition or Power-On Reset, the reset delay is measured from the time that the supply voltage first exceeds the POR level (discussed later in this chapter). If the external pin reset remains asserted at the end of the reset period, the device remains in reset until the pin is deasserted.

At the beginning of reset, all GPIO pins are configured as inputs with pull-up resistor disabled, except PD0 which is shared with the reset pin. On reset, the Port D0 pin is configured as a bidirectional open-drain reset. This pin is internally driven low during port reset, after which the user code may reconfigure this pin as a general purpose output.

During reset, the eZ8 CPU and on-chip peripherals are idle; however, the on-chip crystal oscillator and Watchdog Timer Oscillator continues to run.

On reset, control registers within the register file that have a defined reset value are loaded with their reset values. Other control registers (including the Stack Pointer, Register Pointer and Flags) and general purpose RAM are undefined following the reset. The eZ8 CPU fetches the reset vector at program memory addresses `0002H` and `0003H` and loads that value into the program counter. Program execution begins at the reset vector address.

Because the control registers are reinitialized by a system reset, the system clock after reset is always the IPO. User software must reconfigure the oscillator control block, to enable and select the correct system clock source.

The Voltage Brown-Out circuit can be either enabled or disabled during STOP Mode. Operations during STOP Mode is set by the VBO_AO Flash option bit. See the Flash Option Bits chapter on page 124 for information about configuring VBO_AO.

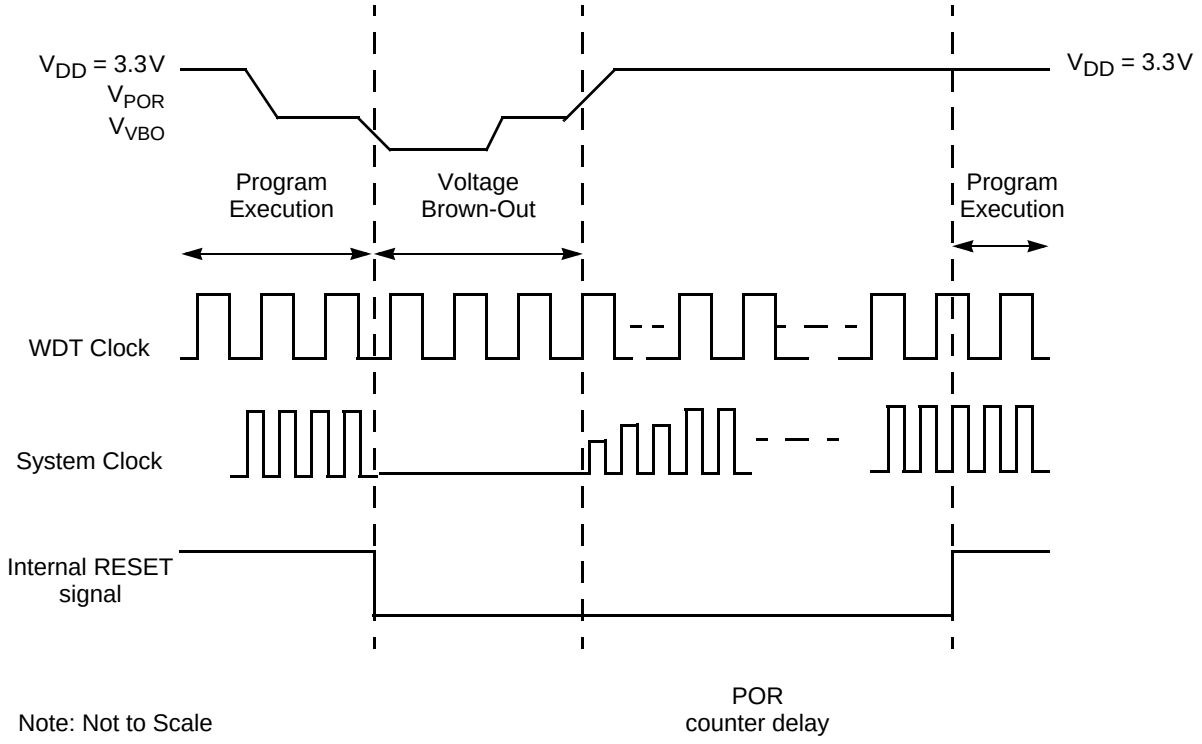

Figure 7. Voltage Brown-Out Reset Operation

Watchdog Timer Reset

If the device is operating in NORMAL or STOP Mode, the Watchdog Timer can initiate a system reset at time-out if the WDT_RES Flash option bit is programmed to 1; this state is the unprogrammed state of the WDT_RES Flash option bit. If the bit is programmed to 0, it configures the Watchdog Timer to cause an interrupt – not a system reset – at time-out. The WDT status bit in the Reset Status (RSTSTAT) Register is set to 1 to signify that the reset was initiated by the Watchdog Timer.

External Reset Input

The $\overline{\text{RESET}}$ pin has a Schmitt-triggered input and an internal pull-up resistor. After the $\overline{\text{RESET}}$ pin is asserted for a minimum of four system clock cycles, the device progresses through the system reset sequence. Because of the possible asynchronicity of the system

Port A–D Alternate Function Subregisters

The Port A–D Alternate Function Subregister is accessed through the Port A–D Control Register by writing 02H to the Port A–D Address Register. See Table 22 on page 42. The Port A–D Alternate Function subregisters enable the alternate function selection on pins. If disabled, the pins function as GPIOs. If enabled, select one of four alternate functions using Alternate Function Set subregisters 1 and 2, as described in the the Port A–D Alternate Function Set 1 Subregisters section on page 47 and the Port A–D Alternate Function Set 2 Subregisters section on page 48**.** See the GPIO Alternate Functions section on page 34 to determine the alternate functions associated with each port pin.

! Caution: Do not enable alternate functions for GPIO port pins for which there is no associated Alternate function. Failure to follow this guideline can result in unpredictable operation.

Table 22. Port A–D Alternate Function Subregisters (PxAF)

Bit	7	6	5	4	3	2	1	0
Field	AF7	AF6	AF5	AF4	AF3	AF2	AF1	AF0
RESET	00H (Ports A–C); 01H (Port D)							
R/W	R/W							
Address	If 02H in Port A–D Address Register, then accessible through the Port A–D Control Register							

Bit	Description
[7:0] AFx	**Port Alternate Function Enable** 0 = The port pin is in NORMAL Mode and the DDx bit in the Port A–D Data Direction Subregister determines the direction of the pin. 1 = The alternate function selected through Alternate function set subregisters is enabled. Port pin operation is controlled by the Alternate function.

Note: x indicates the specific GPIO port pin number (7–0).

Interrupt Request 1 Register

The Interrupt Request 1 (IRQ1) Register, shown in Table 36, stores interrupt requests for both vectored and polled interrupts. When a request is sent to the Interrupt Controller, the corresponding bit in the IRQ1 Register becomes 1. If interrupts are globally enabled (vectored interrupts), the Interrupt Controller passes an interrupt request to the eZ8 CPU. If interrupts are globally disabled (polled interrupts), the eZ8 CPU can read the Interrupt Request 1 Register to determine if any interrupt requests are pending.

Table 36. Interrupt Request 1 Register (IRQ1)

Bit	7	6	5	4	3	2	1	0
Field	PA7I	PA6CI	PA5I	PA4I	PA3I	PA2I	PA1I	PA0I
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FC3H							

Bit	Description
[7] PA7I	**Port A7** 0 = No interrupt request is pending for GPIO Port A. 1 = An interrupt request from GPIO Port A.
[6] PA6CI	**Port A6 or Comparator Interrupt Request** 0 = No interrupt request is pending for GPIO Port A or comparator. 1 = An interrupt request from GPIO Port A or comparator.
[5] PAxI	**Port A Pin *x* Interrupt Request** 0 = No interrupt request is pending for GPIO Port A pin *x*. 1 = An interrupt request from GPIO Port A pin *x* is awaiting service.

Note: x indicates the specific GPIO port pin number (5–0).

Watchdog Timer Reload Upper, High and Low Byte Registers

The Watchdog Timer Reload Upper, High and Low Byte (WDTU, WDTH, WDTL) registers, shown in Tables 60 through 62, form the 24-bit reload value that is loaded into the Watchdog Timer when a WDT instruction executes. This 24-bit value ranges across bits [23:0] to encompass the three bytes {WDTU[7:0], WDTH[7:0], WDTL[7:0]}. Writing to these registers sets the appropriate reload value; reading from these registers returns the current Watchdog Timer count value.

Caution: The 24-bit WDT reload value must not be set to a value less than 000004H.

Table 60. Watchdog Timer Reload Upper Byte Register (WDTU)

Bit	7	6	5	4	3	2	1	0
Field	WDTU							
RESET	0	0	0	0	0	0	0	0
R/W	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*
Address	FF1H							

Note: *A read returns the current WDT count value; a write sets the appropriate reload value.

Bit	Description
[7:0] WDTU	**WDT Reload Upper Byte** Most significant byte (MSB), Bits[23:16], of the 24-bit WDT reload value.

Table 61. Watchdog Timer Reload High Byte Register (WDTH)

Bit	7	6	5	4	3	2	1	0
Field	WDTH							
RESET	0	0	0	0	0	1	0	0
R/W	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*
Address	FF2H							

Note: *A read returns the current WDT count value; a write sets the appropriate reload value.

Bit	Description
[7:0] WDTH	**WDT Reload High Byte** Middle byte, bits[15:8] of the 24-bit WDT reload value.

Bit	Description (Continued)
[1:0] FilterSel*y*	**Filter Select** 2-bit selection for the clock filter mode. 00 = No filter. 01 = Filter low level noise on high level signal. 10 = Filter high level noise on low level signal. 11 = Filter both.

Notes: x indicates bit values 3–1; y indicates bit values 1–0.

Note: The bit values used in Table 89 are set at factory and no calibration is required.

Table 90. ClkFlt Delay Control Definition

DlyCtl3, DlyCtl2, DlyCtl1	Low Noise Pulse on High Signal (ns)	High Noise Pulse on Low Signal (ns)
000	5	5
001	7	7
010	9	9
011	11	11
100	13	13
101	17	17
110	20	20
111	25	25

Note: The variation is about 30%.

Power Failure Protection

NVDS routines employ error-checking mechanisms to ensure that any power failure will only endanger the most recently written byte. Bytes previously written to the array are not perturbed. For this protection to function, the VBO must be enabled (see the Low-Power Modes chapter on page 30) and configured for a threshold voltage of 2.4V or greater (see *the* Trim Bit Address Space *section on page 129*).

A system reset (such as a pin reset or Watchdog Timer reset) that occurs during a write operation also perturbs the byte currently being written. All other bytes in the array are unperturbed.

Optimizing NVDS Memory Usage for Execution Speed

As indicated in Table 93, the NVDS read time varies drastically; this discrepancy being a trade-off for minimizing the frequency of writes that require post-write page erases. The NVDS read time of address N is a function of the number of writes to addresses other than N since the most recent write to address N as well as the number of writes since the most recent page erase. Neglecting the effects caused by page erases and results caused by the initial condition in which the NVDS is blank, a rule of thumb to consider is that every write since the most recent page erase causes read times of unwritten addresses to increase by 0.8µs up to a maximum of 258µs.

Table 93. NVDS Read Time

Operation	Minimum Latency (µs)	Maximum Latency (µs)
Read	71	258
Write	126	136
Illegal Read	6	6
Illegal Write	7	7

Note: For every 200 writes, a maintenance operation is necessary. In this rare occurrence, the write takes up to 58ms to complete.

If NVDS read performance is critical to your software architecture, you can optimize your code for speed by using either of the two methods listed below.

1. Periodically refresh all addresses that are used; this is the more useful method. The optimal use of NVDS, in terms of speed, is to rotate the writes evenly among all addresses planned for use, thereby bringing all reads closer to the minimum read time.

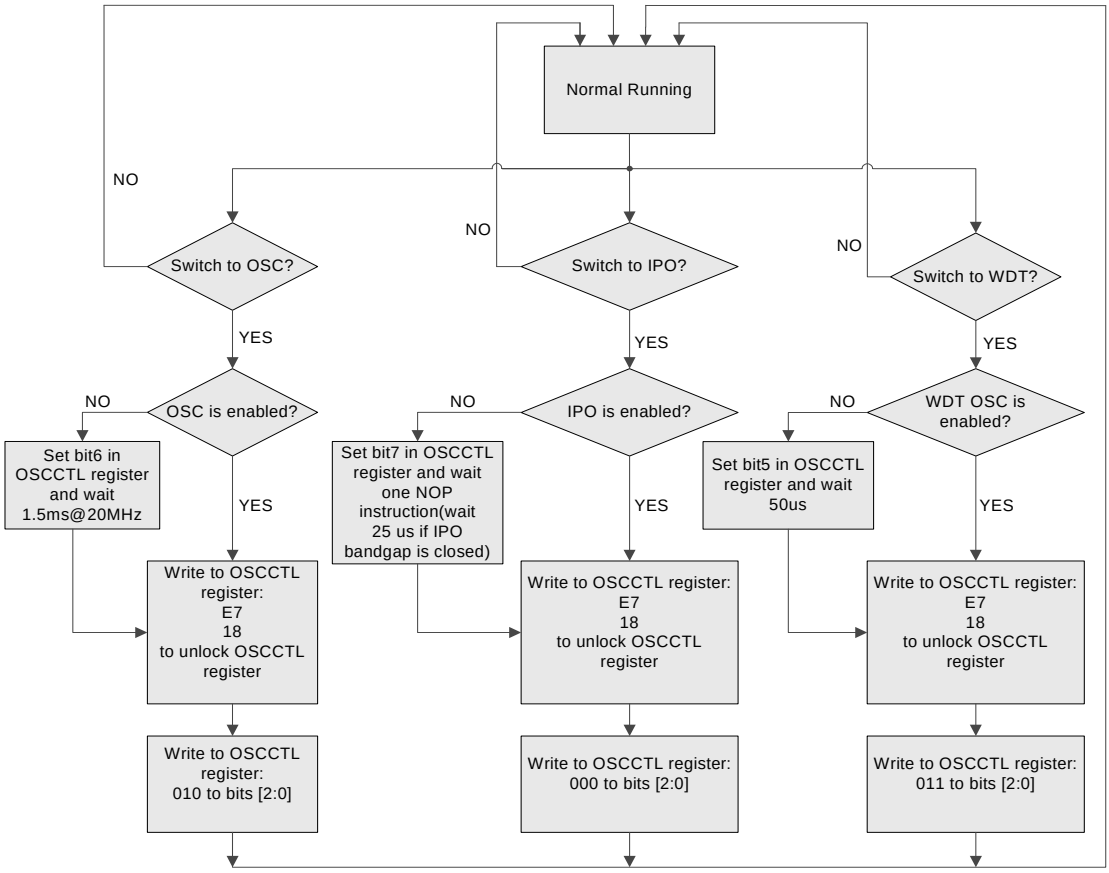

Figure 24. Oscillator Control Clock Switching Flow Chart

Oscillator Operation with an External RC Network

Figure 26 displays a recommended configuration for connection with an external resistor-capacitor (RC) network.

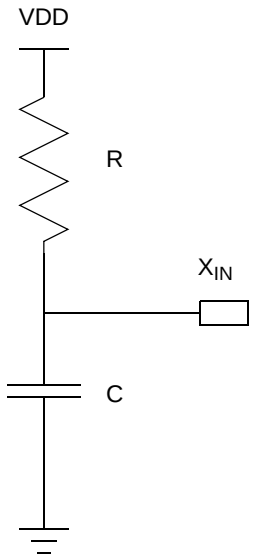

Figure 26. Connecting the On-Chip Oscillator to an External RC Network

An external resistance value of 45 kΩ is recommended for oscillator operation with an external RC network. The minimum resistance value to ensure operation is 40 kΩ. The typical oscillator frequency can be estimated from the values of the resistor (R in kΩ) and capacitor (C in pF) elements using the following equation:

$$\text{Oscillator Frequency (kHz)} = \frac{1\times10^{6}}{(0.4 \times R \times C) + (4 \times C)}$$

Figure 27 displays the typical (3.3 V and 25°C) oscillator frequency as a function of the capacitor (C in pF) employed in the RC network assuming a 45 kΩ external resistor. For very small values of C, the parasitic capacitance of the oscillator X_{IN} pin and the printed circuit board should be included in the estimation of the oscillator frequency.

It is possible to operate the RC oscillator using only the parasitic capacitance of the package and printed circuit board. To minimize sensitivity to external parasitics, external capacitance values in excess of 20 pF are recommended.

Assembly Language Source Program Example

```
JP START          ; Everything after the semicolon is a comment.
START:            ; A label called “START”. The first instruction (JP START) in this
                  ; example causes program execution to jump to the point within the
                  ; program where the START label occurs.
LD R4, R7         ; A Load (LD) instruction with two operands. The first operand,
                  ; Working register R4, is the destination. The second operand,
                  ; Working register R7, is the source. The contents of R7 is
                  ; written into R4.
LD 234H, #%01     ; Another Load (LD) instruction with two operands.
                  ; The first operand, extended mode register Address 234H,
                  ; identifies the destination. The second operand, immediate data
                  ; value 01H, is the source. The value 01H is written into the
                  ; register at address 234H.
```

Assembly Language Syntax

For proper instruction execution, eZ8 CPU assembly language syntax requires that the operands be written as *destination, source*. After assembly, the object code usually reflects the operands in the order *source, destination*, but ordering is op code-dependent.

The following examples illustrate the format of some basic assembly instructions and the resulting object code produced by the assembler. This binary format must be followed by users that prefer manual program coding or intend to implement their own assembler.

Example 1

If the contents of registers 43H and 08H are added and the result is stored in 43H, the assembly syntax and resulting object code is:

Table 101. Assembly Language Syntax Example 1

Assembly Language Code	ADD	43H,	08H	(ADD dst, src)
Object Code	04	08	43	(OPC src, dst)

Table 112. Rotate and Shift Instructions (Continued)

Mnemonic	Operands	Instruction
RR	dst	Rotate Right
RRC	dst	Rotate Right through Carry
SRA	dst	Shift Right Arithmetic
SRL	dst	Shift Right Logical
SWAP	dst	Swap Nibbles

Table 121. Nonvolatile Data Storage

	V_{DD} = 2.7 to 3.6V T_A = 0°C to +70°C			V_{DD} = 2.7 to 3.6V T_A = –40°C to +105°C				
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**	**Notes**
NVDS Byte Read Time				71	–	258	µs	With system clock at 20 MHz
NVDS Byte Program Time				126	–	136	µs	With system clock at 20 MHz
Data Retention				10	–	–	years	25°C
Endurance				100,000	–	–	cycles	Cumulative write cycles for entire memory

Note: For every 200 writes, a maintenance operation is necessary. In this rare occurrence, the write can take up to 58 ms to complete.

Table 122. Analog-to-Digital Converter Electrical Characteristics and Timing

		V_{DD} = 2.7 to 3.6V T_A = 0°C to +70°C			V_{DD} = 2.7 to 3.6V T_A = –40°C to +105°C				
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
	Resolution				–	10	–	bits	
	Differential Nonlinearity (DNL) [1]				–1	–	+4	LSB	
	Integral Nonlinearity (INL) [1]				–5	–	+5	LSB	
	Gain Error					15		LSB	
	Offset Error				–15	–	15	LSB	PDIP package
					–9	–	9	LSB	Other packages
V_{REF}	On chip reference				1.9	2.0	2.1	V	
	Active Power Consumption					4		mA	
	Power Down Current						1	µA	

Note: [1]When the input voltage is lower than 20 mV, the conversion error is out of spec.

On-Chip Debugger Timing

Figure 35 and Table 126 provide timing information for the DBG pin. The DBG pin timing specifications assume a 4 ns maximum rise and fall time.

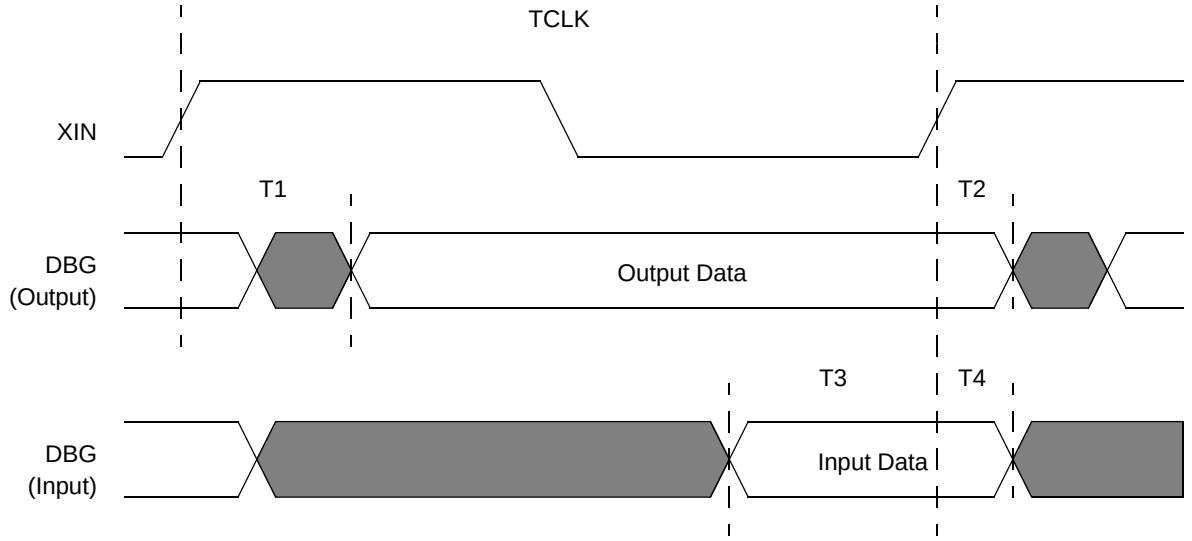

Figure 35. On-Chip Debugger Timing

Table 126. On-Chip Debugger Timing

		Delay (ns)	
Parameter	**Abbreviation**	**Minimum**	**Maximum**
DBG			
T_1	XIN Rise to DBG Valid Delay	–	15
T_2	XIN Rise to DBG Output Hold Time	2	–
T_3	DBG to XIN Rise Input Setup Time	5	–
T_4	DBG to XIN Rise Input Hold Time	5	–

Table 128. Z8 Encore! XP F0830 Series Ordering Matrix

Part Number	Flash	RAM	NVDS	ADC Channels	Description
Z8F1233QH020EG	12KB	256	No	0	QFN 20-pin
Z8F1232SJ020EG	12KB	256	No	8	SOIC 28-pin
Z8F1232HJ020EG	12KB	256	No	8	SSOP 28-pin
Z8F1232PJ020EG	12KB	256	No	8	PDIP 28-pin
Z8F1232QJ020EG	12KB	256	No	8	QFN 28-pin
Z8F1233SJ020EG	12KB	256	No	0	SOIC 28-pin
Z8F1233HJ020EG	12KB	256	No	0	SSOP 28-pin
Z8F1233PJ020EG	12KB	256	No	0	PDIP 28-pin
Z8F1233QJ020EG	12KB	256	No	0	QFN 28-pin
Z8 Encore! F0830 with 8KB Flash					
Standard Temperature: 0°C to 70°C					
Z8F0830SH020SG	8KB	256	Yes	7	SOIC 20-pin
Z8F0830HH020SG	8KB	256	Yes	7	SSOP 20-pin
Z8F0830PH020SG	8KB	256	Yes	7	PDIP 20-pin
Z8F0830QH020SG	8KB	256	Yes	7	QFN 20-pin
Z8F0831SH020SG	8KB	256	Yes	0	SOIC 20-pin
Z8F0831HH020SG	8KB	256	Yes	0	SSOP 20-pin
Z8F0831PH020SG	8KB	256	Yes	0	PDIP 20-pin
Z8F0831QH020SG	8KB	256	Yes	0	QFN 20-pin
Z8F0830SJ020SG	8KB	256	Yes	8	SOIC 28-pin
Z8F0830HJ020SG	8KB	256	Yes	8	SSOP 28-pin
Z8F0830PJ020SG	8KB	256	Yes	8	PDIP 28-pin
Z8F0830QJ020SG	8KB	256	Yes	8	QFN 28-pin
Z8F0831SJ020SG	8KB	256	Yes	0	SOIC 28-pin
Z8F0831HJ020SG	8KB	256	Yes	0	SSOP 28-pin
Z8F0831PJ020SG	8KB	256	Yes	0	PDIP 28-pin
Z8F0831QJ020SG	8KB	256	Yes	0	QFN 28-pin
Extended Temperature: –40°C to 105°C					
Z8F0830SH020EG	8KB	256	Yes	7	SOIC 20-pin
Z8F0830HH020EG	8KB	256	Yes	7	SSOP 20-pin
Z8F0830PH020EG	8KB	256	Yes	7	PDIP 20-pin
Z8F0830QH020EG	8KB	256	Yes	7	QFN 20-pin
Z8F0831SH020EG	8KB	256	Yes	0	SOIC 20-pin

Hex Addresses: F87–F8F

This address range is reserved.

Comparator 0

For more information about the Comparator Register, see the Comparator Control Register Definitions section on page 107.

Hex Address: F90

Table 156. Comparator Control Register (CMP0)

Bit	7	6	5	4	3	2	1	0
Field	Reserved	INNSEL	REFLVL				Reserved	
RESET	0	0	0	1	0	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F90H							

Hex Addresses: F91–FBF

This address range is reserved.

Interrupt Controller

For more information about the Interrupt Control registers, see the Interrupt Control Register Definitions section on page 57.

Hex Address: FC0

Table 157. Interrupt Request 0 Register (IRQ0)

Bit	7	6	5	4	3	2	1	0
Field	Reserved	T1I	T0I	Reserved	Reserved	Reserved	Reserved	ADCI
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FC0H							

Trim Bit Control

For more information about the Trim Bit Control registers, see the Flash Option Bit Control Register Definitions section on page 126.

Hex Address: FF6

Table 189. Trim Bit Address Register (TRMADR)

Bit	7	6	5	4	3	2	1	0
Field	TRMADR - Trim Bit Address (00H to 1FH)							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FF6H							

Hex Address: FF7

Table 190. Trim Bit Data Register (TRMDR)

Bit	7	6	5	4	3	2	1	0
Field	TRMDR - Trim Bit Data							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FF7H							

Flash Memory Controller

For more information about the Flash Control registers, see the Flash Control Register Definitions section on page 118.

Hex Address: FF8

Table 191. Flash Control Register (FCTL)

Bit	7	6	5	4	3	2	1	0
Field	FCMD							
RESET	0	0	0	0	0	0	0	0
R/W	W	W	W	W	W	W	W	W
Address	FF8H							

P

R

V

W

X

Z