



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	23
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f0230pj020sg

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Overview

Zilog's Z8 Encore! MCU family of products are the first in a line of Zilog microcontroller products based on the 8-bit eZ8 CPU. The Z8 Encore! F0830 Series products expand on Zilog's extensive line of 8-bit microcontrollers. The Flash in-circuit programming capability allows for faster development time and program changes in the field. The new eZ8 CPU is upward-compatible with existing Z8 CPU instructions. The rich peripheral set of Z8 Encore! F0830 Series makes it suitable for a variety of applications including motor control, security systems, home appliances, personal electronic devices and sensors.

Features

The key features of Z8 Encore! F0830 Series MCU include:

- 20MHz eZ8 CPU
- Up to 12KB Flash memory with in-circuit programming capability
- Up to 256B register RAM
- 64B Nonvolatile Data Storage (NVDS)
- Up to 25 I/O pins depending upon package
- Internal Precision Oscillator (IPO)
- External crystal oscillator
- Two enhanced 16-bit timers with capture, compare and PWM capability
- Watchdog Timer (WDT) with dedicated internal RC oscillator
- Single-pin, On-Chip Debugger (OCD)
- Optional 8-channel, 10-bit Analog-to-Digital Converter (ADC)
- On-chip analog comparator
- Up to 17 interrupt sources
- Voltage Brown-Out (VBO) protection
- Power-On Reset (POR)
- 2.7V to 3.6V operating voltage
- Up to thirteen 5 V-tolerant input pins
- 20- and 28-pin packages
- 0°C to +70°C standard temperature range and -40°C to +105°C extended temperature operating ranges

Pin Characteristics

Table 5 provides detailed characteristics of each pin available on the Z8 Encore! F0830 Series 20- and 28-pin devices. Data in Table 5 are sorted alphabetically by the pin symbol mnemonic.

Symbol Mnemonic	Direction	Reset Direction	Active Low or Active High	Tristate Output	Internal Pull-Up or Pull-Down	Schmitt- Trigger Input	Open Drain Output	5V Tolerance
AV _{DD}	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
AV _{SS}	N/A	N/A	N/A	N/A	N/A	N/A	N/A	NA
DBG	I/O	I	N/A	Yes	No	Yes	Yes	Yes
PA[7:0]	I/O	Ι	N/A	Yes	Programma- ble pull-up	Yes	Yes, Programma- ble	PA[7:2] only
PB[7:0]	I/O	I	N/A	Yes	Programma- ble pull-up	Yes	Yes, Programma- ble	PB[7:6] only
PC[7:0]	I/O	Ι	N/A	Yes	Programma- ble pull-up	Yes	Yes, Programma- ble	PC[7:3] only
RESET/PD0	I/O	I/O (defaults <u>to</u> RESET)	Low (in RESET mode)	Yes (PD0 only)	Programma- ble for PD0; always on for RESET	Yes	Programma- ble for PD0; always on for RESET	Yes
V _{DD}	N/A	N/A	N/A	N/A			N/A	N/A
V _{SS}	N/A	N/A	N/A	N/A			N/A	N/A

Table 5. Pin Characteristics (20- and 28-pin Devices)



Note: PB6 and PB7 are available only in devices without an ADC function.

Register Map

Table 8 provides an address map of the Z8 Encore! F0830 Series register file. Not all devices and package styles in the Z8 Encore! F0830 Series support the ADC or all of the GPIO ports. Consider registers for unimplemented peripherals as reserved.

Address (Hex)	Register Description	Mnemonic	Reset (Hex)	Page No.
General Purpose	RAM			
000–0FF	General purpose register file RAM	—	XX	
100-EFF	Reserved	_	XX	
Timer 0				
F00	Timer 0 high byte	T0H	00	83
F01	Timer 0 low byte	TOL	01	83
F02	Timer 0 reload high byte	TORH	FF	85
F03	Timer 0 reload low byte	TORL	FF	85
F04	Timer 0 PWM high byte	T0PWMH	00	86
F05	Timer 0 PWM low byte	TOPWML	00	86
F06	Timer 0 control 0	T0CTL0	00	87
F07	Timer 0 control 1	T0CTL1	00	88
Timer 1				
F08	Timer 1 high byte	T1H	00	83
F09	Timer 1 low byte	T1L	01	83
F0A	Timer 1 reload high byte	T1RH	FF	85
F0B	Timer 1 reload low byte	T1RL	FF	85
F0C	Timer 1 PWM high byte	T1PWMH	00	86
F0D	Timer 1 PWM low byte	T1PWML	00	86
F0E	Timer 1 control 0	T1CTL0	00	87
F0F	Timer 1 control 1	T1CTL1	00	83
F10–F6F	Reserved		XX	
Analog-to-Digita	I Converter (ADC)			
F70	ADC control 0	ADCCTL0	00	102
F71	Reserved	_	XX	
F72	ADC data high byte	ADCD_H	XX	103

Table 8. Register File Address Map

Note: XX = Undefined.

Z8 Encore![®] F0830 Series Product Specification

Reset and Stop Mode Recovery

The reset controller in the Z8 Encore! F0830 Series controls RESET and Stop Mode Recovery operations. In a typical operation, the following events can cause a reset:

- Power-On Reset (POR)
- Voltage Brown-Out (VBO)
- Watchdog Timer time-out (when configured by the WDT_RES Flash option bit to initiate a reset)
- External RESET pin assertion (when the alternate RESET function is enabled by the GPIO register)
- On-Chip Debugger initiated reset (OCDCTL[0] set to 1)

When the device is in STOP Mode, a Stop Mode Recovery event is initiated by either of the following occurrences:

- A Watchdog Timer time-out
- A GPIO port input pin transition on an enabled Stop Mode Recovery source

The VBO circuitry on the device generates a VBO reset when the supply voltage drops below a minimum safe level.

Reset Types

The Z8 Encore! F0830 Series provides different types of Reset operations. Stop Mode Recovery is considered a form of reset. Table 9 lists the types of resets and their operating characteristics. The duration of a system reset is longer if the external crystal oscillator is enabled by the Flash option bits; the result is additional time for oscillator startup.

LED Drive Enable Register

The LED Drive Enable Register, shown in Table 31, activates the controlled current drive. The Alternate Function Register has no control over the LED function; therefore, setting the Alternate Function Register to select the LED function is not required. LEDEN bits [7:0] correspond to Port C bits [7:0], respectively.

Bit	7	6	5	4	3	2	1	0
Field				LEDE	N[7:0]			
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address				F8	2H			

Table 31	I FD	Drive	Fnable	(I EDEN)
Table JT.		DIIVE		

Bit	Description
[7:0]	LED Drive Enable
LEDEN	These bits determine which Port C pins are connected to an internal current sink. 0 = Tristate the Port C pin.
	1= Connect controlled current sink to the Port C pin.

LED Drive Level High Register

The LED Drive Level High Register, shown in Table 32, contains two control bits for each Port C pin. These two bits select one of four programmable current drive levels for each Port C pin. Each pin is individually programmable.

Bit	7	6	5	4	3	2	1	0
Field				LEDLV	LH[7:0]			
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address				F8	3H			

Bit Description

[7:0] LED Level High Bits

LEDLVLH {LEDLVLH, LEDLVLL} select one of four programmable current drive levels for each Port C pin. 00 = 3mA.

01= 7 mA.

10= 13mA.

11= 20mA.

Interrupt Request 2 Register

The Interrupt Request 2 (IRQ2) Register, shown in Table 37, stores interrupt requests for both vectored and polled interrupts. When a request is sent to the Interrupt Controller, the corresponding bit in the IRQ2 Register becomes 1. If interrupts are globally enabled (vectored interrupts), the Interrupt Controller passes an interrupt request to the eZ8 CPU. If interrupts are globally disabled (polled interrupts), the eZ8 CPU can read the Interrupt Request 2 Register to determine if any interrupt requests are pending.

Bit	7	6	5	4	3	2	1	0
Field		Rese	erved		PC3I	PC2I	PC1I	PC0I
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address				FC	6H			
Bit	Descriptio	n						
[7:4]	Reserved							
	These regis	sters are res	erved and n	nust be prog	rammed to	0000.		
[3]	Port C Pin	x Interrupt	Request					
PCxI	0 = No inter	D = No interrupt request is pending for GPIO Port C pin x.						
	1 = An inter	= An interrupt request from GPIO Port C pin x is awaiting service.						
Note: x inc	dicates the sp	ates the specific GPIO port pin number (3–0).						

Table 37. Interrupt Request 2 Register (IRQ2)

IRQ0 Enable High and Low Bit Registers

Table 38 lists the priority control values for IRQ0. The IRQ0 Enable High and Low Bit registers, shown in Tables 39 and 40, form a priority-encoded enabling service for interrupts in the Interrupt Request 0 Register. Priority is generated by setting the bits in each register.

IRQ0I	ENH[<i>x</i>]	IRQ0ENL[x]	Priority	Description
	0	0	Disabled	Disabled
	0	1	Level 1	Low
	1	0	Level 2	Nominal
	1	1	Level 3	High
Note:	x indicate	es the register bits in	the range 7–0.	

Table 38. IRQ0 Enable and Priority Encoding

Shared Interrupt Select Register

The shared interrupt select (IRQSS) register determines the source of the PADxS interrupts. See Table 48. The shared interrupt select register selects between Port A and alternate sources for the individual interrupts.

Because these shared interrupts are edge-triggered, it is possible to generate an interrupt just by switching from one shared source to another. For this reason, an interrupt must be disabled before switching between sources.

Bit	7	6	5	4	3	2	1	0
Field	Reserved	PA6CS	Reserved					
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address				FC	EH			

Table 48. Shared Interrupt Select Register (IRQSS)

Bit	Description
[7]	Reserved
	This bit is reserved and must be programmed to 0.
[6]	PA6/Comparator Selection
PA6CS	0 = PA6 is used for the interrupt caused by PA6CS interrupt request.
	1 = The comparator is used for the interrupt caused by PA6CS interrupt request.
[5:0]	Reserved
	These registers are reserved and must be programmed to 000000.

Timer 0–1 PWM High and Low Byte Registers

The Timer 0–1 PWM High and Low Byte (TxPWMH and TxPWML) registers, shown in Tables 54 and 55, control PWM operations. These registers also store the capture values for the CAPTURE and CAPTURE/COMPARE modes.

Bit	7	6	5	4	3	2	1	0		
Field	РѠӍН									
RESET	0	0	0	0	0	0	0	0		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
Address	F04H, F0CH									

Table 54. Timer 0–1 PWM High Byte Register (TxPWMH)

Table 55. Timer 0–1 PWM Low Byte Register (TxPWML)

Bit	7	6	5	4	3	2	1	0		
Field	PWML									
RESET	0	0	0	0	0	0	0	0		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
Address	F05H, F0DH									

Bit Description

o the current
VM output
vhen operat-
-
,

Table 62. Watchdog Timer Reload Low Byte Register (WDTL)

Bit	7	6	5	4	3	2	1	0			
Field	WDTL										
RESET	0	0	0	0	0	0	0	0			
R/W	R/W*										
Address	FF3H										
Note: *A read returns the current WDT count value; a write sets the appropriate reload value.											
Bit Description											

BR	beenpach
[7:0]	WDT Reload Low
WDTL	Least significant byte (LSB), bits[7:0] of the 24-bit WDT reload value.





Figure 11. Analog-to-Digital Converter Block Diagram

Operation

The ADC converts the analog input, ANA_X , to a 10-bit digital representation. The equation for calculating the digital value is represented by:

ADCOutput = $1024 \times (ANA_x \div V_{REF})$

Assuming zero gain and offset errors, any voltage outside the ADC input limits of AV_{SS} and V_{REF} returns all 0s or 1s, respectively. A new conversion can be initiated by a software to the ADC Control Register's start bit.

Initiating a new conversion, stops any conversion currently in progress and begins a new conversion. To avoid disrupting a conversion already in progress, the START bit can be read to determine ADC operation status (busy or available).

Sample Settling Time Register

The <u>Sample Settling</u> Time Register, shown in Table 66, is used to program a delay after the <u>SAMPLE/HOLD</u> signal is asserted and before the START signal is asserted; an ADC conversion then begins. The number of clock cycles required for settling will vary from system to system depending on the system clock period used. The system designer should program this register to contain the number of clocks required to meet a $0.5 \mu s$ minimum settling time.

Bit	7	6	5	4	3	2	1	0		
Field		Rese	erved		SST					
RESET	0				1	1	1	1		
R/W		F	र		R/W					
Address	F74H									

Table 66. Sample Settling Time (ADCSST)

Bit	Description
[7:4]	Reserved These bits are reserved and must be programmed to 0000.
[3:0] SST	0h–Fh = Sample settling time in number of system clock periods to meet 0.5 μ s minimum.

Bit	Description (Continued)
[4] XTLDIS	 State of the Crystal Oscillator at Reset This bit enables only the crystal oscillator. Selecting the crystal oscillator as the system clock must be performed manually. 0 = The crystal oscillator is enabled during reset, resulting in longer reset timing. 1 = The crystal oscillator is disabled during reset, resulting in shorter reset timing.
[3:0]	Reserved These bits are reserved and must be programmed to 1111.

Trim Bit Address Space

All available trim bit addresses and their functions are listed in Tables 83 through 90.

Bit	Description (Continued)					
[1:0]	Filter Select					
FilterSely	2-bit selection for the clock filter mode.					
	00 = No filter.					
	01 = Filter low level noise on high level signal.					
	10 = Filter high level noise on low level signal.					
	11 = Filter both.					
Notes: x ir	Notes: x indicates bit values 3–1; y indicates bit values 1–0.					

Note: The bit values used in Table 89 are set at factory and no calibration is required.

DlyCtl3, DlyCtl2, DlyCtl1	Low Noise Pulse on High Signal (ns)	High Noise Pulse on Low Signal (ns)						
000	5	5						
001	7	7						
010	9	9						
011	11	11						
100	13	13						
101	17	17						
110	20	20						
111	25	25						
Note: The variation is about 30%.								

Table 90. ClkFlt Delay Control Definition

Oscillator Control

The Z8 Encore! F0830 Series device uses five possible clocking schemes. Each one of these is user-selectable.

- On-chip precision trimmed RC oscillator
- On-chip oscillator using off-chip crystal or resonator
- On-chip oscillator using external RC network
- External clock drive
- On-chip low precision Watchdog Timer Oscillator

In addition, Z8 Encore! F0830 Series devices contain clock failure detection and recovery circuitry, allowing continued operation despite a failure of the primary oscillator.

Operation

This chapter discusses the logic used to select the system clock and handle primary oscillator failures. A description of the specific operation of each oscillator is outlined further in this document.

System Clock Selection

The oscillator control block selects from the available clocks. *Table 98* describes each clock source and its usage.

Figure 32 displays the typical current consumption versus the system clock frequency in NORMAL Mode.

Figure 32. I_{CC} Versus System Clock Frequency (NORMAL Mode)

	T _A = 0°C to +70°C			T _A = −40°C to +105°C						
Symbol	Parameter	Min	Тур	Max	Min	Typ ¹	Max	Units	Conditions	
T _{POR}	Power-On Reset Digital Delay				TBD	13	TBD	μs	66 Internal Preci- sion Oscillator cycles	
T _{POR}	Power-On Reset Digital Delay				TBD	8	TBD	ms	5000 Internal Pre- cision Oscillator cycles	
T _{SMR}	Stop Mode Recovery with crystal oscillator disabled				TBD	13	TBD	μs	66 Internal Preci- sion Oscillator cycles	
T _{SMR}	Stop Mode Recovery with crystal oscillator enabled				TBD	8	TBD	ms	5000 Internal Pre- cision Oscillator cycles	
T _{VBO}	Voltage Brown-Out Pulse Rejection Period				_	10	_	μs	V _{DD} < V _{VBO} to gen- erate a Reset.	
T _{RAMP}	Time for V_{DD} to transition from V_{SS} to V_{POR} to ensure valid Reset				0.10	-	100	ms		
Note: ¹ Da	Note: ¹ Data in the typical column is from characterization at 3.3 V and 0°C. These values are provided for design guid-									

Table 118. Power-On Reset and Voltage Brown-Out Electrical Characteristics and Timing

ance only and are not tested in production.

Hex Address: F71

This address range is reserved.

Hex Address: F72

Table 147. ADC Data High Byte Register (ADCD_H)

Bit	7	6	5	4	3	2	1	0			
Field	ADCDH										
RESET	X										
R/W	R										
Address	F72H										

Bit	Description
[7:0]	ADC High Byte
	00h–FFh = The last conversion output is held in the data registers until the next ADC conver-
	sion is completed.

Hex Address: F73

Table 148. ADC Data Low Bits Register (ADCD_L)

Bit	7	6	5	4	3	2	1	0	
Field	ADO	CDL	Reserved						
RESET)	K)	<			
R/W	F	२	R						
Address	F73H								

Bit Position	Description
[7:6]	ADC Low Bits 00–11b = These bits are the two least significant bits of the 10-bit ADC output. These bits are undefined after a reset. The low bits are latched into this register whenever the ADC Data High Byte Register is read.
[5:0]	Reserved These bits are reserved and must be programmed to 000000.

Hex Address: FC1

Bit	7	6	5	4	3	2	1	0	
Field	Reserved	T1ENH	T0ENH	Reserved	Reserved	Reserved	Reserved	ADCENH	
RESET	0	0	0	0	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Address		FC1H							

Hex Address: FC2

Table 159. IRQ0 Enable Low Bit Register (IRQ0ENL)

Bit	7	6	5	4	3	2	1	0		
Field	Reserved	T1ENL	T0ENL	Reserved	Reserved	Reserved	Reserved	ADCENL		
RESET	0	0	0	0	0	0	0	0		
R/W	R	R/W	R/W	R/W	R/W	R	R	R/W		
Address		FC2H								

Hex Address: FC3

Table 160. Interrupt Request 1 Register (IRQ1)

Bit	7	6	5	4	3	2	1	0	
Field	PA7I	PA6CI	PA5I	PA4I	PA3I	PA2I	PA1I	PA0I	
RESET	0	0	0	0	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Address	FC3H								

Hex Address: FC4

Table 161. IRQ1 Enable High Bit Register (IRQ1ENH)

Bit	7	6	5	4	3	2	1	0		
Field	PA7ENH	PA6CENH	PA5ENH	PA4ENH	PA3ENH	PA2ENH	PA1ENH	PA0ENH		
RESET	0	0	0	0	0	0	0	0		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
Address		FC4H								

GPIO Port A

For more information about the GPIO registers, see the <u>GPIO Control Register Definitions</u> section on page 39.

Hex Address: FD0

Table 169. Port A GPIO Address Register (PAADDR)

Bit	7	6	5	4	3	2	1	0			
Field		PADDR[7:0]									
RESET		00H									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
Address	FD0H										

Hex Address: FD1

Table 170. Port A Control Registers (PACTL)

Bit	7	6	5	4	3	2	1	0		
Field	PCTL									
RESET		00H								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
Address	FD1H									

Hex Address: FD2

Table 171. Port A Input Data Registers (PAIN)

Bit	7	6	5	4	3	2	1	0			
Field	PIN7	PIN6	PIN5	PIN4	PIN3	PIN2	PIN1	PIN0			
RESET	Х	Х	Х	Х	Х	Х	Х	Х			
R/W	R	R	R	R	R	R	R	R			
Address		FD2H									

Hex Address: FD7

Bit	7	6	5	4	3	2	1	0		
Field	POUT7	POUT6	POUT5	POUT4	POUT3	POUT2	POUT1	POUT0		
RESET	0	0	0	0	0	0	0	0		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
Address		FD7H								

Table 176. Port B Output Data Register (PBOUT)

Hex Address: FD8

Table 177. Port C GPIO Address Register (PCADDR)

Bit	7	6	5	4	3	2	1	0
Field	PADDR[7:0]							
RESET	00H							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FD8H							

Hex Address: FD9

Table 178. Port C Control Registers (PCCTL)

Bit	7	6	5	4	3	2	1	0
Field	PCTL							
RESET	00H							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FD9H							

Hex Address: FDA

Table 179. Port C Input Data Registers (PCIN)

Bit	7	6	5	4	3	2	1	0
Field	PIN7	PIN6	PIN5	PIN4	PIN3	PIN2	PIN1	PIN0
RESET	Х	Х	Х	Х	Х	Х	Х	Х
R/W	R	R	R	R	R	R	R	R
Address	FDAH							