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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| **Details** | |
|---|---|
| Product Status | Active |
| Core Processor | eZ8 |
| Core Size | 8-Bit |
| Speed | 20MHz |
| Connectivity | - |
| Peripherals | Brown-out Detect/Reset, LED, POR, PWM, WDT |
| Number of I/O | 17 |
| Program Memory Size | 2KB (2K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 256 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 3.6V |
| Data Converters | A/D 7x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 20-SOIC (0.295", 7.50mm Width) |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/z8f0230sh020eg |

# Reset Sources

Table 10 lists the possible sources of a system reset.

**Table 10. Reset Sources and Resulting Reset Type**

| Operating Mode | Reset Source | Special Conditions |
|---|---|---|
| NORMAL or HALT modes | Power-On Reset/Voltage Brown-Out | Reset delay begins after supply voltage exceeds POR level. |
| | Watchdog Timer time-out when configured for reset | None. |
| | $\overline{\text{RESET}}$ pin assertion | All reset pulses less than four system clocks in width are ignored. |
| | On-Chip Debugger initiated reset (OCDCTL[0] set to 1) | System, except the On-Chip Debugger is unaffected by the reset. |
| STOP Mode | Power-On Reset/Voltage Brown-Out | Reset delay begins after supply voltage exceeds POR level. |
| | $\overline{\text{RESET}}$ pin assertion | All reset pulses less than 12 ns are ignored. |
| | DBG pin driven Low | None. |

## Power-On Reset

Each device in the Z8 Encore! F0830 Series contains an internal Power-On Reset circuit. The POR circuit monitors the digital supply voltage and holds the device in the Reset state until the digital supply voltage reaches a safe operating level. After the supply voltage exceeds the POR voltage threshold ($V_{POR}$), the device is held in the Reset state until the POR counter has timed out. If the crystal oscillator is enabled by the option bits, the time-out is longer.

After the Z8 Encore! F0830 Series device exits the Power-On Reset state, the eZ8 CPU fetches the reset vector. Following the Power-On Reset, the POR status bit in the Reset Status (RSTSTAT) Register is set to 1.

Figure 6 displays the Power-On Reset operation. See the Electrical Characteristics chapter on page 184 for the POR threshold voltage ($V_{POR}$).

**Table 16. Port Alternate Function Mapping (Continued)**

| Port | Pin | Mnemonic | Alternate Function Description | Alternate Function Set Register AFS1 |
|---|---|---|---|---|
| **Port B**[2] | PB0 | Reserved | | AFS1[0]: 0 |
| | | ANA0 | ADC analog input | AFS1[0]: 1 |
| | PB1 | Reserved | | AFS1[1]: 0 |
| | | ANA1 | ADC analog input | AFS1[1]: 1 |
| | PB2 | Reserved | | AFS1[2]: 0 |
| | | ANA2 | ADC analog input | AFS1[2]: 1 |
| | PB3 | CLKIN | External input clock | AFS1[3]: 0 |
| | | ANA3 | ADC analog input | AFS1[3]: 1 |
| | PB4 | Reserved | | AFS1[4]: 0 |
| | | ANA7 | ADC analog input | AFS1[4]: 1 |
| | PB5 | Reserved | | AFS1[5]: 0 |
| | | $V_{REF}$ | ADC reference voltage | AFS1[5]: 1 |
| | PB6 | Reserved | | AFS1[6]: 0 |
| | | Reserved | | AFS1[6]: 1 |
| | PB7 | Reserved | | AFS1[7]: 0 |
| | | Reserved | | AFS1[7]: 1 |

Notes:

1. Because there is only a single alternate function for each Port A and Port D (PD0) pin, the Alternate Function Set registers are not implemented for Port A and Port D (PD0). Enabling alternate function selections (as described in the Port A–D Alternate Function Subregisters section on page 42) automatically enables the associated alternate function.
2. Because there are at most two choices of alternate functions for any Port B pin, the AFS2 Alternate Function Set Register is implemented but is not used to select the function. Additionally, alternate function selection (as described in the Port A–D Alternate Function Subregisters section on page 42) must also be enabled.
3. Because there are at most two choices of alternate functions for any Port C pin, the AFS2 Alternate Function Set Register is implemented but is not used to select the function. Additionally, alternate function selection (as described in the Port A–D Alternate Function Subregisters section on page 42) must also be enabled.

## Port A–D Pull-up Enable Subregisters

The Port A–D Pull-Up Enable Subregister is accessed through the Port A–D Control Register by writing `06H` to the Port A–D Address Register. See Table 26. Setting the bits in the Port A–D Pull-Up Enable subregisters enables a weak internal resistive pull-up on the specified port pins.

**Table 26. Port A–D Pull-Up Enable Subregisters (PxPUE)**

| **Bit** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
|---|---|---|---|---|---|---|---|---|
| **Field** | PPUE7 | PPUE6 | PPUE5 | PPUE4 | PPUE3 | PPUE2 | PPUE1 | PPUE0 |
| **RESET** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **R/W** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| **Address** | If 06H in Port A–D Address Register, accessible through the Port A–D Control Register | | | | | | | |

| **Bit** | **Description** |
|---|---|
| [7:0]<br>P*x*PUE | **Port Pull-Up Enable**<br>0 = The weak pull-up on the port pin is disabled.<br>1 = The weak pull-up on the port pin is enabled. |

Note: x indicates the specific GPIO port pin number (7–0).

## Interrupt Request 2 Register

The Interrupt Request 2 (IRQ2) Register, shown in Table 37, stores interrupt requests for both vectored and polled interrupts. When a request is sent to the Interrupt Controller, the corresponding bit in the IRQ2 Register becomes 1. If interrupts are globally enabled (vectored interrupts), the Interrupt Controller passes an interrupt request to the eZ8 CPU. If interrupts are globally disabled (polled interrupts), the eZ8 CPU can read the Interrupt Request 2 Register to determine if any interrupt requests are pending.

**Table 37. Interrupt Request 2 Register (IRQ2)**

| **Bit** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
|---|---|---|---|---|---|---|---|---|
| **Field** | Reserved | | | | PC3I | PC2I | PC1I | PC0I |
| **RESET** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **R/W** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| **Address** | FC6H | | | | | | | |

| Bit | Description |
|---|---|
| [7:4] | **Reserved**<br>These registers are reserved and must be programmed to 0000. |
| [3]<br>PC*x*I | **Port C Pin *x* Interrupt Request**<br>0 = No interrupt request is pending for GPIO Port C pin *x*.<br>1 = An interrupt request from GPIO Port C pin *x* is awaiting service. |
| Note: x indicates the specific GPIO port pin number (3–0). | |

## IRQ0 Enable High and Low Bit Registers

Table 38 lists the priority control values for IRQ0. The IRQ0 Enable High and Low Bit registers, shown in Tables 39 and 40, form a priority-encoded enabling service for interrupts in the Interrupt Request 0 Register. Priority is generated by setting the bits in each register.

**Table 38. IRQ0 Enable and Priority Encoding**

| IRQ0ENH[*x*] | IRQ0ENL[*x*] | Priority | Description |
|---|---|---|---|
| 0 | 0 | Disabled | Disabled |
| 0 | 1 | Level 1 | Low |
| 1 | 0 | Level 2 | Nominal |
| 1 | 1 | Level 3 | High |
| Note: *x* indicates the register bits in the range 7–0. | | | |

Observe the following steps for configuring a timer for PWM DUAL OUTPUT Mode and for initiating the PWM operation:

1. Write to the Timer Control Register to:
   - Disable the timer
   - Configure the timer for PWM DUAL OUTPUT Mode; setting the mode also involves writing to TMODEHI bit in the TxCTL1 Register
   - Set the prescale value
   - Set the initial logic level (High or Low) and PWM High/Low transition for the timer output alternate function
2. Write to the Timer High and Low Byte registers to set the starting count value (typically `0001H`). This write only affects the first pass in PWM Mode. After the first timer reset in PWM Mode, counting always begins at the reset value of `0001H`.
3. Write to the PWM High and Low Byte registers to set the PWM value.
4. Write to the PWM Control Register to set the PWM deadband delay value. The deadband delay must be less than the duration of the positive phase of the PWM signal (as defined by the PWM High and Low Byte registers). It must also be less than the duration of the negative phase of the PWM signal (as defined by the difference between the PWM registers and the Timer Reload registers).
5. Write to the Timer Reload High and Low Byte registers to set the reload value (PWM period). The reload value must be greater than the PWM value.
6. If appropriate, enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers.
7. Configure the associated GPIO port pin for the timer output and timer output complement alternate functions. The timer output complement function is shared with the timer input function for both timers. Setting the timer mode to DUAL PWM will automatically switch the function from timer-in to timer-out complement.
8. Write to the Timer Control Register to enable the timer and initiate counting.

The PWM period is represented by the following equation:

$$\text{PWM Period (s)} = \frac{\text{Reload Value} \times \text{Prescale}}{\text{System Clock Frequency (Hz)}}$$

If an initial starting value other than `0001H` is loaded into the Timer High and Low Byte registers, the ONE-SHOT Mode equation determines the first PWM time-out period.

If `TPOL` is set to 0, the ratio of the PWM output high time to the total period is represented by:

3. Write to the Timer Reload High and Low Byte registers to set the reload value.
4. Clear the timer PWM High and Low Byte registers to `0000H`. This allows user software to determine if interrupts are generated by either a capture event or a reload. If the PWM High and Low Byte registers still contain `0000H` after the interrupt, the interrupt were generated by a reload.
5. Enable the timer interrupt, if appropriate and set the timer interrupt priority by writing to the relevant interrupt registers. By default, the timer interrupt is generated for both input capture and Reload events. The user can configure the timer interrupt to be generated only at the input capture event or the reload event by setting the TICONFIG field of the TxCTL1 Register.
6. Configure the associated GPIO port pin for the timer input alternate function.
7. Write to the Timer Control Register to enable the timer and initiate counting.

In CAPTURE Mode, the elapsed time between the timer start and the capture event can be calculated using the following equation:

$$\text{Capture Elapsed Time (s)} = \frac{(\text{Capture Value} - \text{Start Value}) \times \text{Prescale}}{\text{System Clock Frequency (Hz)}}$$

## COMPARE Mode

In COMPARE Mode, the timer counts up to 16-bit maximum compare value stored in the Timer Reload High and Low Byte registers. The timer input is the system clock. Upon reaching the compare value, the timer generates an interrupt and counting continues (the timer value is not reset to `0001H`). Additionally, if the timer output alternate function is enabled, the timer output pin changes state (from Low to High or from High to Low) upon compare.

If the timer reaches `FFFFH`, the timer resets to `0000H` and continues counting.

Observe the following steps for configuring a timer for COMPARE Mode and for initiating the count:

1. Write to the Timer Control Register to:
   - Disable the timer
   - Configure the timer for COMPARE Mode
   - Set the prescale value
   - Set the initial logic level (High or Low) for the timer output alternate function
2. Write to the Timer High and Low Byte registers to set the starting count value.
3. Write to the Timer Reload High and Low Byte registers to set the compare value.

# *Watchdog Timer*

The Watchdog Timer (WDT) protects from corrupted or unreliable software, power faults and other system-level problems which can place the Z8 Encore! F0830 Series devices into unsuitable operating states. The features of the Watchdog Timer include:

- On-chip RC oscillator
- A selectable time-out response: reset or interrupt
- 24-bit programmable time-out value

## Operation

The Watchdog Timer is a retriggerable one-shot timer that resets or interrupts the Z8 Encore! F0830 Series devices when the WDT reaches its terminal count. The WDT uses a dedicated on-chip RC oscillator as its clock source. The WDT operates only in two modes: ON and OFF. Once enabled, it always counts and must be refreshed to prevent a time-out. Perform an enable by executing the WDT instruction or by setting the WDT_AO Flash option bit. The WDT_AO bit forces the WDT to operate immediately on reset, even if a WDT instruction has not been executed.

The Watchdog Timer is a 24-bit reloadable downcounter that uses three 8-bit registers in the eZ8 CPU register space to set the reload value. The nominal WDT time-out period is calculated using the following equation:

$$\text{WDT Time-out Period (ms)} = \frac{\text{WDT Reload Value}}{10}$$

where the WDT reload value is the 24-bit decimal value provided by {WDTU[7:0], WDTH[7:0], WDTL[7:0]} and the typical Watchdog Timer RC oscillator frequency is 10KHz. The Watchdog Timer cannot be refreshed after it reaches `000002H`. The WDT reload value must not be set to values below `000004H`. Table 58 provides information about approximate time-out delays for the minimum and maximum WDT reload values.

**Table 58. Watchdog Timer Approximate Time-Out Delays**

| WDT Reload Value (Hex) | WDT Reload Value (Decimal) | Approximate Time-Out Delay (with 10KHz Typical WDT Oscillator Frequency) | |
|---|---|---|---|
| | | Typical | Description |
| 000004 | 4 | 400µs | Minimum time-out delay |
| 000400 | 1024 | 102ms | Default time-out delay |
| FFFFFF | 16,777,215 | 28 minutes | Maximum time-out delay |

# Flash Memory

The products in the Z8 Encore! F0830 Series features either 1KB (1024 bytes with NVDS), 2KB (2048 bytes with NVDS), 4KB (4096 bytes with NVDS), 8KB (8192 bytes with NVDS) or 12KB (12288 bytes with no NVDS) of nonvolatile Flash memory with read/write/erase capability. Flash memory can be programmed and erased in-circuit by either user code or through the On-Chip Debugger.

The Flash memory array is arranged in pages with 512 bytes per page. The 512-byte page is the minimum Flash block size that can be erased. Each page is divided into eight rows of 64 bytes.

For program/data protection, Flash memory is also divided into sectors. In the Z8 Encore! F0830 Series, each sector maps to one page (for 1KB, 2KB and 4KB devices), two pages (8KB device) or three pages (12KB device).

The first two bytes of Flash program memory is used as Flash option bits. For more information, see *the* Flash Option Bits chapter on page 124.

Table 69 lists the Flash memory configuration for each device in the Z8 Encore! F0830 Series. Figures 14 through 18 display the memory arrangements for each Flash memory size.

**Table 69. Z8 Encore! F0830 Series Flash Memory Configuration**

| Part Number | Flash Size KB (Bytes) | Flash Pages | Program Memory Addresses | Flash Sector Size (bytes) |
|---|---|---|---|---|
| Z8F123x | 12 (12,288) | 24 | 0000H–2FFFH | 1536 |
| Z8F083x | 8 (8196) | 16 | 0000H–1FFFH | 1024 |
| Z8F043x | 4 (4096) | 8 | 0000H–0FFFH | 512 |
| Z8F023x | 2 (2048) | 4 | 0000H–07FFH | 512 |
| Z8F013x | 1 (1024) | 2 | 0000H–03FFH | 512 |

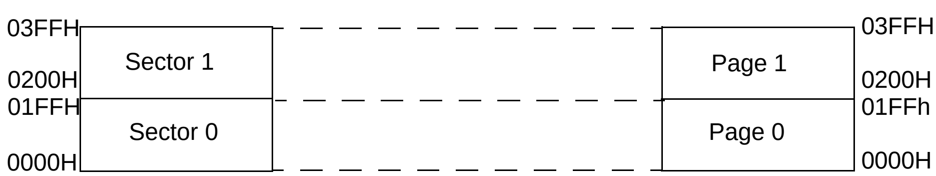


**Figure 14. 1K Flash with NVDS**

**Table 83. Trim Bit Address Space**

| Address | Function |
|---|---|
| 00h | ADC reference voltage |
| 01h | ADC and comparator |
| 02h | Internal Precision Oscillator |
| 03h | Oscillator and VBO |
| 06h | ClkFltr |

**Table 84. Trim Option Bits at 0000H (ADCREF)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | ADCREF_TRIM | | | | | Reserved | | |
| RESET | U | | | | | U | | |
| R/W | R/W | | | | | R/W | | |
| Address | Information Page Memory 0020H | | | | | | | |
| Note: U = Unchanged by Reset. R/W = Read/Write. | | | | | | | | |

| Bit | Description |
|---|---|
| [7:3]<br>ADCREF_TRIM | **ADC Reference Voltage Trim Byte**<br>Contains trimming bits for ADC reference voltage. |
| [2:0] | **Reserved**<br>These bits are reserved and must be programmed to 111. |

**Note:** The bit values used in Table 84 are set at the factory; no calibration is required.

**Table 85. Trim Option Bits at 0001H (TADC_COMP)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | Reserved | | | | | | | |
| RESET | U | U | U | U | U | U | U | U |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | Information Page Memory 0021H | | | | | | | |
| Note: U = Unchanged by Reset. R/W = Read/Write. | | | | | | | | |

| Bit | Description |
|---|---|
| [7:0] | **Reserved**<br>Altering this register may result in incorrect device operation. |

Because the minimum read time is much less than the write time, however, actual speed benefits are not always realized.

2. Use as few unique addresses as possible to optimize the impact of refreshing.

- Watchdog Timer reset
- Asserting the $\overline{\text{RESET}}$ pin Low to initiate a reset
- Driving the DBG pin Low while the device is in STOP Mode initiates a system reset

## OCD Data Format

The OCD interface uses the asynchronous data format defined for RS-232. Each character is transmitted as 1 start bit, 8 data bits (least-significant bit first) and 1 stop bit. See Figure 23.

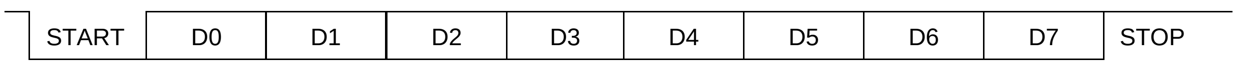


**Figure 23. OCD Data Format**

## OCD Autobaud Detector/Generator

To run over a range of baud rates (data bits per second) with various system clock frequencies, the On-Chip Debugger contains an autobaud detector/generator. After a reset, the OCD is idle until it receives data. The OCD requires that the first character sent from the host is the character `80H`. The character `80H` has eight continuous bits low (one Start bit plus 7 data bits), framed between high bits. The autobaud detector measures this period and sets the OCD baud rate generator accordingly.

The autobaud detector/generator is clocked by the system clock. The minimum baud rate is the system clock frequency divided by 512. For optimal operation with asynchronous datastreams, the maximum recommended baud rate is the system clock frequency divided by 8. The maximum possible baud rate for asynchronous datastreams is the system clock frequency divided by 4, but this theoretical maximum is possible only for low noise designs with clean signals. Table 94 lists minimum and recommended maximum baud rates for sample crystal frequencies.

**Table 94. OCD Baud-Rate Limits**

| System Clock Frequency (MHz) | Recommended Maximum Baud Rate (kbps) | Recommended Standard PC Baud Rate (bps) | Minimum Baud Rate (kbps) |
|---|---|---|---|
| 20.0 | 2500.0 | 1,843,200 | 39 |
| 1.0 | 125.0 | 115,200 | 1.95 |
| 0.032768 (32 KHz) | 4.096 | 2400 | 0.064 |

**Table 113. eZ8 CPU Instruction Summary (Continued)**

| Assembly Mnemonic | Symbolic Operation | Address Mode dst | Address Mode src | Op Code(s) (Hex) | Flags C | Flags Z | Flags S | Flags V | Flags D | Flags H | Fetch Cycles | Instr. Cycles |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LDX dst, src | dst ← src | r | ER | 84 | – | – | – | – | – | – | 3 | 2 |
| | | Ir | ER | 85 | | | | | | | 3 | 3 |
| | | R | IRR | 86 | | | | | | | 3 | 4 |
| | | IR | IRR | 87 | | | | | | | 3 | 5 |
| | | r | X(rr) | 88 | | | | | | | 3 | 4 |
| | | X(rr) | r | 89 | | | | | | | 3 | 4 |
| | | ER | r | 94 | | | | | | | 3 | 2 |
| | | ER | Ir | 95 | | | | | | | 3 | 3 |
| | | IRR | R | 96 | | | | | | | 3 | 4 |
| | | IRR | IR | 97 | | | | | | | 3 | 5 |
| | | ER | ER | E8 | | | | | | | 4 | 2 |
| | | ER | IM | E9 | | | | | | | 4 | 2 |
| LEA dst, X(src) | dst ← src + X | r | X(r) | 98 | – | – | – | – | – | – | 3 | 3 |
| | | rr | X(rr) | 99 | | | | | | | 3 | 5 |
| MULT dst | dst[15:0] ← dst[15:8] * dst[7:0] | RR | | F4 | – | – | – | – | – | – | 2 | 8 |
| NOP | No operation | | | 0F | – | – | – | – | – | – | 1 | 2 |
| OR dst, src | dst ← dst OR src | r | r | 42 | – | * | * | 0 | – | – | 2 | 3 |
| | | r | Ir | 43 | | | | | | | 2 | 4 |
| | | R | R | 44 | | | | | | | 3 | 3 |
| | | R | IR | 45 | | | | | | | 3 | 4 |
| | | R | IM | 46 | | | | | | | 3 | 3 |
| | | IR | IM | 47 | | | | | | | 3 | 4 |
| ORX dst, src | dst ← dst OR src | ER | ER | 48 | – | * | * | 0 | – | – | 4 | 3 |
| | | ER | IM | 49 | | | | | | | 4 | 3 |
| POP dst | dst ← @SP<br>SP ← SP + 1 | R | | 50 | – | – | – | – | – | – | 2 | 2 |
| | | IR | | 51 | | | | | | | 2 | 3 |

Note: Flags Notation:
* = Value is a function of the result of the operation.
– = Unaffected.
X = Undefined.
0 = Reset to 0.
1 = Set to 1.

**Table 116. DC Characteristics (Continued)**

| Symbol | Parameter | $T_A$ = 0°C to +70°C Min | Typ | Max | $T_A$ = –40°C to +105°C Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|---|---|
| $I_{LED}$ | Controlled Current Drive | | | | 1.5 | 3 | 4.5 | mA | See GPIO section on LED description |
| | | | | | 2.8 | 7 | 10.5 | mA | |
| | | | | | 7.8 | 13 | 19.5 | mA | |
| | | | | | 12 | 20 | 30 | mA | |
| $C_{PAD}$ | GPIO Port Pad Capacitance | | | | – | 8.0[2] | – | pF | TBD |
| $C_{XIN}$ | XIN Pad Capacitance | | | | – | 8.0[2] | – | pF | TBD |
| $C_{XOUT}$ | XOUT Pad Capacitance | | | | – | 9.5[2] | – | pF | TBD |
| $I_{PU}$ | Weak Pull-up Current | | | | 50 | 120 | 220 | µA | $V_{DD}$ = 2.7 - 3.6V |
| ICCH[3] | Supply Current in HALT Mode | | | | | TBD | | mA | TBD |
| ICCS | Supply Current in STOP Mode | | | 2 | | | 8 | µA | Without Watchdog Timer running |

Notes:
1. This condition excludes all pins that have on-chip pull-ups, when driven Low.
2. These values are provided for design guidance only and are not tested in production.
3. See Figure 31 for HALT Mode current.

**Table 117. AC Characteristics (Continued)**

| Symbol | Parameter | $V_{DD}$ = 2.7 to 3.6V $T_A$ = 0°C to +70°C Min | Max | $V_{DD}$ = 2.7 to 3.6V $T_A$ = –40°C to +105°C Min | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| $T_{XINR}$ | System Clock Rise Time | | | – | 3 | ns | $T_{CLK}$ = 50 ns |
| $T_{XINF}$ | System Clock Fall Time | | | – | 3 | ns | $T_{CLK}$ = 50 ns |
| $T_{XTALSET}$ | Crystal Oscillator Setup Time | | | – | 30,000 | cycle | Crystal oscillator cycles |
| $T_{IPOSET}$ | Internal Precision Oscillator Startup Time | | | – | 25 | µs | Startup time after enable |
| $T_{WDTSET}$ | WDT Startup Time | | | – | 50 | µs | Startup time after reset |

# On-Chip Peripheral AC and DC Electrical Characteristics

**Table 118. Power-On Reset and Voltage Brown-Out Electrical Characteristics and Timing**

| Symbol | Parameter | $T_A$ = 0°C to +70°C Min | Typ | Max | $T_A$ = –40°C to +105°C Min | Typ[1] | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|---|---|
| $V_{POR}$ | Power-On Reset Voltage Threshold | | | | 2.20 | 2.45 | 2.70 | V | $V_{DD} = V_{POR}$ (default VBO trim) |
| $V_{VBO}$ | Voltage Brown-Out Reset Voltage Threshold | | | | 2.15 | 2.40 | 2.65 | V | $V_{DD} = V_{VBO}$ (default VBO trim) |
| | $V_{POR}$ to $V_{VBO}$ hysteresis | | | | | 50 | 75 | mV | |
| | Starting $V_{DD}$ voltage to ensure valid Power-On Reset. | | | | – | $V_{SS}$ | – | V | |
| $T_{ANA}$ | Power-On Reset Analog Delay | | | | – | 50 | – | µs | $V_{DD} > V_{POR}$; $T_{POR}$ Digital Reset delay follows $T_{ANA}$ |

Note: [1]Data in the typical column is from characterization at 3.3V and 0°C. These values are provided for design guidance only and are not tested in production.

# Low Power Control

For more information about the Power Control Register, see the Power Control Register Definitions section on page 31.

### Hex Address: F80

**Table 151. Power Control Register 0 (PWRCTL0)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | Reserved | | | VBO | Reserved | Reserved | COMP | Reserved |
| RESET | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | F80H | | | | | | | |

### Hex Address: F81

This address range is reserved.

# LED Controller

For more information about the LED Drive registers, see the GPIO Control Register Definitions section on page 39.

### Hex Address: F82

**Table 152. LED Drive Enable (LEDEN)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | LEDEN[7:0] | | | | | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | F82H | | | | | | | |

## Hex Address: FC5

**Table 162. IRQ1 Enable Low Bit Register (IRQ1ENL)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | PA7ENL | PA6CENL | PA5ENL | PA4ENL | PA3ENL | PA2ENL | PA1ENL | PA0ENL |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | FC5H | | | | | | | |

## Hex Address: FC6

**Table 163. Interrupt Request 2 Register (IRQ2)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | Reserved | | | | PC3I | PC2I | PC1I | PC0I |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | FC6H | | | | | | | |

## Hex Address: FC7

**Table 164. IRQ2 Enable High Bit Register (IRQ2ENH)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | Reserved | | | | C3ENH | C2ENH | C1ENH | C0ENH |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | FC7H | | | | | | | |

## Hex Address: FC8

**Table 165. IRQ2 Enable Low Bit Register (IRQ2ENL)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | Reserved | | | | C3ENL | C2ENL | C1ENL | C0ENL |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | FC8H | | | | | | | |

# Trim Bit Control

For more information about the Trim Bit Control registers, see the Flash Option Bit Control Register Definitions section on page 126.

### Hex Address: FF6

**Table 189. Trim Bit Address Register (TRMADR)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | TRMADR - Trim Bit Address (00H to 1FH) | | | | | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | FF6H | | | | | | | |

### Hex Address: FF7

**Table 190. Trim Bit Data Register (TRMDR)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | TRMDR - Trim Bit Data | | | | | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | FF7H | | | | | | | |

# Flash Memory Controller

For more information about the Flash Control registers, see the Flash Control Register Definitions section on page 118.

### Hex Address: FF8

**Table 191. Flash Control Register (FCTL)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | FCMD | | | | | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | W | W | W | W | W | W | W | W |
| Address | FF8H | | | | | | | |

## Hex Address: FF8

**Table 192. Flash Status Register (FSTAT)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | Reserved | | FSTAT | | | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R | R | R | R | R | R | R | R |
| Address | FF8H | | | | | | | |

## Hex Address: FF9

The Flash Page Select Register is shared with the Flash Sector Protect Register.

**Table 193. Flash Page Select Register (FPS)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | INFO_EN | PAGE | | | | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | FF9H | | | | | | | |

**Table 194. Flash Sector Protect Register (FPROT)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | SPROT7 | SPROT6 | SPROT5 | SPROT4 | SPROT3 | SPROT2 | SPROT1 | SPROT0 |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | FF9H | | | | | | | |

## Hex Address: FFA

**Table 195. Flash Frequency High Byte Register (FFREQH)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | FFREQH | | | | | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | FFAH | | | | | | | |