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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | eZ8 |
| Core Size | 8-Bit |
| Speed | 20MHz |
| Connectivity | - |
| Peripherals | Brown-out Detect/Reset, LED, POR, PWM, WDT |
| Number of I/O | 17 |
| Program Memory Size | 2KB (2K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 256 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 3.6V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 20-SSOP (0.209", 5.30mm Width) |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/z8f0231hh020eg |

# Reset and Stop Mode Recovery

The reset controller in the Z8 Encore! F0830 Series controls RESET and Stop Mode Recovery operations. In a typical operation, the following events can cause a reset:

- Power-On Reset (POR)
- Voltage Brown-Out (VBO)
- Watchdog Timer time-out (when configured by the WDT_RES Flash option bit to initiate a reset)
- External $\overline{\text{RESET}}$ pin assertion (when the alternate RESET function is enabled by the GPIO register)
- On-Chip Debugger initiated reset (OCDCTL[0] set to 1)

When the device is in STOP Mode, a Stop Mode Recovery event is initiated by either of the following occurrences:

- A Watchdog Timer time-out
- A GPIO port input pin transition on an enabled Stop Mode Recovery source

The VBO circuitry on the device generates a VBO reset when the supply voltage drops below a minimum safe level.

## Reset Types

The Z8 Encore! F0830 Series provides different types of Reset operations. Stop Mode Recovery is considered a form of reset. Table 9 lists the types of resets and their operating characteristics. The duration of a system reset is longer if the external crystal oscillator is enabled by the Flash option bits; the result is additional time for oscillator startup.

PA0 and PA6 contain two different Timer functions, a timer input and a complementary timer output. Both of these functions require the same GPIO configuration, the selection between the two is based on the TIMER mode. For more details, see the Timers chapter on page 68.

## Direct LED Drive

The Port C pins provide a sinked current output, capable of driving an LED without requiring an external resistor. The output sinks current at programmable levels, 3mA, 7mA, 13mA and 20mA. This mode is enabled through the LED Control registers.

For proper function, the LED anode must be connected to $V_{DD}$ and the cathode to the GPIO pin.

Using all Port C pins in LED drive mode with maximum current may result in excessive total current. See the Electrical Characteristics chapter on page 184 for the maximum total current for the applicable package.

## Shared Reset Pin

On the 20- and 28-pin devices, the Port D0 pin shares function with a bidirectional reset pin. Unlike all other I/O pins, this pin does not default to GPIO function on power-up. This pin acts as a bidirectional input/output open-drain reset with an internal pull-up until the user software reconfigures it as a GPIO PD0. When in GPIO mode, the Port D0 pin functions as output only, and must be configured as an output. PD0 supports the high drive feature, but not the stop-mode recovery feature.

## Crystal Oscillator Override

For systems using a crystal oscillator, the pins PA0 and PA1 are connected to the crystal. When the crystal oscillator is enabled, the GPIO settings are overridden and PA0 and PA1 are disabled. See the Oscillator Control Register Definitions section on page 154.

## 5V Tolerance

In the 20- and 28-pin versions of this device, any pin, which shares functionality with an ADC, crystal or comparator port is not 5V-tolerant, including PA[1:0], PB[5:0] and PC[2:0]. All other signal pins are 5V-tolerant and can safely handle inputs higher than $V_{DD}$ even with the pull-ups enabled, but with excess power consumption on pull-up resistor.

## LED Drive Level Low Register

The LED Drive Level Low Register, shown in Table 33, contains two control bits for each Port C pin. These two bits select one of four programmable current drive levels for each Port C pin. Each pin is individually programmable.

**Table 33. LED Drive Level Low Register (LEDLVLL)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | LEDLVLL[7:0] | | | | | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | F84H | | | | | | | |

| Bit | Description |
|---|---|
| [7:0] LEDLVLL | **LED Level Low Bits**<br>{LEDLVLH, LEDLVLL} select one of four programmable current drive levels for each Port C pin.<br>00 = 3mA.<br>01 = 7mA.<br>10 = 13mA.<br>11 = 20mA. |

# Architecture

Figure 9 displays the Interrupt Controller block diagram.

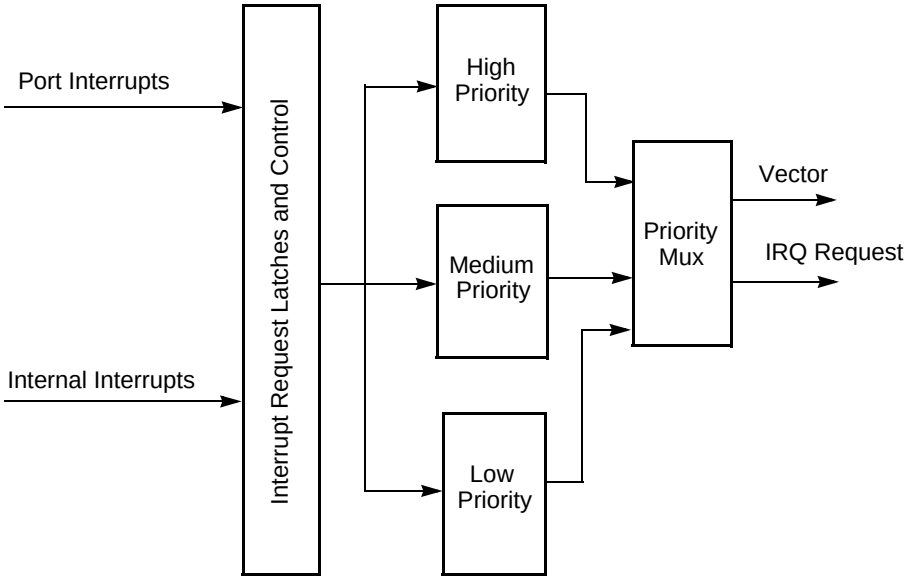



**Figure 9. Interrupt Controller Block Diagram**

# Operation

This section describes the operational aspects of the following functions.

Master Interrupt Enable: see page 55

Interrupt Vectors and Priority: see page 56

Interrupt Assertion: see page 56

Software Interrupt Assertion: see page 57

## Master Interrupt Enable

The master interrupt enable bit (IRQE) in the Interrupt Control Register globally enables and disables the interrupts.

Interrupts are globally enabled by any of the following actions:

- Execution of an EI (enable interrupt) instruction
- Execution of an IRET (return from interrupt) instruction

# Comparator Control Register Definitions

The Comparator Control Register (CMP0) configures the comparator inputs and sets the value of the internal voltage reference. The GPIO pin is always used as positive comparator input.

**Table 68. Comparator Control Register (CMP0)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | Reserved | INNSEL | REFLVL | | | | Reserved | |
| RESET | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | F90H | | | | | | | |

| Bit | Description |
|---|---|
| [7] | **Reserved**<br>This bit is reserved and must be programmed to 0. |
| [6]<br>INNSEL | **Signal Select for Negative Input**<br>0 = internal reference disabled, GPIO pin used as negative comparator input.<br>1 = internal reference enabled as negative comparator input. |
| [5:2]<br>REFLVL | **Internal Reference Voltage Level**<br>This reference is independent of the ADC voltage reference.<br>0000 = 0.0V.<br>0001 = 0.2V.<br>0010 = 0.4V.<br>0011 = 0.6V.<br>0100 = 0.8V.<br>0101 = 1.0V (Default).<br>0110 = 1.2V.<br>0111 = 1.4V.<br>1000 = 1.6V.<br>1001 = 1.8V.<br>1010–1111 = Reserved. |
| [1:0] | **Reserved**<br>These bits are reserved and must be programmed to 00. |

## Flash Sector Protect Register

The Flash Sector Protect Register is shared with the Flash Page Select Register. When the Flash Control Register is locked and written with 5EH, the next write to this address targets the Flash Sector Protect Register. In all other cases, it targets the Flash Page Select Register.

This register selects one of the eight available Flash memory sectors to be protected. The Reset state of each sector protect bit is the zero (unprotected) state. After a sector is protected by setting its corresponding register bit, the register bit cannot be cleared by the user.

To determine the appropriate Flash memory sector address range and sector number for your F0830 Series product, please refer to Table 70 on page 112.

**Table 75. Flash Sector Protect Register (FPROT)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | SPROT7 | SPROT6 | SPROT5 | SPROT4 | SPROT3 | SPROT2 | SPROT1 | SPROT0 |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | FF9H | | | | | | | |

| Bit | Description |
|---|---|
| [7:0]<br>SPROT*x* | **Sector Protection**<br>For Z8F12xx, Z8F08xx and Z8F04xx devices, all bits are used. For Z8F02xx devices, the upper four bits remain unused. For Z8F01xx devices, the upper six bits remain unused. To determine the appropriate Flash memory sector address range and sector number for your F0830 Series product, please refer to Table 69 and to Figures 14 through 18. |

Note: *x* indicates bits in the range 7–0.

## Option Bit Types

This section describes the two types of Flash option bits offered in the F0830 Series.

### User Option Bits

The user option bits are contained in the first two bytes of program memory. User access to these bits is provided because these locations contain application specific device configurations. The information contained here is lost when page 0 of program memory is erased.

### Trim Option Bits

The trim option bits are contained in the information page of the Flash memory. These bits are factory programmed values required to optimize the operation of onboard analog circuitry and cannot be permanently altered by the user. Program memory can be erased without endangering these values. It is possible to alter working values of these bits by accessing the trim bit address and data registers, but these working values are lost after a power loss.

There are 32 bytes of trim data. To modify one of these values, the user code must first write a value between 00H and 1FH into the Trim Bit Address Register. The next write to the Trim Bit Data Register changes the working value of the target trim data byte.

Reading the trim data requires the user code to write a value between 00H and 1FH into the Trim Bit Address Register. The next read from the Trim Bit Data Register returns the working value of the target trim data byte.

**Note:** The trim address range is from information address 20–3F only. The remaining information page is not accessible via the Trim Bit Address and Data registers.

During reset, the first 43 system clock cycles perform 43 Flash accesses. The six bits of the counter provide the lower six bits of the Flash memory address. All other address bits are set to 0. The option bit registers use the 6-bit address from the counter as an address and latch the data from the Flash on the positive edge of the IPO clock, allowing for a maximum of 344-bits (43 bytes) of option information to be read from Flash.

Because option information is stored in both the first two bytes of program memory and in the information area of Flash memory, the data must be placed in specific locations to be read correctly. In this case, the first two bytes at addresses 0 and 1 in program memory are read out and the remainder of the bytes are read out of the Flash information area.

**Table 83. Trim Bit Address Space**

| Address | Function |
|---|---|
| 00h | ADC reference voltage |
| 01h | ADC and comparator |
| 02h | Internal Precision Oscillator |
| 03h | Oscillator and VBO |
| 06h | ClkFltr |

**Table 84. Trim Option Bits at 0000H (ADCREF)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | ADCREF_TRIM | | | | | Reserved | | |
| RESET | U | | | | | U | | |
| R/W | R/W | | | | | R/W | | |
| Address | Information Page Memory 0020H | | | | | | | |

Note: U = Unchanged by Reset. R/W = Read/Write.

| Bit | Description |
|---|---|
| [7:3]<br>ADCREF_TRIM | **ADC Reference Voltage Trim Byte**<br>Contains trimming bits for ADC reference voltage. |
| [2:0] | **Reserved**<br>These bits are reserved and must be programmed to 111. |

**Note:** The bit values used in Table 84 are set at the factory; no calibration is required.

**Table 85. Trim Option Bits at 0001H (TADC_COMP)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | Reserved | | | | | | | |
| RESET | U | U | U | U | U | U | U | U |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | Information Page Memory 0021H | | | | | | | |

Note: U = Unchanged by Reset. R/W = Read/Write.

| Bit | Description |
|---|---|
| [7:0] | **Reserved**<br>Altering this register may result in incorrect device operation. |

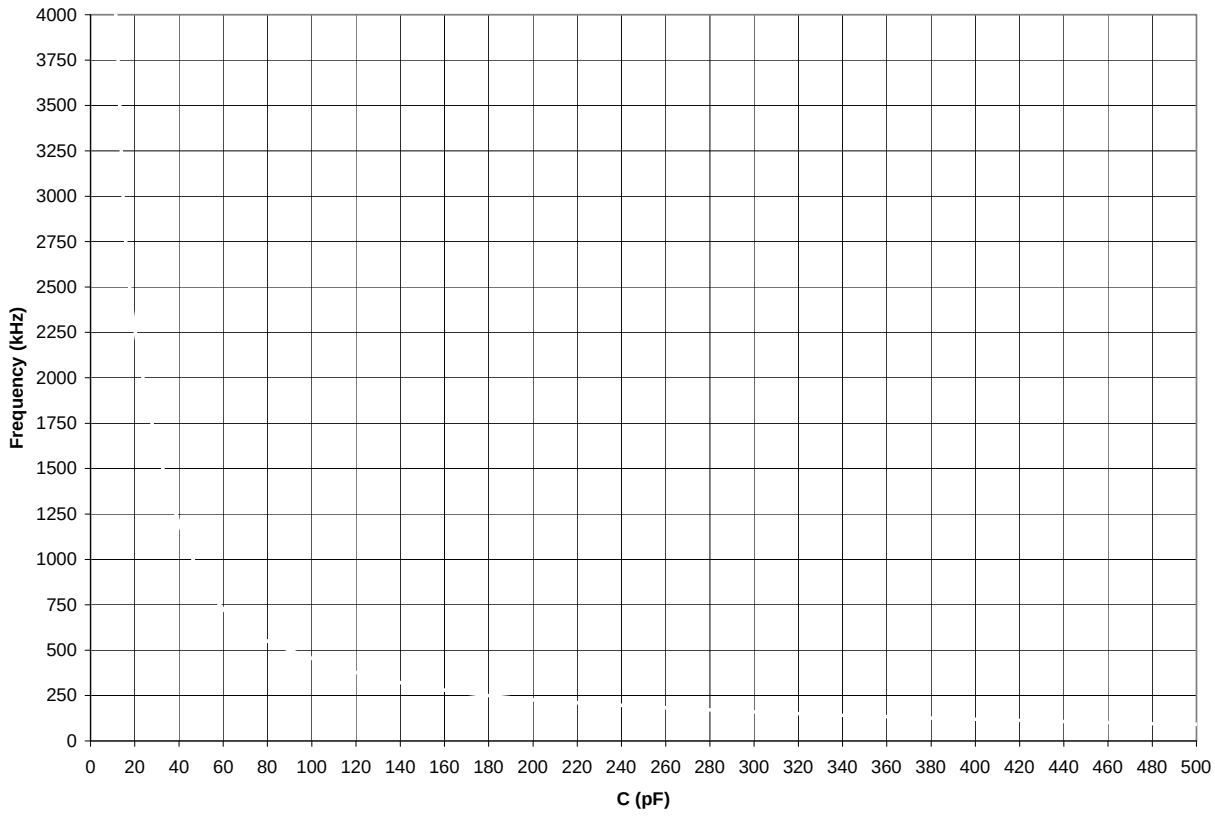
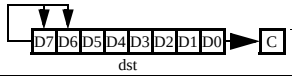
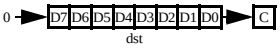



**Figure 27. Typical RC Oscillator Frequency as a Function of External Capacitance with a 45 kΩ Resistor**

**Caution:** When using the external RC OSCILLATOR Mode, the oscillator can stop oscillating if the power supply drops below 2.7V but before it drops to the Voltage Brown-Out threshold. The oscillator resumes oscillation when the supply voltage exceeds 2.7V.

**Table 113. eZ8 CPU Instruction Summary (Continued)**

| Assembly Mnemonic | Symbolic Operation | Address Mode dst | Address Mode src | Op Code(s) (Hex) | Flags C | Z | S | V | D | H | Fetch Cycles | Instr. Cycles |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SRA dst |  | R | | D0 | * | * | * | 0 | – | – | 2 | 2 |
| | | IR | | D1 | | | | | | | 2 | 3 |
| SRL dst |  | R | | 1F C0 | * | * | 0 | * | – | – | 3 | 2 |
| | | IR | | 1F C1 | | | | | | | 3 | 3 |
| SRP src | RP ← src | | IM | 01 | – | – | – | – | – | – | 2 | 2 |
| STOP | STOP Mode | | | 6F | – | – | – | – | – | – | 1 | 2 |
| SUB dst, src | dst ← dst – src | r | r | 22 | * | * | * | * | 1 | * | 2 | 3 |
| | | r | Ir | 23 | | | | | | | 2 | 4 |
| | | R | R | 24 | | | | | | | 3 | 3 |
| | | R | IR | 25 | | | | | | | 3 | 4 |
| | | R | IM | 26 | | | | | | | 3 | 3 |
| | | IR | IM | 27 | | | | | | | 3 | 4 |
| SUBX dst, src | dst ← dst – src | ER | ER | 28 | * | * | * | * | 1 | * | 4 | 3 |
| | | ER | IM | 29 | | | | | | | 4 | 3 |
| SWAP dst | dst[7:4] ↔ dst[3:0] | R | | F0 | X | * | * | X | – | – | 2 | 2 |
| | | IR | | F1 | | | | | | | 2 | 3 |
| TCM dst, src | (NOT dst) AND src | r | r | 62 | – | * | * | 0 | – | – | 2 | 3 |
| | | r | Ir | 63 | | | | | | | 2 | 4 |
| | | R | R | 64 | | | | | | | 3 | 3 |
| | | R | IR | 65 | | | | | | | 3 | 4 |
| | | R | IM | 66 | | | | | | | 3 | 3 |
| | | IR | IM | 67 | | | | | | | 3 | 4 |
| TCMX dst, src | (NOT dst) AND src | ER | ER | 68 | – | * | * | 0 | – | – | 4 | 3 |
| | | ER | IM | 69 | | | | | | | 4 | 3 |

Note: Flags Notation:
* = Value is a function of the result of the operation.
– = Unaffected.
X = Undefined.
0 = Reset to 0.
1 = Set to 1.

# Op Code Maps

A description of the opcode map data and the abbreviations are provided in Figure 28. Table 114 on page 181 lists opcode map abbreviations.

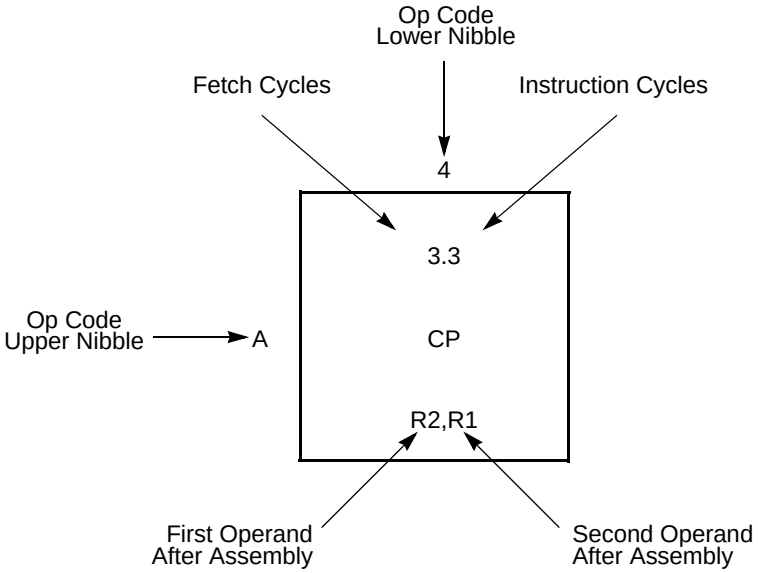



**Figure 28. Op Code Map Cell Description**

# Electrical Characteristics

The data in this chapter represents all known data prior to qualification and characterization of the F0830 Series of products, and is therefore subject to change. Additional electrical characteristics may be found in the individual chapters of this document.

## Absolute Maximum Ratings

Stresses greater than those listed in Table 115 may cause permanent damage to the device. These ratings are stress ratings only. Operation of the device at any condition outside those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. For improved reliability, tie unused inputs to one of the supply voltages ($V_{DD}$ or $V_{SS}$).

**Table 115. Absolute Maximum Ratings**

| Parameter | Minimum | Maximum | Units | Notes |
|---|---|---|---|---|
| Ambient temperature under bias | 0 | +105 | °C | |
| Storage temperature | –65 | +150 | °C | |
| Voltage on any pin with respect to $V_{SS}$ | –0.3 | +5.5 | V | |
| Voltage on $V_{DD}$ pin with respect to $V_{SS}$ | –0.3 | +3.6 | V | |
| Maximum current on input and/or inactive output pin | –5 | +5 | µA | |
| Maximum output current from active output pin | –25 | +25 | mA | |
| **20-pin Packages Maximum Ratings at 0°C to 70°C** | | | | |
| Total power dissipation | | 430 | mW | |
| Maximum current into $V_{DD}$ or out of $V_{SS}$ | | 120 | mA | |
| **28-pin Packages Maximum Ratings at 0°C to 70°C** | | | | |
| Total power dissipation | | 450 | mW | |
| Maximum current into $V_{DD}$ or out of $V_{SS}$ | | 125 | mA | |

**Table 128. Z8 Encore! XP F0830 Series Ordering Matrix**

| Part Number | Flash | RAM | NVDS | ADC Channels | Description |
|---|---|---|---|---|---|
| Z8F0831HH020EG | 8KB | 256 | Yes | 0 | SSOP 20-pin |
| Z8F0831PH020EG | 8KB | 256 | Yes | 0 | PDIP 20-pin |
| Z8F0831QH020EG | 8KB | 256 | Yes | 0 | QFN 20-pin |
| Z8F0830SJ020EG | 8KB | 256 | Yes | 8 | SOIC 28-pin |
| Z8F0830HJ020EG | 8KB | 256 | Yes | 8 | SSOP 28-pin |
| Z8F0830PJ020EG | 8KB | 256 | Yes | 8 | PDIP 28-pin |
| Z8F0830QJ020EG | 8KB | 256 | Yes | 8 | QFN 28-pin |
| Z8F0831SJ020EG | 8KB | 256 | Yes | 0 | SOIC 28-pin |
| Z8F0831HJ020EG | 8KB | 256 | Yes | 0 | SSOP 28-pin |
| Z8F0831PJ020EG | 8KB | 256 | Yes | 0 | PDIP 28-pin |
| Z8F0831QJ020EG | 8KB | 256 | Yes | 0 | QFN 28-pin |
| **Z8 Encore! F0830 with 4KB Flash** | | | | | |
| **Standard Temperature: 0°C to 70°C** | | | | | |
| Z8F0430SH020SG | 4KB | 256 | Yes | 7 | SOIC 20-pin |
| Z8F0430HH020SG | 4KB | 256 | Yes | 7 | SSOP 20-pin |
| Z8F0430PH020SG | 4KB | 256 | Yes | 7 | PDIP 20-pin |
| Z8F0430QH020SG | 4KB | 256 | Yes | 7 | QFN 20-pin |
| Z8F0431SH020SG | 4KB | 256 | Yes | 0 | SOIC 20-pin |
| Z8F0431HH020SG | 4KB | 256 | Yes | 0 | SSOP 20-pin |
| Z8F0431PH020SG | 4KB | 256 | Yes | 0 | PDIP 20-pin |
| Z8F0431QH020SG | 4KB | 256 | Yes | 0 | QFN 20-pin |
| Z8F0430SJ020SG | 4KB | 256 | Yes | 8 | SOIC 28-pin |
| Z8F0430HJ020SG | 4KB | 256 | Yes | 8 | SSOP 28-pin |
| Z8F0430PJ020SG | 4KB | 256 | Yes | 8 | PDIP 28-pin |
| Z8F0430QJ020SG | 4KB | 256 | Yes | 8 | QFN 28-pin |
| Z8F0431SJ020SG | 4KB | 256 | Yes | 0 | SOIC 28-pin |
| Z8F0431HJ020SG | 4KB | 256 | Yes | 0 | SSOP 28-pin |
| Z8F0431PJ020SG | 4KB | 256 | Yes | 0 | PDIP 28-pin |
| Z8F0431QJ020SG | 4KB | 256 | Yes | 0 | QFN 28-pin |
| **Extended Temperature: –40°C to 105°C** | | | | | |
| Z8F0430SH020EG | 4KB | 256 | Yes | 7 | SOIC 20-pin |
| Z8F0430HH020EG | 4KB | 256 | Yes | 7 | SSOP 20-pin |
| Z8F0430PH020EG | 4KB | 256 | Yes | 7 | PDIP 20-pin |

# Low Power Control

For more information about the Power Control Register, see the Power Control Register Definitions section on page 31.

### Hex Address: F80

**Table 151. Power Control Register 0 (PWRCTL0)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | Reserved | | | VBO | Reserved | Reserved | COMP | Reserved |
| RESET | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | F80H | | | | | | | |

### Hex Address: F81

This address range is reserved.

# LED Controller

For more information about the LED Drive registers, see the GPIO Control Register Definitions section on page 39.

### Hex Address: F82

**Table 152. LED Drive Enable (LEDEN)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | LEDEN[7:0] | | | | | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | F82H | | | | | | | |

### Hex Addresses: F87–F8F

This address range is reserved.

## Comparator 0

For more information about the Comparator Register, see the Comparator Control Register Definitions section on page 107.

### Hex Address: F90

**Table 156. Comparator Control Register (CMP0)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | Reserved | INNSEL | REFLVL | | | | Reserved | |
| RESET | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | F90H | | | | | | | |

### Hex Addresses: F91–FBF

This address range is reserved.

## Interrupt Controller

For more information about the Interrupt Control registers, see the Interrupt Control Register Definitions section on page 57.

### Hex Address: FC0

**Table 157. Interrupt Request 0 Register (IRQ0)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | Reserved | T1I | T0I | Reserved | Reserved | Reserved | Reserved | ADCI |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | FC0H | | | | | | | |

### Hex Address: FD3

**Table 172. Port A Output Data Register (PAOUT)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | POUT7 | POUT6 | POUT5 | POUT4 | POUT3 | POUT2 | POUT1 | POUT0 |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | FD3H | | | | | | | |

### Hex Address: FD4

**Table 173. Port B GPIO Address Register (PBADDR)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | PADDR[7:0] | | | | | | | |
| RESET | 00H | | | | | | | |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | FD4H | | | | | | | |

### Hex Address: FD5

**Table 174. Port B Control Registers (PBCTL)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | PCTL | | | | | | | |
| RESET | 00H | | | | | | | |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | FD5H | | | | | | | |

### Hex Address: FD6

**Table 175. Port B Input Data Registers (PBIN)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | PIN7 | PIN6 | PIN5 | PIN4 | PIN3 | PIN2 | PIN1 | PIN0 |
| RESET | X | X | X | X | X | X | X | X |
| R/W | R | R | R | R | R | R | R | R |
| Address | FD6H | | | | | | | |

### Hex Address: FFB

**Table 196. Flash Frequency Low Byte Register (FFREQL)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | FFREQL | | | | | | | |
| RESET | 0 | | | | | | | |
| R/W | R/W | | | | | | | |
| Address | FFBH | | | | | | | |

## G



## H



## I